GaNext

G2N65R070TT-H

650V GaN FET

Datasheet
Preliminary

1. Description

The G2N65 series FETs are hybrid normally-off Gallium Nitride (GaN) field effect transistors with the strongest gate and the lowest reverse voltage drop of all wide-band-gap devices in the market. They allow simple gate drive, offer best-in-class performance and outstanding reliability.

Features

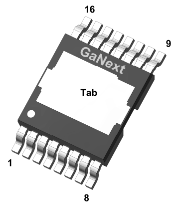
- Strong gate with a high threshold, no need for negative gate drive, and a high repetitive input voltage tolerance of ±20V.
- Fast turn-on/off speed for reduced cross-over losses.
- Low Q_g and simple gate drive for lowest driver consumption at high frequencies.
- Lowest V_F in off-state reverse conduction among all SiC and GaN FETs for low loss during dead-times.
- Negligible Q_{rr} for outstanding hard-switched bridge applications.
- High spike tolerance of 800V for enhanced reliability.
- Top cooling design, better cooling efficiency under water-cooling conditions.

Benefits

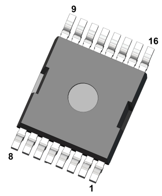
- Enable very high conversion efficiencies.
- Enable higher frequency for compact power supplies.
- End-product cost & size savings due to reduced cooling requirements.
- Improved safety & reliability due to cooler operation temperature.
- Low loop inductance.

Applications

- Datacenter power supplies, telecom power supplies, micro inverters, photovoltaic inverter, high voltage DC/DC converters and EV OBC & DC-DC based on the half-bridge and/or full-bridge topologies for hard and/or soft switching such as Totem pole bridgeless PFC and high frequency LLC.

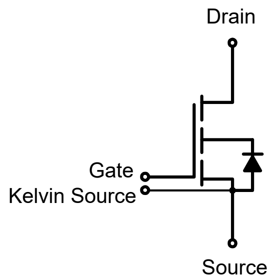


Top View



Bottom View

Drain	1 ~ 8
Gate	9
Kelvin Source	10
Source	11 ~ 16, Tab



RoHS compliant

REACH

Halogen Free

*Lead plating Pb-free
in compliance with RoHS

Key Performance Parameters	
V_{DSS} (V)	650
$V_{DSS(PK),\ non\text{-}repetitive}$ (V) [a]	800
$V_{DSS(PK),\ repetitive}$ (V) [b]	750
$R_{DS(on),\ typ}$ (mΩ) [c]	70
Q_{oss} (nC)	73
Q_g (nC)	15

[a] Duty cycle < 1%, spike duration < 30μs, non-repetitive
[b] Duty cycle < 1%, spike duration < 30μs, repetitive for ≤ 85°C, non-repetitive up to 150°C
[c] Dynamic on-resistance

Part Number & Package Information		
Part #	Package	Package Base
G2N65R070TT-H	TOLT	Source

2. Maximum Ratings

Symbol	Parameter	Value
V_{DSS} (V)	Drain-source maximum voltage (T_J = -55°C to 150°C)	650
$V_{DSS(PK),\ non\text{-}repetitive}$ (V)	Drain-source maximum peak voltage, non-repetitive [a]	800
$V_{DSS(PK),\ repetitive}$ (V)	Drain-source maximum peak voltage, repetitive [b]	750
$V_{GSS,\ DC}$ (V)	Gate-source maximum voltage	±20
$V_{GSS,\ AC}$ (V)	Gate-source maximum voltage ($f \geq$ 50Hz)	±30
P_D (W)	Maximum power dissipation (T_C = 25°C)	96
I_{DS} (A)	Maximum continuous drain current (T_C = 25°C)	26
	Maximum continuous drain current (T_C = 100°C)	16.6
$I_{DS\ (pulse)}$ (A)	Maximum pulsed drain current (T_C = 25°C) [c]	120
T_J (°C)	Operating junction temperature	-55 to 150
T_S (°C)	Storage temperature	-55 to 150
T_{sold} (°C)	Reflow soldering temperature [d]	260

[a] Duty cycle < 1%, spike duration < 30μs, non-repetitive
[b] Duty cycle < 1%, spike duration < 30μs, repetitive for ≤ 85°C, non-repetitive up to 150°C
[c] Pulse width = 10μs
[d] Reflow MSL3

3. Thermal Characteristics

Symbol	Parameter	Typ.
$R_{\Theta JC}$ (°C/W)	Junction-to-case thermal resistance	1.3
$R_{\Theta JA}$ (°C/W)	Junction-to-ambient thermal resistance [a]	40

[a] Soldered on a PCB of 6cm^2 metal area and 70μm thickness

4. Device Characteristics

T_J = 25°C unless specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$V_{GS(th)}$	Gate threshold voltage	3.0	3.5	4.0	V	V_{DS} = V_{GS}, I_D = 2.1mA
$R_{DS(on)}$	Drain-source on resistance [a]	-	70	84	mΩ	V_{GS} = 10V, I_D = 16A
		-	140	-	mΩ	V_{GS} = 10V, I_D = 16A, T_J = 150°C
I_{DSS}	Drain-source leakage current	-	3	30	µA	V_{DS} = 650V, V_{GS} = 0V
		-	12	-	µA	V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-source leakage current	-100	-	100	nA	V_{GS} = ±20V
C_{iss}	Input capacitance	-	960	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 500kHz
C_{oss}	Output capacitance	-	64	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 500kHz
C_{rss}	Reverse transfer capacitance	-	4.5	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 500kHz
$C_{o(er)}$	Equivalent output capacitance (energy related)	-	100	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V
$C_{o(tr)}$	Equivalent output capacitance (time related)	-	183	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V
Q_g	Gate charge total	-	15	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 16A
Q_{gs}	Gate to source charge	-	5.5	-	nC	
Q_{gd}	Gate to drain charge	-	5	-	nC	
Q_{oss}	Output charge	-	73	-	nC	V_{GS} = 0V, V_{DS} = 0V to 400V
$t_{d(on)}$	Turn-on delay time	-	30.4	-	ns	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 16A, R_G = 30Ω, Z_{FB} = 330Ω @100MHz, see Figure 13
t_r	Rise time	-	7.6	-	ns	
$t_{d(off)}$	Turn-off delay time	-	57.6	-	ns	
t_f	Fall time	-	8.9	-	ns	

[a] Dynamic on-resistance

Reverse Device Characteristics, T_J = 25°C unless specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Reverse current	-	-	16	A	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle
$I_{S\ (pulse)}$	Pulsed reverse current	-	-	46	A	V_{GS} = 0V, V_{SD} = 6V, pulse width ≤ 10µs, T_J = 150°C
V_{SD}	Reverse voltage [a)]	-	1.8	-	V	V_{GS} = 0V, I_S = 16A
		-	1.3	-	V	V_{GS} = 0V, I_S = 8A
t_{rr}	Reverse recovery time	-	34.4	-	ns	I_S = 16A, V_{DD} = 400V, di/dt = 1000A/µs
Q_{rr}	Reverse recovery charge [b)]	-	0	-	nC	

[a)] Including the effect of dynamic on-resistance
[b)] Excluding Q_{oss}

5. Typical Characteristics (T_C = 25°C unless specified)

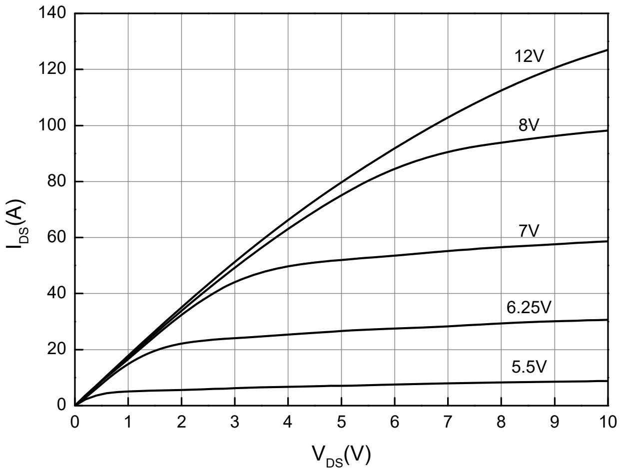


Figure 1. Typical Output Characteristics at T_J = 25°C (Parameter: V_{GS})

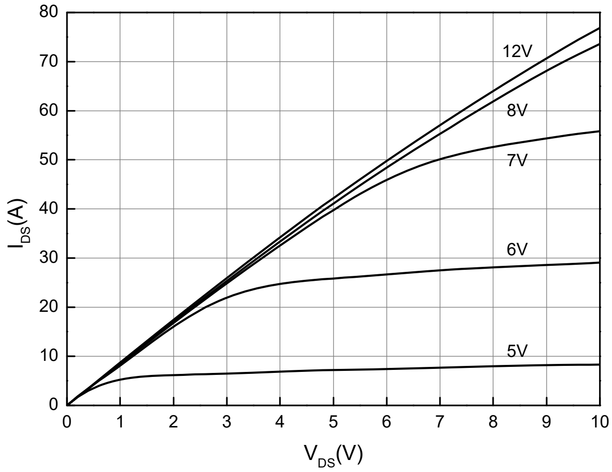


Figure 2. Typical Output Characteristics at T_J = 150°C (Parameter: V_{GS})

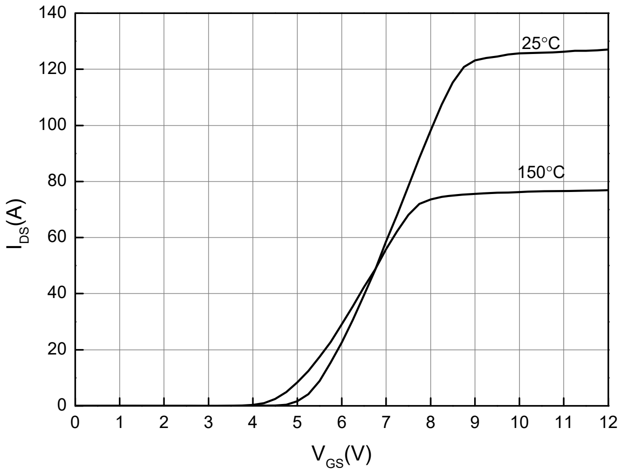


Figure 3. Typical Transfer Characteristics (V_{DS} = 10V, Parameter: T_J)

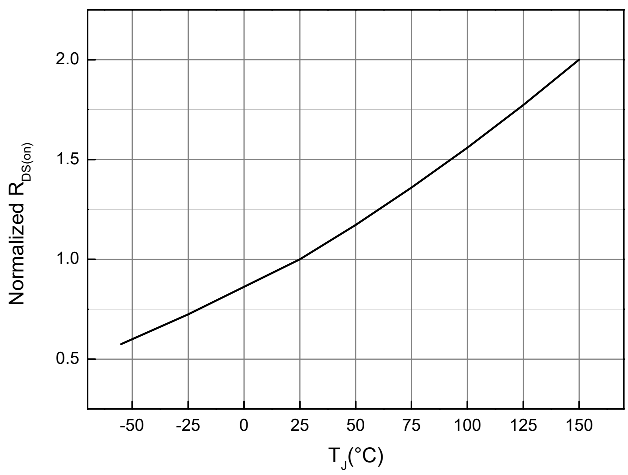


Figure 4. Normalized On-Resistance (I_D = 16A, V_{GS} = 10V)

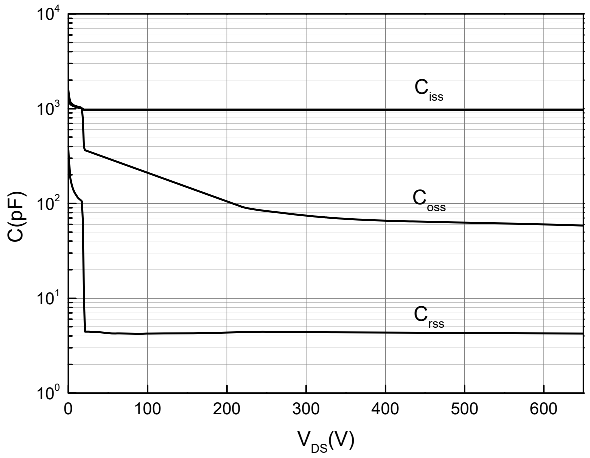


Figure 5. Typical Capacitance
(V_{GS} = 0V, *f* = 500kHz)

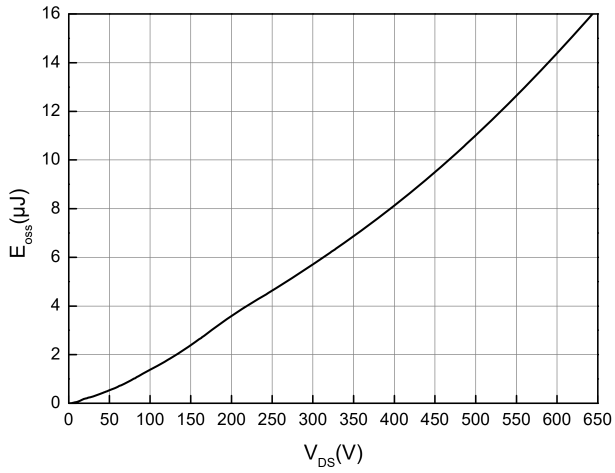


Figure 6. Typical C_{oss} Stored Energy

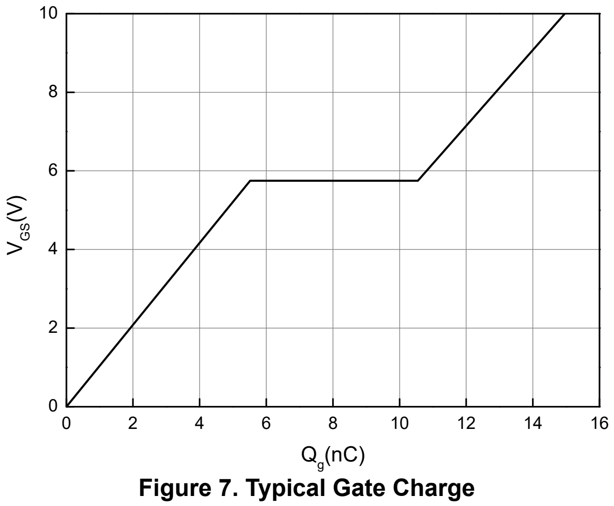


Figure 7. Typical Gate Charge
(I_{DS} = 16A, V_{DS} = 400V)

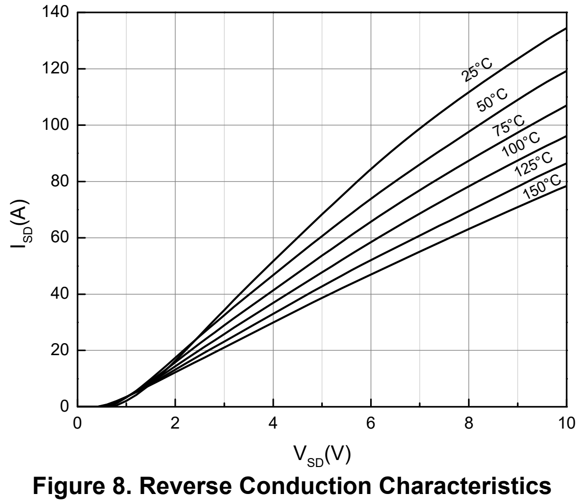


Figure 8. Reverse Conduction Characteristics
(-20V ≤ V_{GS} ≤ 0V, Parameter: T_J)

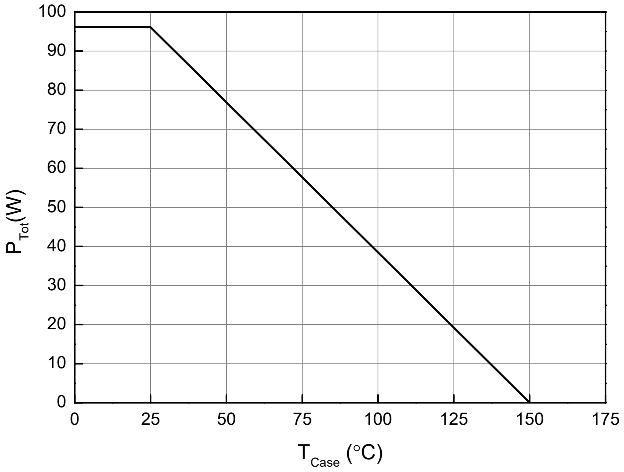


Figure 9. Power Dissipation

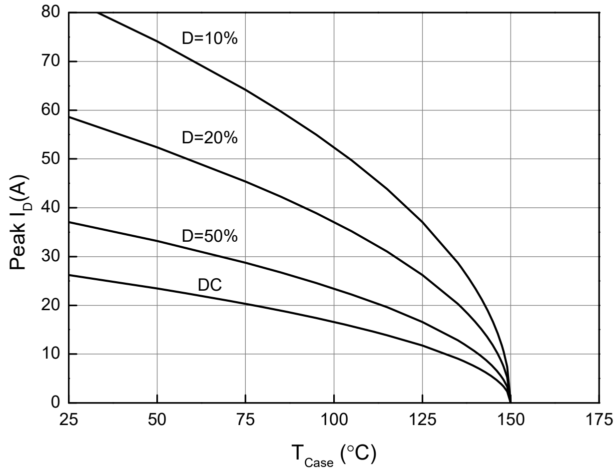


Figure 10. Current Derating
(Pulse Width ≤ 10μs, V_{GS} ≥ 10V)

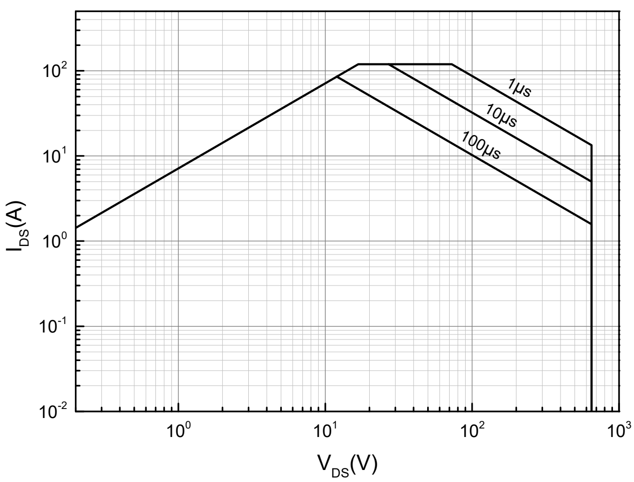


Figure 11. Safe Operating Area at T_C = 25°C

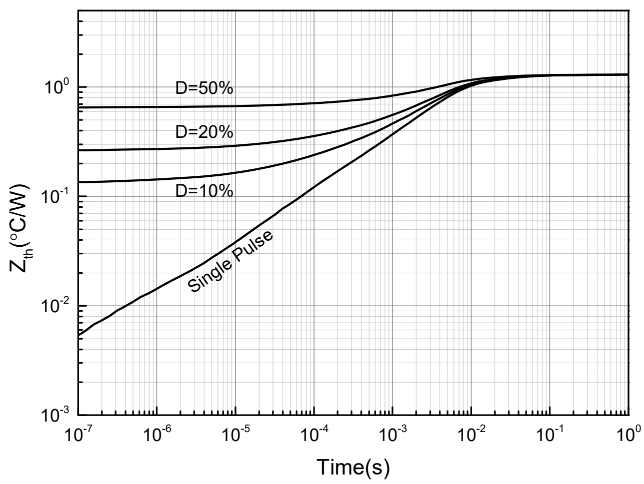


Figure 12. Transient Thermal Resistance

6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

DO	DO NOT
Place gate driver close to the GaN device and separate input traces from output traces	Use long gate drive traces, long lead length and route the output traces next to the input
Use gate ferrite bead and dc-link RC snubber	Use close-by decoupling capacitor without series resistor
Minimize trace length of the PCB layout for both drive loop and power loop	Use a traditional differential voltage probe for V_{gs} of high side device

7. Circuit Implementation

Half-bridge Schematic

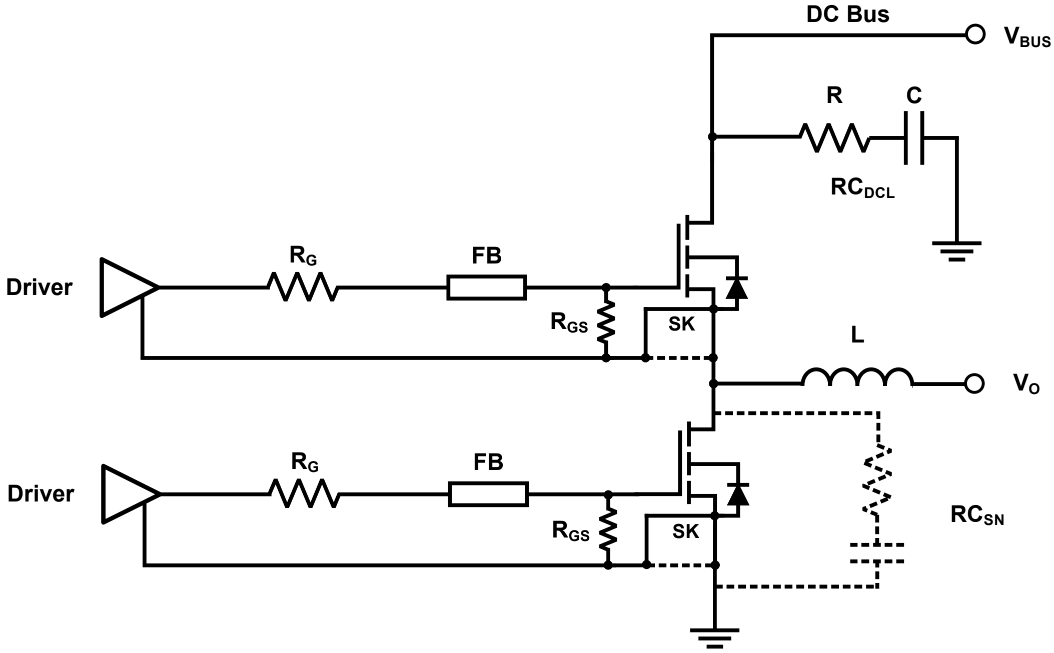


Figure 13. Simplified half-bridge schematic

Recommended gate drive: (0V, 10-12V) with R_G = 30Ω [a)]

Gate Ferrite Bead (FB) [b)]	Required DC Link RC Snubber (RC_{DCL}) [c)]	Recommended Switching Node RC Snubber (RC_{SN})
100-330Ω@100MHz	(10nF+10Ω) × 2	Not necessary, see note **d** and **e** below

Notes:

a) For bridge topologies only. R_G could be smaller in single ended topologies.

b) Examples of material selection: MPZ2012S***AT000(TDK), BLM21PG***SZ1D(Murata).

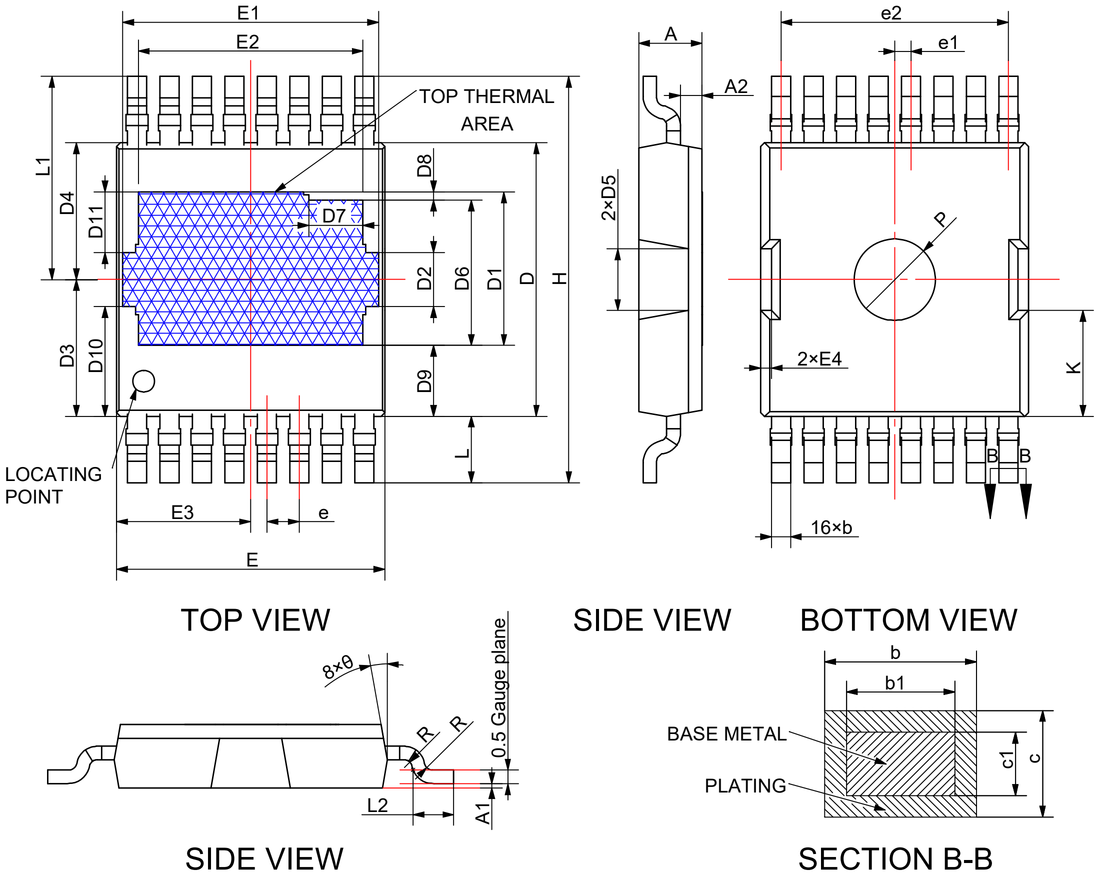
c) RC_{DCL} should be placed as close as possible to the drain pin. Other decoupling capacitors should be located away from the RC_{DCL}.

d) RC_{SN} is needed only if R_G is smaller than recommendations.

e) If required, please use 15Ω+68pF.

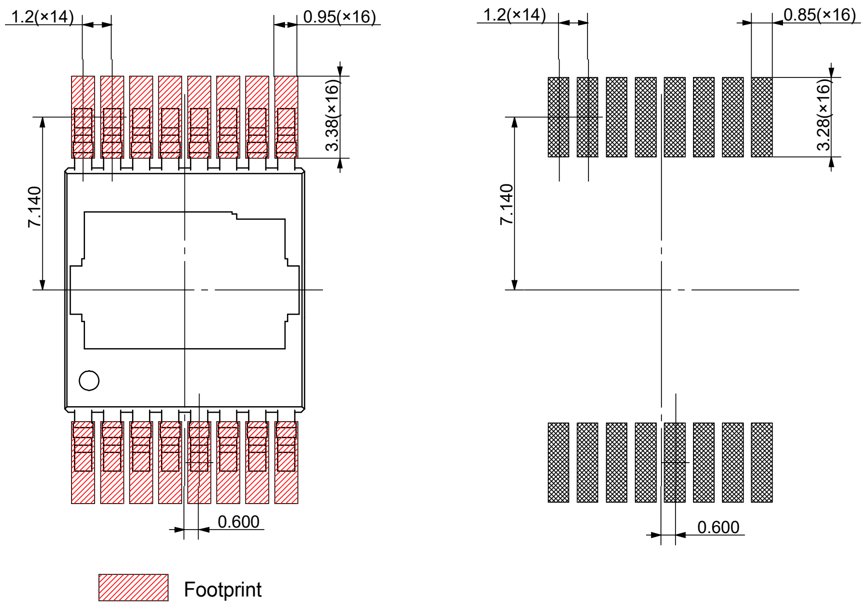
f) The typical value of R_{GS} is 10kΩ.

8. Package Dimensions



DIM.	Millimeters			DIM.	Millimeters		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	2.20	2.30	2.35	D11	2.04	2.24	2.44
A1	0.01	-	0.11	E	9.70	9.90	10.10
A2	0.56	0.76	0.96	E1	9.26	9.46	9.66
b	0.60	0.75	0.85	E2	8.10	8.30	8.50
b1	0.60	0.70	0.80	E3	4.75	4.95	5.15
c	0.45	0.55	0.65	E4	0.20	0.40	0.60
c1	0.45	0.50	0.60	e	1.20 BSC		
D	10.00	10.10	10.30	e1	0.60 BSC		
D1	5.47	5.67	5.87	e2	8.40 BSC		
D2	1.80	2.00	2.20	H	14.80	15.00	15.20
D3	4.85	5.05	5.25	K	3.71	3.91	4.11
D4	5.00	5.05	5.13	L	2.25	2.45	2.65
D5	2.08	2.28	2.48	L1	7.30	7.50	7.70
D6	5.17	5.37	5.57	L2	1.30	1.50	1.70
D7	1.80	2.00	2.20	R	0.07	-	-
D8	0.10	0.30	0.50	P	2.90	3.00	3.10
D9	2.42	2.62	2.82	θ	4 °	-	10 °
D10	3.85	4.05	4.25				
TOLT							
GaNext							
Date：2023.06				Rev.01			

9. Recommended PCB Land Pattern



Recommended PCB Land Pattern

Recommended stencil apertures
(Based on stencil thickness of 0.130mm)

10. Part Marking