

Low Voltage 3Ω SPDT Analog Switch

Features

- Single Supply Voltage Range: 1.8V to 5.5V
- Low On-Resistance: 3Ω (TYP) at $V_+ = 4.5V$
- Fast Switching Times:
 - t_{ON} : 70ns (TYP)
 - t_{OFF} : 40ns (TYP)
- Low On-Resistance Flatness
- -3dB Bandwidth: 400MHz
- High Off-Isolation: -50dB at 10MHz
- TTL/CMOS Compatible
- Rail-to-Rail Single Range
- Break-Before-Make Switching
- Operation Temperature Range: -40°C to 105°C
- Available in a Green SC70-6 Package

Applications

Battery-powered equipment
 Personal digital assistants
 Portable electronic device
 Audio and video signal routing

Typical Application Circuit

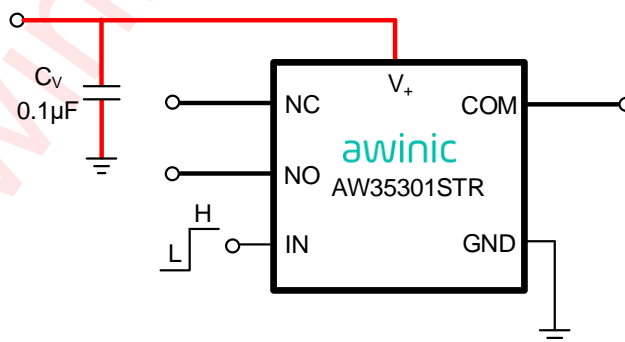


Figure 1 Typical Application Circuit of AW35301STR

General Description

AW35301STR is a high performance, bidirectional, SPDT (single-pole/double-throw) analog switch that features ultra-low R_{ON} of 3Ω (TYP) at 4.5V V_+ . It operates over a wide V_+ range of 1.8V to 5.5V and is designed for break-before-make operation. The select input is TTL-level compatible.

AW35301STR features very low quiescent current even when the control voltage is lower than the V_+ supply. This feature makes it very suitable for multiple applications, such as portable electronic device, audio and video signal routing, etc. Low power consumption is also one of the important reasons that make it a good choice.

AW35301STR is available in a Green SC70-6 package. It operates over an ambient temperature range of -40°C to 105°C.

Pin Configuration And Top Mark

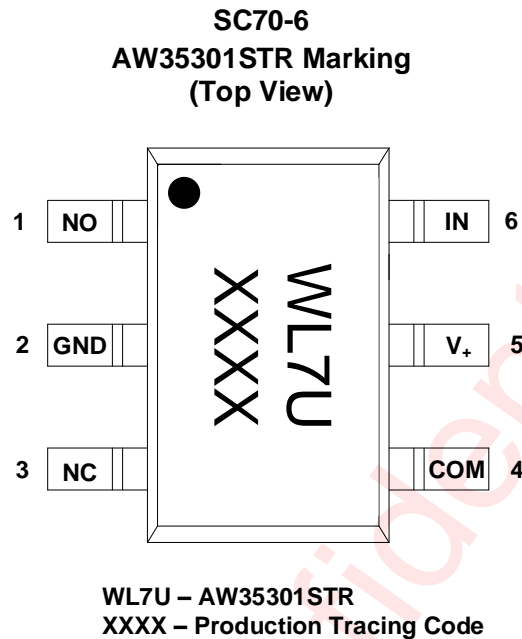


Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
1	NO	Data port (normally open)
2	GND	Ground
3	NC	Data port (normally closed)
4	COM	Common data port
5	V+	Positive power supply
6	IN	Logic control pin to connect the COM pin to the NO or NC pin

Function Table

IN	NC to COM, COM to NC	NO to COM, COM to NO
L	ON	OFF
H	OFF	ON

To allow signals to pass between the NC and COM pins you must set the logic control IN pin low.
To allow signals to pass between the NO and COM pins you must set the logic control IN pin high.

Functional Block Diagram

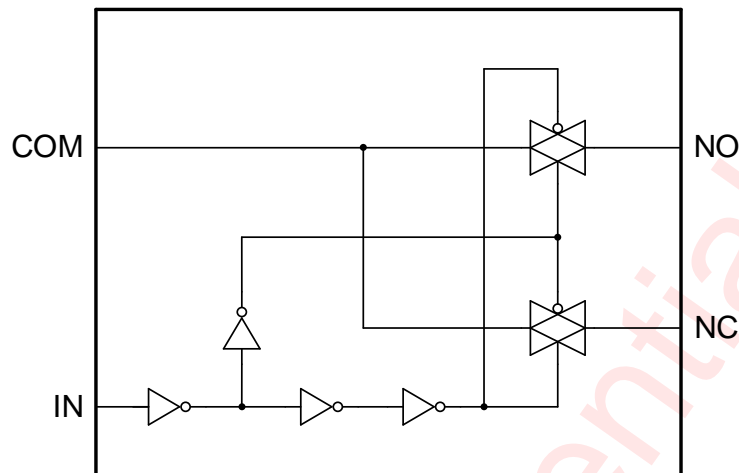


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35301STR	-40°C ~ 105°C	SC70-6	WL7U	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply voltage range V_+	-0.3V to 6V
Logic control input voltage range V_{IN}	-0.3V to 6V
Switch I/O port voltage	-0.3V to $(V_+)+0.3V$
Continuous current NO, NC or COM	$\pm 50mA$
Peak current NO, NC or COM	$\pm 80mA$
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM (Human body model) ^(NOTE2)	$\pm 2kV$
CDM(Charged device model) ^(NOTE3)	$\pm 1.5kV$
Latch-Up	
Latch-Up ^(NOTE4)	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE4: Test Condition: JEDEC78E.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_+	Supply voltage	1.8		5.5	V
V_{IN}	Logic control input voltage	0		V_+	V
V_{NC}, V_{NO}, V_{COM}	Switch I/O port voltage	0		V_+	V
t_r, t_f	Input transition rise and fall rate			10	ns/V
Temp	Operating temperature range	-40		105	°C
C_{V_+}	V_+ capacitance		0.1		μF

Electrical Characteristics— $V_+=5V$

Unless noted otherwise, V_+ voltage range of 4.5V to 5.5V, operating temperature range of -40°C to $+105^{\circ}\text{C}$. Typical values are guaranteed for $V_+=5V$, $T_A=25^{\circ}\text{C}$.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ANALOG SWITCH						
V_{NO}, V_{NC}, V_{COM}	Analog signal range		0		V_+	V
R_{ON}	On-resistance	$V_+=4.5V, 0V \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -10mA$, Test Circuit 1		3	4	Ω
ΔR_{ON}	On-resistance match between channels	$V_+=4.5V, 0V \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -10mA$, Test Circuit 1		0.2	0.5	Ω
$R_{FLAT(ON)}$	On-resistance flatness	$V_+=4.5V, 0V \leq V_{NO}$ or $V_{NC} \leq V_+$, $I_{COM} = -10mA$, , Test Circuit 1		0.6	1	Ω
I_+	Power supply current	$V_+=5V, V_{IN}=0V$ or $5V$			1	μA
$I_{NO(OFF)}, I_{NC(OFF)}$	Switch off leakage current	$V_+=5V, V_{NO}$ or $V_{NC}=1V, 4.5V$, $V_{COM}=4.5V, 1V$			1	μA
$I_{NO(ON)}, I_{NC(ON)}, I_{COM(ON)}$	Switch on leakage current	$V_+=5V, V_{COM}=1V, 4.5V, V_{NO}$ or $V_{NC}=1V, 4.5V$ or floating			1	μA
LOGIC CONTROL INPUTS						
V_{INH}	Input High Voltage	$V_+=4.5V$	1.1			V
V_{INL}	Input Low Voltage	$V_+=4.5V$			0.45	V
I_{IN}	Input Leakage Current	$V_+=5.5V, V_{IN} = 0V$ or $5.5V$		0.4	1	μA
DYNAMIC CHARACTERICS						
t_{ON}	Switch turn-on time	V_{NO} or $V_{NC}=3V, R_L=300\Omega$, $C_L=35pF$, Test Circuit 2		70		ns
t_{OFF}	Switch turn-off time	V_{NO} or $V_{NC}=3V, R_L=300\Omega$, $C_L=35pF$, Test Circuit 2		40		ns
t_{BBM}	Break-Before-Make time	V_{NO} or $V_{NC}=3V, R_L=300\Omega$, $C_L=35pF$, Test Circuit 3		40		ns
O_{ISO}	Off isolation	Signal=0dBm, $R_L=50\Omega, C_L=5pF$, Test Circuit 4	f=10MHz	-50		dB
			f=1MHz	-75		dB
BW	-3dB bandwidth	Signal=0dBm, $R_L=50\Omega, C_L=5pF$, Test Circuit 5		400		MHz
Q	Charge injection	$C_L=1nF$		10		pC
C_{ON}	On capacitance	f=1MHz		15		pF

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C _{OFF}	Off capacitance	f=1MHz		5		pF

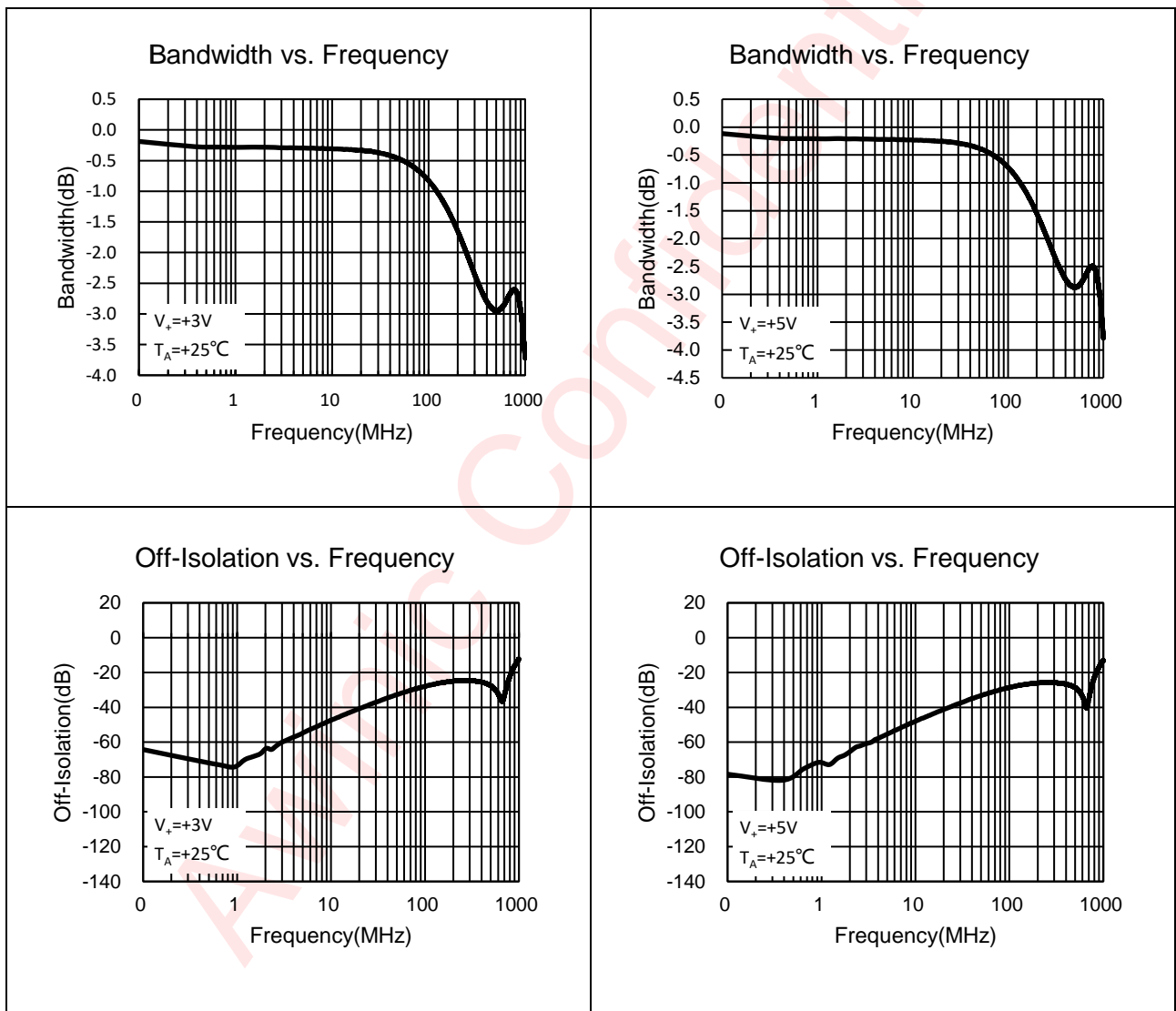
Electrical Characteristics—V₊=3V

Unless noted otherwise, V₊ voltage range of 2.7V to 3.6V, operating temperature range of -40°C to +105°C. Typical values are guaranteed for V₊=3V, TA=25°C.

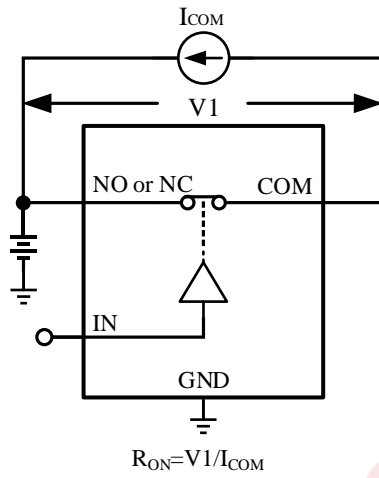
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ANALOG SWITCH						
V _{NO} , V _{NC} , V _{COM}	Analog signal range		0		V ₊	V
R _{ON}	On-resistance	V ₊ =2.7V, 0V ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = -10mA, Test Circuit 1		6	7.5	Ω
ΔR _{ON}	On-resistance match between channels	V ₊ =2.7V, 0V ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = -10mA, Test Circuit 1		0.3	0.6	Ω
R _{FLAT(ON)}	On-resistance flatness	V ₊ =2.7V, 0V ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = -10mA, Test Circuit 1		3	4	Ω
I ₊	Power supply current	V ₊ =3.6V, V _{IN} =0V or 3.6V			1	μA
I _{NO(OFF)} , I _{NC(OFF)}	Switch off leakage current	V ₊ =3.6V, V _{NO} or V _{NC} =0.3V, 3.3V, V _{COM} =3.3V, 0.3V			1	μA
I _{NO(ON)} , I _{NC(ON)} , I _{COM(ON)}	Switch on leakage current	V ₊ =3.6V, V _{COM} =0.3V, 3.3V, V _{NO} or V _{NC} =0.3V, 3.3V or floating			1	μA
LOGIC CONTROL INPUTS						
V _{INH}	Input High Voltage	V ₊ =2.7V	1.0			V
V _{INL}	Input Low Voltage	V ₊ =2.7V			0.36	V
I _{IN}	Input Leakage Current	V ₊ =3.6V, V _{IN} =0V or 3.6V,		0.4	1	μA
DYNAMIC CHARACTERISTICS						
t _{ON}	Switch turn-on time	V _{NO} or V _{NC} =1.5V, R _L =300Ω, C _L =35pF, Test Circuit 2		140		ns
t _{OFF}	Switch turn-off time	V _{NO} or V _{NC} =1.5V, R _L =300Ω, C _L =35pF, Test Circuit 2		80		ns
t _{BBM}	Break-Before-Make time	V _{NO} or V _{NC} =1.5V, R _L =300Ω, C _L =35pF, Test Circuit 3		65		ns
O _{ISO}	Off isolation	Signal=0dBm, R _L =50Ω, C _L =5pF, Test Circuit 4	f=10MHz		-50	dB
			f=1MHz		-75	dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BW	-3dB bandwidth	Signal=0dBm, $R_L=50\Omega$, $C_L=5pF$, Test Circuit 5		400		MHz
Q	Charge injection	$C_L=1nF$		5		pC
C_{ON}	On capacitance	$f=1MHz$		15		pF
C_{OFF}	Off capacitance	$f=1MHz$		5		pF

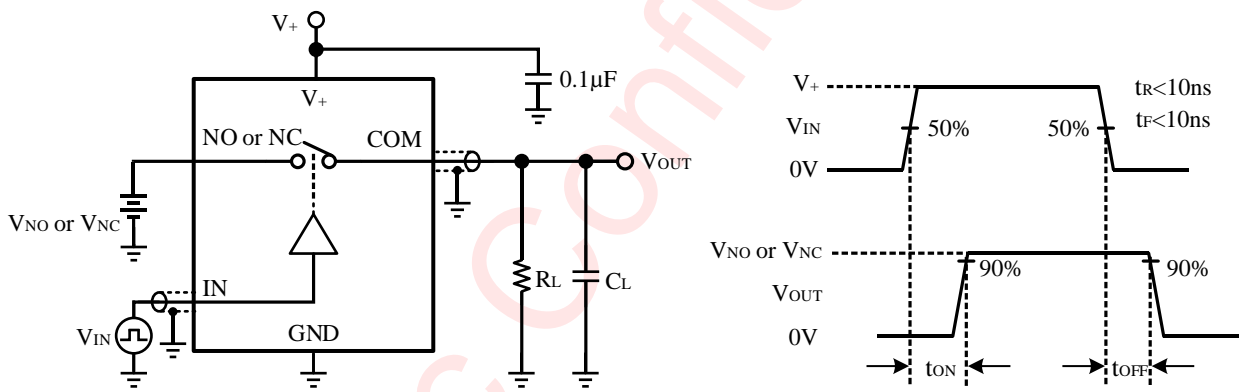
Typical Characteristics



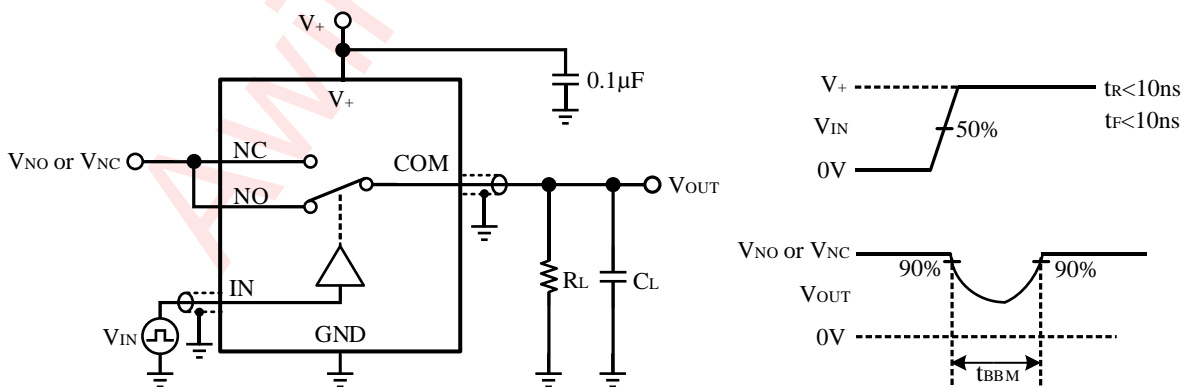
Test Circuits



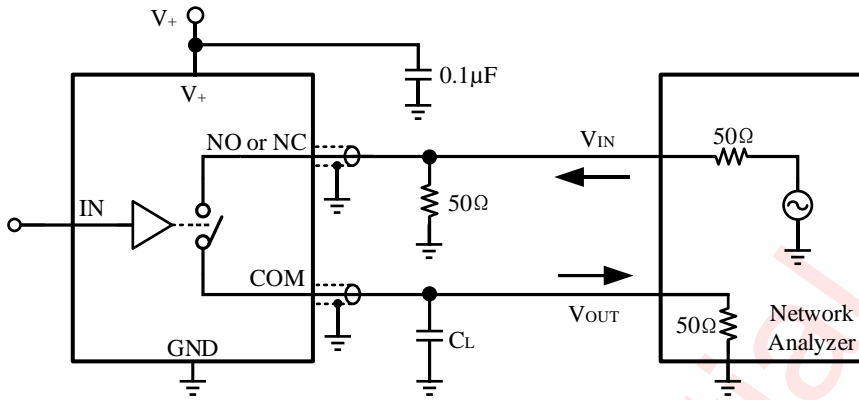
Test Circuit 1 On-Resistance



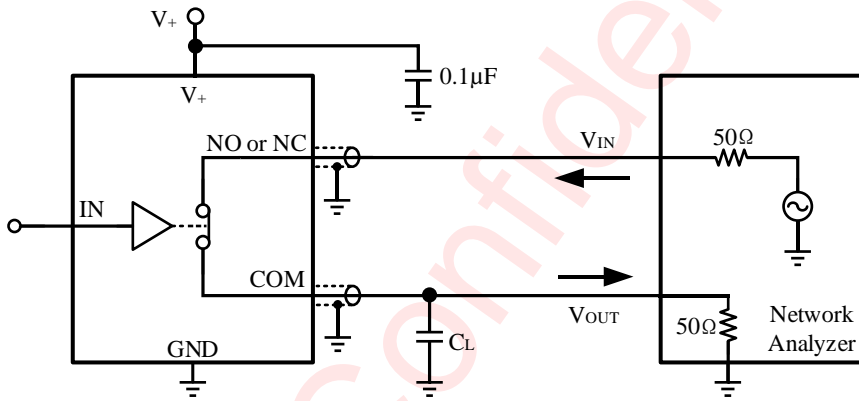
Test Circuit 2 Switching Times



Test Circuit 3 Break-Before-Make Time Delay (t_{BBM})



Test Circuit 4 Off Isolation

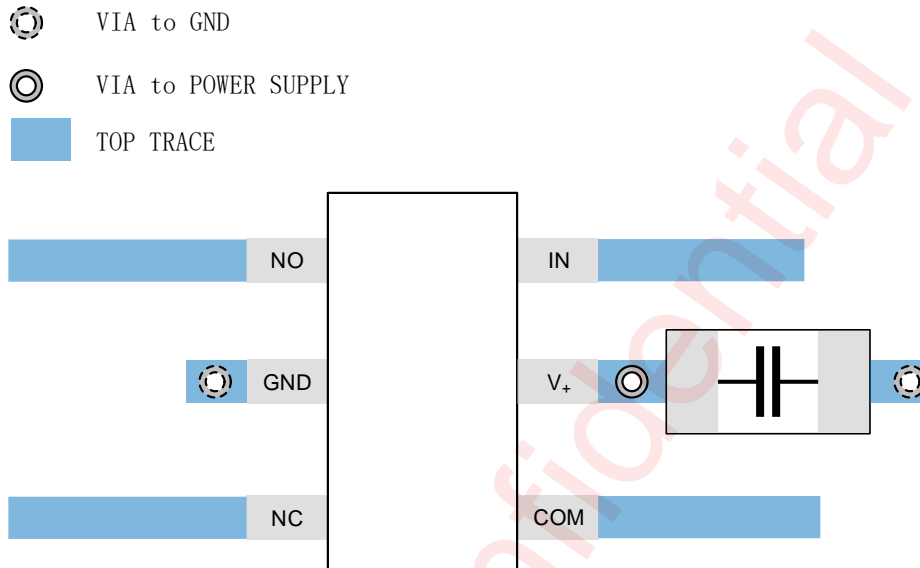


Test Circuit 5 -3dB Bandwidth

PCB Layout Consideration

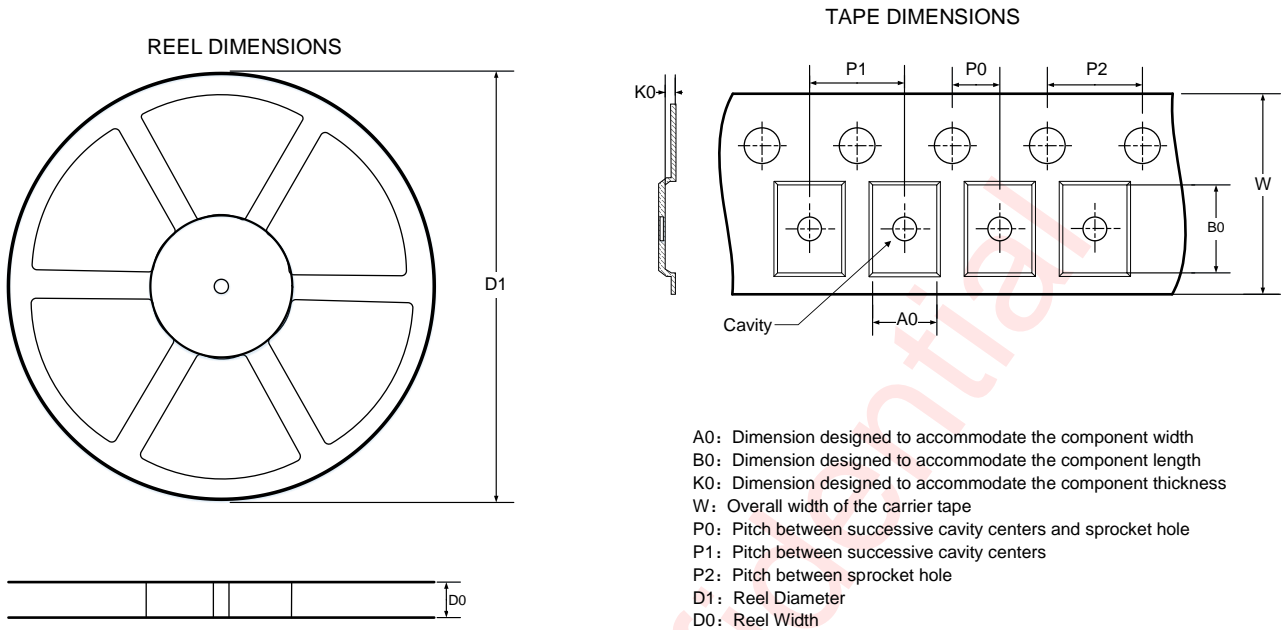
It is recommended to place a bypass capacitor as close to the supply pin V_+ as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Minimize trace lengths and vias on the single paths in order to preserve signal integrity.

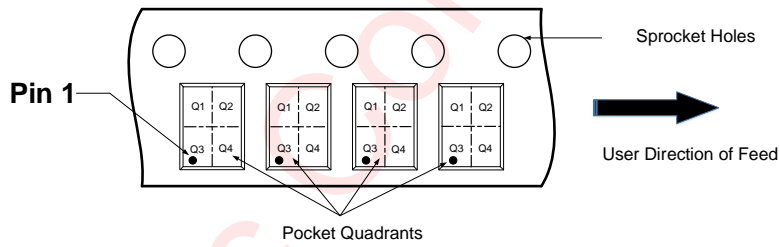


Test Circuit 6 PCB Layout example

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



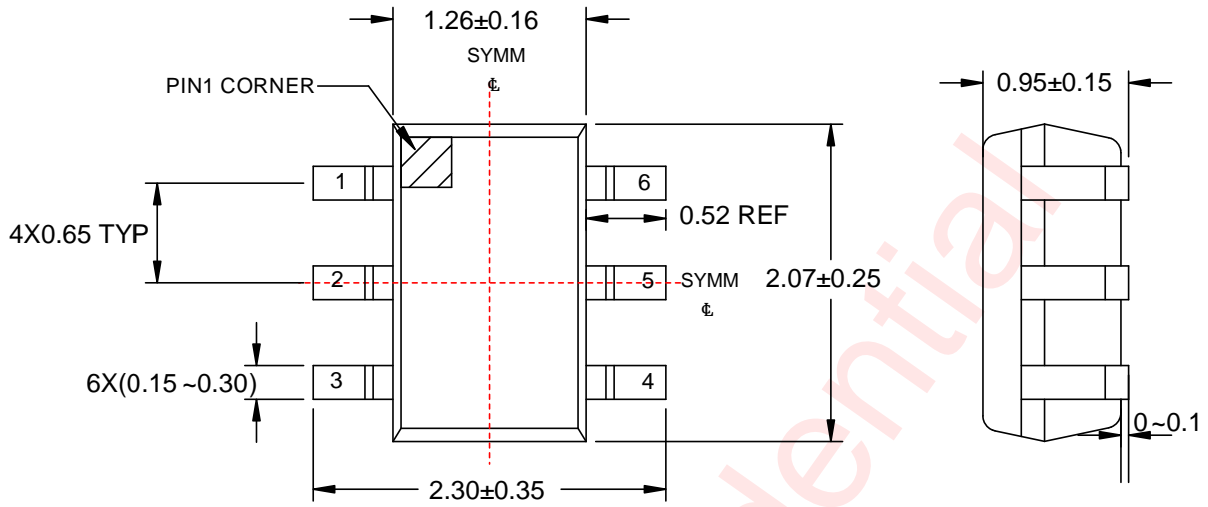
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.4	2.55	1.2	2	4	4	8	Q3

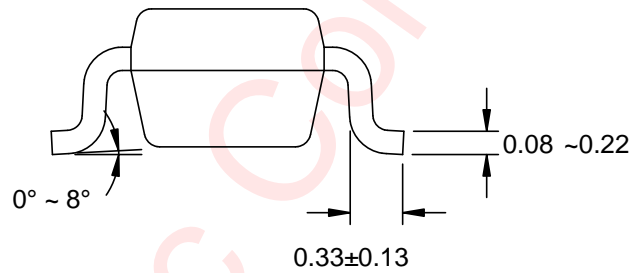
All dimensions are nominal

Package Description



Top View

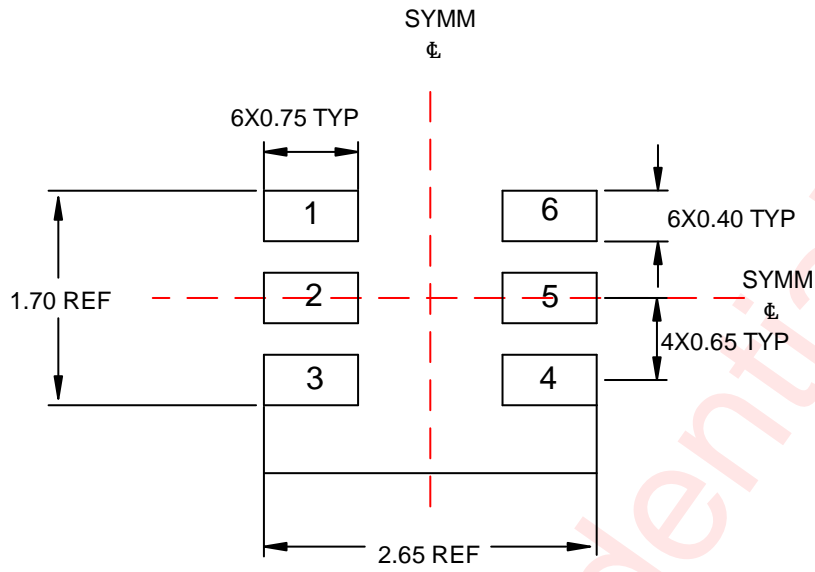
Side View



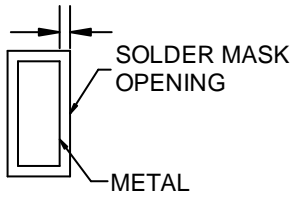
Side View

Unit:mm

Land Pattern Data

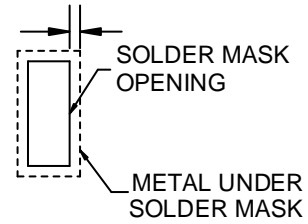


0.05 MAX
All AROUND



NON SOLDER MASK DEFINED

0.05 MIN
All AROUND



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Mar. 2023	Datasheet V1.0 released
V1.1	May 2024	<p>P5, P6: VBAIS=5V update to $V_+=5V$, VBAIS=3V update to $V_+=3V$;</p> <p>P5, P6: Update t_{on}, t_{off}, t_{bbm}, test condition from $R_L=50\Omega$ to $R_L=300\Omega$.</p> <p>P5: Update V_{INL} MAX value from 0.5 to 0.45;</p> <p>P6: Update V_{INL} MAX value from 0.4 to 0.36;</p> <p>P5: Update Switch on leakage current test condition from $V_+=5V$, V_{NO} or $V_N=1V$, 4.5V, $V_{COM}=1V$, 4.5V or floating to $V_+=5V$, $V_{COM}=1V$, 4.5V, V_{NO} or $V_{NC}=1V$, 4.5V or floating</p> <p>P6: Update Switch on leakage current test condition from $V_+=3.6V$, V_{NO} or $V_N=0.3V$, 3.3V, $V_{COM}=0.3V$, 3.3V or floating to $V_+=3.6V$, $V_{COM}=0.3V$, 3.3V, V_{NO} or $V_{NC}=0.3V$, 3.3V or floating</p> <p>Modify package description SOT363-6L to SC70-6.</p>

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