3.2W I²S/TDM Input, Plug-and-Play, High Efficiency, Digital Smart K Audio Amplifier

Features

- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 10μV**
- **Low shutdown current:0.02uA**
- **Fast turn-on times：1ms**
- **THD+N: 0.02%**
- Supports 4Ω Speaker
- Extensive Pop-Click Suppression
- Support spread spectrum
- I²S interface：
  - Standard I²S (A/C), Left-Justified (B/D)
  - Supports 4/6/8 slots TDM (One Subframe)
  - Only supports 8 slots TDM (One Bit Clock)
  - Input Sample Rates from 8kHz to 96kHz
  - Data Width: 16, 20, 24, 32 Bits
- Simplified interface for audio and general settings
- Power Supplies：
  - VDD：2.5V-5.5V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection
- WLCSP 1.403mmX1.183mm-9B package

Applications

- IOT Devices
- Portable Audio Devices

Description

AW88084A is a member of the AW88084A/B/C/D series. This series comprises four models (A/B/C/D) of I²S/TDM input digital audio amplifiers. The digital audio interface configuration is achieved via resistor pull-up on the EN pin, eliminating the need for I²C programming.

The AW88084A/B/C/D series ensures clean audio performance with a 10μV noise floor and ultra-low distortion, while delivering 3.2W output power into 4Ω speakers at 10% THD+N.

The AW88084A/B/C/D series features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface.

The AW88084A/B/C/D series support spread spectrum and edge-rate limiting to enhance EMI performance while reduces output filter size and cost.

The AW88084A/B/C/D series offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection to protect the device.

AW88084A/B have a fast 1ms turn-on time, while AW88084C/D ramp the volume over 13ms during turn-on and turn-off.

The AW88084A/B/C/D series is available in a WLCSP 1.403mmX1.183mm-9B package. All versions share identical pin definitions.

Pin Configuration and Top Mark

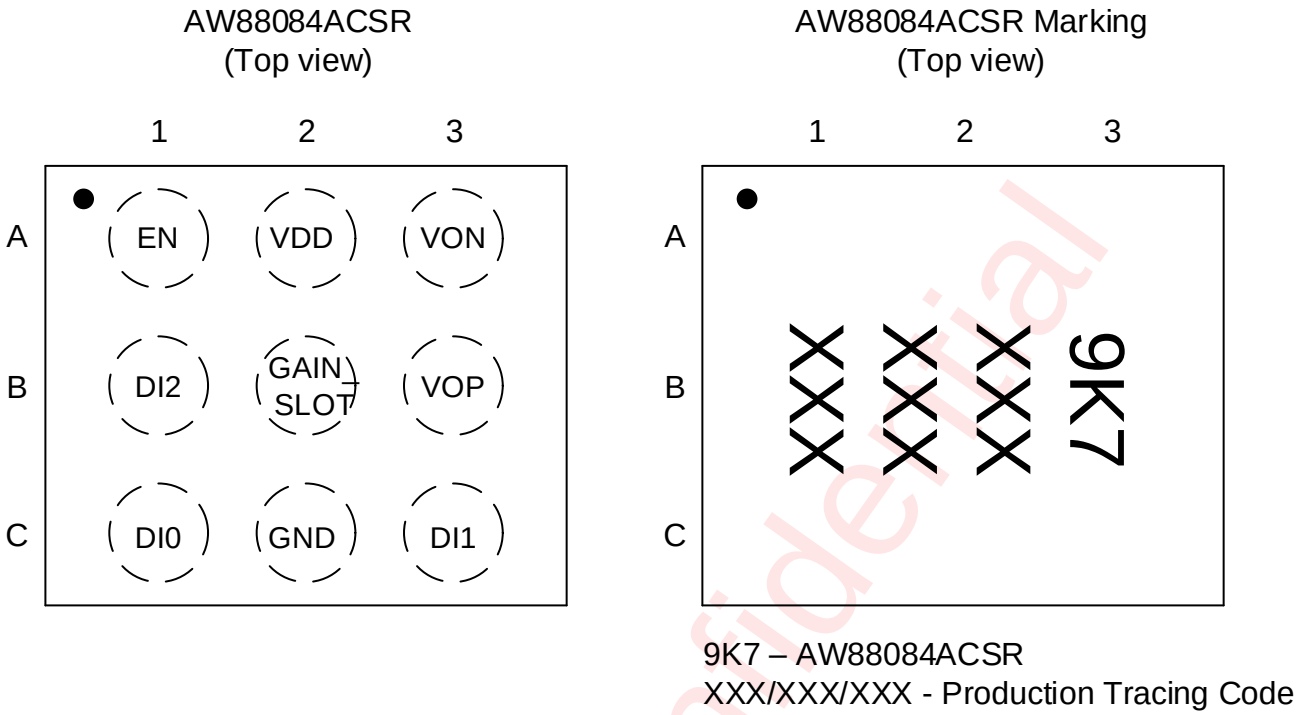

Figure 1 AW88084ACSR pin diagram top view and device marking

Pin Description

Pin No	Pin Name	Description
A1	EN	Enable pin (active High)
A2	VDD	Battery power supply
A3	VON	Inverting Class-D output
B1	DI2	Digital Audio Interface Pin 2
B2	GAIN_SLOT	Gain and Channel Selection
B3	VOP	Non-inverting Class-D output
C1	DI0	Digital Audio Interface Pin 0
C2	GND	GND
C3	DI1	Digital Audio Interface Pin 1

AWINIC AW88084 Family *Note*

Amplifier Name	Turn on&off mode	I²S		TDM		
		Configuration	Edge sampling	Invert	Shift-left	Edge sampling
AW88084**A**CSR	Fast	Standard I²S	Rising	N	Y	Rising
AW88084**B**CSR	Fast	Left-Justified.	Rising	N	N	Trailing
AW88084**C**CSR	Ramp	Standard I²S	Rising	N	Y	Rising
AW88084**D**CSR	Ramp	Left-Justified.	Rising	N	N	Trailing

Note **：** *Please refer to the Detailed Functional Description for detailed differences in audio data formats between different versions*

Functional Block Diagram

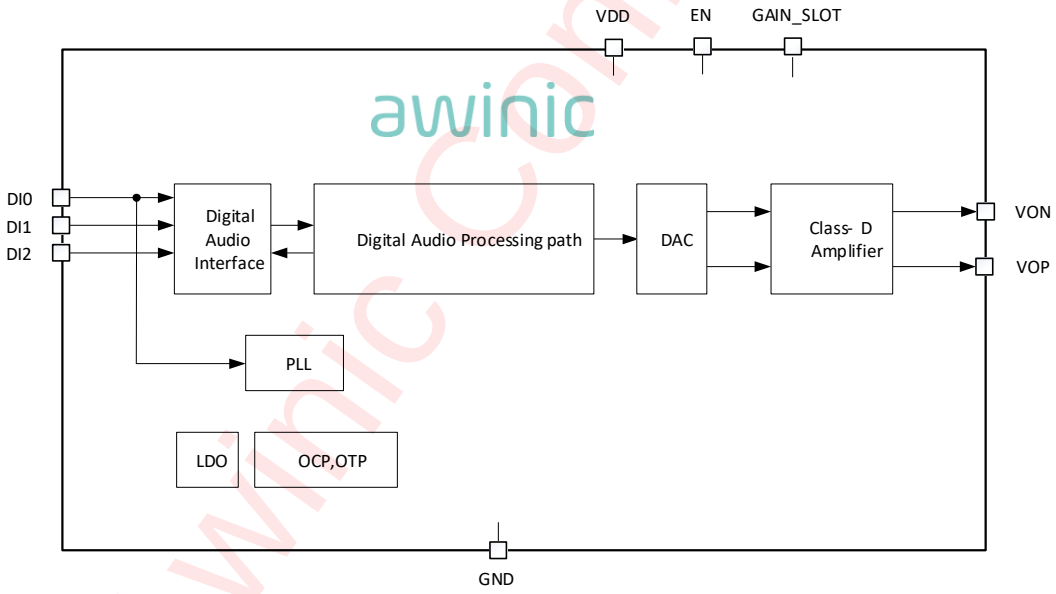

Figure 3 FUNCTIONAL BLOCK DIAGRAM

Application Diagram

I²S MODE:

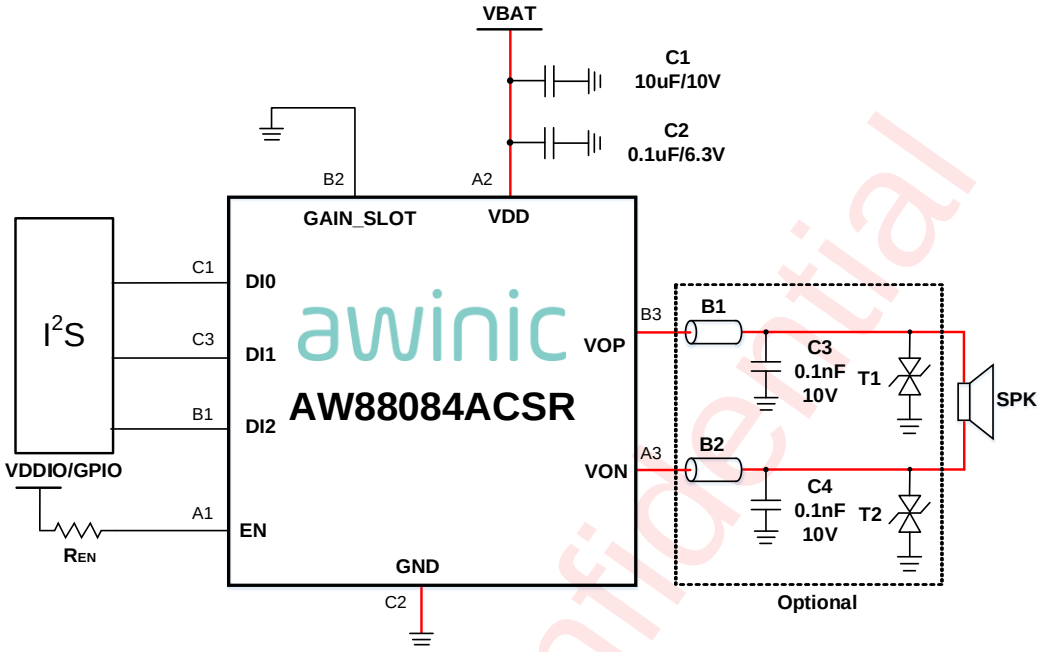

Figure 4 I²S/Left-Justified Left-Channel Application

TDM MODE:

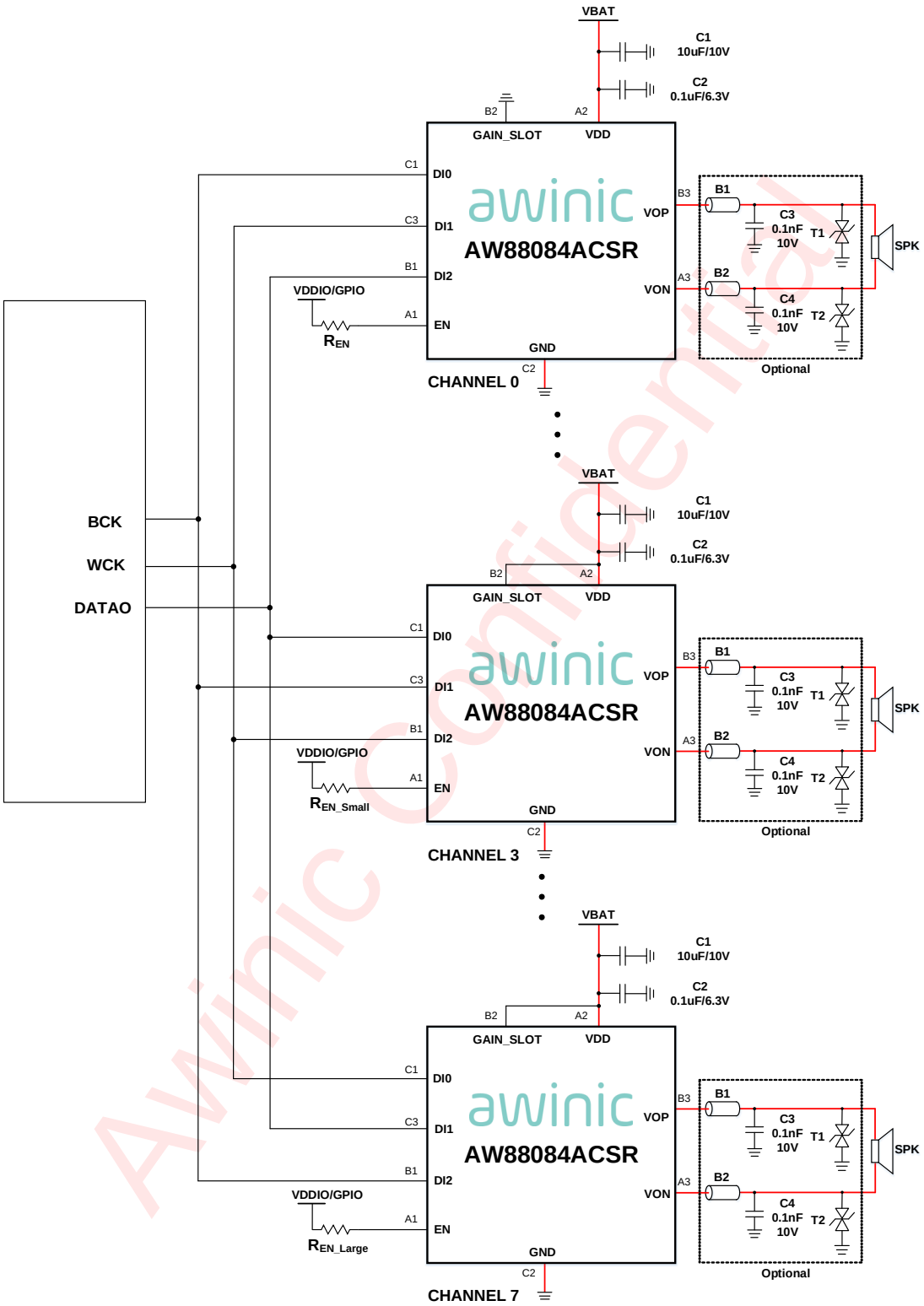

Figure 5 TDM Mode Application

Note: Traces carry high current are marked in red in the above figure

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Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW88084ACSR	-40℃～85℃	WLCSP 1.403mmX1.183 mm-9B	9K7	MSL1	ROHS+HF	2500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATING(NOTE1)

Parameter	Range
Battery Supply Voltage and Digital Interface Voltage (VDD, DI0, DI1, DI2 pins)	-0.3V to 6V
All other pins to GND	-0.3V to V_{VDD}+0.3V
Minimum load resistance R_L	3.2Ω(Note2)
Package Thermal Resistance θ_{JA}	156°C/W(Note3)
Ambient Temperature Range	-40°C to +85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating (Note 4, 5)	
HBM (Human Body Model)	±2000V
CDM (Charge Device Model)	±1500V
Latch-up	
Test Condition：JESD78F.02	+IT: 200mA
	-IT: 200mA

Note 1：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2：*Only support Micro Speaker when the Load resistance RL is less than 5Ω;*

Note 3：*The thermal resistance of the package is a simulated value;*

Note 4：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2024; (Zap 1 pulse, Interval: >=0.1S);*

Note 5：*Test method: ESDA/JEDEC JS -002-2025*

Electrical Characteristics

Test condition: T_A=25°C, VDD=5V, Gain=14.3dB, R_L=8Ω+33μH, f_{wck}=48kHz, f=1kHz (unless otherwise noted)

Symbol	Description	Condition	MIN	TYP	MAX	Units
VDD	Supply Voltage Range		2.5		5.5	V
I_{VDD}	Static VDD supply current	Operating mode; VDD=3.7V		1.8		mA
		EN = 1.8V, TA = +25°C, VDD=5V, all DI pins at 0V		1.5	3	μA
		EN = 1.8V, TA = +25°C, VDD=5V, no toggling on DI pins		10	49	μA
		EN = 0V, TA = +25°C, VDD=5V		0.02	0.5	μA
T_{on}	Turn on time	Time from shutdown or standby to Operating (AW88084A/B)		1		ms
		Time from shutdown or standby to Operating (AW88084C/D)		13		ms
Class D						
P_{out}	RMS Output Power	VDD=3.7V, RL=4Ω+33μH				
		THD+N=1%		1.4		W
		THD+N=10%		1.75		W
		VDD=5.0V, RL=4Ω+33μH				
		THD+N=1%		2.5		W
		THD+N=10%		3.2		W
		VDD=3.7V, RL=8Ω+33μH				
		THD+N=1%		0.77		W
		THD+N=10%		0.95		W
		VDD=5.0V, RL=8Ω+33μH				
		THD+N=1%		1.4		W
		THD+N=10%		1.75		W
		THD+N=1%, RL=20Ω+33μH				
		VDD=3.7V		0.3		W
		VDD=5.0V		0.58		W
Vos	Output offset voltage	I^2S signal input 0	-1		1	mV
f_{PWM}	PWM Switching Frequency	VDD = 2.5V to 5.5V	332.5	350	367.5	kHz
f_{SS}	Spread-Spectrum Bandwidth	VDD = 2.5V to 5.5V		±17.5		kHz
Eff	Total Efficiency	THD+N=10%, RL=8Ω+33μH, VDD=5V		92		%

Symbol	Description	Condition	MIN	TYP	MAX	Units
FR	Frequency Response		-0.2		0.3	dB
E_N	Output Noise	A-weighting		10		μV
THD+N	Total harmonic distortion plus noise	f=1kHz, Pout=0.7W, RL=8Ω		0.02		%
SNR	Signal-to-noise ratio	VDD=5V Po=0.3W, RL=20Ω		108		dB
DNR	Dynamic Range	A-weighted, -60dBFS Method,		108		dB
PSRR	Power supply rejection ratio	F=217Hz, V_{ripple}=200mV		81		dB
		F=1kHz, V_{ripple}=200mV		81		dB
Gain	Total Gain	I^2S/Left-justified mode Connect Gain_Slot PIN to GND		14.3		dB
		I^2S/Left-justified mode Gain_Slot PIN unconnected		11.3		dB
		I^2S/Left-justified mode Connect Gain_Slot PIN to VDD		8.3		dB
		TDM mode		14.3		dB
DAC DIGITAL FILTERS/ NONLINEAR FIR LOWPASS FILTER (LRCLK < 30kHz)						
f_{pass}	Passband	Ripple < δ_P	0.405*fs			Hz
		Droop < 3dB	0.449*fs			Hz
f_{stop}	Stopband	Attenuation > δ_S			0.559*fs	Hz
δ_P	Passband Ripple	f < f_{Pass}, referenced to signal level at 1kHz	-0.05		+0.05	dB
δ_S	Stopband Attenuation	f > f_{stop}	74.6			dB
DAC DIGITAL FILTERS/ LINEAR FIR LOWPASS FILTER (LRCLK ≥ 30kHz)						
f_{pass}	Passband	Ripple < δ_p	0.405*fs			Hz
		Droop < 3dB	0.455*fs			Hz
f_{stop}	Stopband	Attenuation > δ_S			0.589*fs	Hz
δ_p	Passband Ripple	f < f_{Pass}, referenced to signal level at 1kHz	-0.05		+0.05	dB
δ_S	Stopband Attenuation	f > f_{stop}	74.6			dB
DAC DIGITAL FILTERS/DIGITAL DC BLOCKING FILTER						
f_C	DC Blocking Filter - 3dB Cutoff Frequency	Fs=96kHz		1.86		Hz
		Fs=48kHz		1.86		
		Fs=44.1kHz		1.71		
		Fs=8kHz		1.24		
V_{IL}	Logic input low voltage	DI0, DI1, DI2			0.496	V
		EN			0.296	V

Symbol	Description	Condition	MIN	TYP	MAX	Units
V_{IH}	Logic input high voltage	DI0, DI1, DI2	0.883			V
		EN	0.909			V
f_{wck}	WCK Frequency Range		8		96	kHz
f_{Bck}	BCK Frequency Range		0.2432		25.804	MHz
T_{sd}	Over Temperature Protection Threshold			150		℃
$T_{sd}r$	Over Temperature Protection Recovery Threshold			130		℃
UVP	Under Voltage Protection Threshold			2.1	2.3	V
UVP	Under Voltage Protection Hysteresis Threshold			100		mV
OCP	Output current Protection			2.8		A

DIGITAL AUDIO INTERFACE TIMING

I²S

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WCK	8	-	96	kHz
f_{bck}	Bit clock frequency, on pin BCK	32fs		128fs	Hz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns

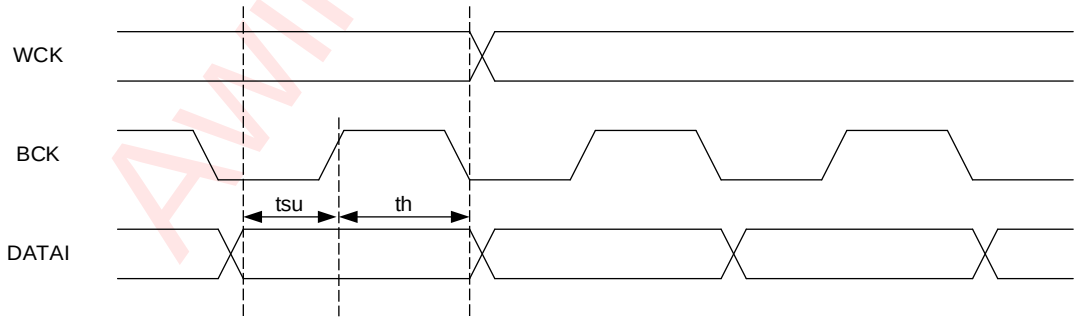
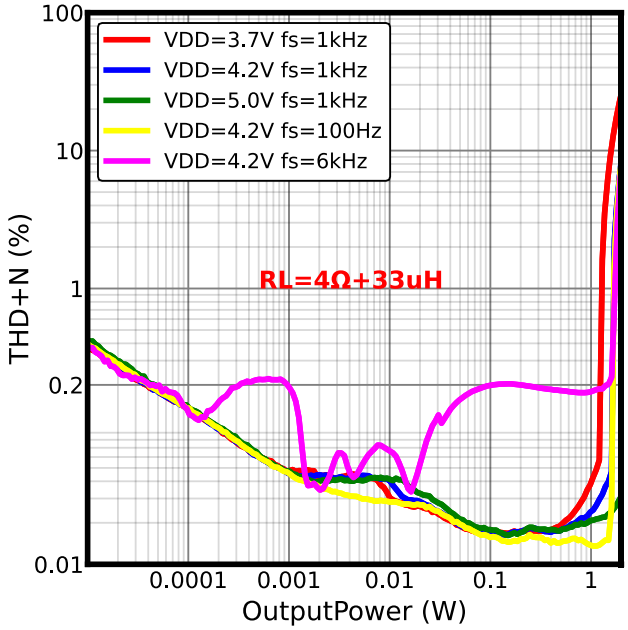


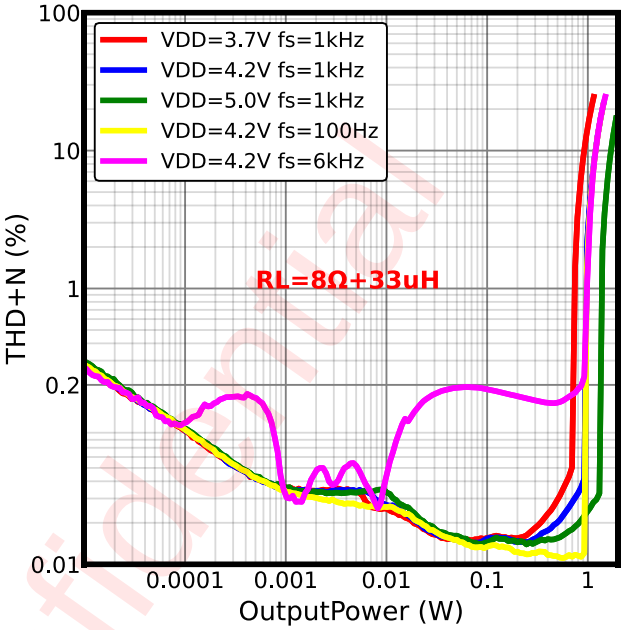
Figure 1 I²S Digital Audio Interface Timing

TYPICAL CHARACTERISTIC CURVES

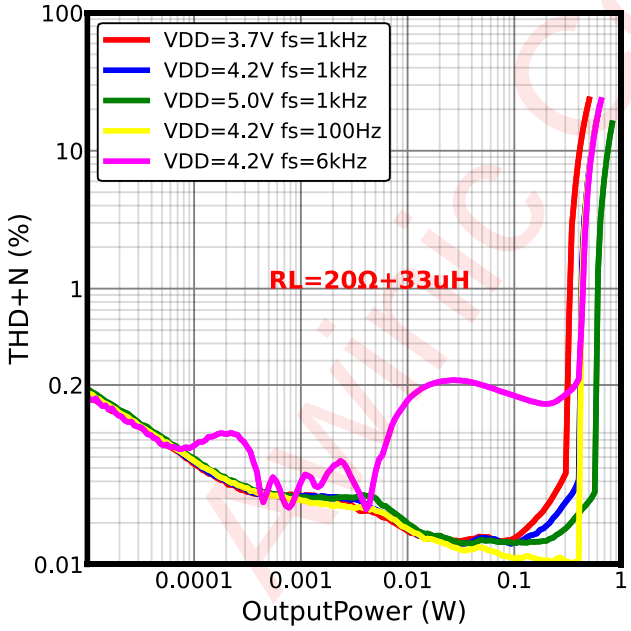
THD+N VS. OUTPUT POWER



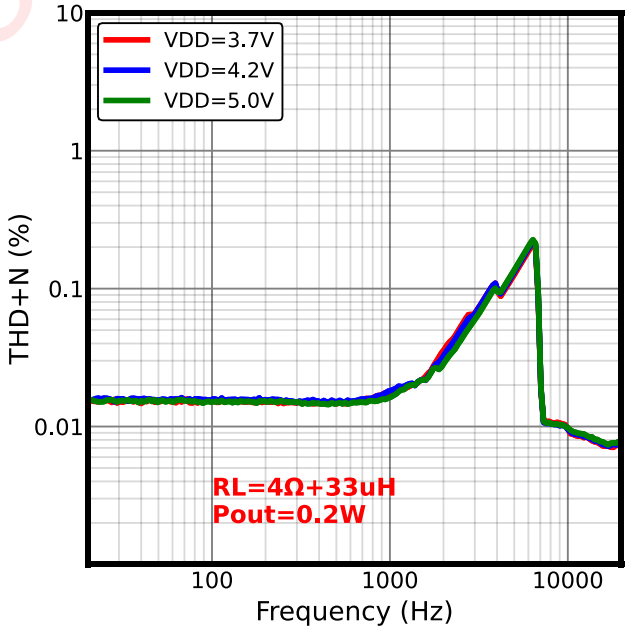
THD+N VS. OUTPUT POWER



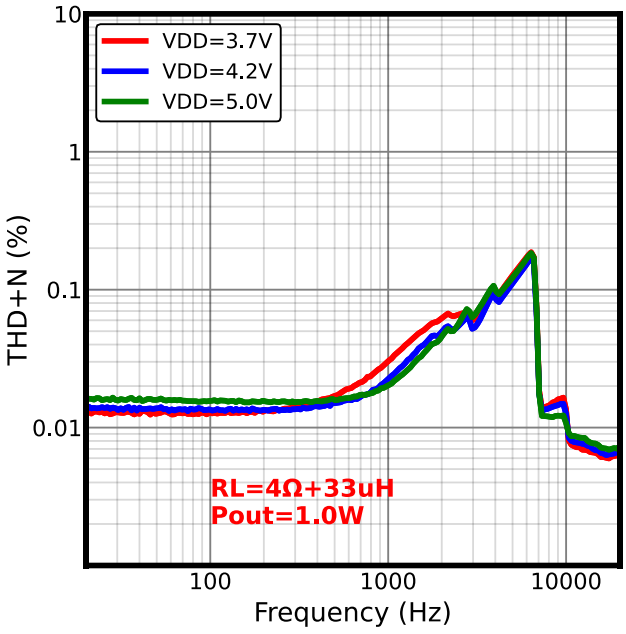
THD+N VS. OUTPUT POWER



THD+N VS. FREQUENCY



THD+N VS. FREQUENCY



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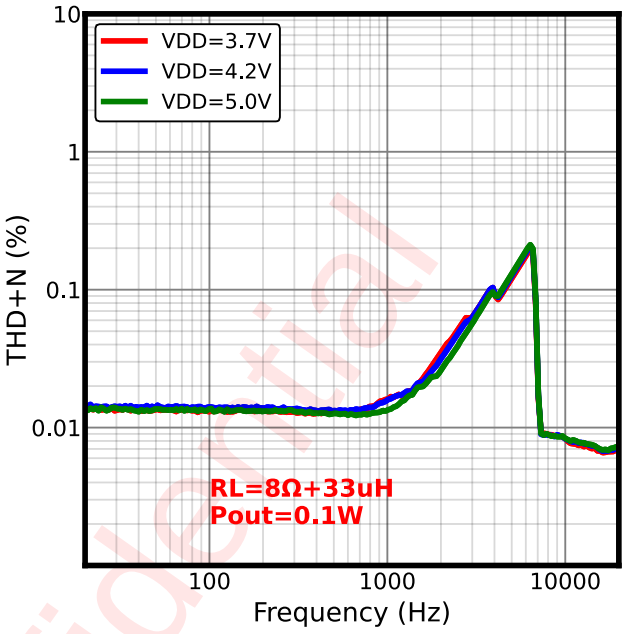
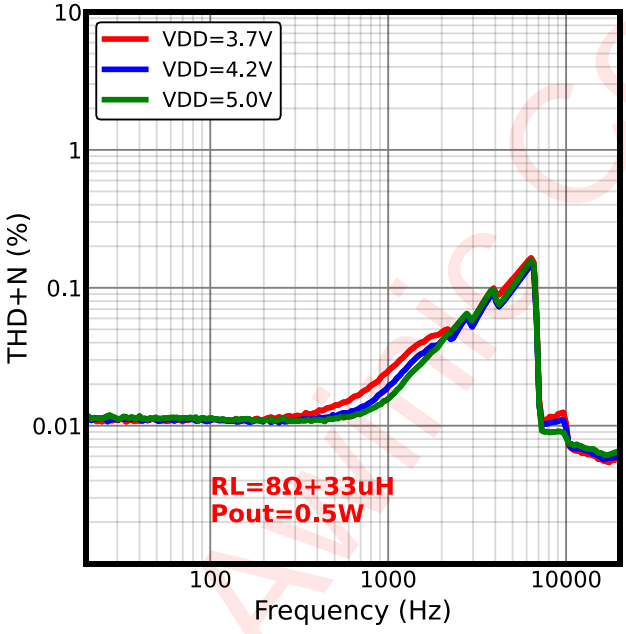
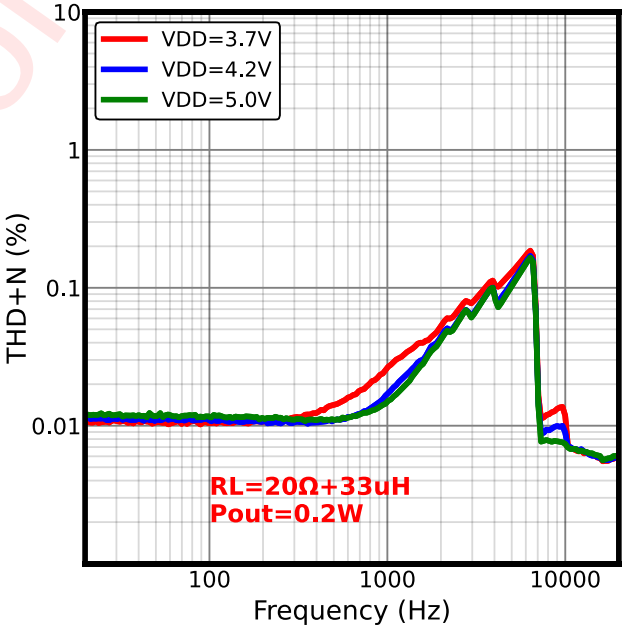


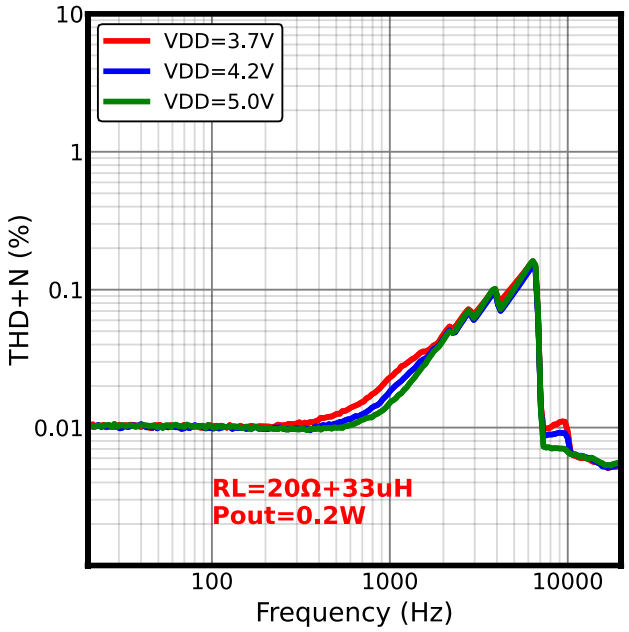
THD+N VS. FREQUENCY



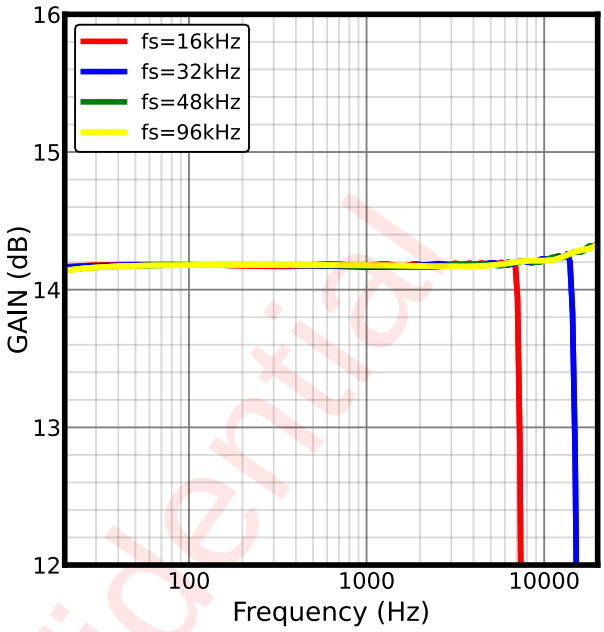
THD+N VS. FREQUENCY



THD+N VS. FREQUENCY

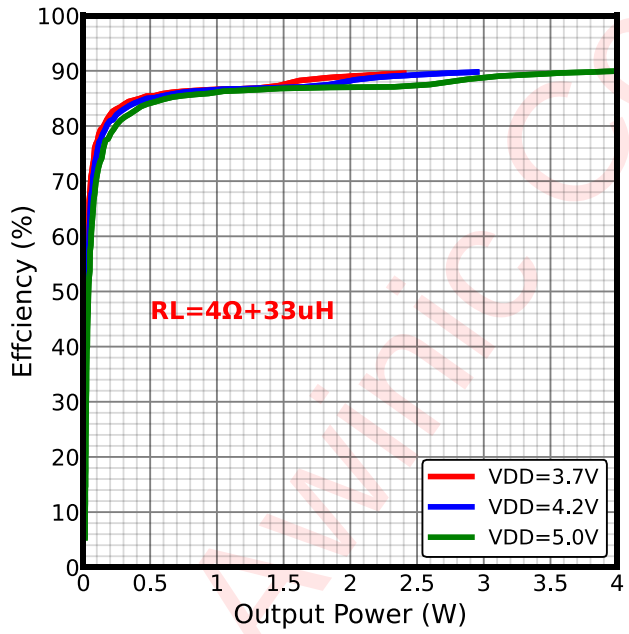


GAIN VS. FREQUENCY



I

EFF VS. OUTPUT POWER



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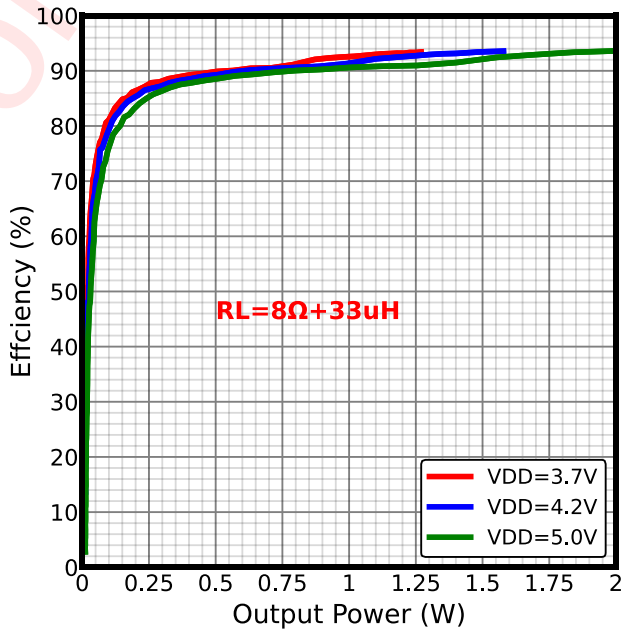

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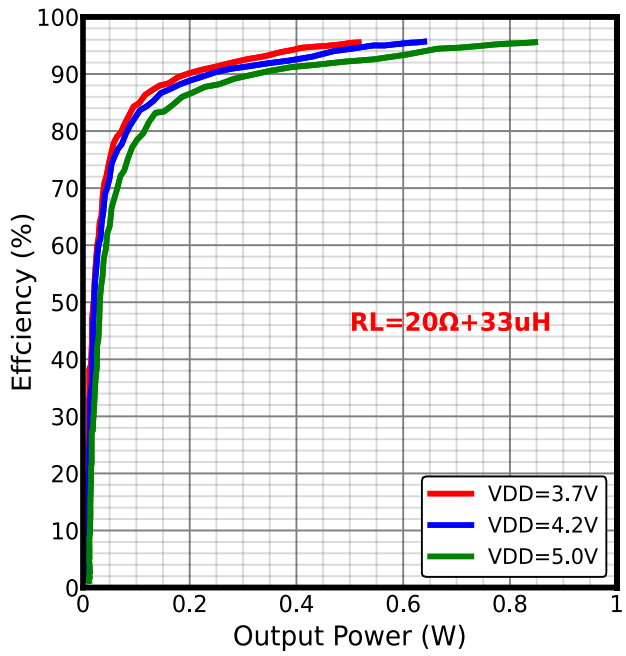
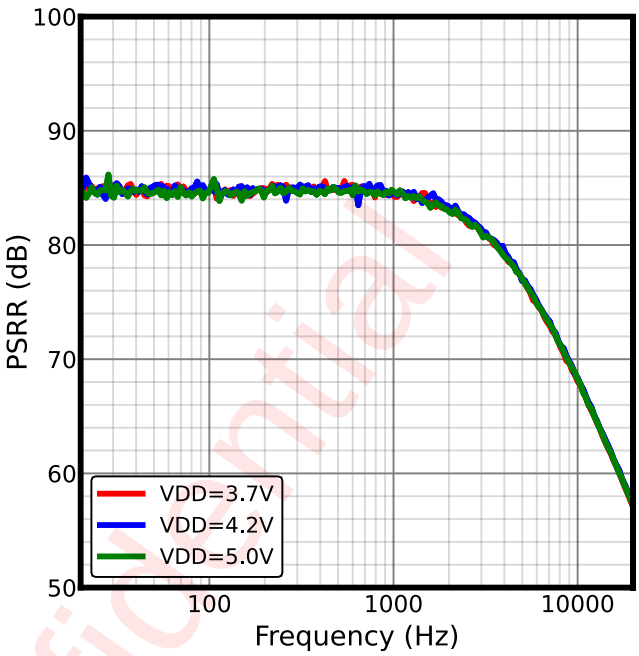
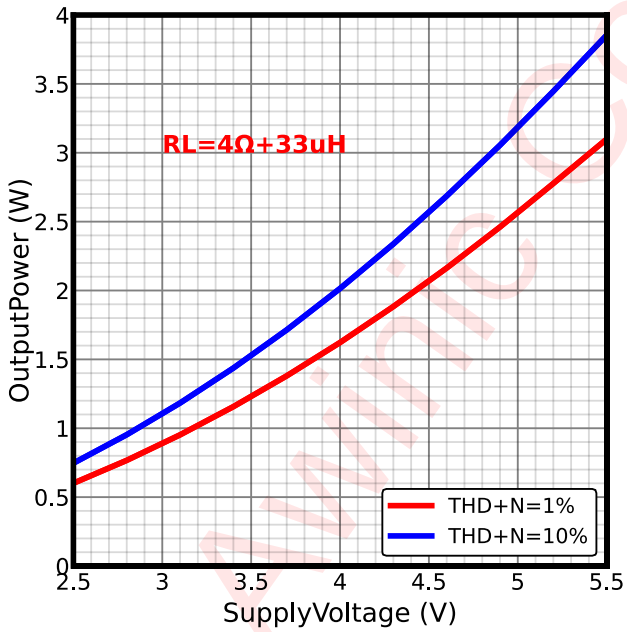


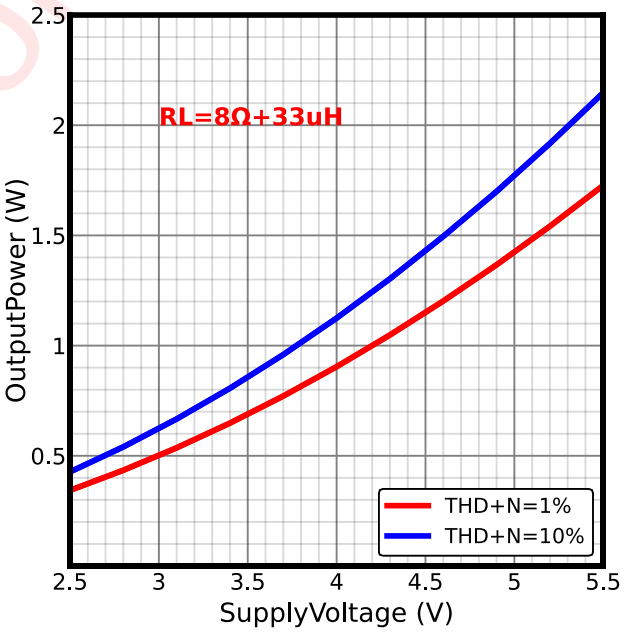
EFF VS. OUTPUT POWER



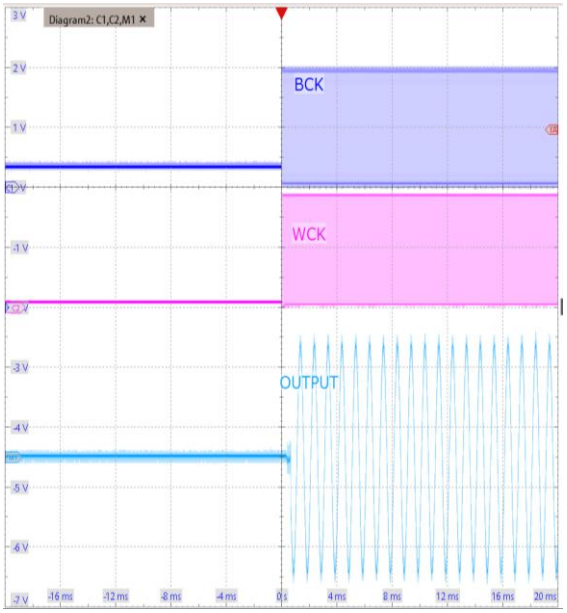
OUTPUT POWER VS. SUPPLY VOLTAGE



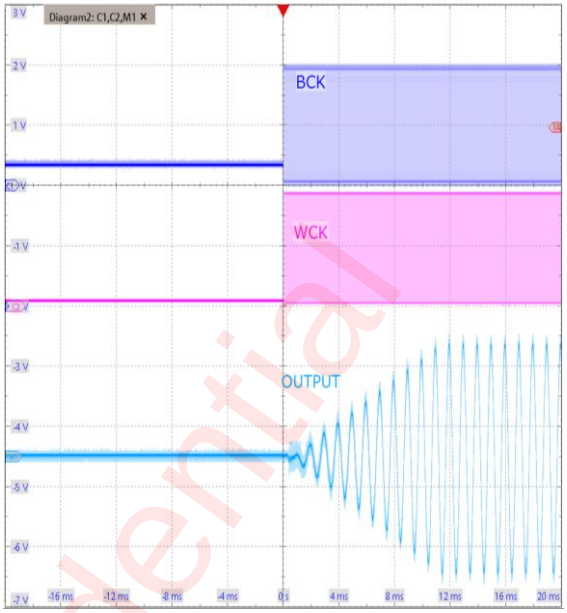
OUTPUT POWER VS. SUPPLY VOLTAGE



TURN-ON RESPONSE (Fast mode)



TURN-ON RESPONSE (Ramp mode)



DETAIL FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VDD supply voltage. When the VDD supply voltage raises from 0V to 1.8V. The internal reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 4 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	V_{VDD} < 1.8V EN Low	Power supply is not ready, chipset is power down.
Stand-By	V_{VDD} > 2.3V EN High	Power supply is ready, most parts of the device are power down for low power consumption
Operating	Normal I^2S	Amplifier is fully operating

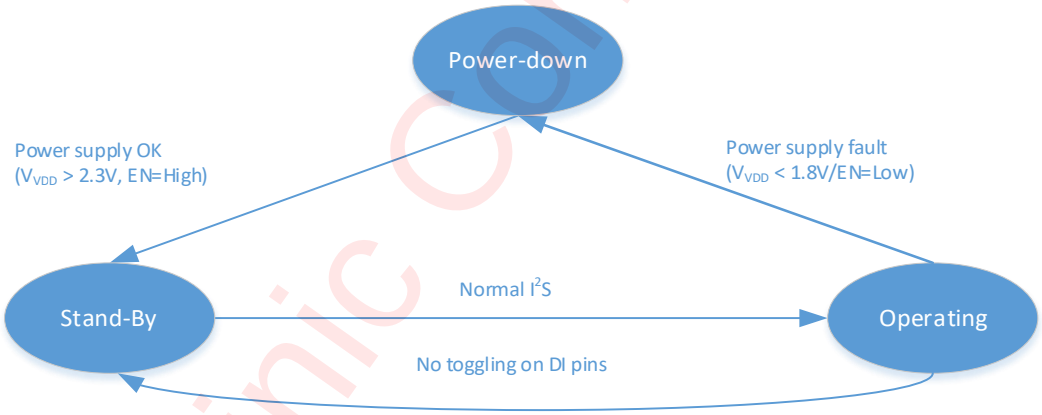


Figure 2 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- V_{VDD} < 1.8 V
- EN pin goes LOW

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. all the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all the supply voltages are OK:

V_{VDD} >2.3V and EN goes HIGH *Note*

Note ： *The voltage of the EN pin must comply with Absolute Maximum Rating restrictions and not exceed VDD +0.3V.*

STAND-BY MODE

The device enters Stand-By mode when the power supply voltage is within specification, the EN pin is High, and there is no signal toggling on the DI pins.

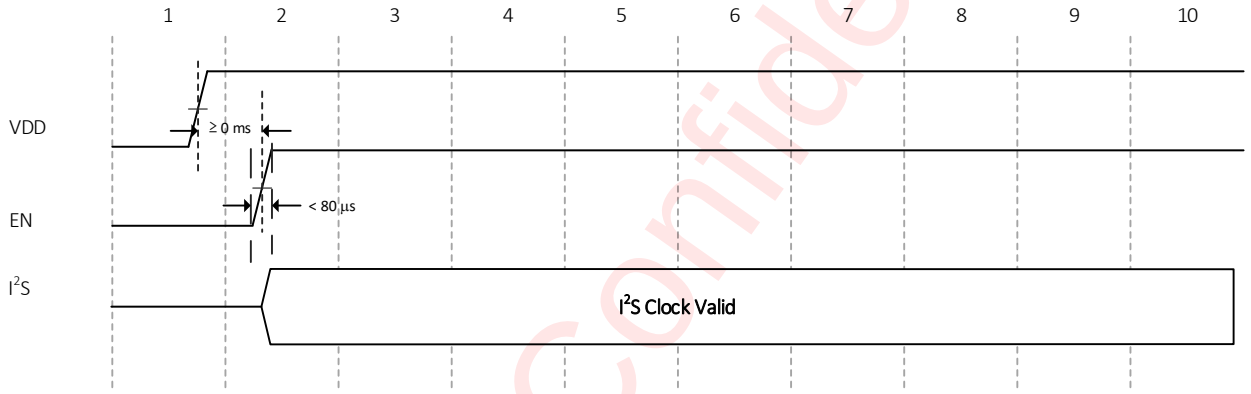
During Power-down to Standby power-up, the device identifies the EN pin's pull-up resistor value to determine line sequence. When VDD stabilizes and EN transitions from low to high, its internal recognition module activates, setting the channel based on the resistor value.

OPERATING MODE

The device is fully operational in this mode. Amplifier loop will start to work. Applying the BCK clock and WCK clock will case the device switch from STAND-BY mode to OPERATING mode.

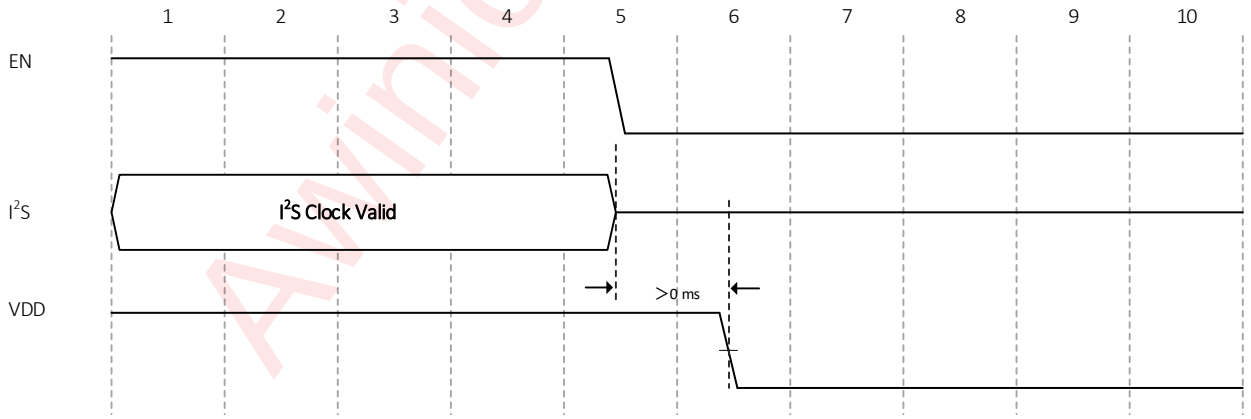
POWER UP AND POWER DOWN TIMING

- Power up sequence considering I²S timing shows as below:

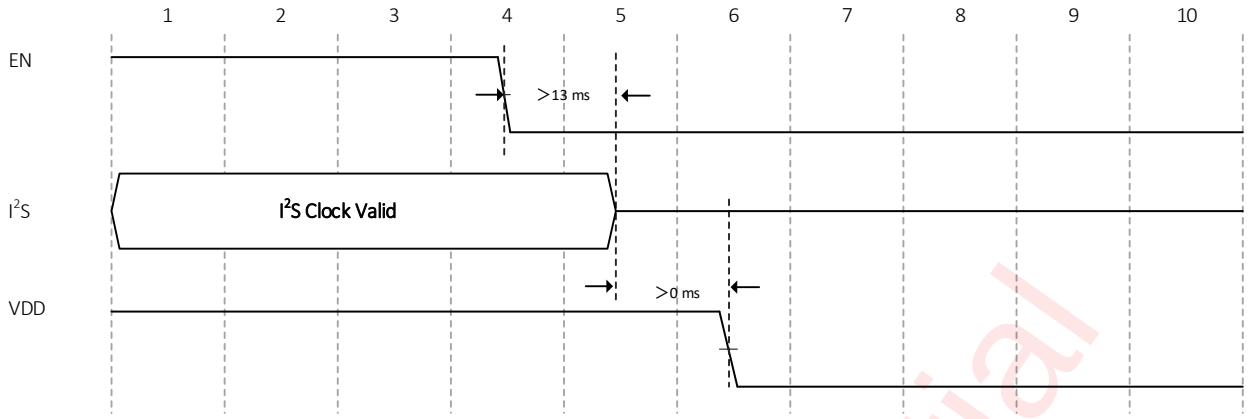


For device Power up, either I²S provision or EN pin pull-up can occur first. And the rising edge time of EN pin needs to be less than 80us.

- Power down sequence considering I²S, timing shows as below:



For device in **fast mode** power-down, stopping I²S and pulling down the EN pin do not require a specific sequence.



For the device in **ramp mode** power-down, disconnect I²S after 13 ms following pulling down the EN pin; Otherwise, it cannot achieve ramp power down

GAIN_SLOT PIN

GAIN_SLOT IN STANDARD I2S & LEFT-JUSTIFIED MODE

GAIN_SLOT pin is used to select gain (I²S & left-justified):

- Select the 14.3dB gain level by connecting the pin to ground;
- Select the 11.3dB gain level by leaving the pin floating.
- Select the 8.3dB gain level by connecting the pin to VDD;

GAIN_SLOT IN TDM MODE

The GAIN_SLOT pin enables channel selection through its connection configurations, combined with EN pin states and DI settings. Please refer to the CONFIGURATION section of DIGITAL AUDIO INTERFACE.

- The gain of the device in TDM mode is fixed at 14.3dB.

DIGITAL AUDIO INTERFACE

The state of each digital input and output are shown in below table. After power on, the input signal pin DI0, DI1, DI2 are set to high impedance by default.

Table 2 Detail Description of Digital I/O

Digital I/O	Type	Description (Default State)
EN	Input	Weak pull down
DI0	Input	Hi-Z
DI1	Input	Hi-Z
DI2	Input	Hi-Z

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 3 dedicated pins:

- DI0
- DI1

■ DI2

The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz and 96 kHz.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32). The frequency of BCK can be calculated according to the following equation:

BCK frequency = ***SampleRate*** * ***SlotLength*** * ***SlotNumber***

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 4-slot supported in TDM mode.

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

Different version supports specific bit synchronization modes under different TDM configurations, while the fundamental distinction between TDM and I²S protocols resides in the number of supported audio slots per frame.

Table 3 Supported I²S &TDM interface parameters

Mode	Frame Pulse	Slot	Bit depth	BCK frequency
Standard I²S	One Subframe	2	16b/20b/24b/32b	32fs/48fs /64fs
Left-justified				
TDM	One BCK	8	16b/20b/24b/32b	32fs/48fs /64fs
	One Subframe	4/6/8	16b/20b/24b/32b	32fs/48fs /64fs

STANDARD I²S MODE

Only AW88084A/C supports standard I²S.

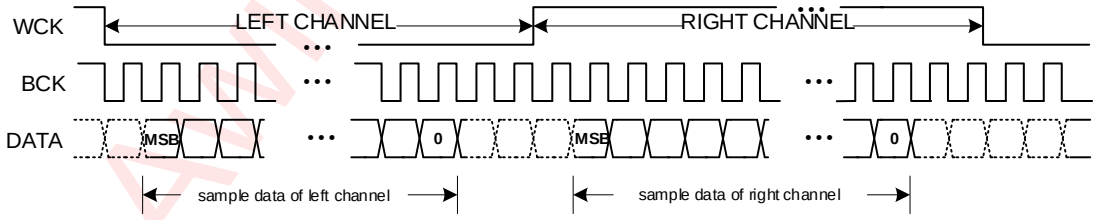


Figure 3 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

- Data sampling occurs at the rising edge of BCK, with a setup time (tsu) of 10ns and hold time (th) of 10ns to ensure signal integrity.

LEFT-JUSTIFIED MODE

Only AW88084B/D supports LEFT-JUSTIFIED.

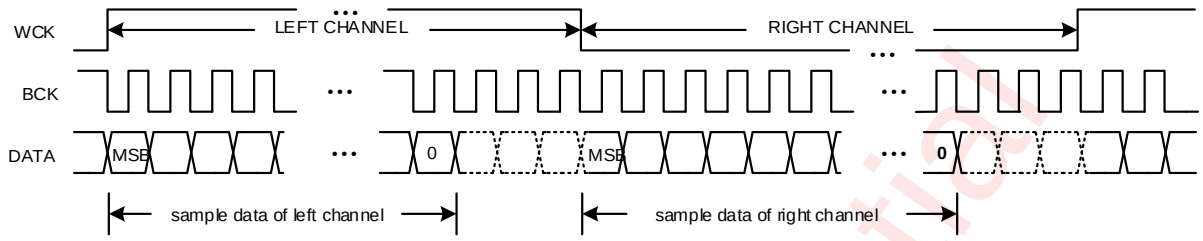


Figure 4 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.
- Data sampling occurs at the rising edge of BCK, with a setup time (tsu) of 10ns and hold time (th) of 10ns to ensure signal integrity.

TDM MODE

The fundamental distinction between TDM and I²S protocols resides in the number of supported audio slots per frame.

- The high-level pulse width of WCK signal can be one period of BCK, in which case the device only supports 8 slots.

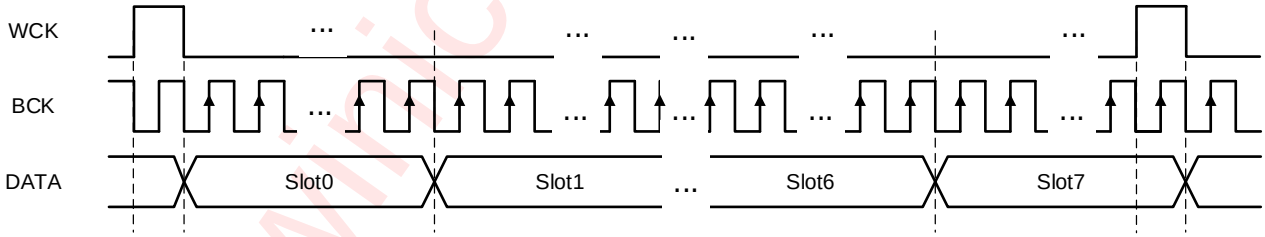


Figure 5 AW88084A/C TDM Timing (One BCK)

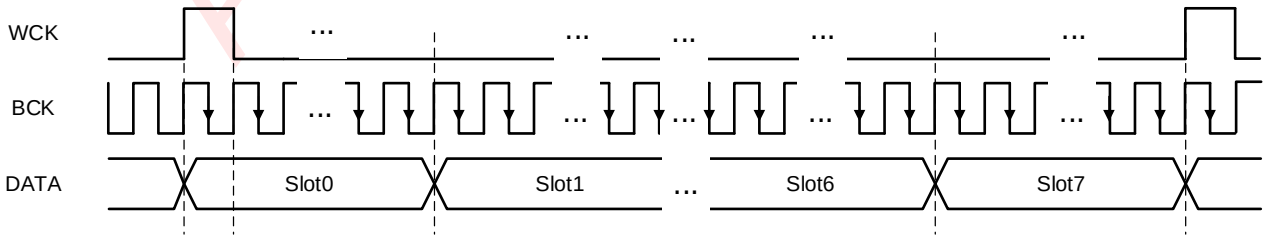


Figure 1 AW88084B/D TDM Timing (One BCK)

- The high-level pulse width of WCK signal can be one slot time, in which case the device supports 4/6/8 slots.

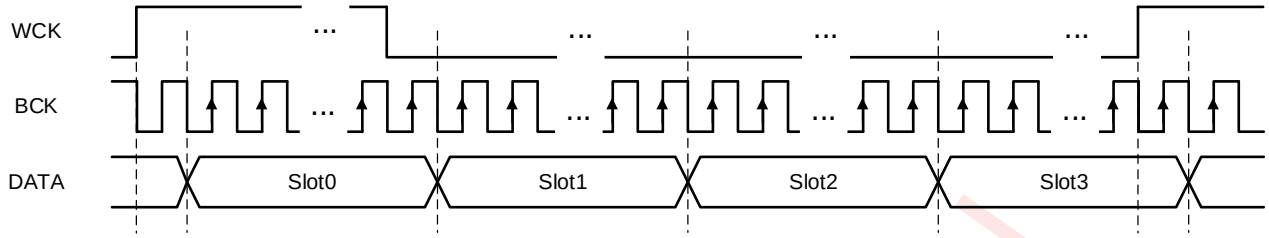


Figure 1 AW88084A/C TDM Timing (One Subframe)

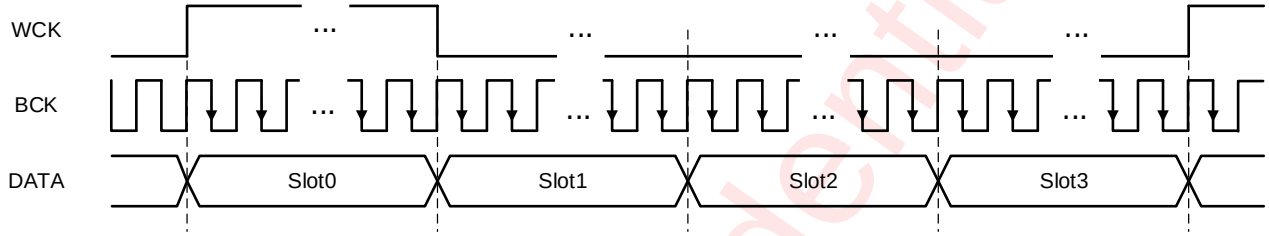


Figure 1 AW88084B/D TDM Timing (One Subframe)

CHANNEL CONFIGURATION

The device can select different channel by connecting pull-up resistors (R_{EN}) of varying resistance values to the EN pin, and must connect the digital audio bit clock (BCK), the digital audio word clock (WCK), and the digital audio data (DATA) to the DI pins in the corresponding line sequence.

Table 4 DI Configurations:

DI Mode	BCK	WCK	DATA
A	DI0	DI1	DI2
B	DI1	DI2	DI0
C	DI2	DI0	DI1

Table 5 Channel Selection in I²S Mode:

EN STATUS	DI Mode	CHANNEL
High (R_{EN}=1kΩ/0Ω) Note	A	Left
Pullup through R_{EN_Small}	B	Right
Pullup through R_{EN_Large}	C	Mono：Left/2+Right/2

Note ： *This configuration directly pulls up the EN pin; since certain GPIO outputs are open-drain types, the EN pin can be connected to VDDIO via a 1kΩ pull-up resistor. Please refer to Table 7 for the selection of R_{EN} resistance values.*

In TDM mode, channel selection requires not only identifying the R_{EN} resistance and DI line sequence connection method, but also considering the Gain_Slot pin connection method; in this mode, the device gain is fixed at 14.3dB.

Table 6 Channel Selection in TDM Mode:

EN STATUS	GAIN_SLOT	DI Mode	CHANNEL
High (R_{EN}=1kΩ/0Ω)	GND	A	0
High (R_{EN}=1kΩ/0Ω)	VDD	A	1
High (R_{EN}=1kΩ/0Ω)	Unconnected	A	2
Pullup through R_{EN_Small}	VDD	B	3
Pullup through R_{EN_Small}	GND	B	4
Pullup through R_{EN_Large}	GND	C	5
Pullup through R_{EN_Large}	Unconnected	C	6
Pullup through R_{EN_Large}	VDD	C	7

Table 7 R_{EN} resistance selection

LOGIC VOLTAGE LEVEL(VDDIO/GPIO) (V)	R_{EN}(kΩ)	
	Small	Large
1.2	38	250
1.8	100	400
3.3	177	775

FAST AND RAMP MODE

- AW88084A/B is fast Mode, device have 1ms turn-on and turn-off time.
- AW88084C/D is ramp Mode; Once I^2S/TDM is ready, the device ramps audio volume within 13ms upon EN transitions.

SPREAD SPECTRUM

The AW88084 series integrates edge rate control and spread spectrum modulation technologies, eliminating the traditional requirement for external LC filters to reduce electromagnetic interference（EMI） in Class-D amplifiers. This design compliance with EN55032B EMI regulatory standards. By implementing edge rate control and spread spectrum modulation, the chip significantly reduces EMI emissions while maintaining normal output performance. Specifically, the spread spectrum modulation module dynamically randomizes the PWM output frequency within a f_{SS} range centered on the modulation frequency (f_{PWM}).

PROTECTION MECHANISMS

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

Over Current (short) Protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to VDD/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

APPLICATION INFORMATION

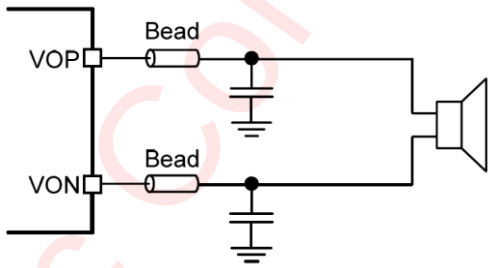
EXTERNAL COMPONENTS

SUPPLY DECOUPLING CAPACITOR

The device is a high-performance audio amplifier that requires adequate power supply decoupling. A 0.1μF low equivalent-series-resistance (ESR) ceramic capacitor are recommended. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the DEVICE is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

If the PA is close to the EMI sensitive circuits and/or there are long leads from amplifier to speaker, a ferrite bead filter could be used, and placed as close as possible to the output pins of the PA. When choosing a ferrite bead, select a ferrite bead with adequate current rating to prevent distortion of the output signal. In addition, a 0.1nF ceramic capacitor is typically recommended, and its rated voltage should be above 10V.

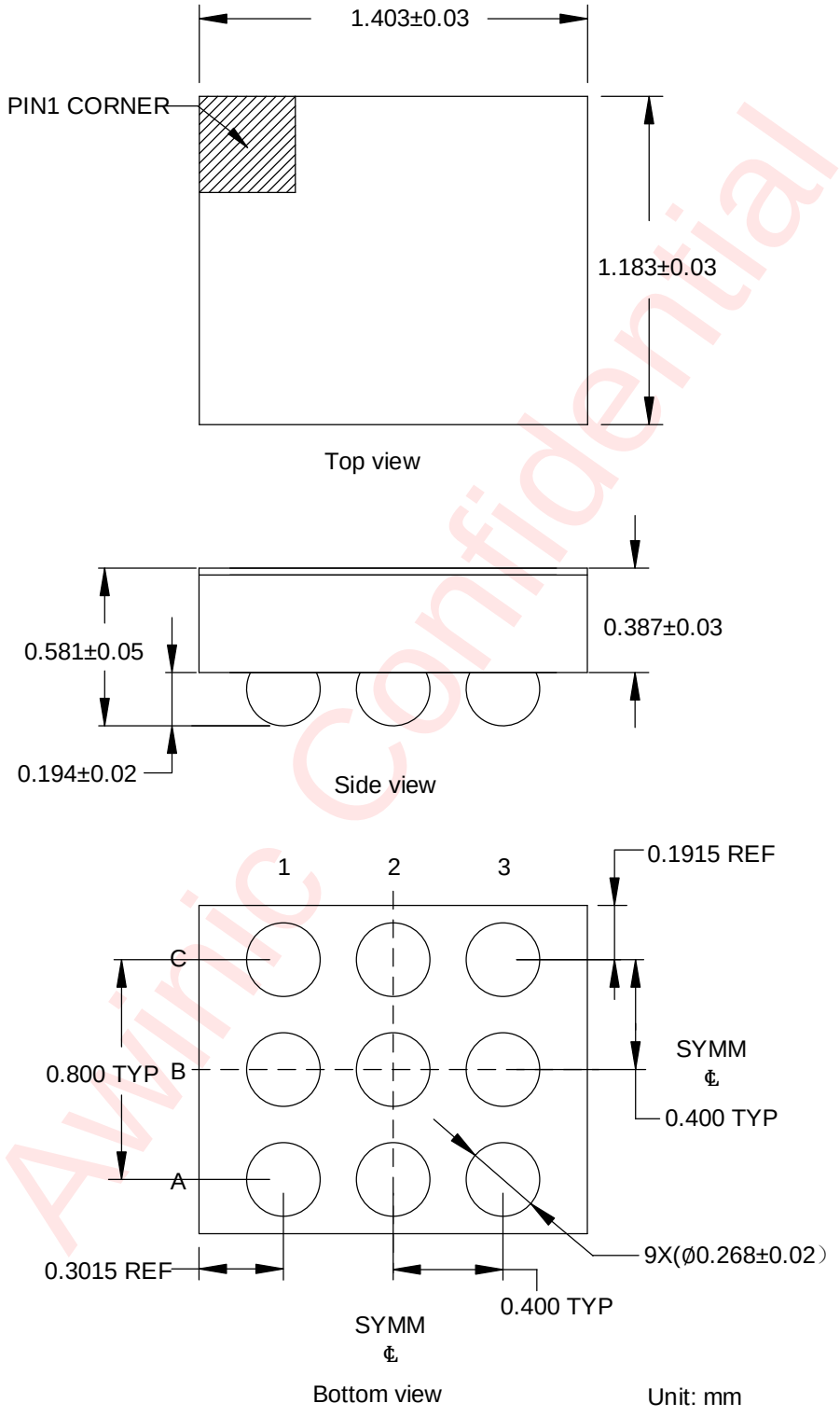


LAYOUT CONSIDERATION

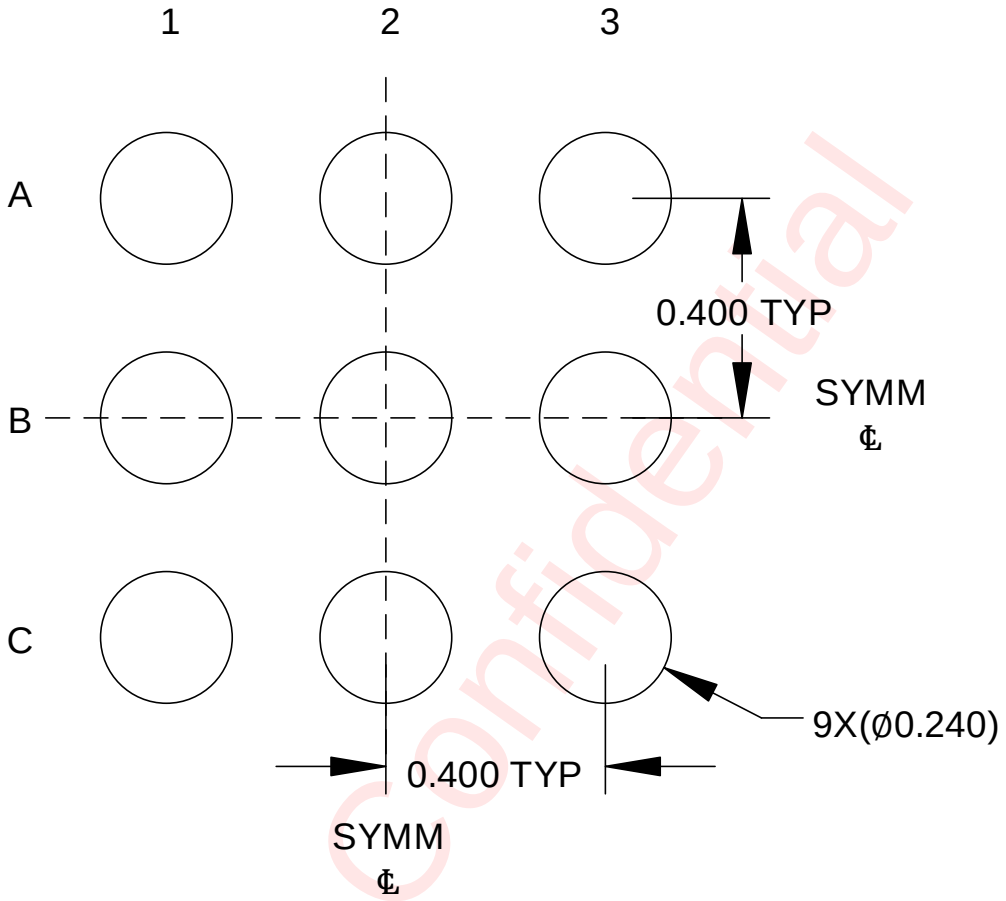
To obtain excellent performance of the amplifier, the below PCB layout guidelines should be followed:

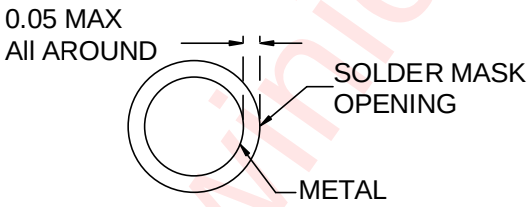
1. The filter capacitors of VDD should be placed close to the corresponding pins of the amplifier, and the small high -frequency filter capacitors are closer to the pins than the large.
2. VDD input of the audio power amplifier must first pass through the capacitor and then go to the pins of the chip, and the line width requirements can meet the maximum current required for the current set power output, so it is necessary to pay attention to the line width and the number of vias when routing the wire, so as to avoid the insufficient number of line width and vias, which will cause the voltage drop on the line to be too large and affect the final output of the audio power amplifier;
3. The signal line using the differential connection method is completely treated as equal length and width according to the requirements of the differential line, which not only requires the equal length and width between the signal lines, but also requires the distance between the signal line and the ground on both sides to be of equal width.
4. The beads and capacitor should be placed close to the VON and VOP pin. The output line from PA to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.
5. The capacitance on the output lines or on the long speaker tracks should be less than 1nF.

Package Description

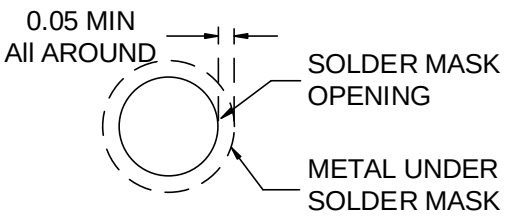


Land Pattern Data





NON SOLDER MASK DEFINED

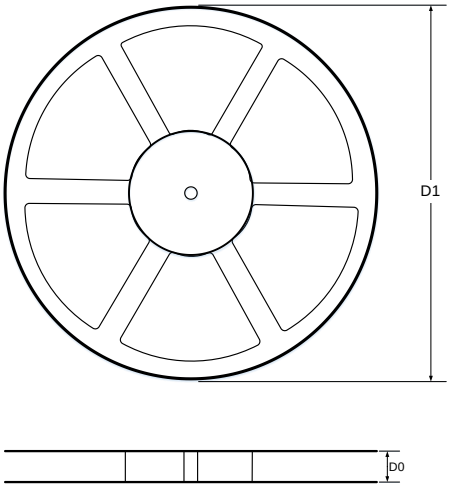


SOLDER MASK DEFINED

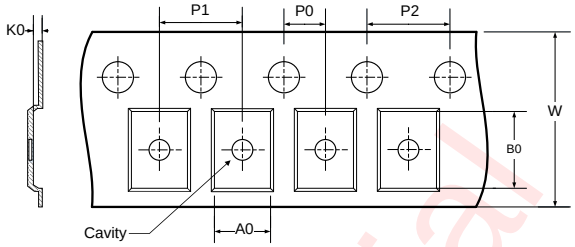
Unit: mm

Tape And Reel Information

REEL DIMENSIONS

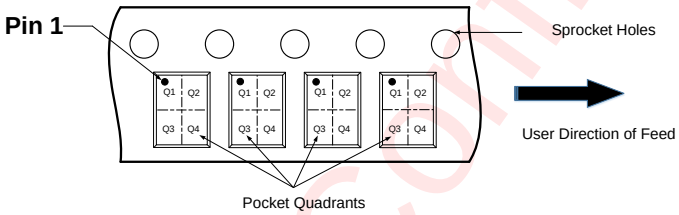


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.55	1.35	0.75	2	4	4	8	Q1

All dimensions are nominal

Revision History

Version	Date	Change Record
V1.0	Dec. 2025	Official released

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