

DPDT USB Switch With Over Voltage Protection

Features

- USB 2.0 Hi-speed DPDT switch
- Typical -3dB bandwidth: 1.0 GHz
- Reverse blocking back-to-back MOSFETs
- Over voltage protection : 3.83V typical
- 24V DC protection on D+ and D- Ports
- +30V surge protection on D+ and D-
- Supply voltage range: 2.7V to 5.5V
- 5.8Ω switch on-resistance typical
- C_{ON}: 6pF typical
- I_{CC}: 38μA typical
- WLCSP 1.57mmX1.17mmX0.574mm-12B package

Applications

- Smartphones
- Tablets

General Description

The AW35743G is a Hi-Speed USB 2.0(480Mbps) DPDT (Double Pole Double Throw) switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch.

The AW35743G protection on the D+/D- pins can tolerate up to 24V DC, when D+ or D- voltage is greater than the OVP(Over-Voltage Protection) threshold, the switch will be automatically shutoff to protect downstream devices.

The device operates over 2.7V to 5.5V supply range with independent control bits for each switch pair and an on/off enable pin for shutdown mode. Additional features include low switch on resistance and capacitance along with a fault flag to alert the system processor to overvoltage fault events.

The AW35743G is available in a WLCSP 1.57mmX1.17mmX0.574mm-12B package.

Typical Application Circuit

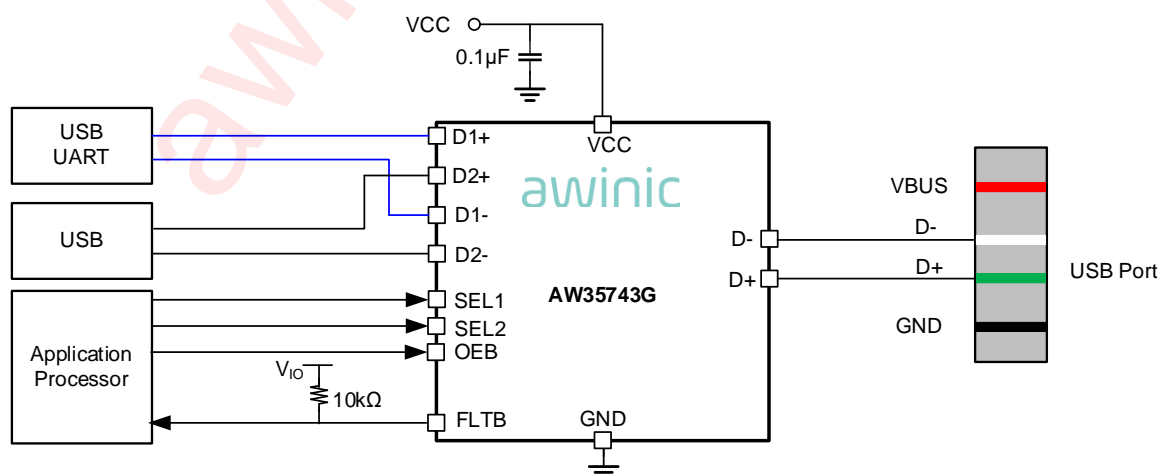


Figure 1 Typical Application Circuit of AW35743G

Pin Configuration And Top Mark

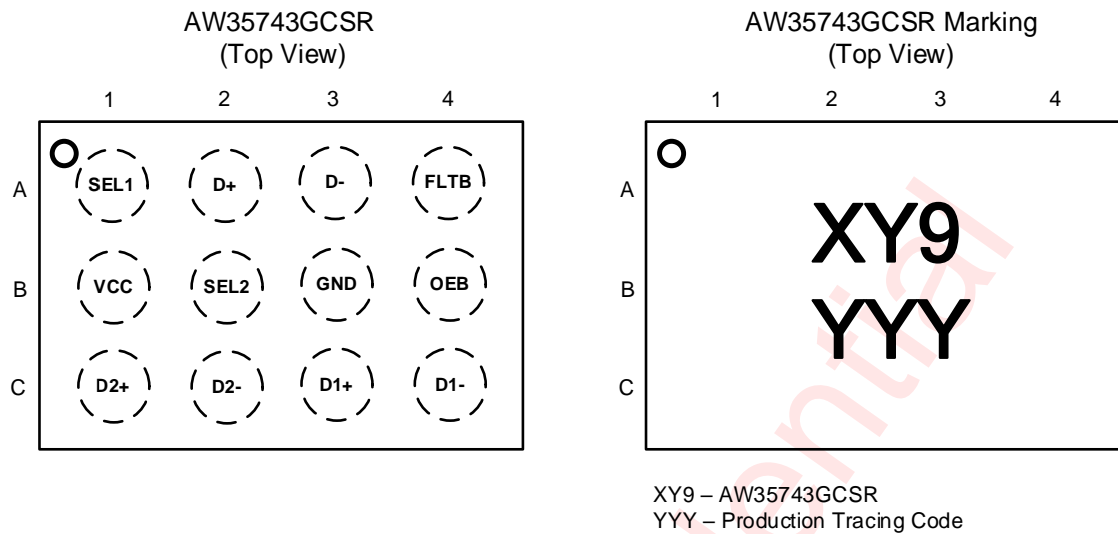


Figure 2 Pin Configuration And Top Mark

Pin Definition

PIN	NAME	DESCRIPTION
A1	SEL1	Switch select1, active high
A2	D+	Common high speed data port, differential +
A3	D-	Common high speed data port, differential -
A4	FLT B	Fault indicator output, active low, open drain
B1	VCC	Supply voltage
B2	SEL2	Switch select2, active high
B3	GND	Ground
B4	OEB	Output enable, active low
C1	D2+	Multiplexed high speed data port2, differential +
C2	D2-	Multiplexed high speed data port2, differential -
C3	D1+	Multiplexed high speed data port1, differential +
C4	D1-	Multiplexed high speed data port1, differential -

Pin Functions

OEB	SEL1	SEL2	D- CONNECTION	D+ CONNECTION
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+

Functional Block Diagram

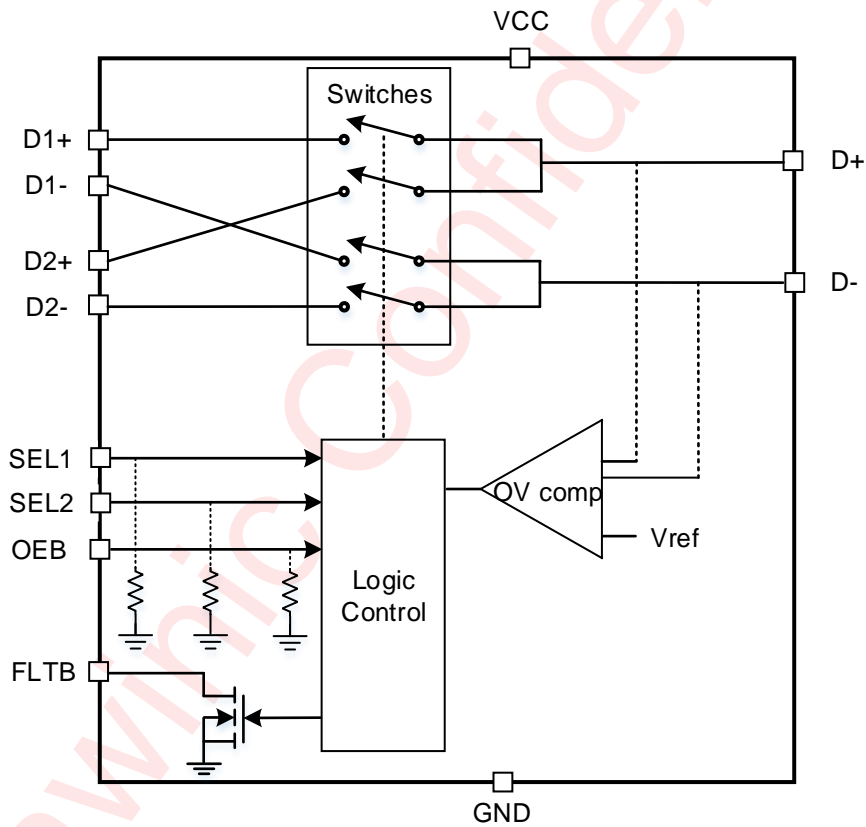


Figure 3 Functional Block Diagram

Typical Application Circuits

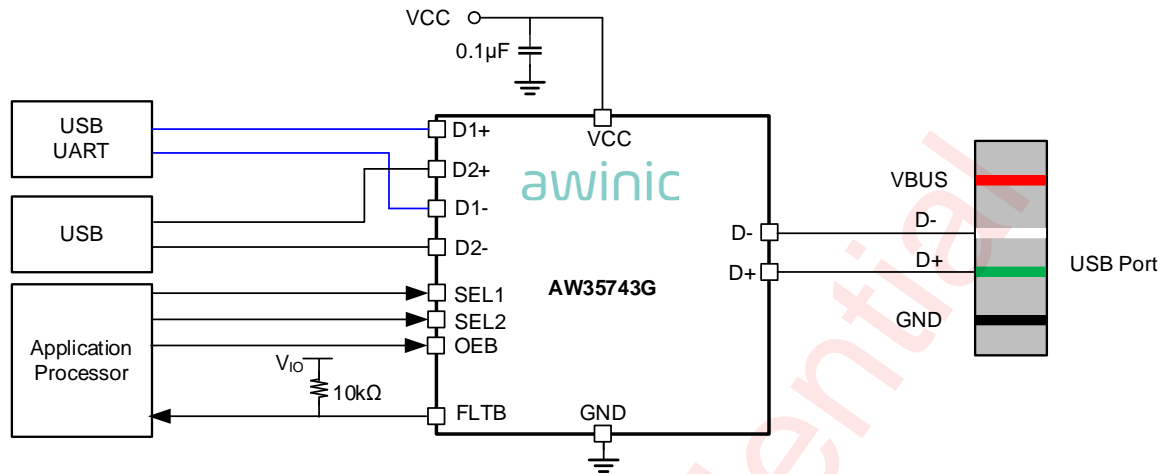


Figure 4 Typical Application Circuit of AW35743G

Notice for Typical Application Circuits:

1. The AW35743G has internal 5.8-M Ω pull down resistors on SEL1, SEL2, and OEB, so no external resistors are required on the logic pins.
2. Internal pull-down resistor on SEL1 and SEL2 pins ensures the D1+ and D1- channels are selected by default.
3. If FLTB is not used, it can be left floating.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35743GCSR	-40°C~85°C	WLCSP 1.57mmX1.17mm X0.574mm-12B	XY9	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC		-0.3V to 6V
Input/Output DC voltage(D+, D-)		-0.3V to 24V
Input/Output DC voltage(D1+, D1-, D2+, D2-)		-0.3V to 6V
Input voltage range	SEL1, SEL2, OEB	-0.3V to 6V
Output voltage range	FLTB	-0.3V to 6V
Junction-to ambient thermal resistance θ_{JA}		95°C/W
Maximum operating junction temperature T_{JMAX}		150°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
Human Body Model (All pins, per JEDEC JS-001) ^(NOTE2)		±2kV
Charged Device Model (All pins, per JEDEC JS-002) ^(NOTE3)		±1kV
Latch-up		
Test condition: JEDEC78E		±200mA

NOTE1: Conditions out of those ranges listed in “absolute maximum ratings” may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in “recommended operating conditions”. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: Test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	5.5	V
V _{I/O}	Analog input/output voltage(D _±)	0	24	V
	Analog input/output voltage(Dn _±)	0	3.6	
V _I	Digital input voltage(SEL1, SEL2, OEB)	0	5.5	V
T _A	Operating free-air temperature T _A	-40	85	°C

Electrical Characteristics

$V_{CC}=3.3V$ $T_A=25^{\circ}C$ for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	5.5	V
I_{CC}	Active supply current	OEB=0V SEL1, SEL2=0V $0V < V_{D\pm} < 3.6V$		38		μA
I_{CC_PD}	Standby supply current	OEB= V_{CC} SEL1, SEL2=0V		0.5		μA
DC Characteristics						
R_{ON}	On-state resistance	$V_{I/O}=0.4V$, $I_{SINK}=8mA$		5.8		Ω
ΔR_{ON}	On-state resistance match between channels	$V_{I/O}=0.4V$, $I_{SINK}=8mA$		0.1		Ω
$R_{ON(FLAT)}$	ON-state resistance flatness	$V_{I/O}=0V$ to $0.4V$, $I_{SINK}=8mA$		0.1		Ω
I_{OFF}	I/O pin OFF leakage current on D+/D-	$V_{D\pm} = 0V$ or $3.6V$ $V_{D1\pm}$ or $V_{D2\pm} = 3.6V$ or $0V$			10	μA
		$V_{D\pm} = 0V$ or $24V$ $V_{D1\pm}$ or $V_{D2\pm} = 0V$			420	μA
I_{ON}	ON leakage current on D+/D-	$V_{D\pm} = 0V$ or $3.6V$ $V_{D1\pm}$ and $V_{D2\pm} = high-Z$		2	10	μA
Digital Characteristics						
V_{IH}	Input logic high	SEL1, SEL2, OEB	1.4			V
V_{IL}	Input logic low	SEL1, SEL2, OEB			0.4	V
V_{OL}	Output logic low	FLTB $I_{OL}=1mA$			0.5	V
R_{PD}	Internal pull-down resistor on digital input pins			5.8		$M\Omega$
Protection						
V_{OVP_TH}	OVP threshold	D+/D- rising	3.66	3.83	4	V
V_{OVP_HYST}	OVP threshold hysteresis	D+/D- falling		120		mV
t_{OVP}	OVP Protection Response time	$V_{D\pm} = 1V$ to $10V$ step		50		ns
t_{OVPR}	OVP Protection Recovery Time	$V_{D\pm} = 10V$ to $1V$ step		1.5		μs

Electrical Characteristics (Continued)V_{CC}=3.3V T_A= 25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Dynamic Characteristics						
C _{ON}	IO pins ON capacitance	V _{D±} = 0 or 3.3 V, f = 240 MHz, switch ON		6		pF
O _{ISO}	Differential off isolation	R _L = 50 Ω C _L = 5 pF f = 100 kHz, switch OFF		-60		dB
		R _L = 50 Ω C _L = 5 pF f = 240MHz, switch OFF		-20		dB
X _{TALK}	Channel to channel crosstalk	R _L = 50 Ω C _L = 5 pF f = 100 kHz, switch ON		-60		dB
BW	-3dB bandwidth	R _L = 50 Ω, switch ON		1.0		GHz
t _{switch}	Switching time between channels (SEL1, SEL2 to output)	V _{D±} = 0.8 V		2.5	5	μs
t _{on}	Device turn on time (OEB to output)	R _L = 50 Ω C _L = 5 pF, V _{CC} = 2.7 V to 5.5 V		22		μs
t _{off}	Device turn off time (OEB to output)			53		ns
t _{pd}	Propagation delay	V _{D±} = 0.4 V R _L = 50 Ω, C _L = 5 pF, V _{CC} = 2.7 V to 5.5 V		200		ps

Timing Diagram

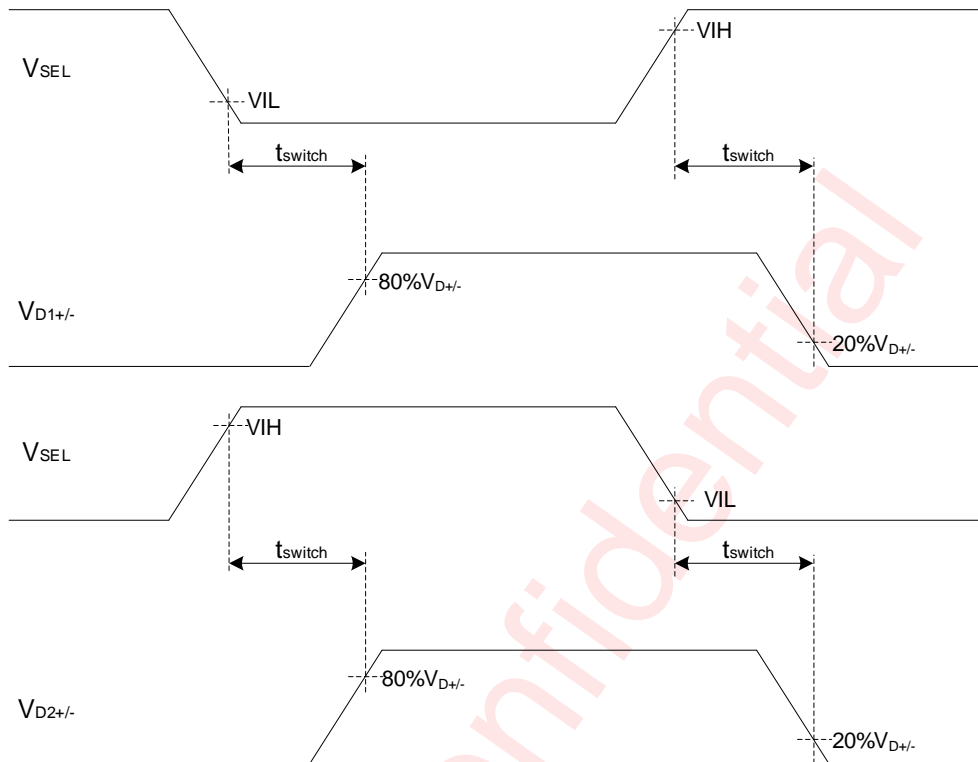


Figure 5 Switching Time Between Channels

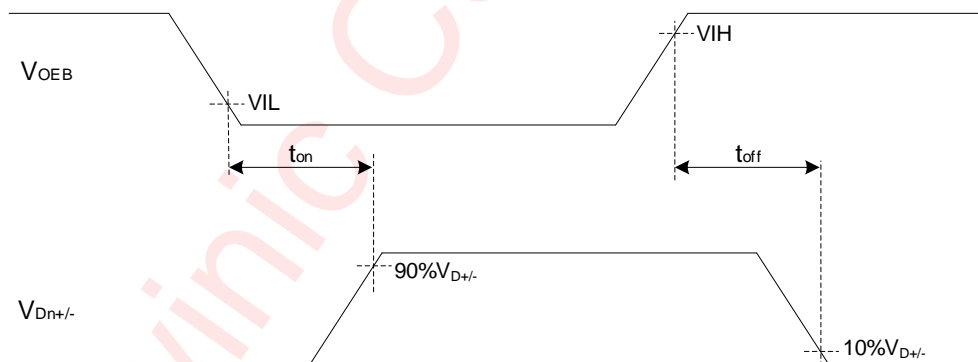


Figure 6 Device Turn On Time

Timing Diagram (Continued)

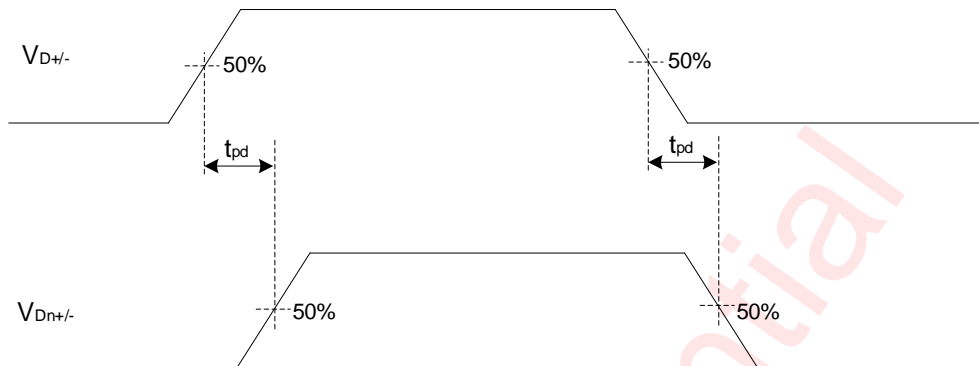


Figure 7 Propagation delay

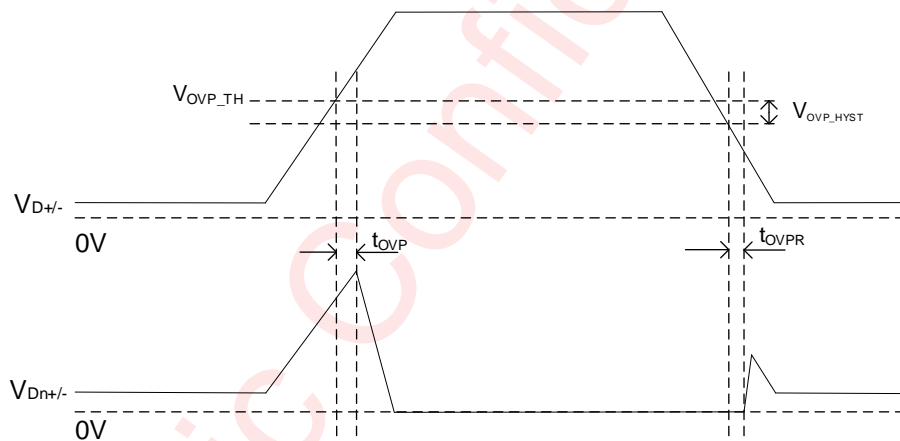


Figure 8 Overvoltage Protection

Application Information

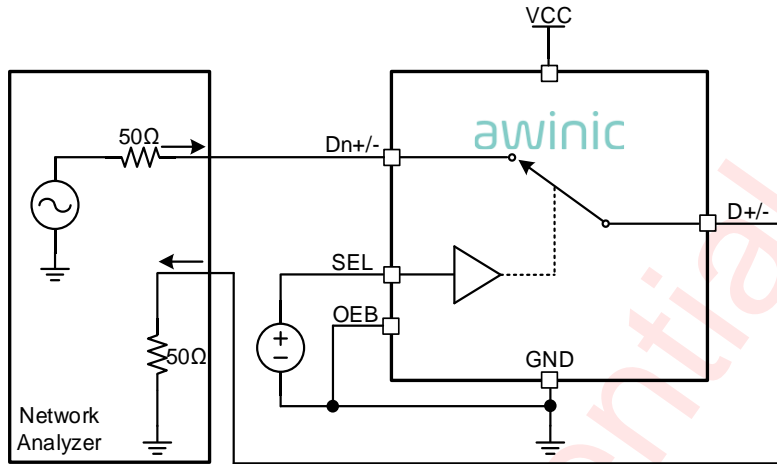


Figure 9 BW and Insertion Loss

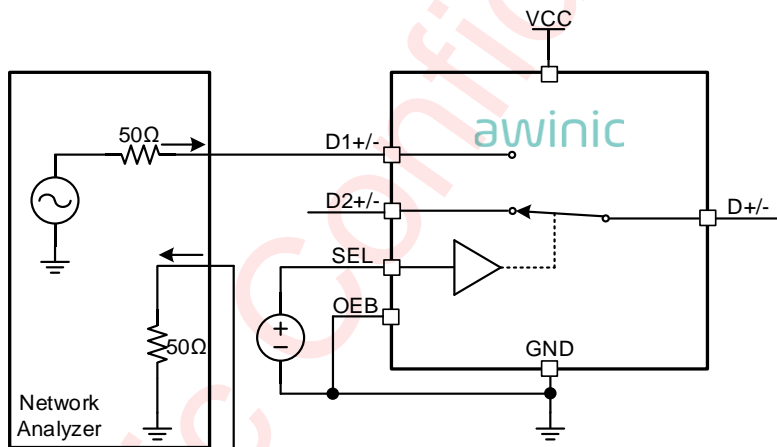


Figure 10 OFF Isolation

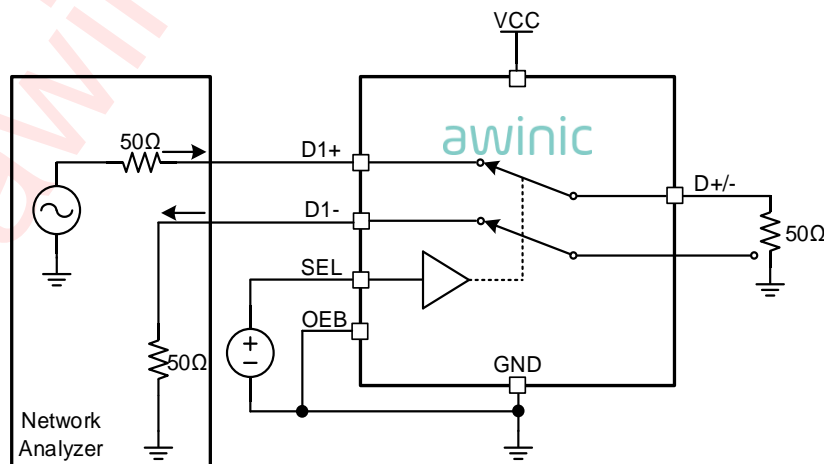


Figure 11 Cross Talk

Detailed Functional Description

The AW35743G is a Hi-Speed USB 2.0 DPDT switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch. The AW35743G will protect D+ and D- pins when stressed with voltages up to 24V. The device can pass signals with bandwidth 1GHz to maintain signal integrity and eye compliance.

Over-Voltage Protection

AW35743G is designed to protect the system from damage. Over-voltage event happens when voltage on D+/D- exceeds 3.83V(typ.), and device will activate OVP to disconnect the switches, the FLTB will also be pulled low to indicate there is OV event to the system.

Reverse-Blocking Switches

The switches in the AW35743G are reverse-blocking, using back-to-back MOSFET switches in each path. When the switches are OFF, current is blocked in both directions from D1+, D2+ or D1-, D2- to D+ or D-. This provides more system flexibility for USB transceivers or other I/O devices connected in the system.

High Impedance Mode

When OEB is logic high, the AW35743G is in high impedance mode, all the signal paths are in Hi-Z state.

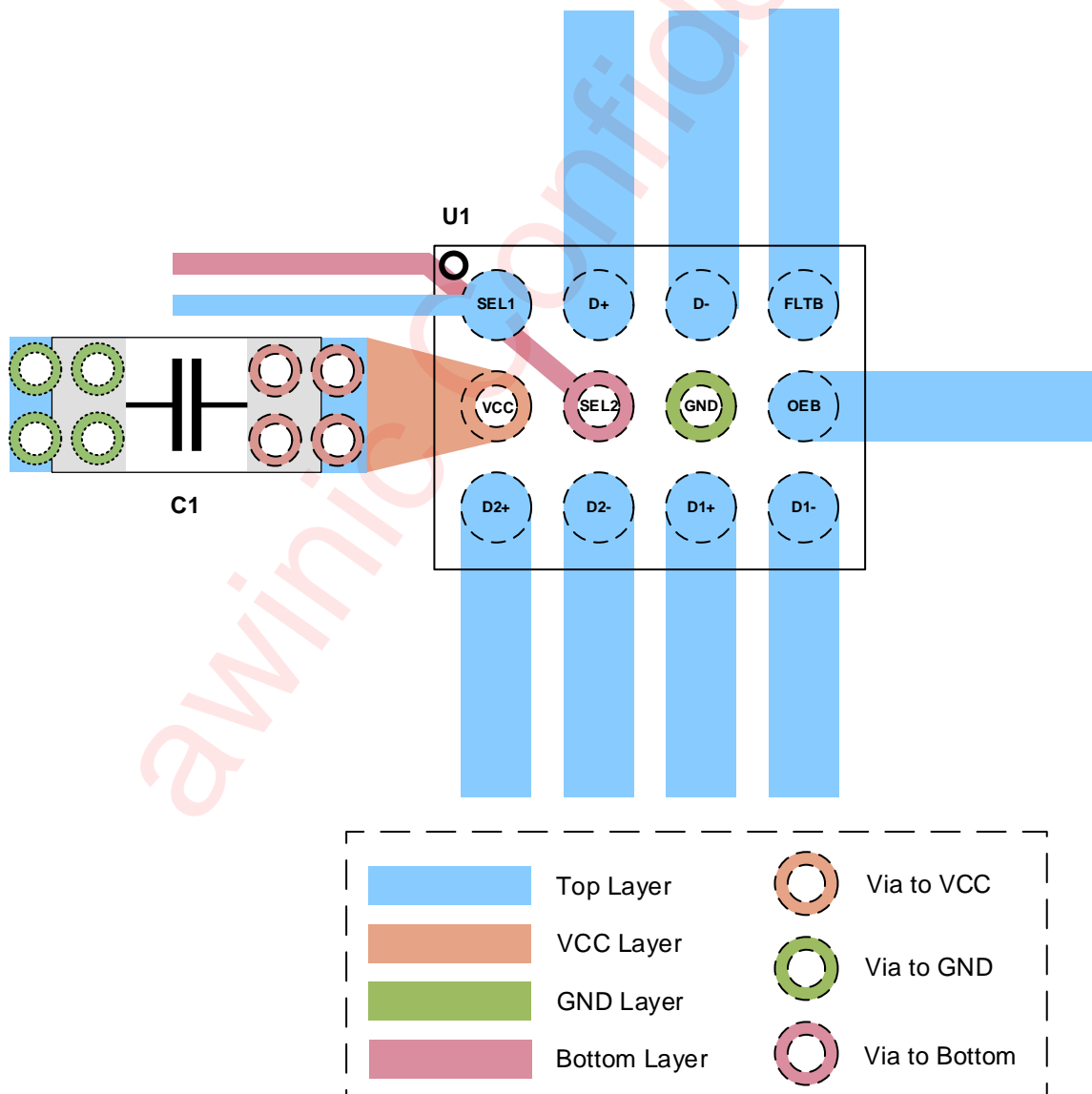
OEB	SEL1	SEL2	D- Connection	D+ Connection
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+

PCB Layout Consideration

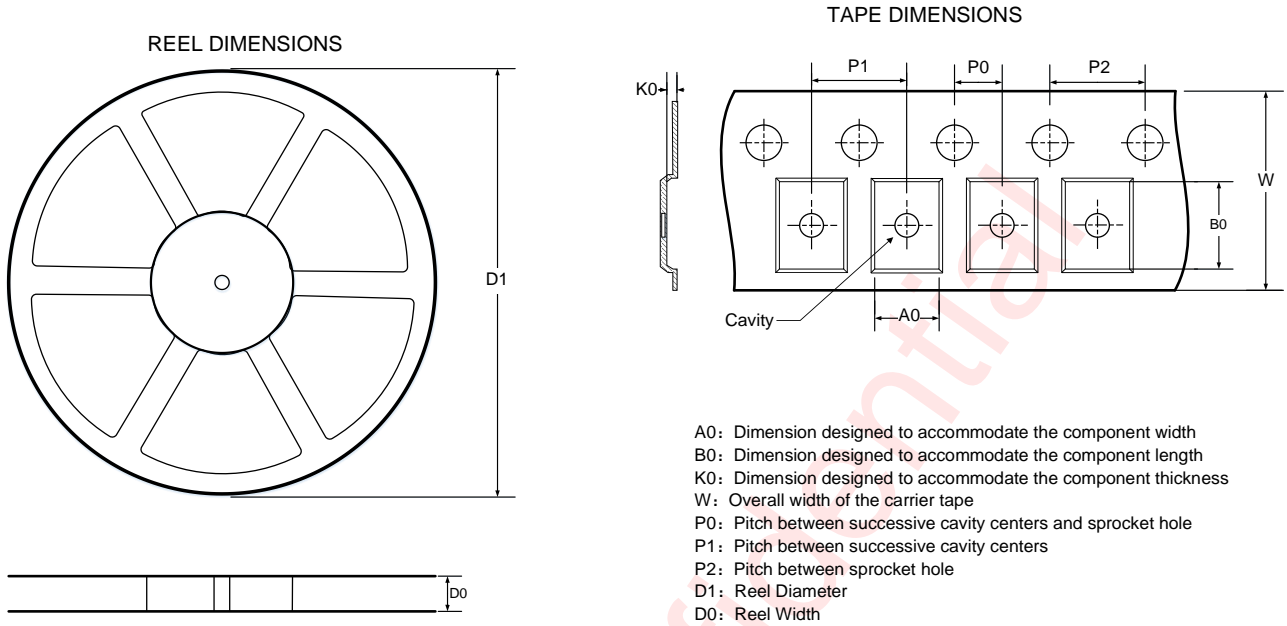
To obtain the optimal performance of AW35743G, PCB layout should be considered carefully. Here are some

guidelines:

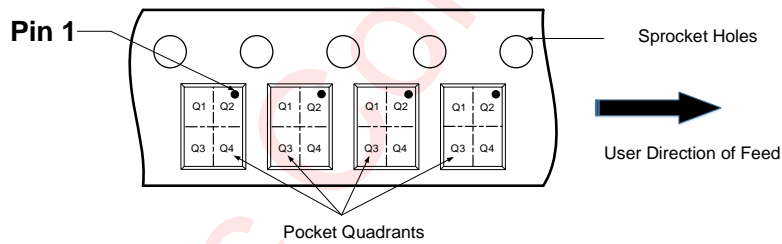
1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass capacitors near the D+/D- traces.
2. The differential characteristic impedance of D+ and D- traces is suggested to be 90Ω , and it's better to shield D+ and D- traces by ground planes.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals because they cause signal reflections.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.



Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



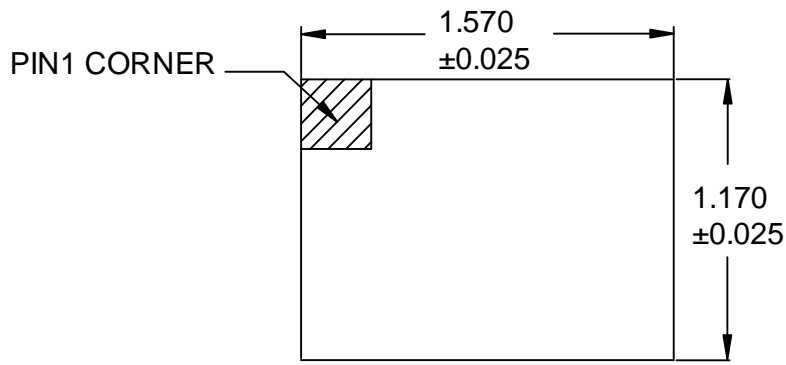
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

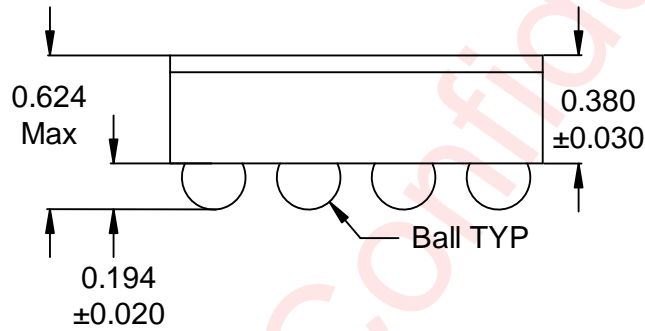
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	9.50	1.30	1.70	0.75	2.00	4.00	4.00	8.00	Q2

All dimensions are nominal

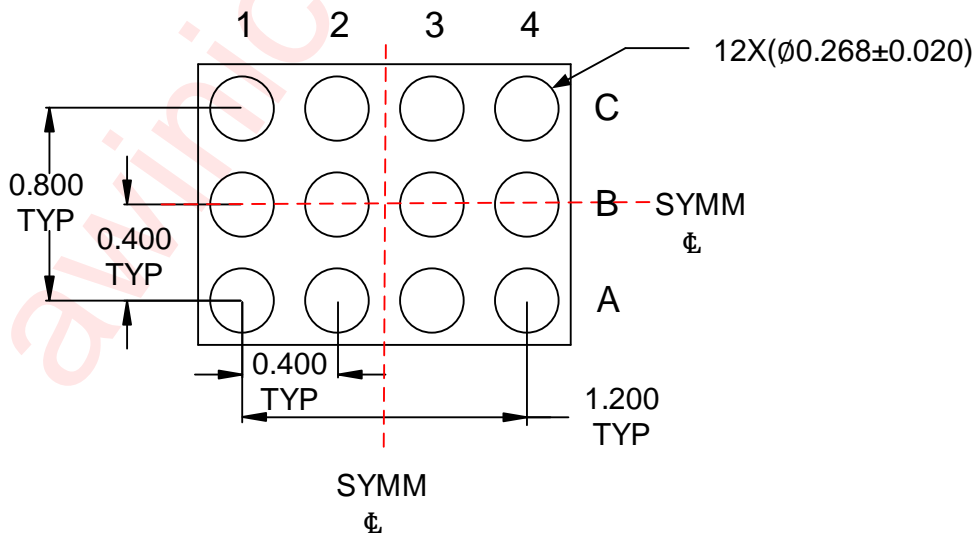
Package Description



Top View



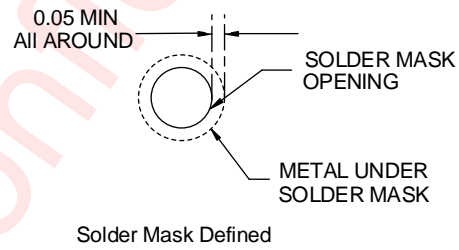
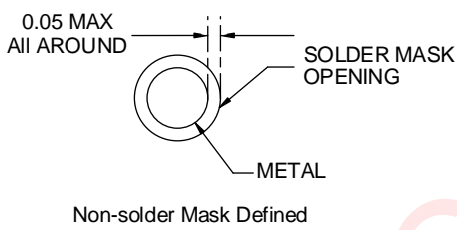
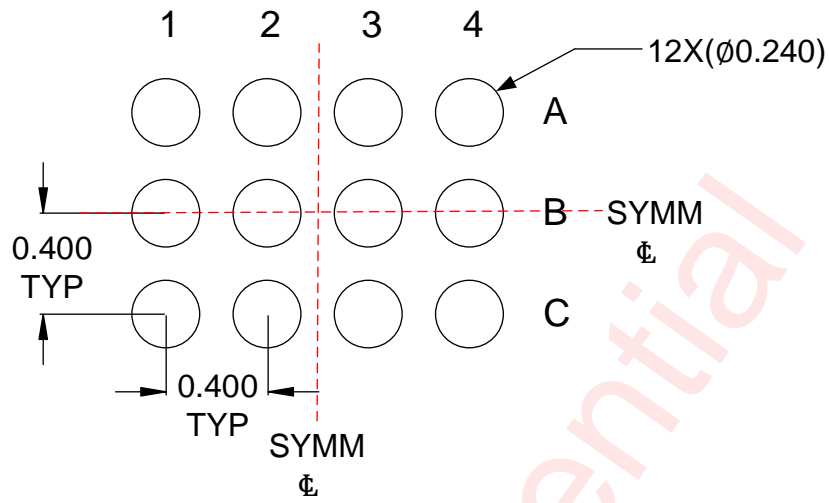
Side View



Bottom View

Unit: mm

Land Pattern Data



Unit: mm

Revision History

Version	Date	Change Record
V1.0	Aug. 2023	Officially released
V1.1	Nov.2023	Added the description of the reverse-blocking(P11)

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