

TECHNICAL DOCUMENTATION

Project:	X-NUCLEO-SPINAND-TOSH
Customer:	ARROW ELECTRONICS s.r.l.
FAE++ code:	2016-3025
Date:	03/01/2017
Revision:	001
Author:	Andrés Valda
Customer contact:	Amir Sherman

DOCUMENT REVISION

Revision	Date	Description
001	03/01/2017	First draft

INDICE

1	INTRODUCTION.....	3
2	BOARD DESCRIPTION AND GETTING STARTED	4
3	HARDWARE REQUIREMENTS.....	4
4	BOARD DRIVER	4
5	DRIVER CONFIGURATION	5
6	BASIC OPERATIONS	5
7	FIRMWARE EXAMPLE	6
8	BOARD SCHEMATIC AND PCB	6
8.1	STACKUP	6
8.2	PCB - GLOBAL VIEW	7
8.3	PCB – TOP VIEW	7
8.4	PCB - BOTTOM FLIP VIEW.....	8
8.5	PCB – SOLDER TOP VIEW	8
8.6	PCB – SOLDER BOTTOM FLIP VIEW.....	9
8.7	PCB – SILKSCREEN TOP VIEW.....	9
8.8	PCB – TOPOGRAPHIC TOP VIEW	10
8.9	PCB – MECHANICAL VIEW	10
9	BILL OF MATERIALS	11

1 INTRODUCTION

This document provides detailed hardware requirements and board connections for the TC58CVG2S0HRAIF Spi Nand Flash evaluation board based on chip TC58CVG2S0HRAIx from TOSHIBA. This board is part of Arrows' offering of evaluation boards designed around the Spi Nand Flash



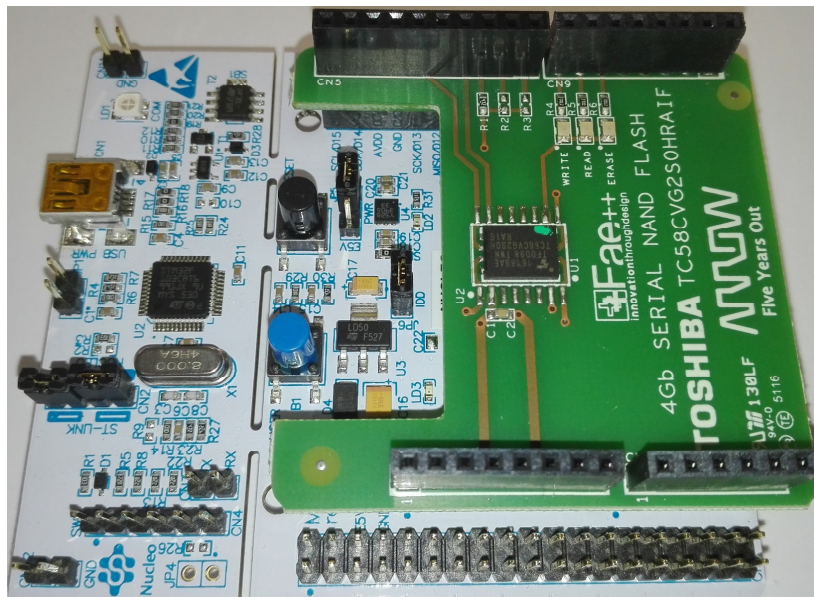
2 BOARD DESCRIPTION AND GETTING STARTED

The X-NUCLEO-SPINAND-TOSH board is the Toshiba TC58CVG2S0HRAIF 4Gb SPI NAND Flash evaluation board (shield) for STM32 Nucleo boards. It is compatible with the Arduino UNO R3 connector layout.

The X-NUCLEO-SPINAND-TOSH interfaces the memory with the STM32 MCU via SPI pin, and the user can change the default SPI clock.

3 HARDWARE REQUIREMENTS

The X-NUCLEO-SPINAND-TOSH is an expansion board intended for use with STM32 Nucleo boards. This shield have to be plugged on STM32 Nucleo (NUCLEO-F401RE) board as shown in Figure below



4 BOARD DRIVER

We provide a basic open source driver to read and write to the memory. Additional functions to drive the LEDs are provided too.

The driver is provided inside a firmware example built with STM32CubeMX, developed for the following platform:

- IAR Workbench

Using STM32CubeMX you should be able to migrate to other platforms such as:

- MDK 5
- MDK 4
- TRUEStudio
- SW4STM32

The files of the driver are:

- TC58_FPP_CMD.c
- MX35_FPP_CMD.h
- MX35_FPP_DEF.h

It depends on the ST HAL Libraries and it does not initialize the SPI peripheral (the code generated from the STM32CubeMX does that).

5 DRIVER CONFIGURATION

The driver can be customized through the following preprocessor directives:

DEFINE	VALUE	DESCRIPTION
FlashID	0x98CD	Memory identification value
FlashSize	0x20000000	Total size of the memory (512Mbyte)
FlashBlockNum	2048	Number of block in total
FlashBlockSize	0x40000	Size of a single block
FlashPageNum	64	Number of pages per block
FlashPageSize	4096	Size of the page data region
GPIO_SPI	NOT_DEFINED	If defined does not use any SPI peripheral but GPIO toggling
FLASH_TIMEOUT_VALUE	1000	Maximum time to wait for an operation in microseconds

6 BASIC OPERATIONS

Initialization can be performed with the following function:

void Initial_Spi().

Internally it sets WP and CS of the SPI peripheral and waits for a short delay to be sure that the memory is ready.

ID check operation can be formed by calling:

ReturnMsg CMD_RDID((uint16*)&flash_id);

Read operation can be performed by calling:

ReturnMsg CMD_READ(flash_addr);

ReturnMsg CMD_READ_CACHE(0, buffer, FlashPageSize, 0);

This sequence reads a page starting at flash_addr.

Erase operation can be performed by calling:

ReturnMsg CMD_BE(flash_addr);

Write operation can be performed by calling:

ReturnMsg CMD_PP_LOAD(0, buffer, FlashPageSize, 0);

ReturnMsg CMD_PROGRAM_EXEC(flash_addr);

Check TC58CVG2S0HRAIF/TC58CVG2S0HRAIG datasheet for additional informations.

7 FIRMWARE EXAMPLE

The firmware example provied performs:

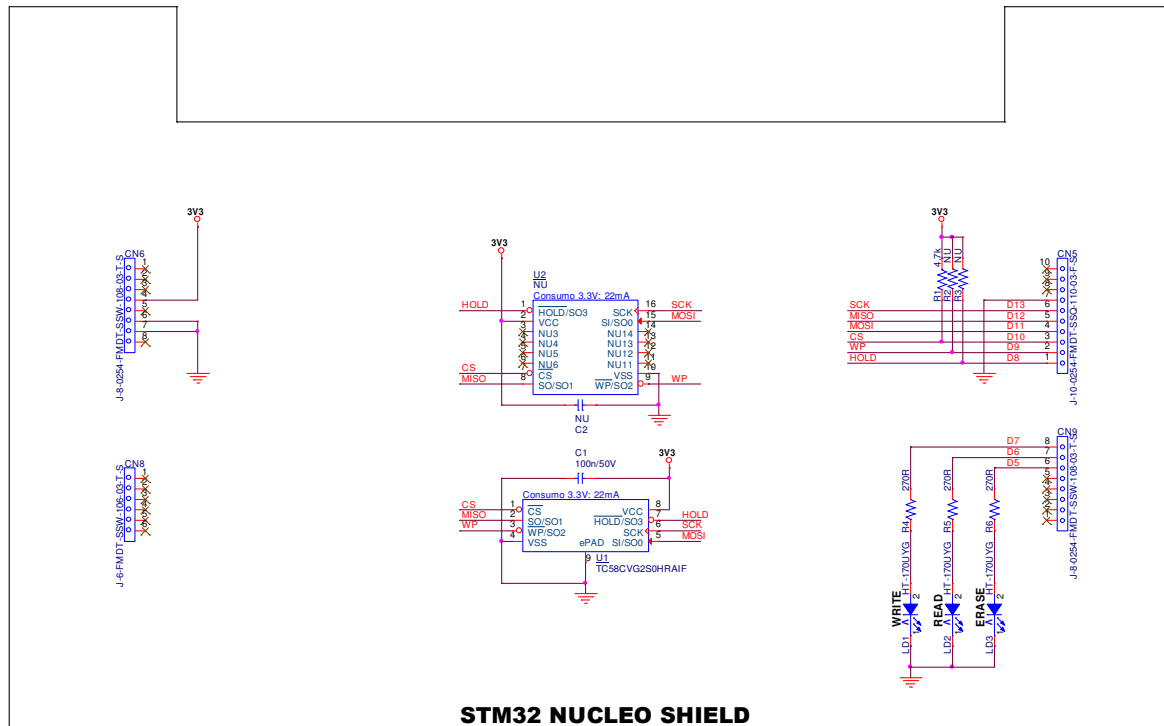
- Initial scan of bad blocks (**SearchBadBlock function**)
- Erase,Write,Read and data check of every non-bad block (**FlashTest function**)
- Read and data check for every non-bad-block from the previously written data (**VerifyTest function**)

Every LED on the board turns on according to the active operation.

You can also check the status of the operations by watching these global variables:

BadBlockCnt	Number of bad blocks detected
BlockNum	Current block that is being wirten or read
error_cnt	How many errors we have met so far, should be always 0

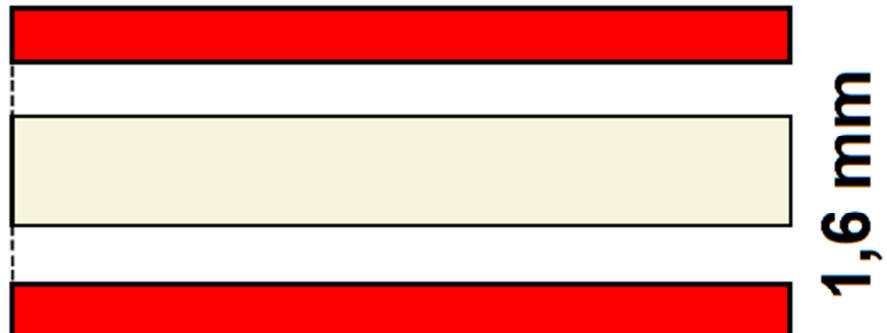
8 BOARD SCHEMATIC AND PCB



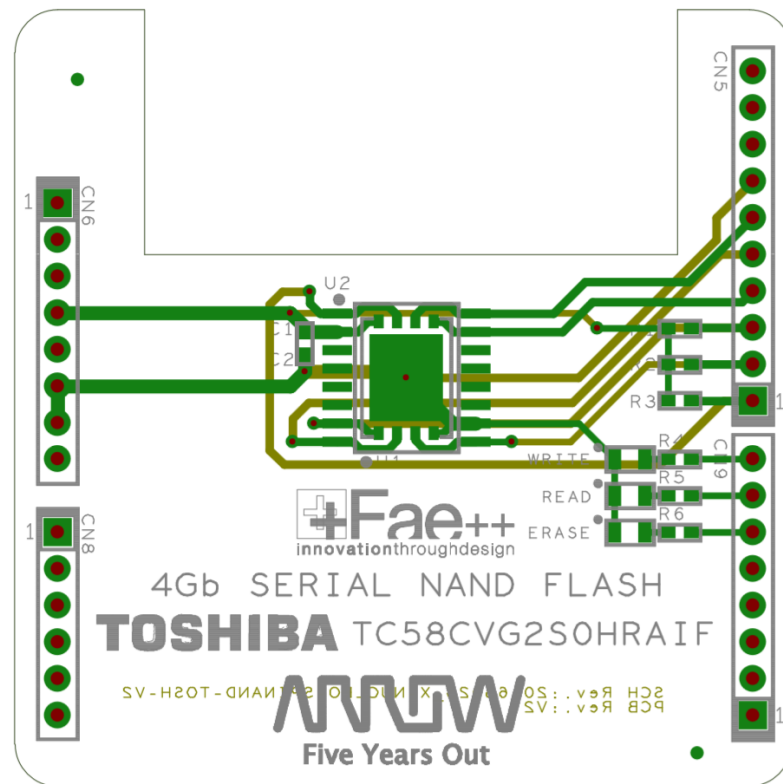
8.1 STACKUP

TOP

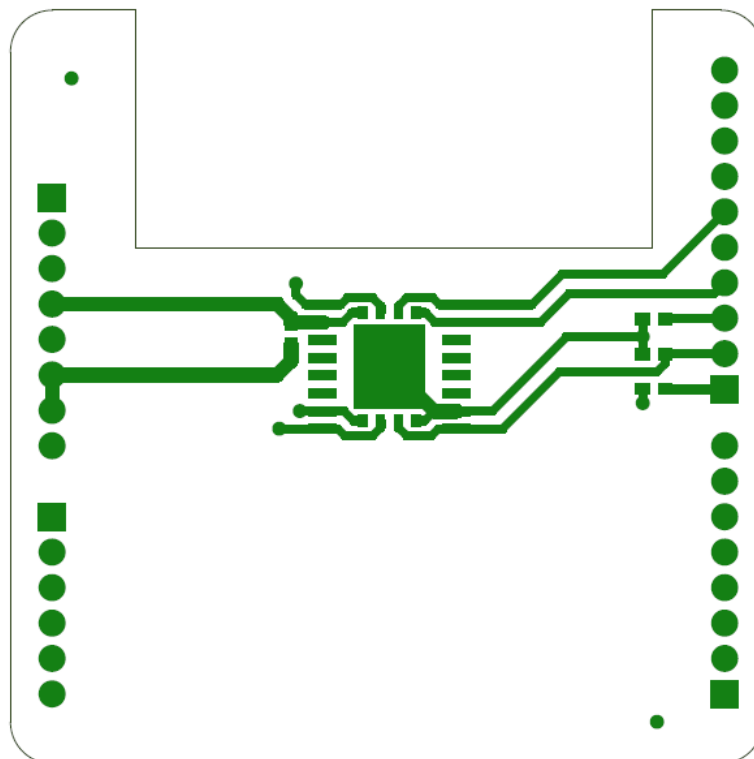
BOTTOM



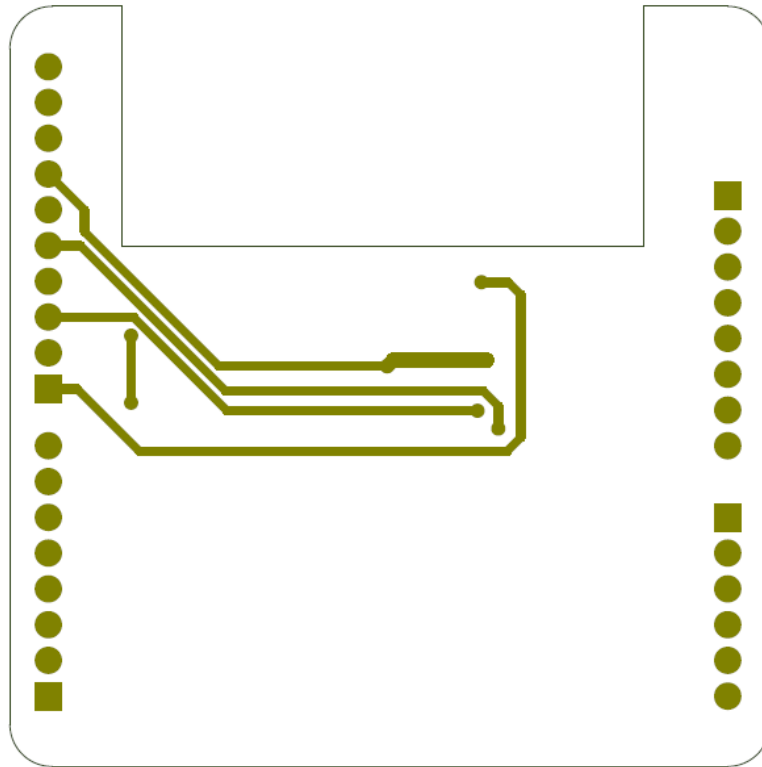
8.2 PCB - GLOBAL VIEW



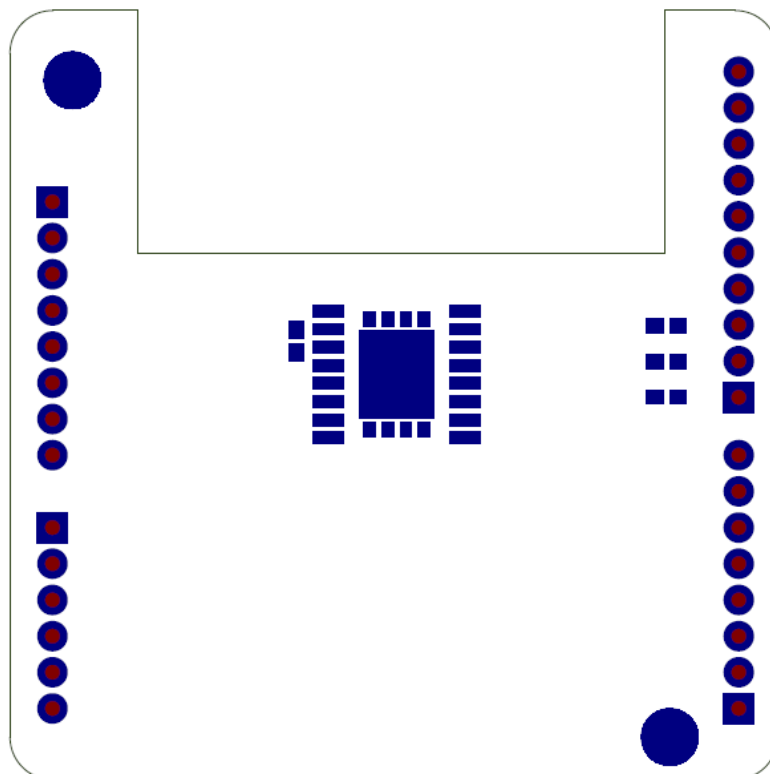
8.3 PCB – TOP VIEW



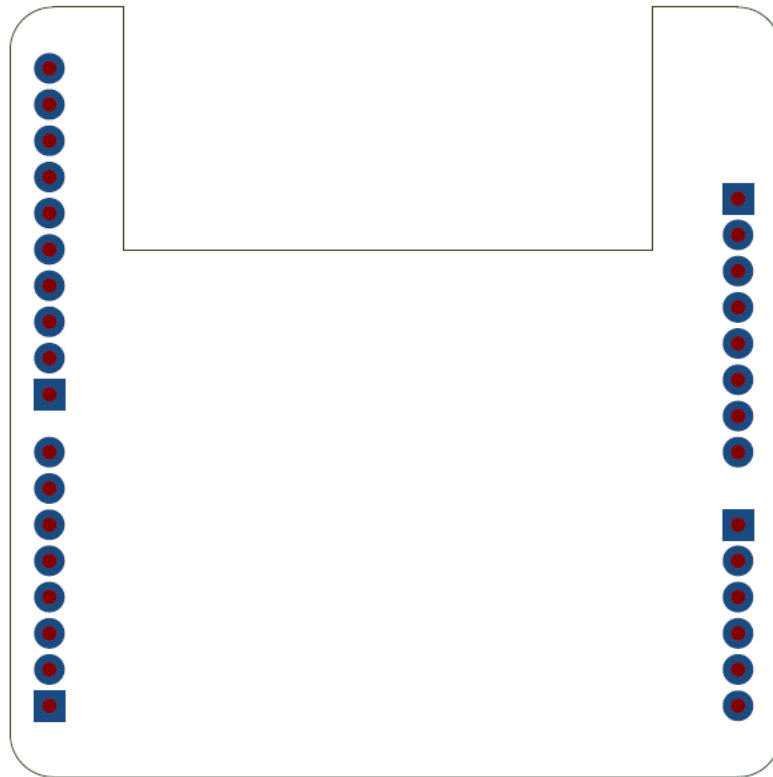
8.4 PCB - BOTTOM FLIP VIEW



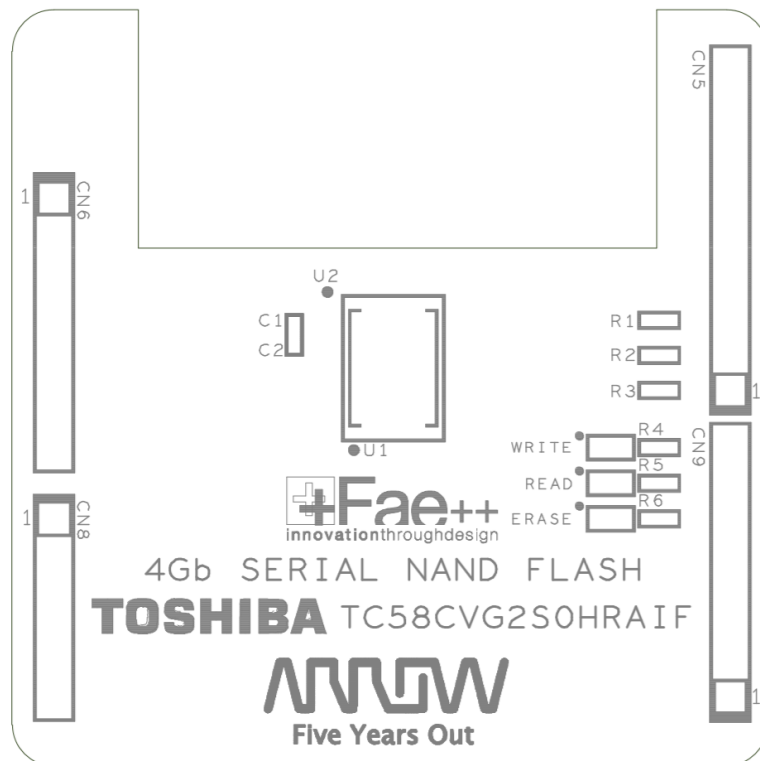
8.5 PCB – SOLDER TOP VIEW



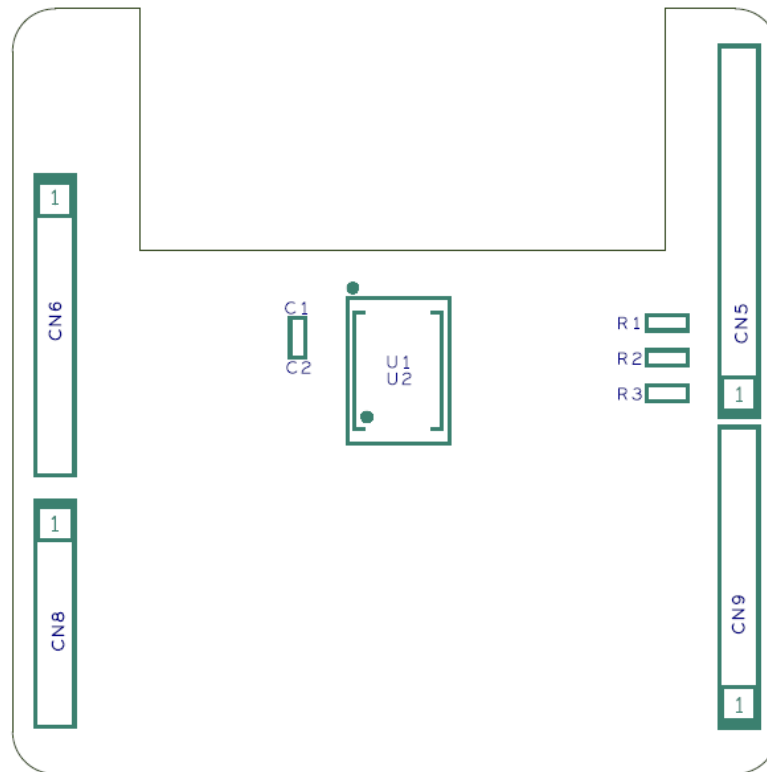
8.6 PCB – SOLDER BOTTOM FLIP VIEW



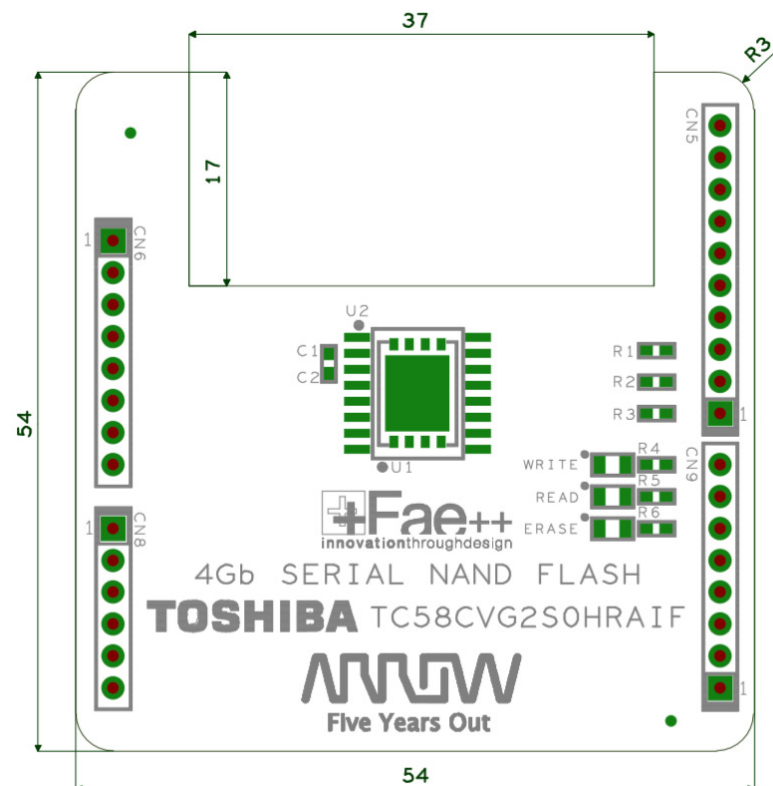
8.7 PCB – SILKSCREEN TOP VIEW



8.8 PCB – TOPOGRAPHIC TOP VIEW



8.9 PCB – MECHANICAL VIEW



9 BILL OF MATERIALS

Item	Quantity	Reference	Part	Description
1	1	CN5	J-10-0254-FMDT-SSQ-110-03-F-S	STRIP 10P F/D P=2.54 SSQ-110-03-F-S
2	2	CN6,CN9	J-8-0254-FMDT-SSW-108-03-T-S	STRIP 8P F/D P=2.54 SSW-108-03-T-S
3	1	CN8	J-6-FMDT-SSW-106-03-T-S	STRIP 6P F/D P=2.54 SSW-106-03-T-S
4	1	CS1	CS V1 2L 35um	C.S. X-NUCLEO-SPINAND-TOSH V1 (54x54)mm 2L/SO/SR sp=1.6mm Cu=35um
5	1	C1	100n/50V	CHIP CAP.CER. 100nF 50V 10% X7R 0603
6	3	LD1,LD2,LD3	HT-170UYG	DIODO LED VERDE HT-170UYG-DT HARVATEK 0805 SMT
7	1	R1	4.7k	CHIP RES. 4K7 0603 1/16W 1%
8	3	R4,R5,R6	270R	CHIP RES. 270R 0603 1/16W 1%
9	1	U1	TC58CVG2S0HRAIF	INTEGRATO TC58CVG2S0HRAIF WSON8 TOSHIBA SMT

NOT MOUNTED

1	1	C2	NU	CHIP CAP.CER. 100nF 50V 10% X7R 0603
2	2	R2,R3	NU	CHIP RES. 4K7 0603 1/16W 1%
3	1	U2	NU	INTEGRATO TC58CVG2S0HQAIE SOP16 TOSHIBA SMT