5V Synchronous Buck Converter

Features

- Up to 95% Efficiency
- 2.5V to 5.5V Input Voltage Range
- Adjustable Output Voltage from 0.6 V to VIN
- Low RDS(ON) Switches 50 mΩ / 30 mΩ
- 1.5MHz Typical Switching Frequency
- 3A Maximum Output Current
- Low Dropout With 100% Duty Cycle
- Power Save Mode for Light Load Efficiency
- 35μA Operating Quiescent Current
- Power Good Output
- Over Current Protection
- Over Temperature Protection
- Internal Soft Startup
- Available in FCSOT563-6L and FCDFN 1.6×1.2-6L Package

Applications

Mobile Phones
Set Top Box
Wireless Router
General Purpose POL Supply
Network Video Camera

General Description

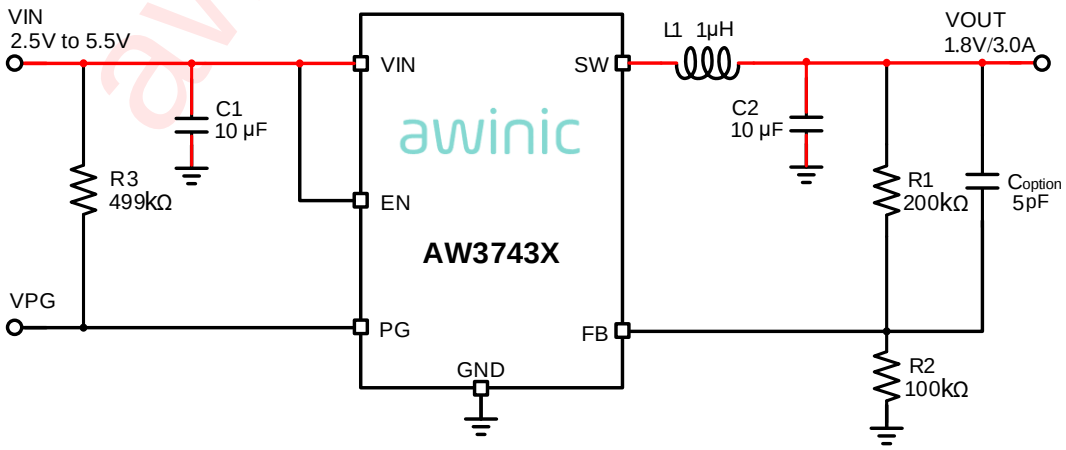
The AW3743X is a synchronous step-down buck DC-DC converter with high efficiency and low power consumption. The device integrates switches capable of delivering an output current up to 3 A.

The device operates at typically 1.5 MHz frequency pulse width modulation (PWM) at medium to heavy load currents. At light load, the device automatically converts to power save mode (PSM) to maintain high efficiency over the entire load current range. In shutdown, the current consumption less than 2 μA.

The AW3743X provides an adjustable output voltage via an external resistor divider. It has internal soft start circuit to limit the inrush current during startup. Other features like over current protection, over temperature protection and power good are built-in. The device is available in FCSOT563-6L and FCDFN 1.6×1.2-6L package.

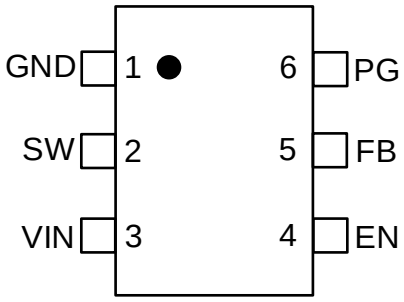
The AW3743X has two part numbers.The AW37431 can work in buck mode and bypass mode, the AW37430 can only work in buck mode.

Typical Application Circuit

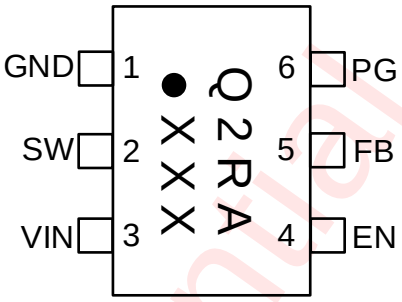


Pin Configuration And Top Mark

AW37430STR
(Top View)

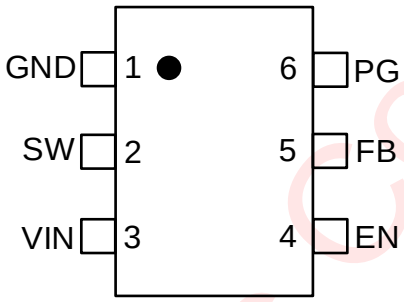


AW37430STR Marking
(Top View)

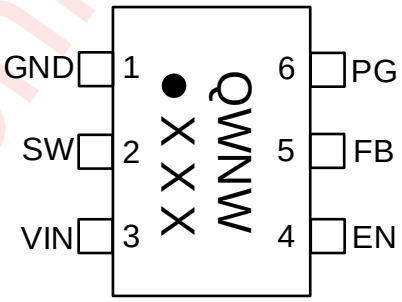


Q2RA - AW37430STR
XXX - Production Tracing Code

AW37431STR
(Top View)

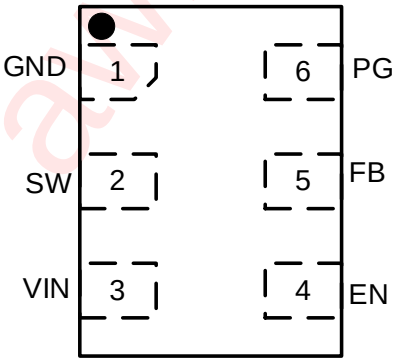


AW37431STR Marking
(Top View)

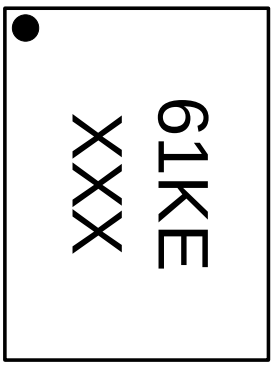


QWNW - AW37431STR
XXX - Production Tracing Code

AW37430FDR
(Top View)



AW37430FDR Marking
(Top View)

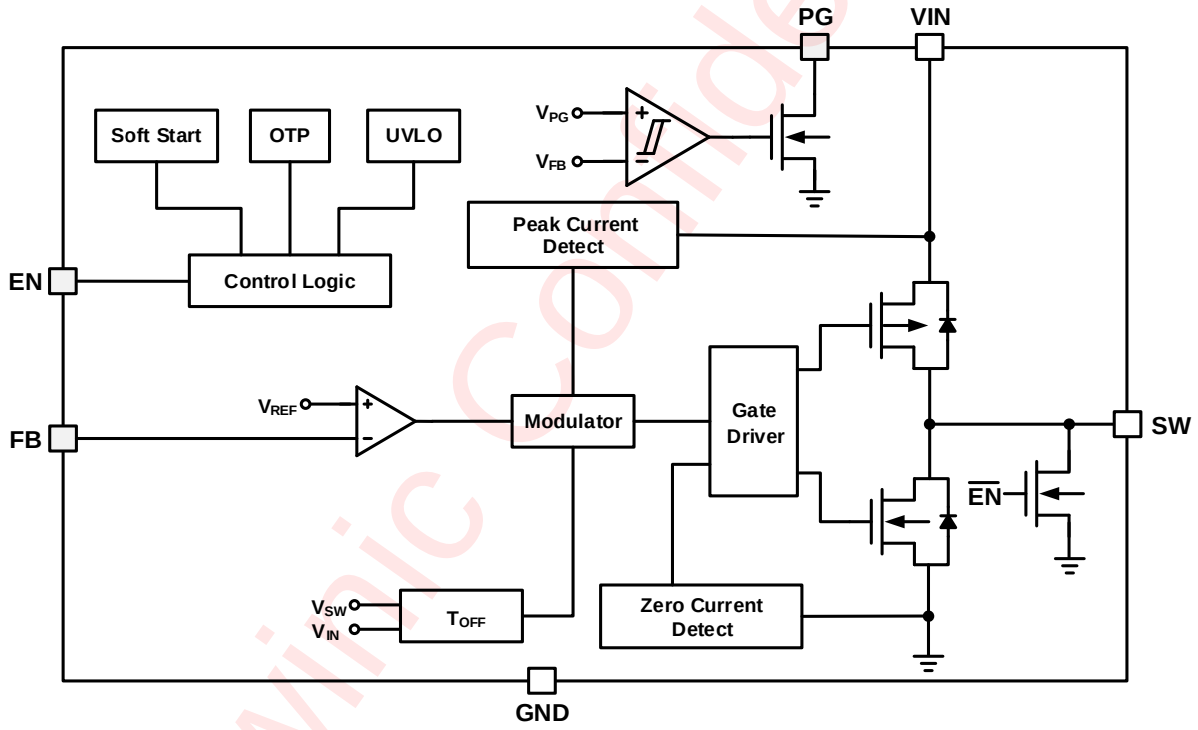


61KE - AW37430FDR
XXX - Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
1	GND	Ground pin.
2	SW	Switch pin of the converter, it is connected to the inductor.
3	VIN	IC power supply input.
4	EN	IC enable pin.
5	FB	Adjustable output voltage to converter's voltage feedback.
6	PG	Power good open drain out pin.

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37430STR	-40°C ~ 85°C	FCSOT563-6L	Q2RA	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW37431STR	-40°C ~ 85°C	FCSOT563-6L	QWNW	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW37430FDR	-40°C ~ 85°C	FCDFN 1.6×1.2-6L	61KE	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Voltage	VIN, EN, PG	-0.3V to 6V
	SW(DC)	-0.3V to VIN+0.3V
	SW(AC, less than 10ns)	-3V to 9V
	FB	-0.3V to 5.5V
Junction-to-ambient thermal resistance $R_{\theta JA}$		135.69°C /W (FCSOT563-6L)
		187.18°C /W (FCDFN1.6×1.2-6L)
Maximum operating junction temperature T_{JMAX}		150°C
Operating free-air temperature range T_J		-40°C to 150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM)		
HBM(NOTE 2)		±2kV
CDM(NOTE 3)		±1.5kV
Latch-Up		
Test condition: JESD78F		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

Symbol	PARAMETERS	Min	Typ	Max	Unit
VIN	Input voltage	2.5		5.5	V
VOUT	Output voltage	0.6		VIN	V
IOUT	Output current	0		3	A
T_A	Operating free-air temperature range	-40		85	°C
I_{SINK_PG}	Sink current at PG pin			1	mA
C1	Input capacitor	10	10		μF
C2	Output capacitor	10	10		μF

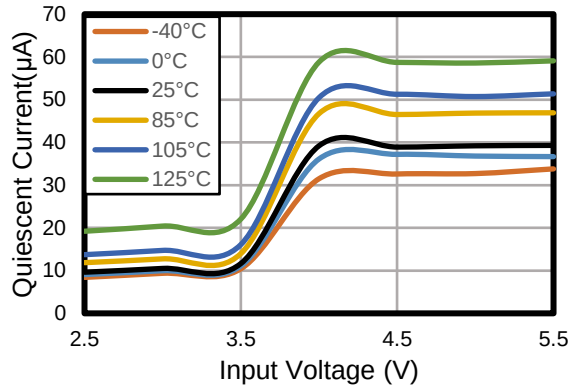
Electrical Characteristics

VIN=5.0V, T_A=25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN pin	Not switching		35		μA
I_{SD}	Shutdown current into VIN pin	EN =Low		0.1	2	μA
V_{UVLO}	Under voltage lock out	VIN falling		2.37	2.45	V
	Under voltage lock out hysteresis			120		mV
T_{OTP}	Over temperature protection	Junction temperature rising		150		°C
		Junction temperature falling		130		
LOGIC INTERFACE						
V_{IH}	High-level threshold at EN pin	2.5 V ≤ VIN ≤ 5.5 V	1.2			V
V_{IL}	Low-level threshold at EN pin	2.5 V ≤ VIN ≤ 5.5 V			0.4	V
t_{SS}	Soft startup time			700		μs
V_{PG}	Power good threshold	VFB rising, referenced to VFB nominal		95		%
		VFB falling, referenced to VFB nominal		90		%
$V_{PG,OL}$	Power good low-level output voltage	I_{SINK} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01		μA
$t_{PG,DLY}$	Power good delay time	VFB falling		30		μs
OUTPUT						
V_{FB}	Feedback regulation voltage		0.588	0.6	0.612	V
$R_{DS(on)}$	High-side FET on resistance			50		mΩ
	Low-side FET on resistance			30		
I_{LIM}	High-side FET current limit			4		A
f_{SW}	Switching frequency	VOUT = 2.5 V		1.5		MHz

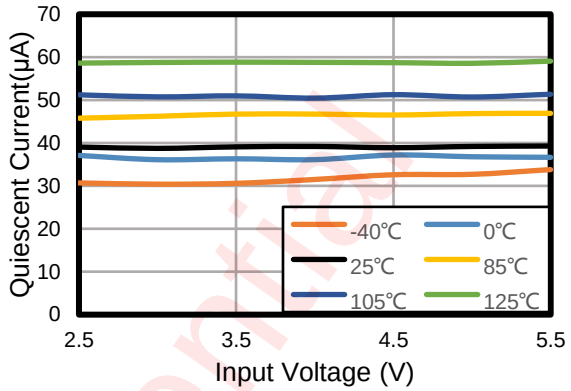
Typical Characteristics

T_A=25°C, VIN=5V, C1=10μF, C2=10μF, Cop=5pF, L=1μH, unless otherwise noted.



AW37431

Figure 1 IQ vs Input Voltage



AW37430

Figure 2 IQ vs Input Voltage

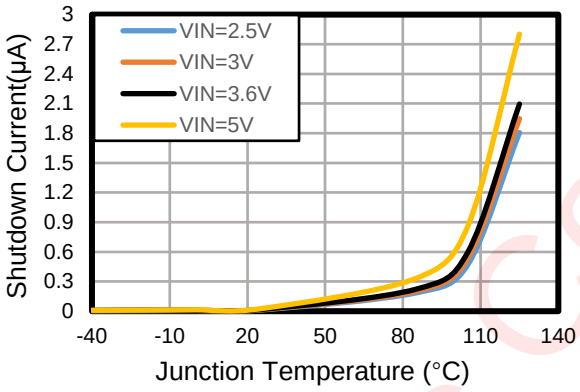


Figure 3 ISD vs Junction Temperature

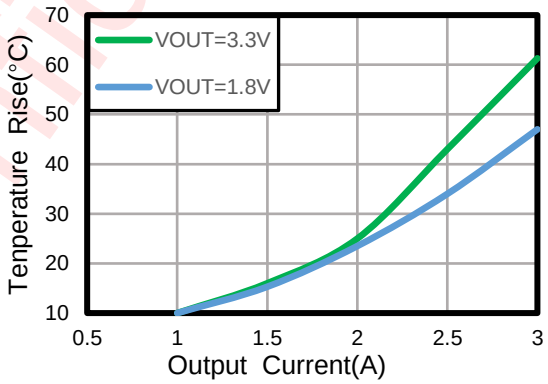
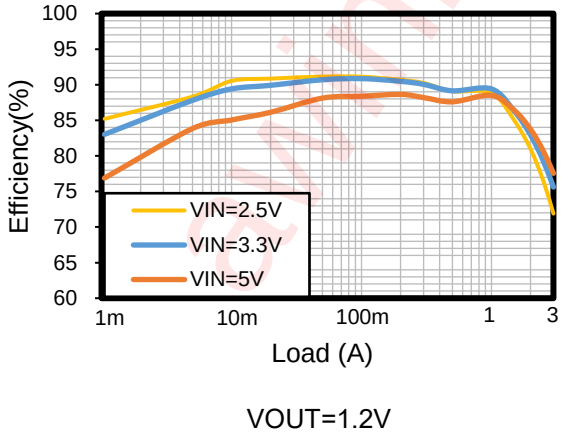
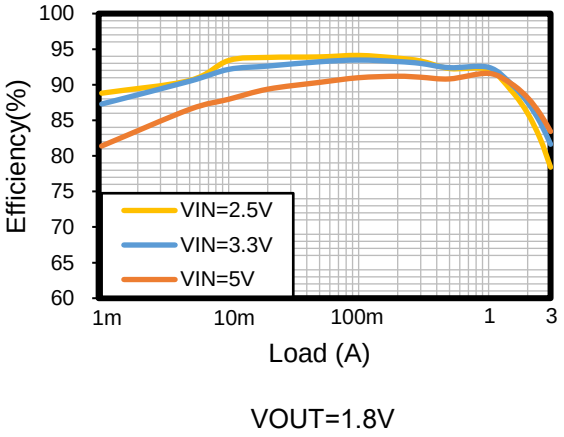


Figure 4 Temperature Rise on EVM



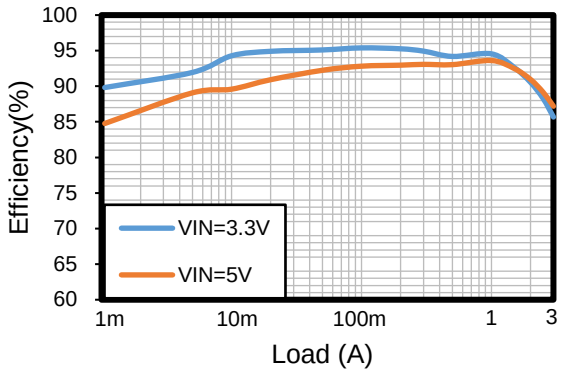
VOUT=1.2V

Figure 5 Load Efficiency with Different Inputs



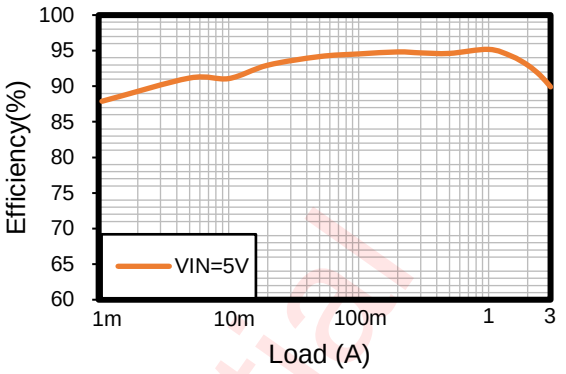
VOUT=1.8V

Figure 6 Load Efficiency with Different Inputs



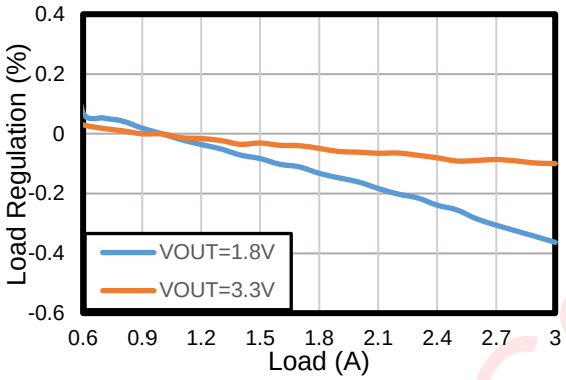
VOUT=2.5V

Figure 7 Load Efficiency with Different Inputs



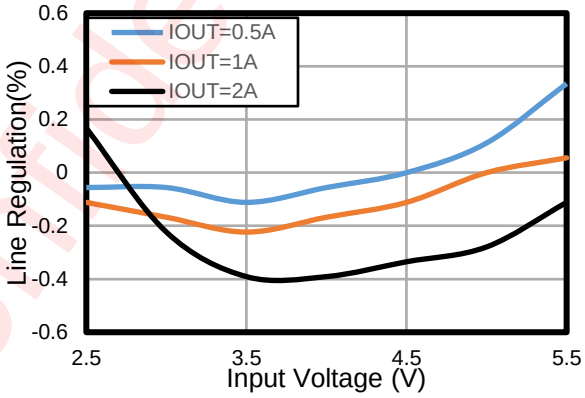
VOUT=3.3V

Figure 8 Load Efficiency with Different Inputs



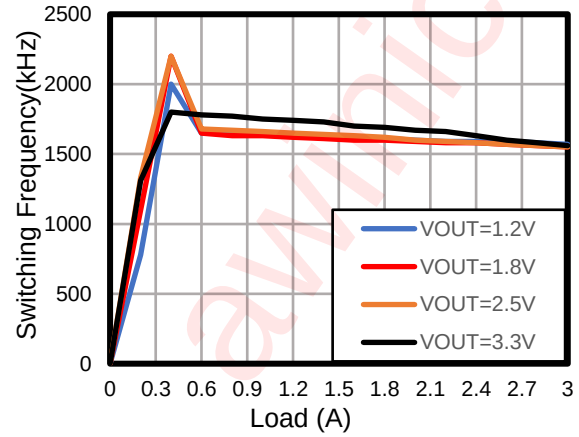
VIN = 5V

Figure 9 Load Regulation



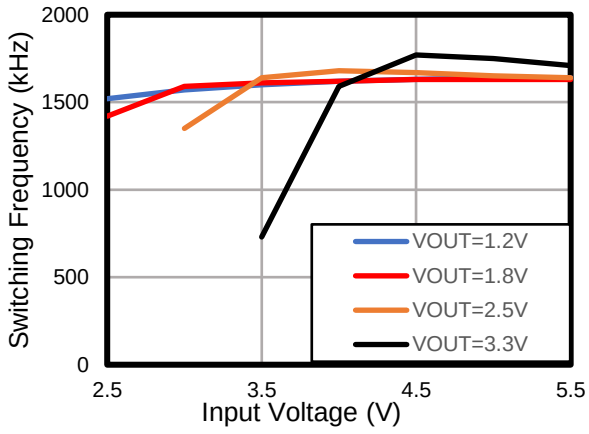
VOUT = 1.8V

Figure 10 Line Regulation



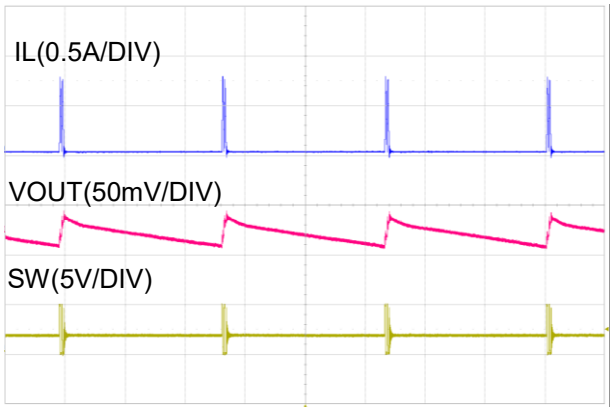
VIN = 5V

Figure 11 Switching Frequency



IOUT = 1A

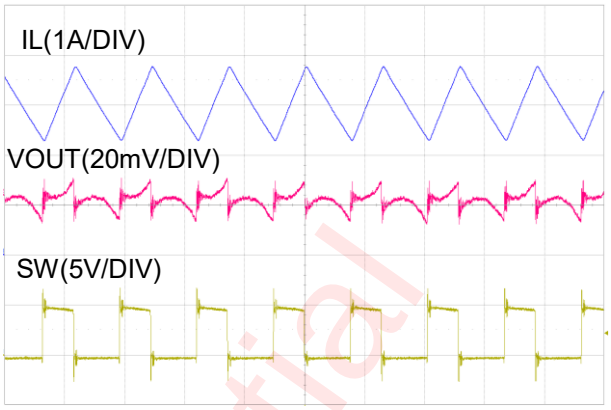
Figure 12 Switching Frequency



Time-10μs/DIV

VOUT = 1.8V IOUT = 0.01A

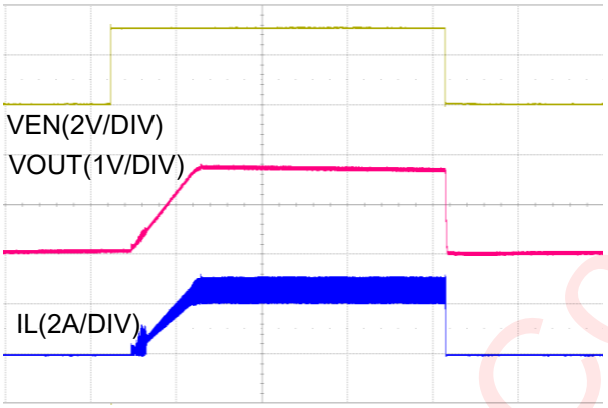
Figure 13 Power Save Mode Operation



Time-500ns/DIV

VOUT = 1.8V IOUT = 3A

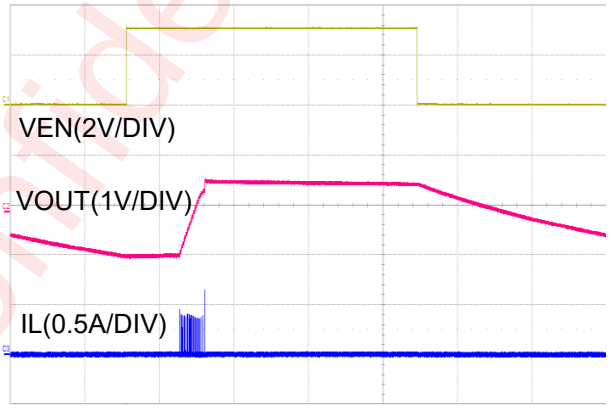
Figure 14 PWM Operation



Time-640μs/DIV

VOUT = 1.8V IOUT=3A

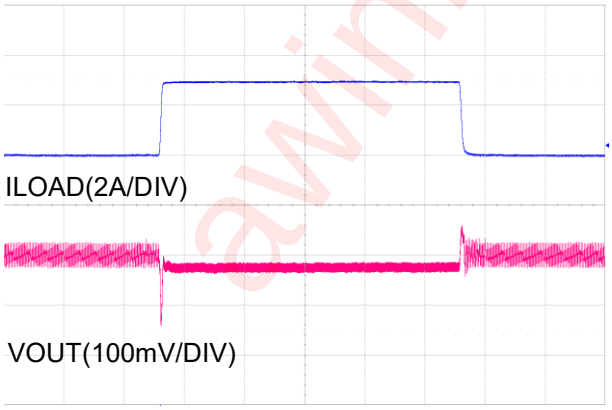
Figure 15 Start-Up and Shut-Down with Load



Time-640μs/DIV

VOUT = 1.8V IOUT=0A

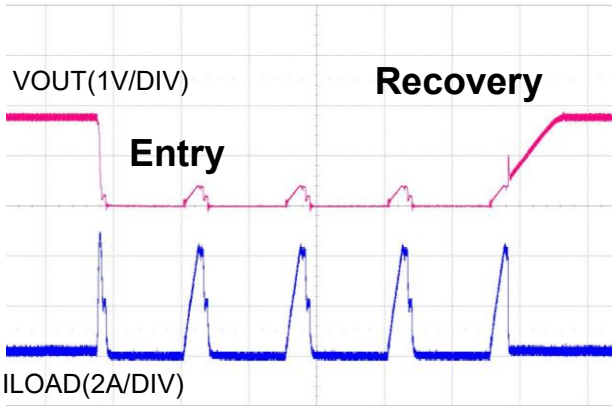
Figure 16 Start-Up and Shut-Down without Load



Time-200μs/DIV

VOUT = 1.8V IOUT = 0.1 A to 3 A

Figure 17 Load Transient



Time-200μs/DIV

VOUT = 1.8V IOUT = 0.1 A

Figure 18 Output Short Protection (HICCUP)

Detailed Functional Description

The AW3743X is a synchronous step-down buck DC-DC converter which operates with an adaptive off-time with peak current control scheme. At medium to heavy loads, the device operates in pulse width modulation (PWM) mode with 1.5MHz switching frequency. Based on the VIN/VOUT ratio, a circuit sets the required off time for the low-side MOSFET, which makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

Soft Reset

Internal soft startup circuitry ramps up the output voltage after enabling the device. During a startup time, the AW3743X starts with the applied bias voltage and ramps the output voltage to its nominal value. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

Under-voltage Lockout

An insufficient supply voltage may cause malfunctions in the device circuitry. An under-voltage lockout (UVLO) is implemented to avoid wrong operation of the device at low input voltages. It shuts down the device when voltages lower than V_{UVLO} with a hysteresis. When the input voltage exceeds the rising UVLO threshold, the device restarts with a fresh startup sequence. The hysteresis of UVLO is 120mV.

Switch Current Limit and Short Circuit Protection (HICCUP)

The AW3743X has the switch current limit, which can prevent the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or an over load or shorted output circuit condition. When the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off-time.

When this switch current limits is triggered 32 times, the device reduces the current limit for further 32 cycles and then stops switching to protect the output. The device will start a new startup after a typical delay time of 500μs. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the startup.

Over temperature protection

To protect the device from overheating damage, the temperature of die is monitored. If it exceeds the shutdown threshold, the switching will be stopped and the device shuts down. Once the device temperature falls below the falling threshold, the device returns to normal operation automatically.

Enable and Disable

The AW3743X is enabled by setting the EN pin to logic high, and shutdown mode is forced when the EN pin is pulled low with a shutdown current of typically 0.1μA. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal output discharge FET discharges the output through the SW pin smoothly.

Power Good

The AW3743X has a power good output. When the output is up to 95% of the nominal voltage, the PG pin goes high. The PG pin will be driven low when the output voltage falls to 90% of the nominal voltage.

The PG pin is an open-drain output, which specified to sink up to 1 mA. It requires a pull-up resistor connecting to any voltage rail less than 5.5V. The PG signal can be used to sequence multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not sed.

Low Dropout Operation with 100% Duty Cycle

The AW3743X can operate at 100% duty cycle for minimal input-to-output voltage difference. During this mode, the AW3743X keep the high-side switch constantly on and low-side switch constantly off. The lowest input voltage for keeping the output regulated in this mode is determined by load current, DC resistance(DCR) of the inductor and the on-resistance of the rectifying PMOS as the following formula:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L)$$

where：

V_{IN_MIN} is minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is maximum output current.

R_L is DC resistance(DCR) of the inductor.

R_{DSON} is high-side MOSFET on-resistance.

Bypass

The AW37431STR will works in bypass mode when VIN is below 3.6V. In bypass mode, the device stops switching and works as a load switch. The high-side switch constantly turns on and low-side switch constantly turns off. Different with the 100% duty cycle, the determination of bypass mode is only related to input voltage. In bypass mode, the AW37431STR shuts down some modules to reduce the quiescent current below 10μA. When VIN raising above 3.7V, the AW37431STR automatically switches from bypass mode to buck mode.

Application Information

Setting The Output Voltage

The output voltage is set by an external resistor divider according to:

$$VOUT = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right)$$

R_2 must not be higher than 100kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. The inductor current ripple is determined by the Inductance value. The below equation indicates how to calculate the maximum inductor current under static load conditions.

$$I_{L,MAX} = I_{LOAD,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = VOUT \times \frac{1 - \frac{VOUT}{VIN}}{L \times F_{SW}}$$

where

$I_{LOAD,MAX}$ = maximum output current

ΔI_L = inductor current ripple

F_{SW} = switching frequency

L = inductor value

We recommend choosing the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$. A higher inductor value is also useful to lower ripple current but increases the transient response time as well. Selecting an inductor with low DCR provides better efficiency.

The AW3743X has different performance with different inductance. At light load, an inductor of 1μH is recommended for high efficiency, and at medium to heavy loads, use an inductor of 0.47μH to maintain higher efficiency.

Input and Output Capacitor Selection

The architecture of the AW3743X allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications,10μF input capacitor is sufficient, a larger value reduces input voltage ripple.

The AW3743X is designed to operate with an output capacitor of 10μF to 22μF. A feed forward capacitor reduces the output ripple in PSM and improves the load transient response.

Output Filter Design

The inductor and the output capacitor together provide a low-pass filter for removing switching AC components and passing the DC voltage to the output. To simplify the seletion process, the following table outlines possible inductor and capacitor value combinations for most applications. Note that variations as high as +20% to -30% in the effective induance due to tolerances and saturation/derating is expected. Similarly, for the output capacitor output capacitor, due to tolerances and bias voltage derating the effictive capacitance can vary by +20% to -50%. For better performance and stability, a feed forward capacitor of 5pF should be used. Next table lists some suitable high frequency inductor and ceramic capacitor combinations that can be applied for most applications.

Some Suitable Combinations L and C Values for the LC Filter

VOUT[V]	L[μH]	C_{OUT}[μF]		
		4.7	10	22
≥1.2V	0.47		✓	✓
	1		✓✓	✓
< 1.2V	0.47			✓
	1			✓

Note: '✓✓' means more recommended for most applications.

For lower ripple at small output voltages (< 1.2V), a larger output capacitance is needed (at least 22μF).

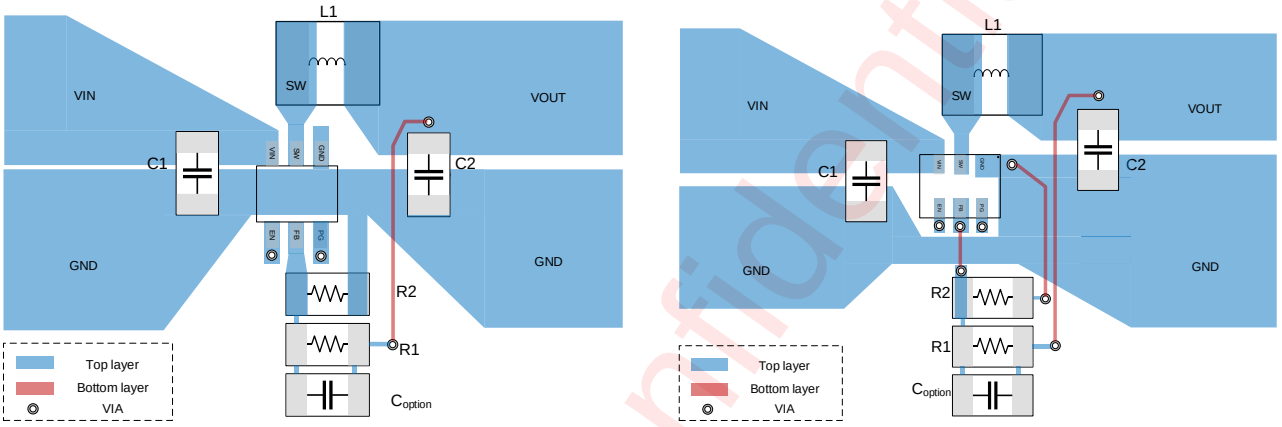
PCB Layout Consideration

The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.

The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.

The sense traces connected to FB is a signal trace. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.

A common ground should be used. GND layers might be used for shielding.



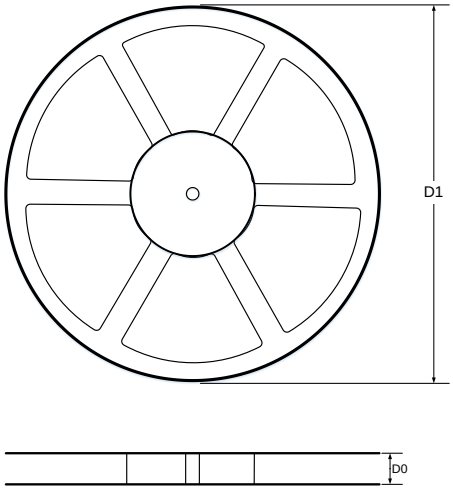
AW37430/431STR PCB Layout AW37430FDR PCB Layout

Figure 19 PCB Layout Recommendation

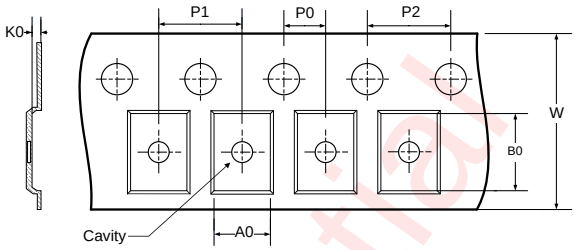
Tape And Reel Information

FCSOT563-6L

REEL DIMENSIONS

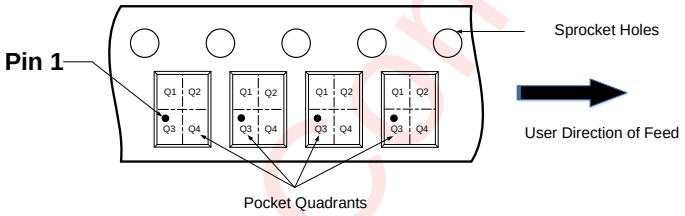


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

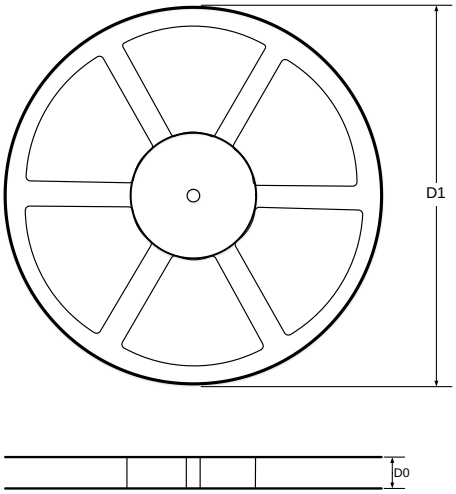
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179	8.6	1.80	1.83	0.75	2	4	4	8	Q3

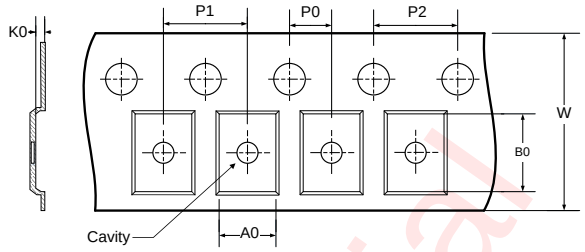
All dimensions are nominal

FCDFN 1.6×1.2-6L

REEL DIMENSIONS



TAPE DIMENSIONS



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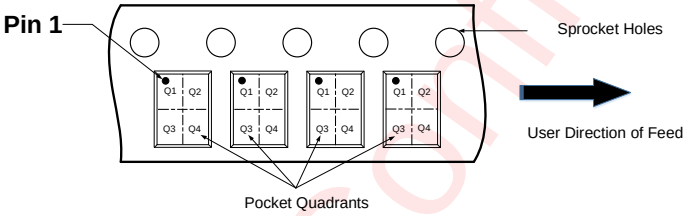
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

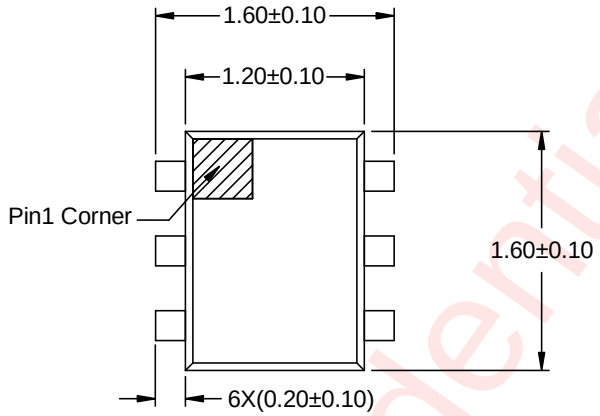
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.40	1.37	1.77	0.55	2	4	4	8	Q1

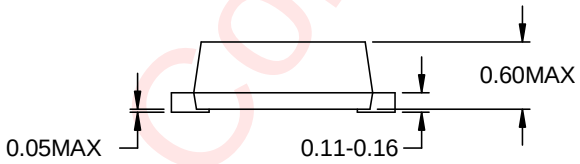
All dimensions are nominal

Package Description

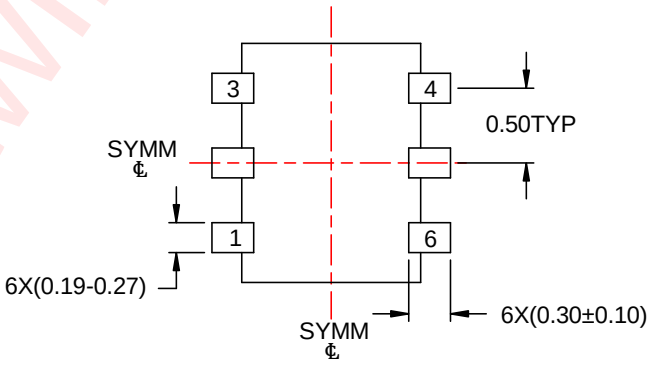
FCSOT563-6L



Top View



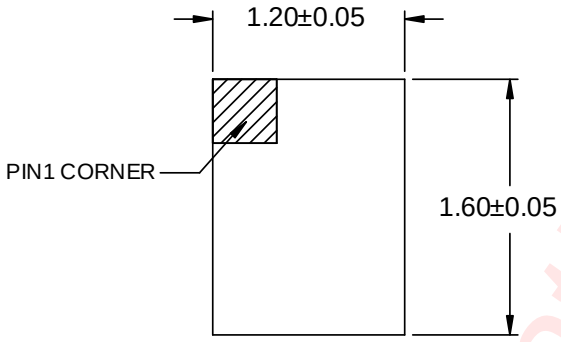
Side View



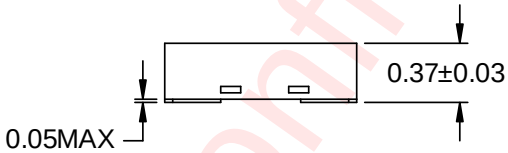
Bottom View

Unit:mm

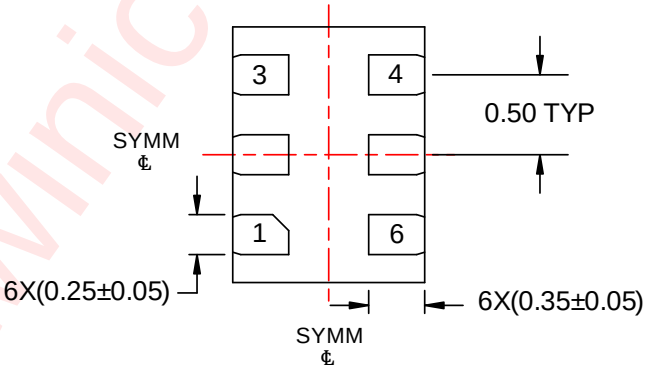
FCDFN 1.6×1.2-6L



Top View



Side View

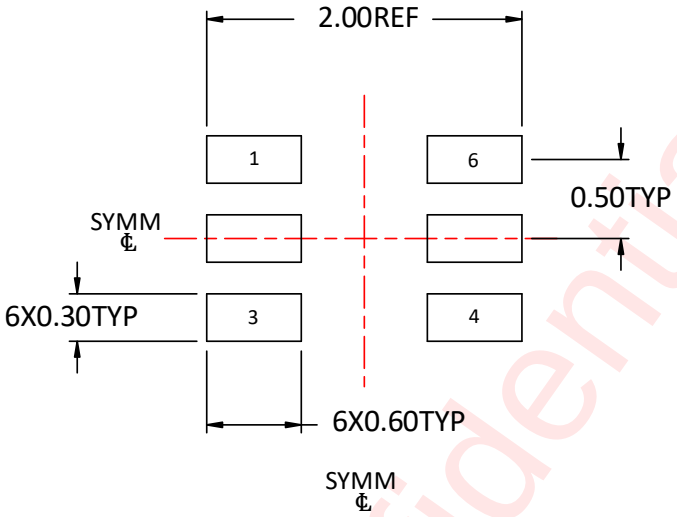


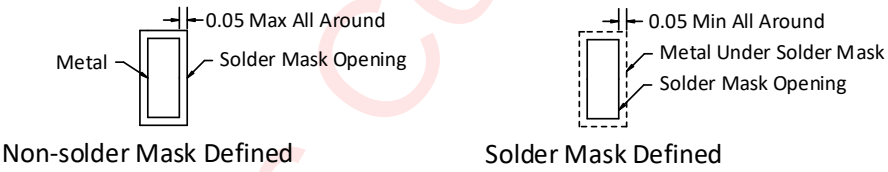
Bottom View

Unit:mm

Land Pattern Data

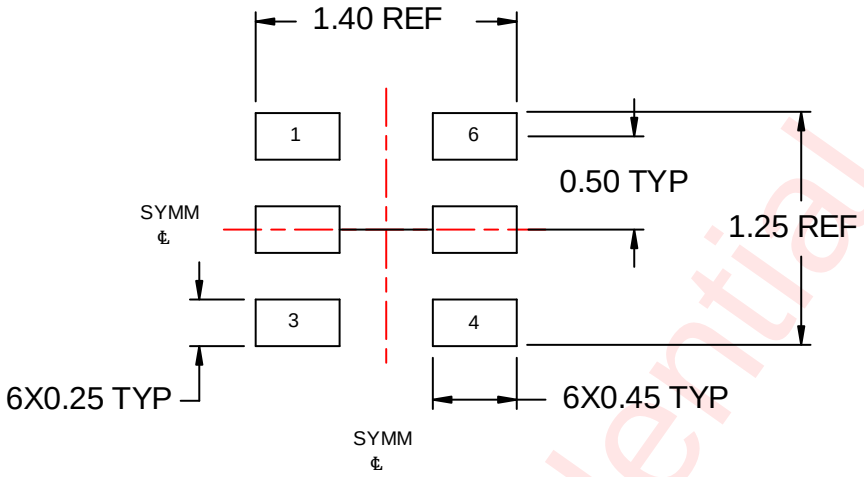
FCSOT563-6L

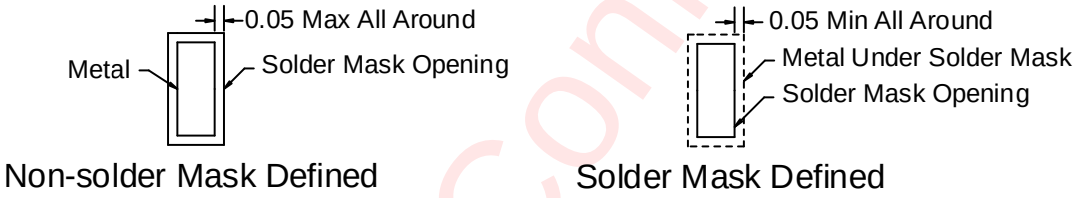




Unit: mm

FCDFN 1.6×1.2-6L





Unit: mm

Revision History

Version	Date	Change Record
V1.0	Mar. 2023	Officially released
V1.1	Apr.2023	Added the content of the AW37430FDR
V1.2	Jun.2023	1. Added the value range of T_A in recommended operating conditions.(P4) 2. Added the chapter of “Low Dropout Operation with 100% Duty Cycle” and modified the chapter of “Bypass”.(P10) 3. Modified the chapter of “Output Filter Design”.(P12)

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