6-Channel Capacitive Touch Controller with 9-LED Driver

FEATURES

- 6-channel capacitive input with sensitivity configurable
  - RF noise suppression
  - Intrinsic capacitance cancelling
  - Adaptive environmental variation compensation
  - Auto calibration
- User-configurable gesture detection (slide and click)
- 9 LED driver controlled by SRAM program
  - 256word x16bit program SRAM
  - Individual 8-step DC current, max 24.5mA
  - Individual 256 step PWM dimming, 9 bit PWM resolution
- Touch and gesture triggers LED lighting program
- I^2C compatible Interface: 1.8V ~ 2.8V, device address 0x2C/0x2D selectable
- Interrupt output pin
- Single power supply: 3.0V~4.5V
- TSSOP7.8mm×6.4mm_24L Package

GENERAL DESCRIPTION

AW9069 integrates 6-channel capacitive input detection and a smart SRAM-controlled 9-LED driver. By SRAM programming and register configuration, the touch and/or gesture could trigger pre-defined program to generate funny and complicated LED lighting effect as feedback without the aid of external MCU, so as to greatly enhance the interactive experience and reduce power consumption.

High performance sigma-delta capacitance digital conversion technology is adapted to detect input capacitance, and further touch and gesture decision is implemented by internal DSP.

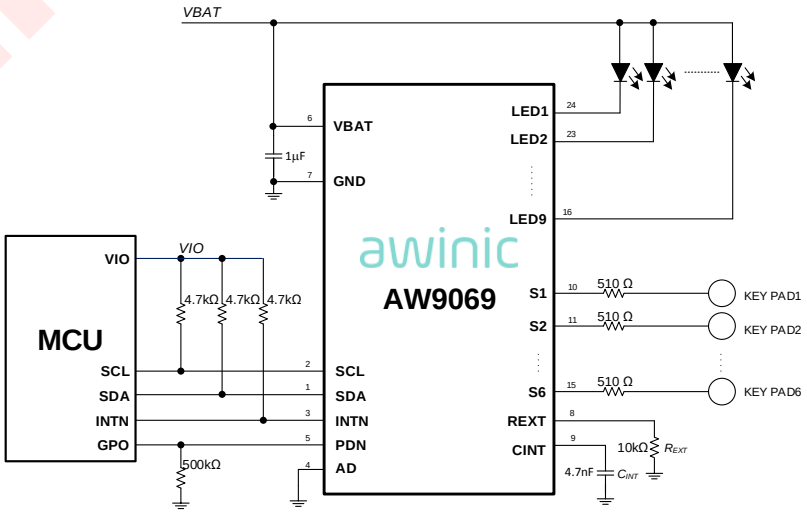
9 LEDs are driven by independent constant current sinks with PWM duty adjustment. Each LED is selectable to be controlled by I^2C interface directly or internal program in SRAM.

The device provides 400kHz fast I^2C compatible interface with device address set by AD pin. The operating voltage range is 3.0V~4.5V.

APPLICATIONS

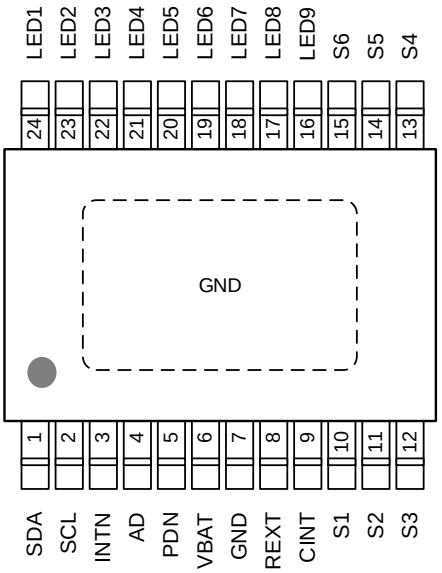
White goods appliances, Intelligent devices

TYPICAL APPLICATION CIRCUIT

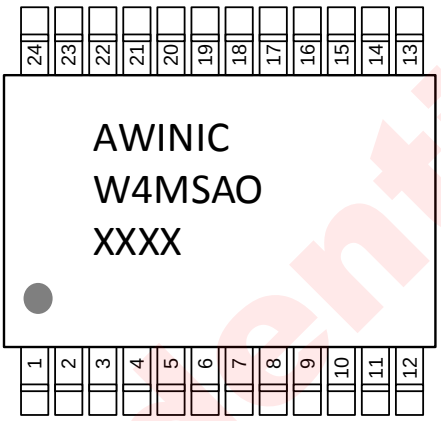


PIN CONFIGURATION AND TOP MARK

Pin Configuration
(Top View)



Top Mark
(Top View)



AWINIC - Company Logo
W4MSAO - Part Marking
XXXX - Manufacture tracing code

Figure 1 AW9069 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	SDA	Serial data I/O for I^2C interface
2	SCL	Serial clock input for I^2C interface
3	INTN	Interrupt output (Open-drain), low Active. (Typically tie 4.7kΩ resistor to V_{IO}).
4	AD	I^2C device address selection. Internally pulled down to GND.
5	PDN	Power down pin, low active(internal 1Mohm pull-down resistor)
6	VBAT	Power supply (3.0V to 4.5V)
7	GND	Ground
8	REXT	External resistor for adjusting sensitivity (typical is 10kΩ)
9	CINT	External reference capacitor(typical is 4.7nF)
10	S1	Capacitive touch input S1, floating if un-used
11	S2	Capacitive touch input S2, floating if un-used
12	S3	Capacitive touch input S3, floating if un-used
13	S4	Capacitive touch input S4, floating if un-used
14	S5	Capacitive touch input S5, floating if un-used
15	S6	Capacitive touch input S6, floating if un-used
16	LED9	LED9 cathode driver, anode connected to VBAT

17	LED8	LED8 cathode driver, anode connected to VBAT
18	LED7	LED7 cathode driver, anode connected to VBAT
19	LED6	LED6 cathode driver, anode connected to VBAT
20	LED5	LED5 cathode driver, anode connected to VBAT
21	LED4	LED4 cathode driver, anode connected to VBAT
22	LED3	LED3 cathode driver, anode connected to VBAT
23	LED2	LED2 cathode driver, anode connected to VBAT
24	LED1	LED1 cathode driver, anode connected to VBAT
Thermal Pad	GND	Ground

FUNCTIONAL BLOCK DIAGRAM

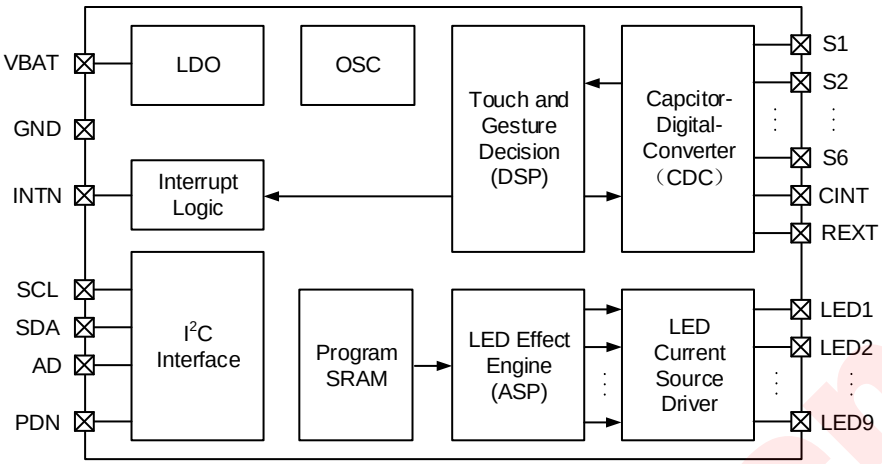


Figure 2 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

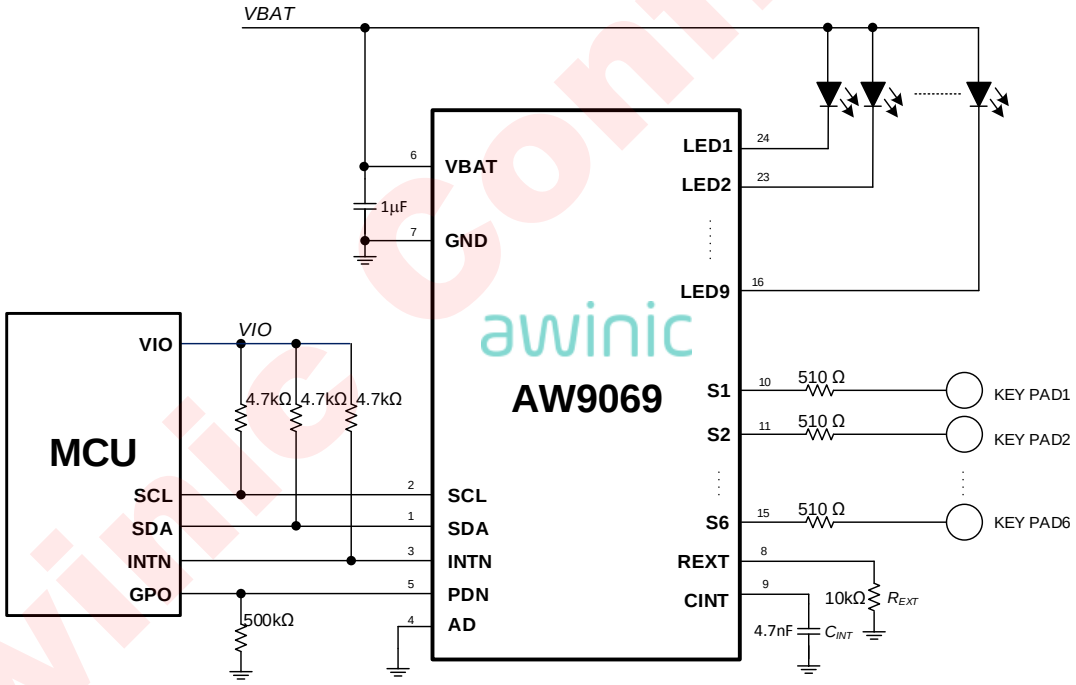


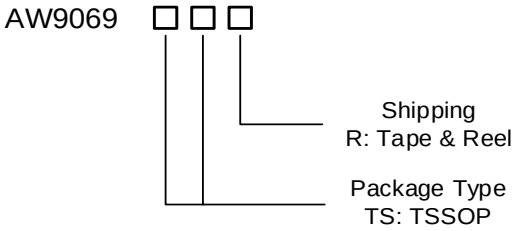
Figure 3 AW9069 Typical Application Circuit

NOTE1. Pin S1 - S6 must be connected to a 500Ω ~ 600Ω resistor.

NOTE2. C_{INT} and R_{EXT} should be placed as close as possible to the chip.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW9069TSR	-40℃~85℃	TSSOP 7.8mmX6.4mm -24L	AWINIC W4MSAO	MSL3	ROHS+HF	3000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATINGS(NOTE 3)

PARAMETERS		RANGE
Supply voltage range V_{BAT}		-0.3V to 5V
Input voltage range	SCL, SDA, AD	-0.3V to 3.6V
	PDN, LED1~9	-0.3V to 4.5V
Output voltage range	SDA, INTN	-0.3V to 3.6V
Junction-to-ambient thermal resistance θ_{JA}		29℃/W
Operating free-air temperature range		-40℃ to 85℃
Maximum Junction temperature T_{JMAX}		150℃
Storage temperature T_{STG}		-65℃ to 150℃
Lead Temperature (Soldering 10 Seconds)		260℃
ESD(NOTE 4)		
HBM		±4000V
CDM		±2000kV
Latch-up		
Test Condition: JEDEC STANDARD NO.78E SEPTEMBER 2016		+IT：450mA -IT：-450mA

NOTE3: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE4: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9*

ELECTRICAL CHARACTERISTICS

V_{BAT}=3.8V, T_A=25℃ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{BAT}	Power supply		3.0	3.8	4.5	V
$I_{SHUTDOWN}$	Current in Shutdown mode	PDN=GND		8	15	μA
$I_{STANDBY}$	Current in Standby mode	PDN=V_{IO}		130	160	μA
I_{ACTIVE}	Current in LED Active mode	PDN=V_{IO}, GCR=0x01		0.55	0.8	mA
	Current in Touch Active mode	PDN=V_{IO}, GCR=0x02		0.85	1.0	mA
	Current in Touch & LED Active mode	PDN=V_{IO}, GCR=0x03		1.0	1.5	mA
F_{OSC}	Internal oscillator Frequency		15.2	16	16.8	MHz
Digital Logical Interface						
V_{IL}	Logic input high level	SDA,SCL,AD,PDN	-0.3		0.45	V
V_{IH}	Logic input low level	SDA,SCL,AD,PDN	0.9			V
I_{IL}	Low level input current	SDA,SCL,AD,PDN		5		nA
I_{IH}	High level input current	SDA,SCL,AD,PDN		5		nA
V_{OL}	Logic output low level	SDA, INTN I_{OUT}=3mA			0.4	V
I_{OL}	Maximum output current	SDA, INTN			10	mA
I_L	Output leakage current	SDA,INTN Open drain			1	μA
Capacitive Sensor						
CX_{range}	Range(NOTE5)	S1 to S6	0		80	pF
$CX_{resolution}$	Resolution(NOTE5)	S1 to S6	0.02			pF
F_{SCAN}	Scan frequency			30		Hz
T_{DET}	Response time			100		ms
LED Driver						
I_{MAX}	Max LED current of LED1~9	I_{LED}=24.5mA	18.5	24.5	30.5	mA
I_{MATCH}	Matching accuracy	I_{LED}=24.5mA			10	%
$V_{DROPOUT}$	Drop-out voltage	I_{LED}=24.5mA			300	mV
F_{PWM}	PWM frequency	LCR.FREQ=1	110	122	135	Hz
		LCR.FREQ=0	220	244	270	Hz

NOTE5：the value is tested in default configuration.

I²C INTERFACE TIMING

Parameter Name			MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs

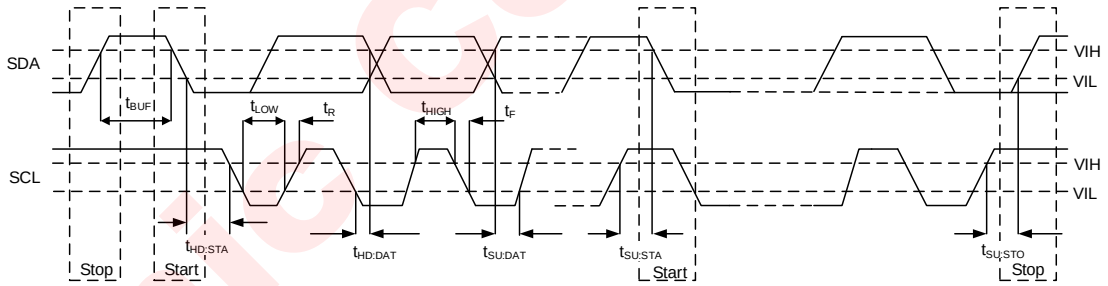


Figure 4 I²C Timing

FUNCTIONAL DESCRIPTION

WORK MODE

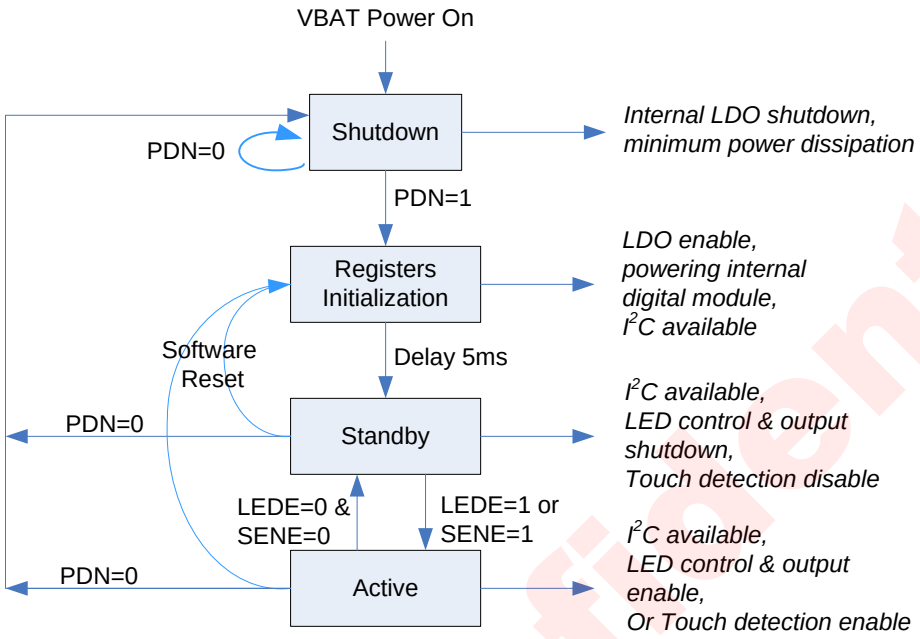


Figure 5 AW9069 Work Mode

After VBAT powered on, if pin PDN is low, the AW9069 is in shut-down mode, the current consumption is typically less than 10μA. When PDN pin becomes high, the internal LDO is activated, and a power-on reset (POR) signal is generated to reset all internal registers, the device enters standby mode in low power consumption state, when all circuit functions are disabled. In standby mode, I^{2}C interface is active, all internal configuration register can be written. If control bit GCR.SENE or/and GCR.LEDE is set to “1”, the device enters the active mode.

RESET

Hardware Reset

When pin PDN changes from low to high, the power-up reset (POR) signal is generated, all internal registers are reset.

Software Reset

Writing 0x55AA to register RSTR via I^{2}C interface will activate a software reset to reset all internal registers.

I^{2}C INTERFACE

AW9069 supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. I^{2}C interface voltage range is 1.8V~3.3V.

Device Address

The I²C device address (7-bit, followed by the R/$\overline{W}$ bit(Read=1/Write=0)) of AW9069 depends on the status of pin AD. When pin AD is tied low or floating, the device address is 0x2C; when pin AD is tied high, the device address is 0x2D.

0	1	0	1	1	0	AD	R/$\overline{W}$

Figure 6 Device Address Configuration

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

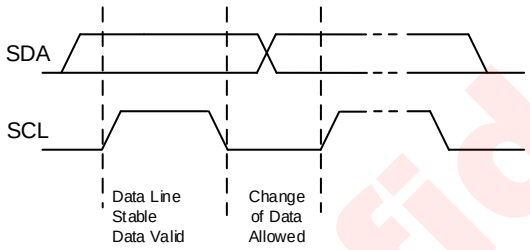


Figure 7 Data Validation Diagram

ACK(Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be releases; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, AW9069 sends 8bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, AW9069 sends the next data. If ACK is not sent by master, AW9069 stops to send data and waits for I²C stop.

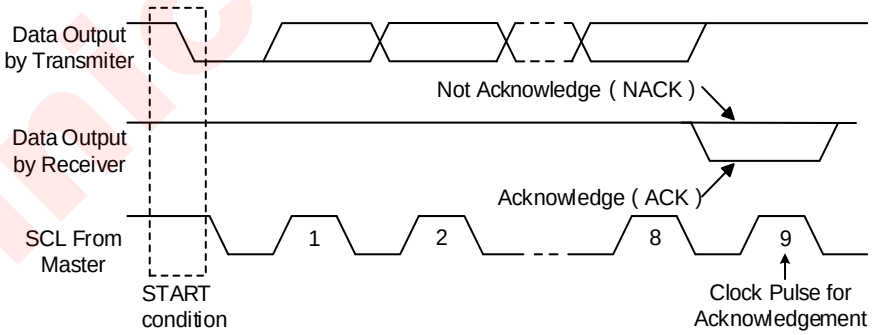


Figure 8 I²C ACK Timing

I²C Start/Stop

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

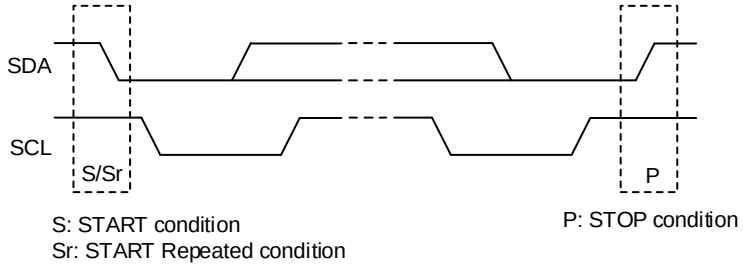


Figure 9 I²C Start/Stop Condition Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit ($R/\overline{W}$ = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data high 8Bit to be written to the addressed register

g) Slave sends acknowledge signal

h) Master sends data low 8Bit to be written to the addressed register

I) Slave sends acknowledge signal

j) Master generates STOP condition to indicate write cycle end

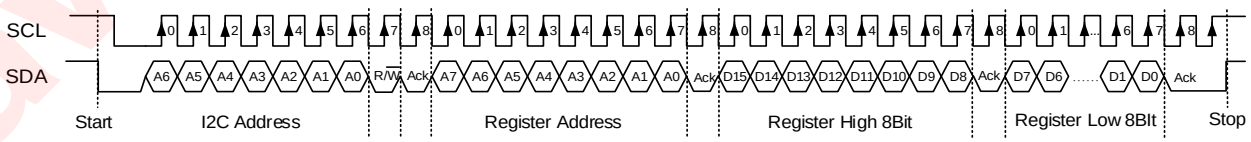


Figure 10 AW9069 I²C Write Timing

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/$\overline{W}$ = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/$\overline{W}$ = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data high 8Bit from addressed register.

j) Master sends acknowledge signal

k) Slave sends data low 8Bit from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. If master sends no acknowledge signal, the slave device stop to send data and wait for STOP condition.

m) If the master device generates STOP condition, the read cycle is ended.

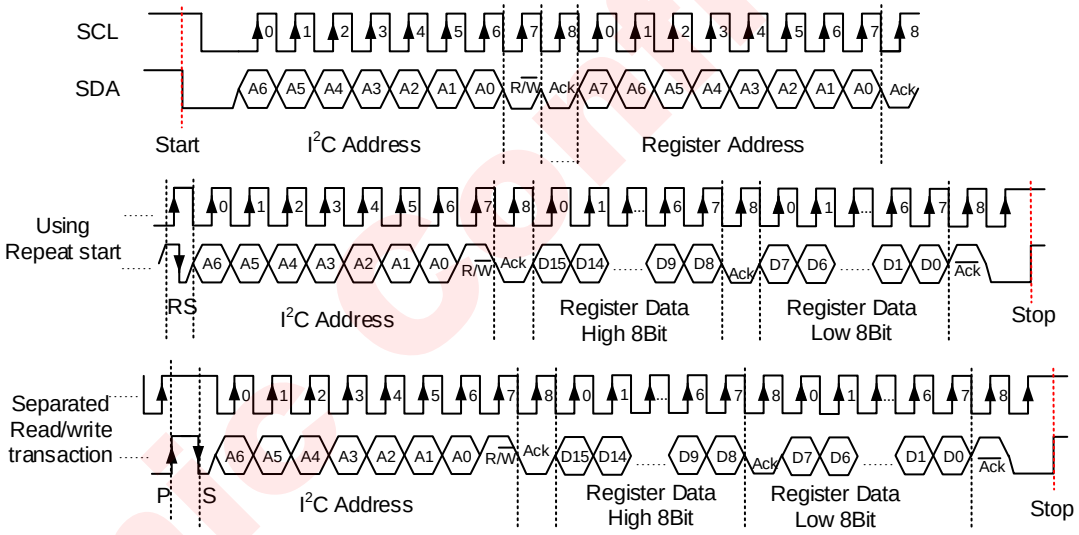


Figure 11 AW9069 I²C Read Timing

OSCILLATOR

An internal oscillator provides clock for both capacitive touch detecting and LED controlling circuit. If bit SENE or LENE in register GCR is set, the OSC starts to work, the start-up time is about 5 us. When both the register bit SENE and LEDE are “0”, the internal OSC stops.

CAPACITIVE TOUCH DETECTION

With high performance sigma-delta capacitive digital conversion technology, the capacitance on pin Sx is measured, the finger touch decision is made according to the increment of Sx capacitance. Before finger touched, the key capacitance is only formed by the sensing electrode and surrounding ground, which is called intrinsic capacitance usually. When finger touched, an additional parallel plate capacitor (electrode-media-finger) is formed, resulting in the capacitance value increment on pin Sx. In general,

because of the variation of different electrode size and dielectric characteristic of media materials, the capacitance increment caused by finger touch varies in a range of about 0.5pF~5pF.

In AW9069, the resolution of CDC data is 12-bit. the sampling period can be set by control register. The capacitive sample are send to DSP for further processing, including digital filtering, base-line compensation, touch and gesture judge, and so on.

The capacitive sensitivity can be adjusted by externally connected resistance R_{EXT} between pin REXT and GND. The bigger the R_{EXT} value, the higher the sensitivity. By default, R_{EXT} is recommended to be 10kΩ.

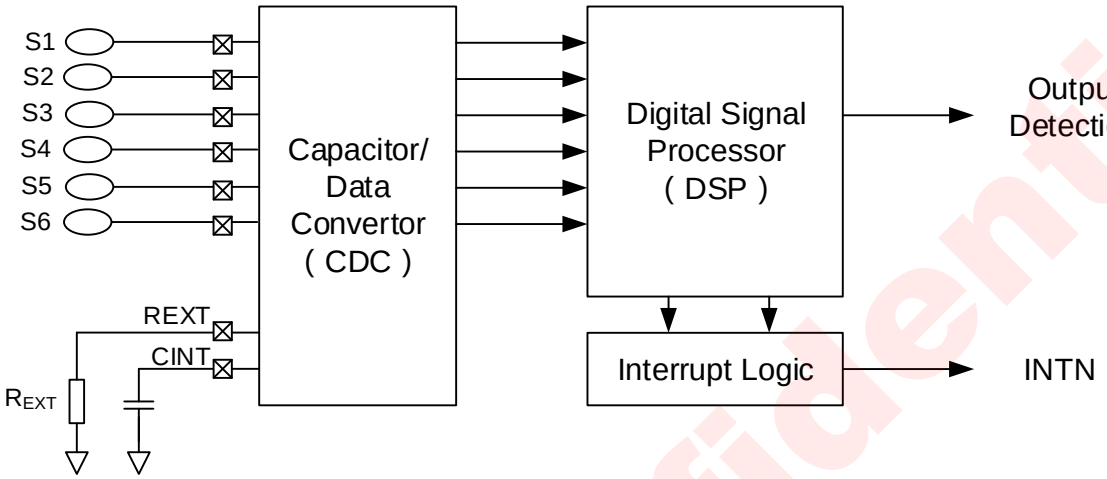


Figure 12 Functional Block of Capacitive Touch Detection

When control bit SENE in register GCR is 0, all capacitive touch detection circuit is reset. When control bit SENE is set, the SLPR register control the enable/disable touch detection. If control bits SLPx (x=1,2,..,6) in register SLPR is 0, touch detection on pin Sx is activated. If control bits SLPx is set to 1, touch pin Sx is disabled to save power consumption.

Touch Status

In AW9069, the raw touch detection result of pin S1~S6 can be read via register RAWST (address 0x31).

Adjacent key suppression

Usually when a touch key is designed small and very close to the adjacent key, it is very possible that one finger touch trigger not only the intend key, but the surrounding keys also. The AW9069 supports the so-called adjacent suppression (AKS) function.

The register AKSCR(address 0x07) defines the AKS group, select which keys are included for AKS recognition. When more than one key in AKS group are triggered at the same time, the AKS algorithm identify the only most likely key in AKS group, and output the detect result with AKS function in register KEYST (address 0x32).

Touch Interrupt

Touching status can generate the interrupt output on pin INTN, the interrupt enable control is defined by register KINTER (address 0x03). There are 4 interrupt mode selections defined by control bits KIMD[1:0] in register KINTER to select interrupt triggered by different event.

- KIMD[1:0] =00 interrupt triggered when touch status changed
- KIMD[1:0] =01 interrupt triggered when touch status changed from 1 to 0 (key released)
- KIMD[1:0] =10 interrupt triggered when touch status changed from 0 to 1 (key touched)
- KIMD[1:0] =11 interrupt triggered when touch status is 1 (touch active)

The INTN pin is driven in Open-drain mode, and usually connected to VIO via pull-up resistor.

When interrupt is active, the corresponding bit in interrupt status register KISR (0x30) will be set, and if the corresponding enable bit in register KINTER (address 0x03) is “1”, the pin INTN is pulled down to GND to inform interrupt to the external MCU. Once the interrupt status register KISR is read via I^2C interface, it will be cleared, then the pin INTN will be released and pulled up to V_{IO} by external resistor.

Gesture Detection

Besides for touch detection, AW9069 provides gesture detection function, such as slide and click (single, double and triple click), which is implemented automatically by internal gesture recognition module. Once one gesture is detected, the corresponding bit in gesture interrupt status register GISR (address 0x2E) will be set. The enable bit in gesture interrupt enable register GIER (address 0x2D) defines whether gesture event output to pin INTN.

Slip gesture

The slider is consisted of several sense electrodes (keys). When finger touching slips over the slider, touched state will be detected one by one in certain sequence. The gesture detection module identifies the gesture based on the comparing of occurring order of touch detected with the predefined sequence in register GSTRx,.

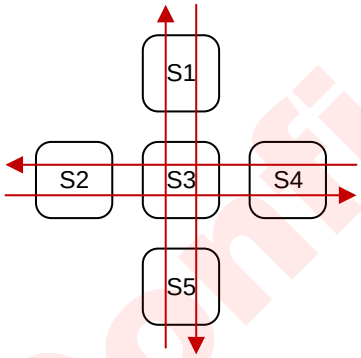


Figure 13 An Example of Slide Gesture

The figure above gives a general touch key application supporting slide gesture. The left-slide and right-slide are defined as slip along keys S4-S3-S2 and along keys S2-S3-S4 respectively. The down-slide and up-slide gesture are defined as touch along keys S1-S3-S5 and along keys S5-S3-S1 respectively.

Tap gesture

Tap gesture means that finger click the touchpad quickly. there are 3 types of tap can be recognized by AW9069: single click, double click and triple click, and usually the single click and double click are adapted mostly. The continuously, fast finger clicks on touch sensor will make the touch detection status switching between ON and OFF state quickly. By analyzing the touch status and timing of ON/OFF transition, pre-defined tap gesture can be detected.

Gesture configuration

The registers GDCR (address 0x20) , GDTR(address 0x21),TDTR(address 0x22) defines the basic configuration of gesture detection, such as the sensor selection for tap gesture, the max OFF time during slide detection, the max ON and OFF time during tap detection, and so on. The bit7 (GSTMD) of register GDCR set the time to report gesture detected. If GSTMD=0, gesture detected status is set when finger has left the touch pad completely. If GSTMD=1, gesture status is set as soon as the predefined sequence of touch event is checked.

The register GSSR1~4 (address 0x23~0x26) configure 4 user-defined slide gestures.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	KCODE1			0	KCODE2			0	KCODE3			0	KCODE4		

KCODE1~4 is the encoding of pin Sx (x=1~6), which is defined as “000” for pin S1, “001” for pin S2, …, “110” for S6. If KCODEx=”000”, no touch pin is selected.

The touch sequence of current slide gesture is always defined as : KCODE1 – KCODE2-KCODE3 – KCODE4. In AW9069, any slide gesture needs more than 3 touch input involved. If the slider only contains only 3 inputs, KCODE1~3 must be set, and KCODE4 must be set as “000”.

Register TAPR(address 0x27) defines the click gesture.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	CSEL						TIMES	

Bits TIMES[1:0] selects different mode of click gesture. If TIMES =“01”, single click mode is enabled; if TIMES=“10”, double click mode is enabled; if TIMES=“11”, triple click is enabled.

Bits CEL[5:0] select the touch inputs relevant to click gesture, if CSEL[x]=1, pin Sx is selected for click gesture detection. If more than one touch input are set, all input will be looked as one key to detect gesture.

By default, 4 slide and 1 double-click have been defined in relevant registers, which is shown in the table below.

Register Name	Default Value	Input Selection	Gesture Defined
GSSR1	2340h	S2-S3-S4	Slip to Right Side
GSSR2	4320h	S4-S3-S2	Slip to Left Side
GSSR3	1350h	S1-S3-S5	Slip to upper Side
GSSR4	5310h	S5-S3-S1	Slip to bottom Side
TAPR1	0012h	S3	Double clock on S3

Gesture Interrupt

The result of gesture detection can be read in interrupt status register GISR (address 0x2E). If the an pre-defined gesture is detected, the bit GISx or TISx in register GISR will be set. The register GIER(address 0x2D) is interrupt enable register of gesture detection.

If a gesture is detected and the corresponding interrupt is enable, interrupt will occur to pull down INTN pin. After a reading of register via I^2C interface, the interrupt would be removed, pin INTN be released and then pulled high, the register GISR be cleared to “0x0000”.

LED DRIVER

In AW9069, 9 LED is driven by independent constant current sinks to drive LEDs. A dedicated Application-Specific-Processor (ASP)is designed to produce versatile lighting effect for different application.

If the control bit GCR.LEDE is 0 , LED driver circuit is in reset state, all 9 LED outputs are disabled. If control bit LEDE in register GCR is set to “1”, the LED driver circuit is enabled, the control bits LENx (x=1 to 9) in register LER configure the corresponding LED channel is active or not.

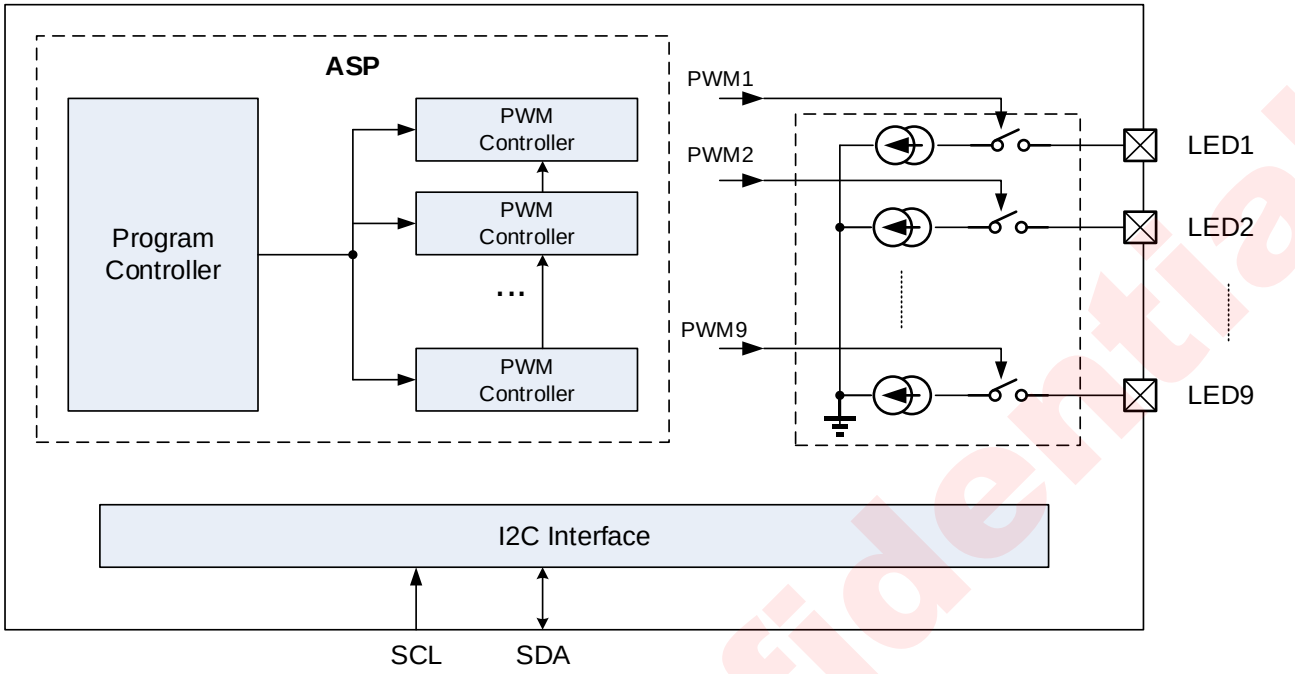


Figure 14 AW9069 LED Dimming Control Module Diagram

LED brightness controller

In AW9069, Pulse Width Modulation (PWM) is used to adjust the brightness of LED. The PWM is 8-bit /256-step programmable with 12-bit resolution. And the frequency of PWM could be configured between 125Hz or 250Hz by control bit FREQ in register LCR (address 0x52).

The ASP execute the user-preloaded program in a 256word x 16bit SRAM, and control the PWM level of all LEDs to produce complicated LED lighting effect.

With the setting of register CGRS (address 0x55), each LED controller can be selected to be controlled by SRAM program or by I^2C directly.

- CTRS[n] = 0, LEDn controller is controlled by the internal SRAM instruction;
- CTRS[n] = 1, LEDn controller is controlled by the external I^2C instruction.

LED Constant current driver

For each LED, the output DC current is set by register IMAX (address 0x57~0x59), there are 8-step of current options, and the max current is 24.5mA. The constant current output of each LED driver is regulated by PWM level from ASP for dimming adjustment.

The register LER (address 0x50) controls individual LED to be work or not. If bit LEx is set to “1”, the corresponding LEDx output is enabled. If bit LEx is “0”, the pin LEDx output is disabled.

ASP

In AW9069, the ASP is consisted of one program controller and 9 PWM controllers.

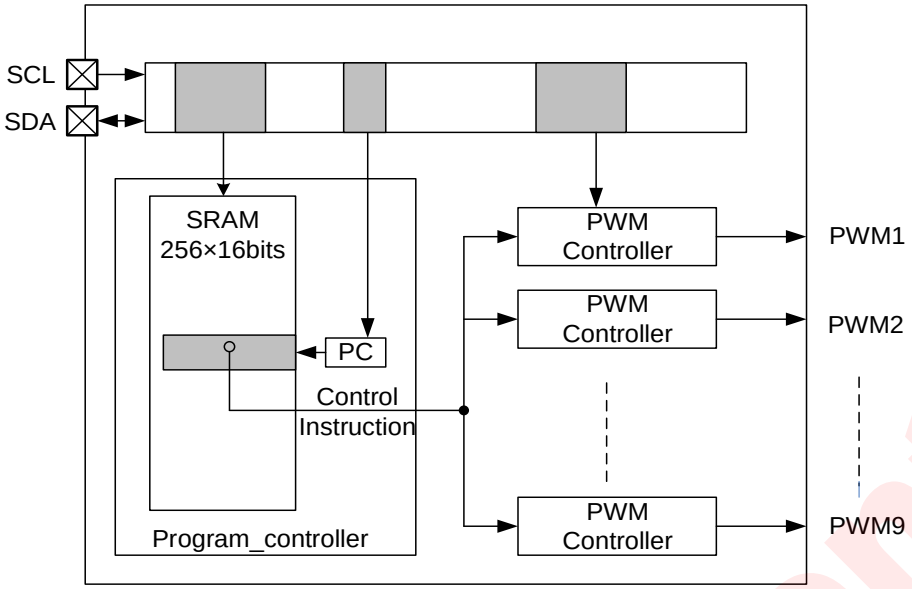


Figure 15 ASP Structure Diagram

Program Controller

The program controller is clocked by 32kHz internal clock, each instruction is executed in one clock cycle.

The program controller contains a program SRAM, an algorithmic logic unit (ALU) , timer and other internal registers. The 256x16bit internal SRAM is used to store LED lighting effect program loaded through I^2C interface, the I^2C interface also can start or stop the program execution.

There are 4 internal registers RA/RB/RC/RD participating ALU operation so as to generate complicated program control, such as repeating and looping. Except for that, there are 8 8-bit temporary data registers(R1~R8) and 5 special function registers. Their internal address and function description is shown in the table below.

Table 1 ASP Internal Data Registers List

Register	Address(HEX)	Illustration
R1	00	R1 data temporary register, 8bit, I^2C readable
R2	01	R2 data temporary register, 8bit, I^2C readable
R3	02	R3 data temporary register, 8bit, I^2C readable
R4	03	R4 data temporary register, 8bit, I^2C readable
R5	04	R5 data temporary register, 8bit, I^2C readable
R6	05	R6 data temporary register, 8bit, I^2C readable
R7	06	R7 data temporary register, 8bit, I^2C readable
R8	07	R8 data temporary register, 8bit, I^2C readable
AKST	08	Touch status with AKS
KST	09	Raw touch status
TISR1	0a	Key interrupt status register, clear after reading
TISR2	0b	Key interrupt status register, clear after reading
-	0c	reserved
GMSK1	0d	Global control mask register(M8~M1)
GMSK2	0e	Global control mask register(M9)

Table 2 Particular registers detail illustration

Register	B7	B6	B5	B4	B3	B2	B1	B0	Illustration

KST	-	-	K6	K5	K4	K3	K2	K1	Touch status, Kx=1 means Sx is touched.
KST_AKS	-	-	AST6	AST5	AST4	AST3	AST2	AST1	AKS touch status, ASTx=1 means that Sx is touched.
TISR1	-	-	KINT6	KINT5	KINT4	KINT3	KINT2	KINT1	Touch interrupt status. Cleared by ASP reading.
TISR2	-	-	-	TAP	G4	G3	G2	G1	Gesture interrupt status. Cleared by ASP reading.
GMSK1	M8	M7	M6	M5	M4	M3	M2	M1	Mask control for global control instruction. When Mn=1, LEDn will not be affected by global control instruction.
GMSK2	-	-	-	-	-	-	-	M9	

PWM Controller

The PWM controller is execution unit of LED control instruction. There are 9 PWM controllers receiving the LED effect instruction from SRAM, and generate 8bit PWM code, which will be convert to 12bit duty cycle control code by logarithmic l transformation. If bits LOGLN[1:0] of register LCR is “00”, the transformation is natural logarithm($\log_e$). If LOGLN[1:0] is “01”, the transformation is logarithm of 10 ($\log_{10}$), otherwise the 8b-to-12b transformation of PWM code is linear..

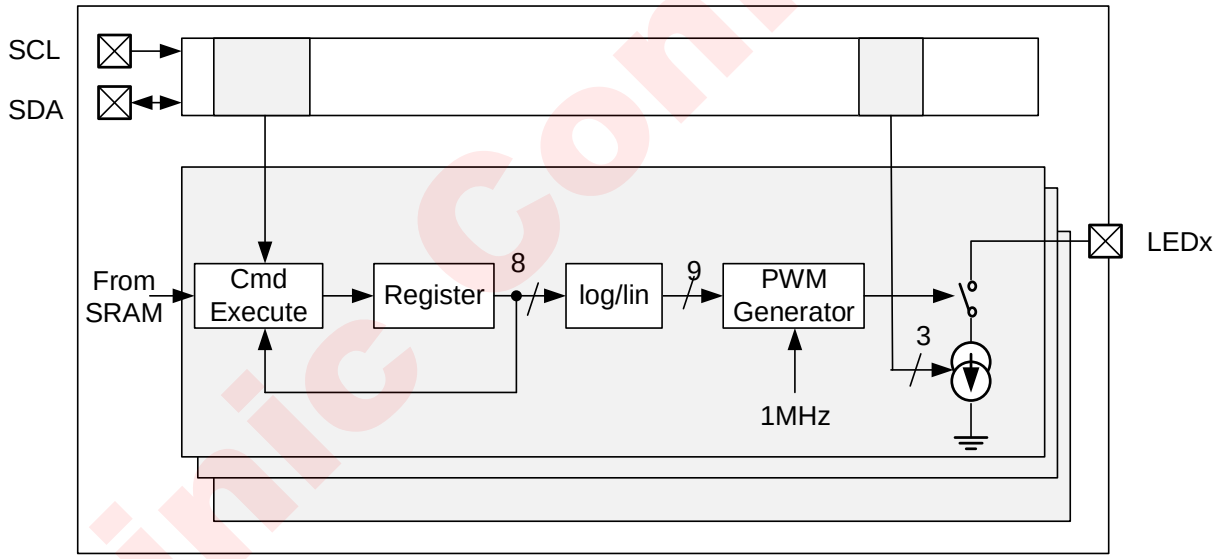


Figure 16 PWM Controller

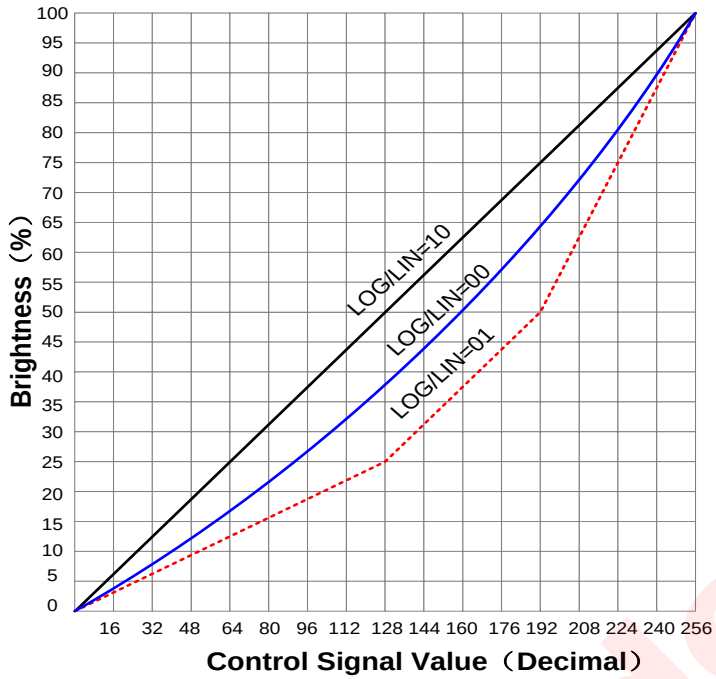


Figure 17 PWM Dimming Curve

Program Loading and execution

a) Program loading

It is recommended to load SRAM program only when control bits PROGMD[1:0] of register PMD is “00”. In this state, the internal program can be read/write through I^2C interface. When loading program, please write the SRAM loading address in register WADDR(address 0x7E) at first, and then write the 16bit LED effect instruction to register WDATA(address 0x7F). Continuously loading program is supported, after a 16b instruction is written through register WDATA, the value of WADDR will automatically plus by 1.

b) Program execution

Register bits PROGMD[1:0] in register PMD controls the loading and execution mode of SRAM program.

When PROGMD[1:0]= “00”, program execution is shut down, SRAM program and program pointer(PC) are permitted to be loaded.

When PROGMD[1:0] is written to be “01” from another value, current program will stop , and PC will be reload by register SADDR, and then executes the SRAM program starting from the address of PC

When PROGMD[1:0] =“10”, the SRAM program will be executed by the mode defined by register bit RMD.RUNMD[1:0]

Table 3 Program running mode control register

RMD.RUNMD	Function Description
0 0	Hold mode. program stop and PC hold after one instruction is finished.
0 1	Single step mode, only used for debugging. Once writing 01 to bits RUNMD[1:0] in register RMD, only one instruction will be executed with PC+1, and then RUMND is cleared (return to hold mode)
1 0	Continuously running mode, program starts from the address of PC.
1 1	Repeating mode, only used for debugging. Once writing 11 to RUNMD, current instruction will be executed without PC+1, and then RUMND is cleared (return to hold mode)

SRAM program instructions

There are 27 commands in ASP instruction set, including LED control command, data operation and transfer command, wait and branch control command. The Rx, Ry and Rz in instruction list means the internal register RA, RB, RC and RD, each of them can participate the ALU operation as source or destination register.

Table 4 LED Effect Instruction

Command	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JP	0	0	0	0	0	0	0	0	ADDR[7:0]							
NOP	0	0	0	0	0	0	0	1	-	-	-	-	-	-	-	-
JPZ Addr	0	0	0	0	0	1	0	0	ADDR[7:0]							
JPNZ Addr	0	0	0	0	0	1	0	1	ADDR[7:0]							
JPS Addr	0	0	0	0	0	1	1	0	ADDR[7:0]							
JPNS Addr	0	0	0	0	0	1	1	1	ADDR[7:0]							
LD Rz Im	0	0	0	0	1	0	Rz		Im[7:0]							
CMPI Rz Im	0	0	0	0	1	1	Rz		Im[7:0]							
ANDR Rz Im	0	0	0	1	0	0	Rz		Im[7:0]							
ORR Rz Im	0	0	0	1	0	1	Rz		Im[7:0]							
RDR Rz Addr	0	0	0	1	1	0	Rz		ADDR[7:0]							
WDR Rz Addr	0	0	0	1	1	1	Rz		ADDR[7:0]							
ADDI Rz Im	0	0	1	0	0	0	Rz		Im[7:0]							
AUBI Rz Im	0	0	1	0	0	1	Rz		Im[7:0]							
ADDR Rx Ry	0	0	1	0	1	0	Rz		-	-	-	-	Rx		Ry	
SUBR Rx Ry	0	0	1	0	1	1	Rz		-	-	-	-	Rx		Ry	
CMPR Rx Ry	0	0	1	1	0	0	0	0	-	-	-	-	Rx		Ry	
END Int Rst	0	0	1	1	0	1	0	0	-	-	-	-	-	-	Int	Rst
INTN_MASKOFF	0	0	1	1	0	1	1	0	-	-	-	-	-	-	-	-
INTN_MASKON	0	0	1	1	0	1	1	1	-	-	-	-	-	-	-	-
WAITI Pre Time	0	0	1	1	1	Pre	T[9:0]									
SETPWMR Rx Ry	0	1	0	0	0	0	0	-	-	0	0	0	Rx		Ry	
RAMPR Dir Rx Ry	0	1	0	0	0	0	1	Dir	-	0	0	0	Rx		Ry	
SETSTEPTMRR Pre Rx Ry	0	1	0	0	0	1	0	-	Pre	0	0	0	Rx		Ry	
SETSTEPTMRI Pre Ch Im	1	0	0	Ch[4:0]					Pre	-	Im[5:0]					
SETPWMI Ch Im	1	0	1	Ch[4:0]					Im[7:0]							
RAMPI Dir Ch Im	1	1	Dir	Ch[4:0]					Im[7:0]							

a) Special LED Control Command

There are 3 kinds of LED control command.

- **SETPWM:** set the brightness level (0~255)for specified LED channel;
- **RAMP:** set the specified LED channel fade in or fade out for expected step(0~255)
- **SETSTEP:** set the fading slope for specified LED channel;

All control parameter in above commands can either come from specified register (RA~RD), or from immediate data contained in command..

All LED control command supports broadcast mode, one instruction may send to multiple or all LEDs

When SRAM program running, if Ch field or value of Rx in LED control command is “11111”, the current command is active for all LED with setting of CTRSR.bitn=0. If Ch field or value of Rx in LED control command is “11110”, the current command is only active for those channel with setting of GMSKx=0.

When LED instruction is come from I^2C interface directly, it is recommended to use only the command with immediate data. If the Ch field in command is “11111”, the current command is only active for those LED with STRSR.bitn=1..

Table 5 LED Control Instruction explanation

Instruction	Description
Register Parameter	
SETPWMR Rx Ry	**Set the PWM brightness level with parameter in register** Rx: LED channel number, 0~8 for LED1~ LED9 respectively Ry: Brightness level, 0~255
RAMPR Dir Rx Ry	**Set the Fade-in/Fade-out for specified step with parameter in register** Dir: 1: Fade-in; 0: Fade-out Rx: LED channel number, 0~8 for LED1~ LED9 respectively Ry: the step number of Fade-in/Fade-out
SETSTEPTMRR Pre Rx Ry	**Set the RAMP slope with parameter in register** Pre: basic time unit, 0: 0.5ms; 1: 16ms Rx: LED channel number, 0~8 for LED1~ LED9 respectively Ry: RAMP step time = (Ry+1)*Pre, 0~255
Immediate Data	
SETPWMI Ch Im	**Set the PWM brightness level with immediate parameter** Ch: LED channel number, 0~8 for LED1~ LED9 respectively Im: Brightness level, 0~255
RAMPI Dir Ch Im	**Set the Fade-in/Fade-out for specified steps with immediate parameter** Dir: 1: Fade-in; 0: Fade-out Ch: LED channel number, 0~8 for LED1~ LED9 respectively Im: the steps of Fade-in/Fade-out
SETSTEPTMRI Pre Ch Im	**Set the RAMP step time with immediate parameter** Pre: basic unit of time, 0: 0.5ms; 1: 16ms Ch: LED channel number, 0~8 for LED1~ LED9 respectively Im: RAMP step time = (Im +1)*Pre, 0~255

Table 6 Program Control and operation Instruction

Instruction	Encoding	Description
branch Instruction		
JP Addr	0x00xx	Immediate Jump, jump to PC = Addr
JPZ Addr	0x04xx	Conditional Jump, If Rz is 0, jump to PC = Addr
JPNZ Addr	0x05xx	Conditional Jump, If Rz is not 0, jump to PC = Addr
JPS Addr	0x06xx	Conditional Jump, If Rz < 0, jump to PC = Addr
JPNS Addr	0x07xx	Conditional Jump, If Rz >= 0, jump to PC = Addr
Data Transfer Instruction		
LD Rz Im	0x08xx - 0x0bxx	Rz = Im
RDR Rz Addr	0x18xx - 0x1bxx	Rz = *Addr
WDR Rz Addr	0x1cxx - 0x1fxx	*Addr = Rz
Computation Instruction		
CMPI Rz Im	0x0cxx - 0x0fxx	Rz – Im, only change S/Z flag
CMPR Rx Ry	0x30xx	Rx – Ry, only change S/Z flag
ANDR Rz Im	0x10xx - 0x13xx	Rz = Rz & Im, affect S/Z flag
ORR Rz Im	0x14xx - 0x17xx	Rz = Rz | Im, affect S/Z flag
ADDI Rz Im	0x20xx - 0x23xx	Rz = Rz + Im, affect S/Z flag
SUBI Rz Im	0x24xx - 0x27xx	Rz = Rz - Im, affect S/Z flag
ADDR Rz Rx Ry	0x28xx - 0x2bxx	Rz = Rz + Ry, affect S/Z flag
SUBR Rz Rx Ry	0x28xx - 0x2bxx	Rz = Rz - Ry, affect S/Z flag
Control Instruction		
END Int Rst	0x34xx	Program end with optionally reset register RMD and generate interrupt

		Int= 0: no interrupt after instruction executed; Int= 1: generate interrupt after instruction executed Rst=0: PC add 1 after instruction executed; Rst=1: Reload PC with SADDR after instruction executed
INTN_MASKOFF	0x36xx	Unmask internal interrupt
INTN_MASKON	0x37xx	Mask internal interrupt
WAITI Pre Time	0x38xx - 0x3fxx	Wait for specified time Pre: time of basic waiting cycle, 0: 0.5ms; 1: 16ms Time: number of waiting cycle, max value is 1023, wait time=Pre*Time

Example

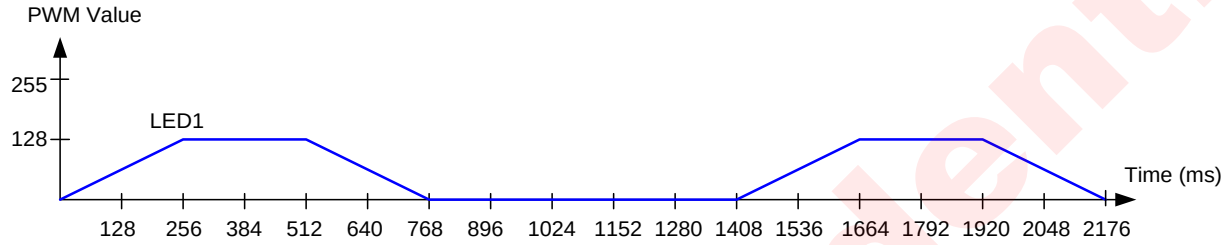


Figure 18 LED Effect Programming Diagram

Table 7 Reference Instruction of LED Effect Programming

PC	Assemble Instruction	Machine Code	explanation
0	SETSTEPTMRI 0x00 0x1F 0x03	0x9F03	RAMPI step time: 2ms
1	SETPWMI 0x1F 0x00	0xBF00	ALL LED turn off
	START:		Address Label “START” (01H)
2	RAMPI 0x01 0x00 0x80	0xE080	LED1 fade in, 128 steps breath
3	WAITI 0x01 0x20	0x3C20	Wait 512ms
4	RAMPI 0x00 0x00 0x80	0xC080	LED1 fade out, 128 steps breath
5	WAITI 0x01 0x38	0x3C38	Wait 896ms
6	JP START	0x0002	Jump to START, PC=2

Step1: Power On, configure register

- VBAT power on, 4.2V
- Pull pin PDN to 3V
- Wait 5ms
- Write register GCR = 0x0001 // enable LED module
- Writer register LER = 0x0001 // enable LED1
- Write register PMD=0x0000 // bits PROGRMD[1:0] = 00,hold mode
- Write register RMD=0x0000 // bits RUNMD[1:0] = 00,hold mode

Step2: Load Instruction to SRAM

- Write register WADDR= 0x0000 // load program starting at address =0x0000
- Write register WDATA = 0x9F03
- Write register WDATA = 0xBF00
- Write register WDATA = 0xE080
- Write register WDATA = 0x3C20
- Write register WDATA = 0xC080
- Write register WDATA = 0x3C38

- Write register WDATA = 0x0002

Step3: Run

- Write register SADDR = 0x0000
- Write register RMD=0x0002 // bits RUNMD[1:0] = 10,change to run mode,
- Write register PMD=0x0001 // bit PROGMD[1:0] = 01 ,start program from 0x0000

Link Touch Status to LED Lighting Effect

There are two optional ways to connect touch status to LED lighting effect inside the device: direct output mode and program mode .

In direct output mode, the touch detection status directly turn on or off the specified LED. In program mode, user can adapt internal touch and gesture interrupt to start LED lighting effect program to generate complex touch feedback.

Direct output mode

If bit OEx (x=1~6) in register OSRn (n=1~3) is 1, the touch status on pin Sx directly output to the LED defined by bits LSELx[3:0] in register OSRn. When touch detected, the LED turn on, when touch released, the LED turns off.

The control bit LSELx[3:0] of register OSRn defines which LED display the touch status of pin Sx:

LSELx[3:0]=0000, touch status sent to LED1
LSELx[3:0]=0001, touch status sent to LED2
…
LSELx[3:0]=1000, touch status sent to LED9

The control bit FONx, FOFx in register OSRn select the transition way between state on and off

FONx=1, turn on LED in smooth way (fade in) when Sx touch detected;
FONx=0, turn on LED immediately (without fade-in) when Sx touch detect;

FOFx=1, turn off LED in smooth way (fade out) when Sx touch released
FOFx=0, turn off LED immediately (without fade-out) when Sx touch released

When FOFx=1 or FONx=1, the speed of fade in/fade out is set by external MCU control command (SETSTEP) through I^2C interface.

Program link mode

Internal ASP can read several touch/gesture-related register to obtain the status of touch/gesture detection, such as register KST (Key Status), TISR1, TISR2 (Touch Interrupt status register). Once an event of touch or gesture is detected, program can jump to execute special subroutine to generate user-predefined lighting effect.

Besides invoking touch feedback lighting by polling the touch/gesture status, the touch feedback subroutine can be invoked by interrupt control mode. When touch and gesture are detected, the register bits KISx(x=1~6), GISy (y=1~2) and TAP in register TISR 1/TISR2 will be set; if corresponding interrupt enable bits KIEx, GIEy, and TIE in register TIER are set, internal interrupt mechanism is triggered. After interrupt occurs, ASP's PC pointer jumps to the beginning address defined by register TIVEC at once to execute interrupt subroutine.

Generally interrupt subroutine would read registers TISR1/TISR2 first to resolve the interrupt source, and then to execute the corresponding touch-related lighting program. After register TISR1/TISR2 read out, they will be cleared automatically.

The register TIER (Touch Interrupt Enable) contains 3 types of interrupt enable bits: KIE, GIE and TIE. The KIEx is the touch status interrupt, which has 4 types operating mode configured by bits INMD[1:0] in register

LCR. The GIEy are the slide gesture interrupt enable bits, and TIE is the tap gesture interrupt enable bit. All interrupts have the same priority.

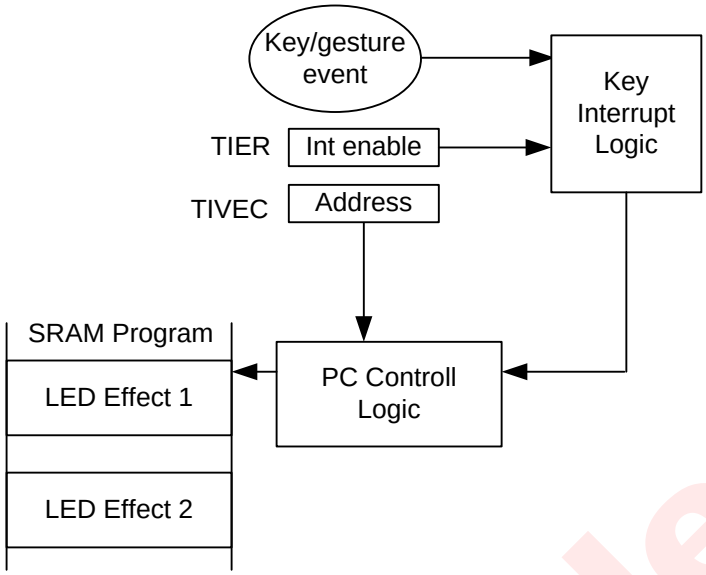


Figure 19 Touch/Gesture Event triggers LED Program Interrupt

REGISTER DESCRIPTION

REGISTER CONFIGURATION

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	IDRST	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x01	GCR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SENE	LEDE
0x02	SLPR	0	0	0	0	0	0	0	0	0	0	SLP6	SLP5	SLP4	SLP3	SLP2	SLP1
0x03	KINTER	0	0	0	0	0	0	KIMD		FRME	0	IE6	IE5	IE4	IE3	IE2	IE1
0x04	OSR1	OE2	FON2	FOF2	0	LSEL2				OE1	FON1	FOF1	0	LSEL1			
0x05	OSR2	OE4	FON4	FOF4	0	LSEL4				OE3	FON3	FOF3	0	LSEL3			
0x06	OSR3	OE6	FON6	FOF6	0	LSEL6				OE5	FON5	FOF5	0	LSEL5			
0x07	AKSCR	0										ASEL					
0x08	SLSR	0	0	SLID_INTV						RME	0	SLIDSEL					
0x0A~0x0F	JDGTH1~3	CLRTH								SETTH							
0x10	NOISETH	0	0	0	0	1	0	0	0	NOISTH							
0x11	SCFG1	0	0	0	0	0	0	0	0	SCMD	0	NSMD	SCNUM				
0x12	SCFG2	0	0	0	0	0	SEED			RFFLTEN		0	SENS				
0x13	OFSR1	0	0	0	EN2	OFFSET2				0	0	0	EN1	OFFSET1			
0x14	OFSR2	0	0	0	EN4	OFFSET4				0	0	0	EN3	OFFSET3			
0x15	OFSR3	0	0	0	EN6	OFFSET6				0	0	0	EN5	OFFSET5			
0x16	DOFCR1	DOF4				DOF3				DOF2				DOF1			
0x17	DOFCR2	0	0	0	0	0	0	0	0	DOF6				DOF5			
0x18	IDLECR	INCR[7:0]								0	IPER[6:0]						
0x19	MOTR	0								MOT							
0x1A	DISMAX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x1B	SETCNT	CCNT								SCNT							
0x1C	BLCTH	BLU								BLD							
0x1D	BLDTH	0	0	0	0	0	0	0	0	BLDTH							
0x1E	MDSR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSEL	
0x20	GDCR	0	0	0	0	0	0	GSTMD		AKST	AKSG	S6	S5	S4	S3	S2	S1
0x21	GDTR	0	0	0	0	0	0	0	0	GOFFMAX							
0x22	TDTR	ONMAX								TOFFMAX							
0x23	GSSR1	0	KCODE1			0	KCODE2			0	KCODE3			0	KCODE4		
0x24	GSSR2	0	KCODE1			0	KCODE2			0	KCODE3			0	KCODE4		
0x25	GSSR3	0	KCODE1			0	KCODE2			0	KCODE3			0	KCODE4		
0x26	GSSR4	0	KCODE1			0	KCODE2			0	KCODE3			0	KCODE4		
0x27	TAPR	0	0	0	0	0	0	0	0	K6	K5	K4	K3	K2	K1	TIMES	
0x2D	GIE	0	0	0	0	0	0	0	0	0	0	0	TIE1	GIE4	GIE3	GIE2	GIE1
0x2E	GIS	0	0	0	0	0	0	0	0	0	0	0	TIS1	GIS4	GIS3	GIS2	GIS1
0x2F	GTIM	0	0	0	0	0	0	0	0	GESTTIMER							
0x30	KISR	0	0	0	0	0	0	0	IDST	0	-	INT6	INT5	INT4	INT3	INT2	INT1
0x31	RAWST	0	0	0	0	0	0	0	0	0	0	S6	S5	S4	S3	S2	S1
0x32	KEYST	0	0	0	0	0	0	0	0	SBI	0	S6	S5	S4	S3	S2	S1
0x35	SMOVCNT	0	0	0	0	0	0	0	0	MOVCNT							
0x36~0x3B	KDATA1~6	KDATA															
0x3C	DUM0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
0x3D	DUM1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	LER	0	0	0	0	0	0	0	LE9	LE8	LE7	LE6	LE5	LE4	LE3	LE2	LE1
0x51	-	Reserved															
0x52	LCR	0	0	0	0	0	0	0	SRMINI	LIRMD		TIMD		LIE	FREQ	LOG/LIN	
0x53	PMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROGMD	
0x54	RMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNMOD	
0x55	CTRS	0	0	0	0	0	0	0	CTRSEL								
0x57	IMAX1	0	IMAX4			0	IMAX3			0	IMAX2			0	IMAX1		
0x58	IMAX2	0	IMAX8				IMAX7			0	IMAX6			0	IMAX5		
0x59	IMAX3	0	0	0	0	0	0	0	0	0	0	0	0	0	IMAX9		
0x5C	TIER	0	0	0	0	0	TIE1	0	0	GIE2	GIE1	KIE6	KIE5	KIE4	KIE3	KIE2	KIE1

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x5D	TIVEC	0	0	0	0	0	0	0	0	TIVEC							
0x5E	ISR2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIS
0x5F	SADDR	0	0	0	0	0	0	0	0	SADDR							
0x60	PCR	0	0	0	0	0	0	0	0	PC							
0x61	CMDR	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x62	RA	0	0	0	0	0	0	0	0	RA							
0x63	RB	0	0	0	0	0	0	0	0	RB							
0x64	RC	0	0	0	0	0	0	0	0	RC							
0x65	RD	0	0	0	0	0	0	0	0	RD							
0x66~0x6D	R1~R8	0	0	0	0	0	0	0	0	R1~R8							
6E	GRP	0	0	0	0	0	0	0	GRPSEL								
7D	WP	WPW								0	0	0	0	0	0	0	0
7E	WADDR	0	0	0	0	0	0	0	0	ADDR							
7F	WDATA	CODE															

GLOBAL REGISTER DESCRIPTION

IDRST, Chip ID and Software Reset

Address: 0x00, R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit	Symbol		Description												
15:0	IDRST		Chip ID and software reset control. Read-out is always 0xA223 as chip ID. Write 0x55aa to this address will reset the whole chip, including all configuration register												

GCR, Global Control Register

Address: 0x01, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SENE	LEDE
Bit	Symbol		Description												
0	LEDE		LED driver function enable 0: disable LED driver 1: enable LED driver												
1	SENE		Capacitive touch detection function enable 0: disable capacitive touch detection 1: enable capacitive touch detection												

CAPACITIVE TOUCH DETECTION REGISTERS

SLPR, Sensor Channel Sleep Control Register

Address: 0x02, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	SLP6	SLP5	SLP4	SLP3	SLP2	SLP1
Bit	Symbol		Description												
5:0	SLP6 ~ SLP1		Channel sleep control for pin Sx (x=1~6) 0: pin Sx input detection is enabled 1: pin Sx input detection is shut down												

KINTER, Touch Key Interrupt Enable Register

Address: 0x03, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	KIMD		FRME	0	IE6	IE5	IE4	IE3	IE2	IE1
Bit	Symbol		Description												
5:0	IEx		Touch Key Interrupt enable. If interrupt occurs, pin INTN is pulled down to GND in												

		open-drain mode.. 0: disable interrupt 1: enable interrupt
6	-	Reserved, must be 0
7	FRME	Interrupt enable for frame boundary for touch scan sampling. External MCU can use this interrupt to obtain the latest CDC sampling data. 0: disable scan frame interrupt 1: enable scan frame interrupt
9:8	KIMD	Interrupt trigger mode selection. 00: interrupt triggered when touch status change 01: interrupt triggered when touch status changes from 1 to 0 10: interrupt triggered when touch status changes from 0 to 1 11: interrupt triggered when touch status is 1

OSR1~3, Output Touch Status to LED Register

Address: 0x04~0x06, R/W, default: 0x0000																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OE2	FON2	FOF2	0	SEL2				OE1	FON1	FOF1	0	LSEL1				
OE4	FON4	FOF4	0	LSEL4				OE3	FON3	FOF3	0	LSEL3				
OE6	FON6	FOF6	0	LSEL6				OE5	FON5	FOF5	0	LSEL5				
Bit	Symbol		Description													
15/7	OEx		Enable Capacitive input status of Sx(x=1~ 6) output to LED 0: disable association 1: enable association													
14/6	FONx		LED fade in mode enable for Touch/LED association 0: LED turn on immediately 1: LED turn on smoothly													
13/5	FOFx		LED fade-out mode enable for Touch/LED accociation 0: LED turn off immediately 1: LED turn off smoothly													
11:8/ 3:0	LSELx		Output LED selection for Sx. Multiple keys binding to the same LED is permitted. LSEL is the internal code of pin LEDy (y=1~9). 0000: output to LED1 0001: output to LED2 … 1000: output to LED9													
12:11/4:3	-		Reserved, must be 0													

AKSCR, Adjacent Key Suppression Configuration Register

Address: 0x07, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	ASEL					
Bit	Symbol		Description												
5:0	ASEL		Adjacent Key Group selection. In the application that multiple touch keys are placed very close to each other, and only one key is active for one touch, AKS algorithm helps to identify the most likely key among all the touched keys. ASELx=1, Sx is included in AKS groups ASELx=0, Sx is not included in AKS groups The touch detection result without AKS algorithm outputs to register RAWST, and the touch detection result with AKS outputs to register KEYST.												

SLSR, Slide Selection Register

Address: 0x08, R/W, default: 0x0200															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SLID_INTV						RME	0	SLIDSEL					
Bit	Symbol		Description												
5:0	SLIDSEL		Slide Bar Configuration, defines which Sx that the slide bar is consisted of. 0: pin Sx is not contained in slide bar 1: pin Sx is contained in slide bar												

6	-	Reserved, must be 0
7	RME	Slider Ring Mode Enable. 0: Slider is in shape of bar 1: Slider is in shape of ring
13:8	SLID_INTV	Slider Detection Timing Setting. Used in the case that the margin between two adjacent key in a slide bar is bigger than normal. T=SLIDINTVAL*Tscan

JDGTHn, key status judge configuration register

Address: 0x0A~0x0F, R/W, default: 0x080F															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRTH								SETTH							

Bit	Symbol	Description
7:0	SETTH	Touch-on decision threshold
15:8	CLRTH	Touch-off decision threshold

NOISETH, Noise Threshold Register

Address: 0x10, R/W, default: 0x080F															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x08								NOISETH							

Bit	Symbol	Description
7:0	NOISETH	Noise threshold Setting.
15:8	-	Reserved

SCFG1, Scan Configuration Register 1

Address: 0x11, R/W, default: 0x0004															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0		0		0		SCNMD	0	NSMD	SCNUM				

Bit	Symbol	Description
4:0	SCNUM	Scan Cycle Number Setting, default is 4. The bigger is the scan cycle number selected, the longer is the scan time, and the higher is the sensitivity of CDC. 00000: Scan cycle is 256, Others: Scan cycle is SCNUM*512
5	NSMD	Not Scanned Channel Status Setting. 0: connected to GND (default) 1: High-Z
6	-	Reserved, must be 0
7	SCNMD	Scan Mode Selection 0: scan all 6 keys, the cycle time is constant 1: scan the selected keys
15:8	-	Reserved, must be 0

SCFG2, Scan Configuration Register 2

Address: 0x12, R/W, default: 0x0107															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	SEED			RFFLTEN		0		SENS			

Bit	Symbol	Description
3:0	SENS	Sensitivity configuration, the litter SENS, the higher sensitivity (16 level sensitivity) 0000: highest sensitivity 0001: 1/2 highest sensitivity 0011: 1/4 the highest sensitivity 0111: 1/8 the highest sensitivity (default) 1111: 1/16 the highest sensitivity
5:4	-	Reserved, must be 0
7:6	RFFLTEN	RF filter enable, only used when register SCFG1's bit SCNUM is >4. 00/11: RF filter off 01: RF filter mode 1 10: RF filter mode 2 (strongest) Notice: when RF filter is enable, the Sx sampling is divided into several segment, the

		abnormal segment samples are discarded
10:8	SEED	CDC output accuracy selection 000: CDC/16 001: CDC/8 010: CDC/4 011: CDC/2 100: CDC/1

OFSR1, Key Capacitance Offset Register 1

Address: 0x13, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OFSEN2	OFFSET2				0	0	0	OFSEN1	OFFSET1			

Bit	Symbol	Description
3:0	OFFSET1	S1 capacitance offset selection. The bigger of OFFSET1, the larger the compensation capacitance on S1.
4	OFSEN1	S1 capacitance offset enable
7:5	-	Reserved, must be 0
11:8	OFFSET2	S2 capacitance offset value. The bigger of OFFSET2, the larger the compensation capacitance on S2.
12	OFSEN2	S2 capacitance offset enable
15:13	-	Reserved, must be 0

OFSR2, Key Capacitance Offset Register

Address: 0x14, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OFFSEN4	OFFSET4				0	0	0	OFSEN3	OFFSET3			

Bit	Symbol	Description
3:0	OFFSET3	S3 capacitance offset value. The bigger of OFFSET3, the larger the compensation capacitance on S3.
4	OFSEN3	S3 capacitance offset enable
7:5	-	Reserved, must be 0
11:8	OFFSET4	S4 capacitance offset value. The bigger of OFFSET4, the larger the compensation capacitance on S4.
12	OFSEN4	S4 capacitance offset enable
15:13	-	Reserved, must be 0

OFSR3, Key Capacitance Offset Register

Address: 0x14, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OFSEN6	OFFSET6				0	0	0	OFSEN5	OFFSET5			

Bit	Symbol	Description
3:0	OFFSET5	S5 capacitance offset value. The bigger of OFFSET5, the larger the compensation capacitance on S5.
4	OFSEN5	S5 capacitance offset enable
7:5	-	Reserved, must be 0
11:8	OFFSET6	S6 capacitance offset value. The bigger of OFFSET6, the larger the compensation capacitance on S6.
12	OFSEN6	S6 capacitance offset enable
15:13	-	Reserved, must be 0

DOFCR1-2, CDC Digital Offset Register

Address: 0x16-0x17, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DOF4				DOF3				DOF2				DOF1			
-								DOF6				DOF5			

Bit	Symbol	Description
15:0	DOF6 DOF5 DOF4 DOF3 DOF2 DOF1	DOFx: CDC digital offset of Sx CDC data will over 12 bits when key parasitic capacitance is too big. The digital offset can make the CDC data within acceptable range by minus the setting offset. 0000 : offset is 0 0001: offset is 2000 0010: offset is 4000 0011: offset is 6000 0100: offset is 8000 0101: offset is 10000 0110: offset is 12000 0111: offset is 14000 Others: undefined

IDLECR, IDLE Status Configuration Register

Address: 0x18, R/W, default: 0x1805															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INCR								0	IPER						

Bit	Symbol	Description
6:0	IPER	Scan Period Setting in IDLE mode. In idle mode, the scan rate is reduced to 1/(IPER+1) times of normal scan rate to save power consumption. By default, IPER is 5.
7	-	Reserved, must be 0
15:8	INCR	IDLE Entering Time Setting. If touch has not detected on all sensors for more than INCR*TSCAN*16, the scan enters IDLE mode for power consumption.

MOTR, Maximum Touch-On Time Register

Address: 0x19, R/W, default:0x0010															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								MOT							

Bit	Symbol	Description
7:0	MOT	Maximum Permitted Touch-On Time 0x00: No max touch-on time limition Other: time of touch-on is limited to MOT*TSCAN*128. TSCAN : capacitance touch key scanning cycle, TSCAN = N * SCNUM * 2us (here N is number of toch keys)
15:8	-	Reserved, must be 0

DISMAX, Maximum Margin of Valid Data Register

Address: 0x1A, R/W, default: 0x0040															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISMAX															

Bit	Symbol	Description
15:0	DISMAX	Maximum margin of valid data When the absolute difference between new raw data and the previous one is bigger than DISMAX, discard the raw data. The default value is 64.

SETCNT, Touch Judge De-bounce Counter

Address: 0x1B, R/W, default: 0x0404															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCNT								SCNT							

Bit	Symbol	Description
7:0	SCNT	De-bounce Time of Touch-on judgment. When delta of input has been larger than SETTH for SCNT times continuously, touch-on status is detected.
15:8	CCNT	De-bounce time of Touch-release judgment. When delta of input has been below CLRTHR for CCNT times continuously, Touch

		status is detected to be released.

BLCTH, Baseline Trace Configuration Register

Address: 0x1C, R/W, default: 0x1008															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLU								BLD							

Bit	Symbol	Description
7:0	BLD	Baseline trace-down speed control. When raw data has been lower than baseline for more than BLD times, baseline increment by 1. The bigger is the BLD, the slower is the trace-down speed.
15:8	BLU	Baseline trace-up speed control. When raw data has been higher than baseline for BLU times, baseline decrement by 1.The bigger is the BLU, the slower is the trace-up speed.

BLDTH, Baseline Reset Threshold

Address: 0x1D, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								BLDTH							

Bit	Symbol	Description
7:0	BLDTH	Baseline reset function is used for preventing raw data below the baseline abnormally. 0 : baseline reset when (baseline - raw data)> SETTHR others: Baseline reset when (baseline – row data) > BLDTH
15:8	-	Reserved, must be 0

MDSR, Monitor Data Selection Register

Address: 0x1E, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-			DSEL	

Bit	Symbol	Description
1：0	DSEL	Monitor Data Selection for register KDATA1~6 00: KDATAx is 0 01: KDATAx is the delta value (Raw data – baselin) 10: KDATAx is baseline value 11: KDATAx is the raw data of CDC

GDCFGR, Gesture Detection Configuration Register

Address: 0x20, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	GSTMD		AKST	AKSG	S6	S5	S4	S3	S2	S1

Bit	Symbol	Description
5:0	S6~S1	Gesture detection Enable for input S1~S6 0: disable gesture detection for Sx 1: enable gesture detection for Sx
6	AKSG	Slide Gesture Detection Data Source Selection 0: gesture detection don't use AKS key status 1: gesture detection use AKS key status
7	AKST	Tap Gesture Detection Data Source Selection 0: tap detection don't use AKS key status 1: tap detection using AKS key status
9:8	GSTMD	Gesture Detection interrupt report mode 00: report after certain time passed after finger leaves 01: report as soon as finger leaves 1x: report as soon as gesture criteria has been met

GDTR, Gesture Detection Time Register

Address: 0x21, R/W, default: 0x07															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	GOFFMAX							

Bit	Symbol	Description
7:0	GOFFMAX	Maximum touch-off time during gesture detection. TOFFMAX=GOFFMAX*TSCAN. When finger swift on touch area of gesture detection, it is allowed that no touch is detected for a short time. If no-touch time detected is than the TGOFFMAX, , current gesture is considered to be over.

TDTR, Tap Detection Register

Address: 0x22, R/W, default: 0x080F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TONMAX								TOFFMAX							

Bit	Symbol	Description
15:8	TONMAX	Maximum touch on time of tap detection The tap is invalid when touch on time is longer than TONMAX=TONMAX*TSCAN.
7:0	TOFFMAX	Maximum touch off time of tap detection During finger tap detection, if touch off status has been lasting for more than TOFFMAX (TOFFMAX*TSCAN), the tap gesture is considered to be end.

GSSR1~2, Gesture of Slide Selection Register

GSSR1: address: 0x23, R/W, default: 0x2340
GSSR2: address: 0x24, R/W, default: 0x4320
GSSR3: address: 0x23, R/W, default: 0x1350
GSSR4: address: 0x24, R/W, default: 0x5310

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	KCODE1			0	KCODE2			0	KCODE3			0	KCODE4		

Bit	Symbol	Description
14:12	KCODE1	Code of the first senor in slider 000: None 001: S1 010: S2 011: S3 100: S4 101: S5 110: S6
10:8	KCODE2	Code of the 2nd senor in slider 000: None 001: S1 010: S2 011: S3 100: S4 101: S5 110: S6
6:4	KCODE3	Code of the 3rd senor in slider 000: None 001: S1 010: S2 011: S3 100: S4 101: S5 110: S6
2:0	-	Code of the 4th senor in slider 000: None 001: S1 010: S2 011: S3 100: S4 101: S5 110: S6

Note: The touch state is always detected one by one when finger slide on capacitive sensors in particular order. AW9069 judges slide gesture by checking touch state and comparing its sequence with predefined

one.KCODE1 is the first touching sensor code of slide gesture, and KCODE2/3/4 are the sensor code followed. Each gesture configuration must contain more than 2 sensors, and max 4 sensors. If only 3 sensors are used, KCODE4 should be 000. If KCODE1 is 0, this register is invalid.

TAPR, Tap Configuration Register

Address: 0x27, R/W, default: 0x12															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	K6	K5	K4	K3	K2	K1	TIMES	
Bit	Symbol		Description												
1:0	TIMES		Click times selection 01: single click 10: double click 11: triple click												
7:2	K6~K1		Tap sensor channel selection, define the whether sensor (Sx) is involved in tap detection or not. Kx=0, pin Sx is detected for tap gesture. Kx=1, pin Sx is not included in tap gesture												

GIER, Gesture Interrupt Enable Register

Address: 0x2D, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	TIE	GIE4	GIE3	GIE2	GIE1
Bit	Symbol		Description												
3:0	GIE4 ~ GIE1		Gesture detection interrupt for predefined slide gesture1~ 4 respectively. 0: disable interrupt 1: enable interrupt												
4	TIE		Tap detection interrupt 0: disable interrupt 1: enable interrupt												
15:5	-		Reserved, must be 0												

GISR, Gesture Interrupt Status Register

Address: 0x2E, R(clear by reading), default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	TIS	0	0	GIS2	GIS1
Bit	Symbol		Description												
1:0	GIS2, GIS1		Gesture detection interrupt status 0: no gesture interrupt 1: gesture interrupt												
4	TIS		Tap detection interrupt status 0: no tap interrupt 1: tap interrupt												
15:5	-		Reserved												

GTIMR, Gesture Duration Register

Address: 0x2F, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	GTIMR							
Bit	Symbol		Description												
7:0	GTIM		Gesture duration timer, from touch on to touch off T_{GEST} = GTIMR*T_{SCAN}, 0: no limit												

RAWST, Raw Key Status Register

Address: 0x30, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IDLST	0	0	S6	S5	S4	S3	S2	S1
Bit	Symbol		Description												

5:0	S6 ~ S1	Touch status for sensor 6~1 respectively 0: no touch 1: touch on
8	IDST	IDLE status 0: normal scan status 1: IDLE mode status

KEYST, AKS Key Status Register

Address: 0x31, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	S6	S5	S4	S3	S2	S1

Bit	Symbol	Description
5:0	S6 ~ S1	AKS key status 0: no touch detected 1: touch detected

KISR, Key Interrupt Status Register

Address:0x32, R(cleared after read), default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SBI	-	IS6	IS5	IS4	IS3	IS2	IS1

Bit	Symbol	Description
5:0	IS6~1	Key interrupt status 0: no key interrupt 1: key interrupt
6	-	Reserved. Must be 0
7	SBI	Scan Boundary Interrupt. Set every frame scan finishes, cleared by I^2C reading

MOVCNTR, Slider Move Counter Register

Address: 0x35, R (cleared after read), default: 0x00															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	MOVCNTR							

Bit	Symbol	Description
7:0	MOVCNTR	Bit7 is sign bit, means the slide direction. Bit6-0 is the slide data.

KDATAn, Key Data Register

Address: 0x36~0x3B, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KDATAx															

Bit	Symbol	Description
15:0	KDATAx	Sx data (refer to register MCR(0x1E))

DUM0, Reserved Register

Address: 0x3C, R/W, default: 0x0FFF															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUM0															

Bit	Symbol	Description
15:0	DUM0	Reserved register, default is 0x0FFF

DUM1, Reserved Register

Address: 0x3D, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUM1															

Bit	Symbol	Description
15:0	DUM1	Reserved register, default is 0x0000

LED Control Register

LER1, LED Driver Enable Register

Address: 0x50, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LE9	LE8	LE7	LE6	LE5	LE4	LE3	LE2	LE1

Bit	Symbol	Description
8:0	LEx	LEDx output enable 0: disable output 1: enable output
15:8/1:0	-	Reserved, must be 0

LCR, LED Effect Configuration Register

Address: 0x52, R/W, default: 0x0080															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SRMINI	LIRMD		TIMD		LIE	FREQ	LOGLIN	

Bit	Symbol	Description
1:0	Log/Lin	Log/Linear dimming 00: log dimming 1, log(e) 01: log dimming 2, log10 1x: linear dimming
2	FREQ	PWM Frequency Selection 0: 244Hz 1: 122Hz
3	LIE	LED Program interrupt enable. LED program controller can generate interrupt to inform external host MCU after lighting effect is finished. 0: disable 1: enable
5:4	TIMD	Touch interrupt mode for LED program controller. 00: touch status change 01: touch status change from 1 to 0 10: touch status change from 0 to 1 11: v status is 1
7:6	LIRMD	LED effect code run mode after interrupt response 00: hold mode, PC point can be changed, program hold and wait for RMD.RUNMD, only used in debug. 01: step mode, only used in debug. 10: run mode (default)
8	SRMINI	SRAM reset control. Write 1 to initialize all SRAM data

PMD, Program Mode Register

Address: 0x53, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROGMD	

Bit	Symbol	Description
1:0	PROGMD	Program Mode Control 00: load program by I^2C interface (default) 01: re-load program and execute, set PC point with SADDR and change PROGMD to 10, run program 10: run program 11: undefined

RMD, Program Run Mode Register

Address: 0x54, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNMD	

Bit	Symbol	Description
1:0	RUNMD	SRAM program run mode (CTRSEL=0)

		00: hold mode, program stop and hold PC point 01: step mode, execute the current program, PC point add 1 and set RUNMD to 00 10: run mode, program run from PC point 11: repeat mode, execute the current program, set PC point to 00

CTRSR, LED Control Source Register

Address: 0x55, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CTRSEL								
Bit	Symbol		Description												
8:0	CTRSEL		LED Control Source Selection for pin LEDx (x=1~9) 0: LEDx controlled by SRAM program 1: LEDx controlled by I^2C interface												

IMAX1~IMAX3 LEDx Maximum Output Current Register

Address: 0x57~0x59, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	IMAX4			0	IMAX3			0	IMAX2			0	IMAX1		
0	IMAX8			0	IMAX7			0	IMAX6			0	IMAX5		
0000000000000													IMAX9		
Bit	Symbol		Description												
2:0 6:4 10:8 14:12 2:0 6:4 10:8 14:2 2:0	IMAX1 IMAX2 IMAX3 IMAX4 IMAX5 IMAX6 IMAX7 IMAX8 IMAX9		LEDx maximum output current setting for 9 LED output, 3-bit/ 8-step, default value is 000. 000: 0mA 001: 3.5mA 010: 7.0mA 011: 10.5mA 100: 14.0mA 101: 17.5mA 110: 21.0mA 111: 24.5mA												

TIER, Touch Key Interrupt for LED Enable Register

Address: 0x5C, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	TIE	0	0	GIE2	GIE1	KIE6	KIE5	KIE4	KIE3	KIE2	KIE1
Bit	Symbol		Description												
5:0	KIE6 ~ KIE1		Touch key interrupt enable 0: disable 1: enable												
7:6	GIE2, GIE1		Gesture interrupt enable 0: disable 1: enable												
10	TIE		Tap interrupt enable 0: disable 1: enable												

TIVEC, Touch Key Interrupt Vector Register

Address: 0x5D, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TIVEC							
Bit	Symbol		Description												
7:0	TIVEC		Touch key interrupt vector, the entry address of SRAM LED lighting program. Once SRAM controller response the touch interrupt, PC point jumps to the target address (TIVEC) at once and the begin to execute from it.												

LISR, LED Interrupt Status Register

Address: 0x5E, R(clear by reading), default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIS

Bit	Symbol	Description
0	LIS	LED program end interrupt status, END command can request interrupt to report external MCU when LED SRAM code finish. 0: no interrupt 1: interrupt request

SADDR, Program Start Address Register

Address: 0x5F, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SADDR							

Bit	Symbol	Description
7:0	SADDR	SRAM program starting address Program start to run from SADDR when PMD.PROGMD=01.

PCR, LED Program Control Point Register

Address: 0x60, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PC							

Bit	Symbol	Description
7:0	PC	SRAM Program Control Point(PC) PC point can be changed in any state by I^2C interface. Generally it is recommended to set the PC point when bits PROGMD is 00.If bit PROGMD is changed from 00 to 10, program will start from current PC.

CMDR, LED Command Register

Address: 0x61, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD															

Bit	Symbol	Description
15:0	CMD	External Control Instruction via I^2C interface, only active for those LED which select to be controlled by external MCU (CTRSEL bit is 1 in register CTRSR) The format of external control is the same as internal SRAM program controller. .

RA/RB/RC/RD,LED Internal Program Register

Address: 0x62~0x65, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	RA							
0	0	0	0	0	0	0	0	RB							
0	0	0	0	0	0	0	0	RC							
0	0	0	0	0	0	0	0	RD							

Bit	Symbol	Description
7:0	RA/RB/RC/RD	LED internal program register, can be read via I^2C for monitoring.

R1~R8, LED Internal Data Register

Address: 0x66~0x6D, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	R1							
0	0	0	0	0	0	0	0	R2							
0	0	0	0	0	0	0	0	R3							
0	0	0	0	0	0	0	0	R4							
0	0	0	0	0	0	0	0	R5							
0	0	0	0	0	0	0	0	R6							
0	0	0	0	0	0	0	0	R7							
0	0	0	0	0	0	0	0	R8							

Bit	Symbol	Description

7:0	R1~R8	LED internal data register, can be read via I²C

GRP, LED Group Operation Register

Address: 0x6E, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	GRPSEL								

Bit	Symbol	Description
4:2	GRPSEL	LEDx group definition, used for group control for multiple LED When the LED instruction channel code is 0x1E, it is active for all channels specified by bits GRPSEL[8:0]. 0: LEDx is excluded 1: LEDx is included in group control.

WADDR, LED Program Loading Address Register

Address: 0x7E, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ADDR							

Bit	Symbol	Description
7:0	ADDR	LED program loading address

WDATA, LED Program Loading Data Register

Address: 0x7F, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE															

Bit	Symbol	Description
15:0	CODE	16bit LED program instruction code

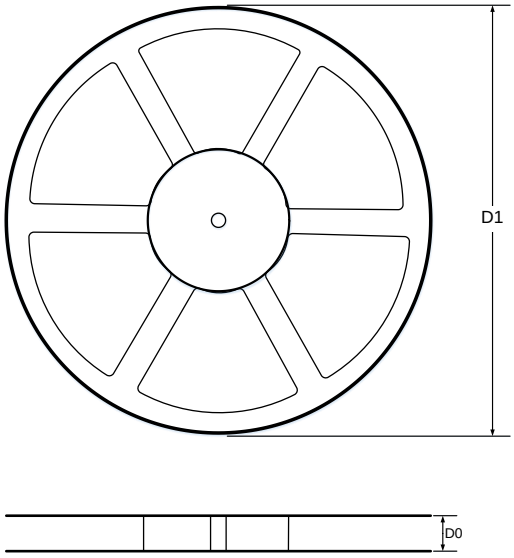
WPR, Writing Protection Register

Address: 0x7D, R/W, default: 0x5500															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPW								0	0	0	0	0	0	0	0

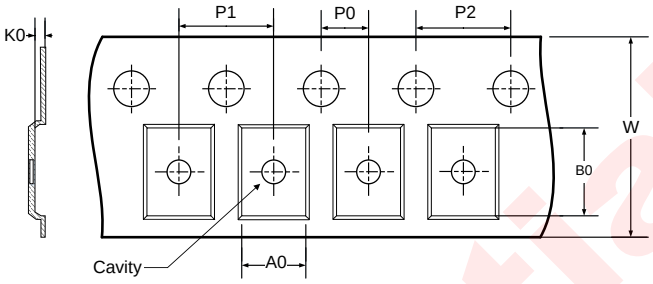
Bit	Symbol	Description
15:8	WPW	Writing protection word, 8-bit.When WPW is 55H, all internal configuration registers are allowed to be written via I²C interface. When WPW is not 55H, the all configuration registers except for register WPR cannot be written.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

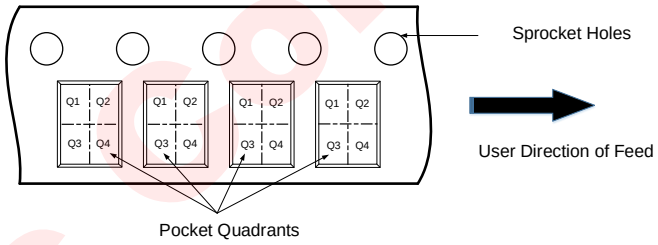


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel width
D1：Reel diameter

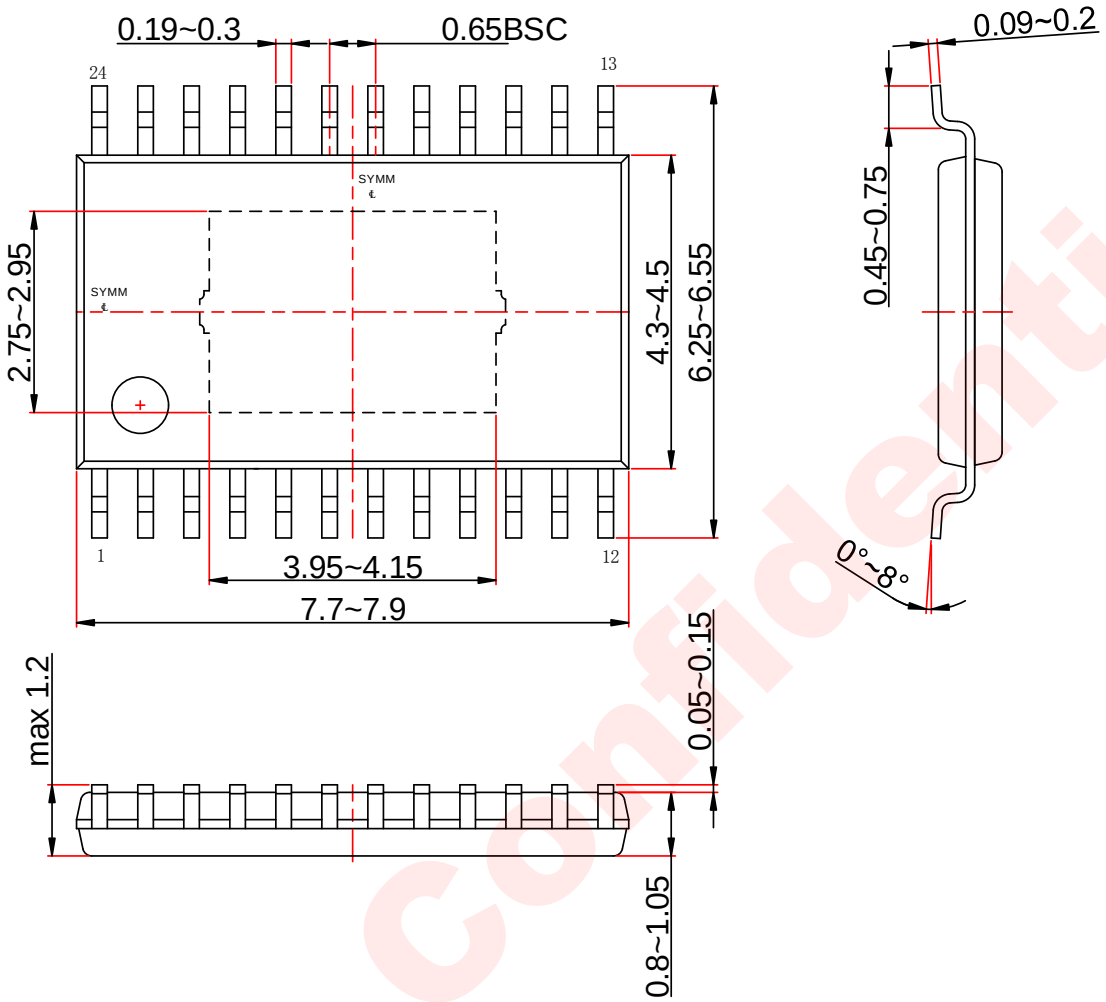
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal

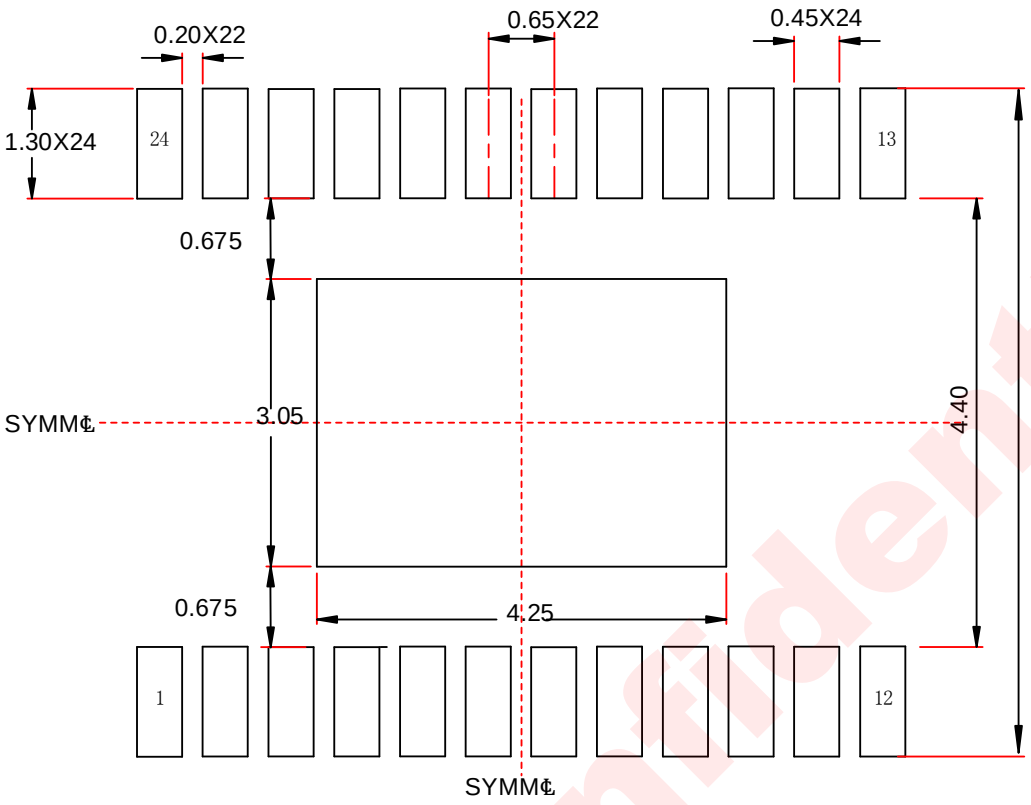
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	16.4	6.8	8.3	1.35	2	8	4	16	Q1

PACKAGE DESCRIPTION

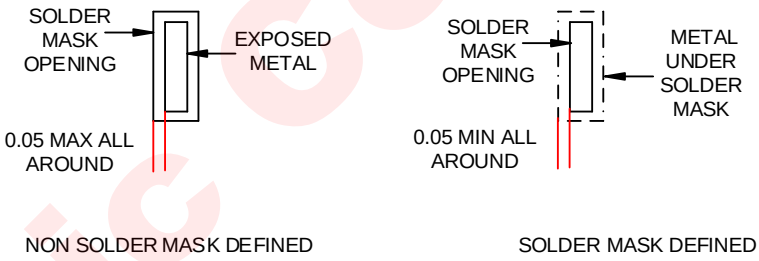


All Dimensions Are In Millimeters

RECOMMENDED LAND PATTERN



LAND PATTERNNN EXAMPLE



SOLDER MASK DETAILS

Unit：mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Nov. 2017	Officially released

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