SIM Card Interface Level Shifter with EMI Filter and ESD Protection

Features

- Clock speeds up to 50 MHz clock
- Host microcontroller operating voltage range: 1.08V to 1.98V
- SIM card supply voltages range: 1.62V to 3.6V
- Automatic level translation of I/O,RST and CLK between SIM card and host side interface with capacitance isolation
- Suitable for all ETSI,IMT-2000 and ISO-7816-3 SIM/Smart card interface requirements
- Integrated EMI filters suppress higher harmonics of digital I/Os
- ESD protection:
  IEC61000-4-2 level 4,contact and air discharge on all SIM card-side pins are ±8kV and ±15kV
- QFN 1.8×1.4-10L package and FOWLP 1.060×1.060-9B package

General Description

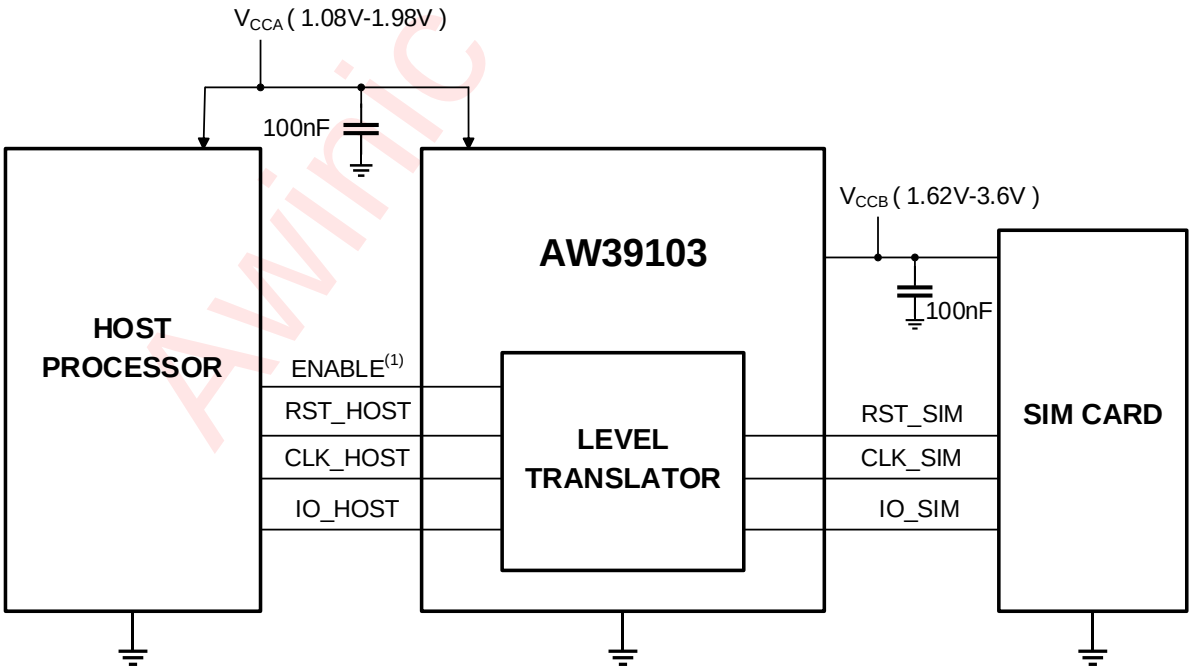
The AW39103 is designed to provide a single low-voltage host-side interface for the SIM card. The AW39103 has three level shifters to convert the I/O data, RST and CLK signals between a SIM card and a host-controller. In addition, the automatic bidirectional control structure of the I/O port ,makes it unnecessary to control the signal transmission direction by additional input signals.

The AW39103 is suitable for all ETSI, IMT-2000 and ISO-7816-3 SIM/Smart card interface requirements.

Applications

- Mobile and personal phones
- Wireless modems
- SIM card terminals

Typical Application Circuit

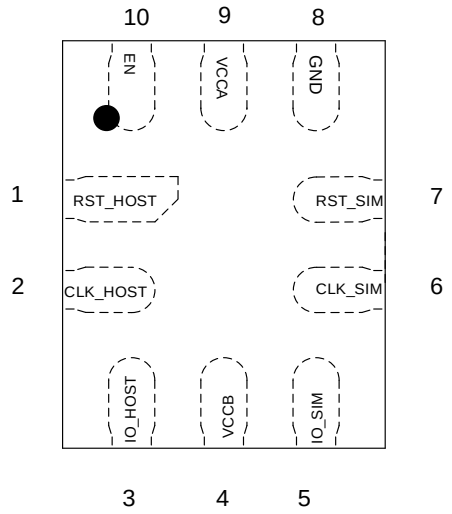


Note1: QFN 1.8×1.4-10L package only

Figure 1 Typical Application Circuit of AW39103

Pin Configuration And Top Mark

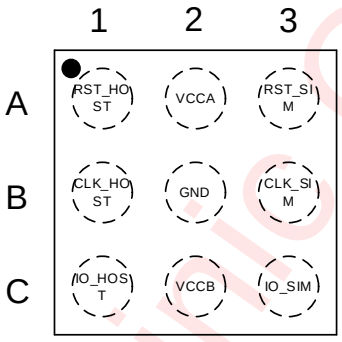
AW39103QNR (Top View)



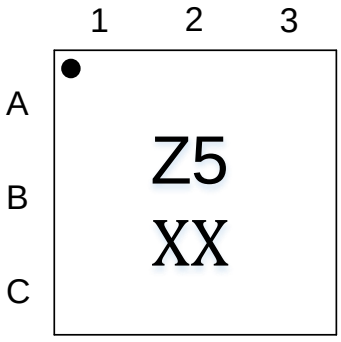
AW39103QNR Marking (Top View)

UXGY – AW39103QNR
XXXX - Production Tracing Code

AW39103FOR (Top View)



AW39103FOR Marking (Top View)



Z5 - AW39103FOR
XX - Production Tracing Code

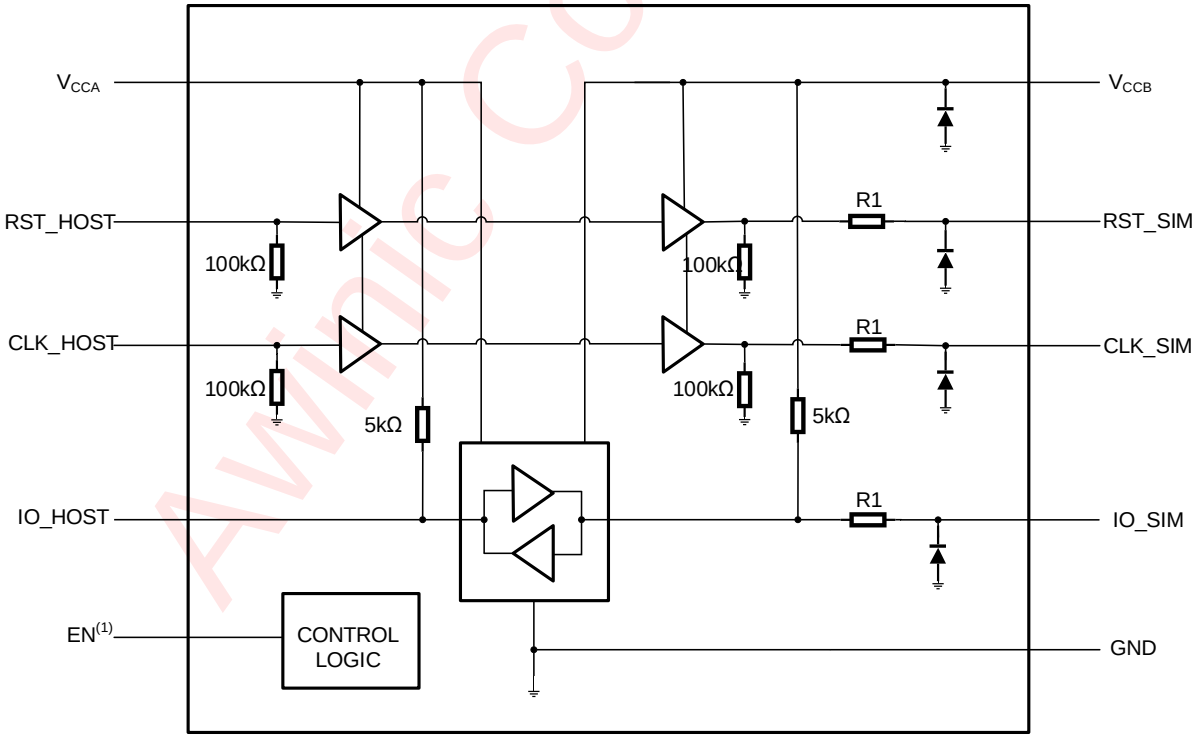
Figure 2 Pin Configuration and Top Mark

Pin Definition

No.		NAME	DESCRIPTION
QFN 1.8×1.4-10L	FOWLP 1.060×1.060-9B		
1	A1	RST_HOST	Reset input from the host controller.
2	B1	CLK_HOST	Clock input from the host controller.

3	C1	IO_HOST	Host controller bidirectional data input/output. The host output must be on an open-drain driver.
4	C2	V_{CCB}	SIM card supply voltage. When V_{CCB} is below the $V_{CCBdisable}$, the device is disabled, 1.62V ≤ V_{CCB} ≤ 3.6V. This pin should be bypassed with a 0.1 μF ceramic capacitor close to the pin.
5	C3	IO_SIM	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.
6	B3	CLK_SIM	Clock output pin for the SIM card.
7	A3	RST_SIM	Reset the output pin for the SIM card.
8	B2	GND	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
9	A2	V_{CCA}	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST), 1.08V ≤ V_{CCA} ≤ 1.98V. This pin should be bypassed with a 0.1μF ceramic capacitor close to the pin.
10	-	EN	Host controller driven enable pin. This pin should be HIGH (V_{CCA}) for normal operation, and LOW to help avoid race conditions specifically during the shutdown sequence.

Functional Block Diagram



Note1: QFN 1.8×1.4-10L package only

Figure 3 AW39103 Function Block

Typical Application Circuits(1)

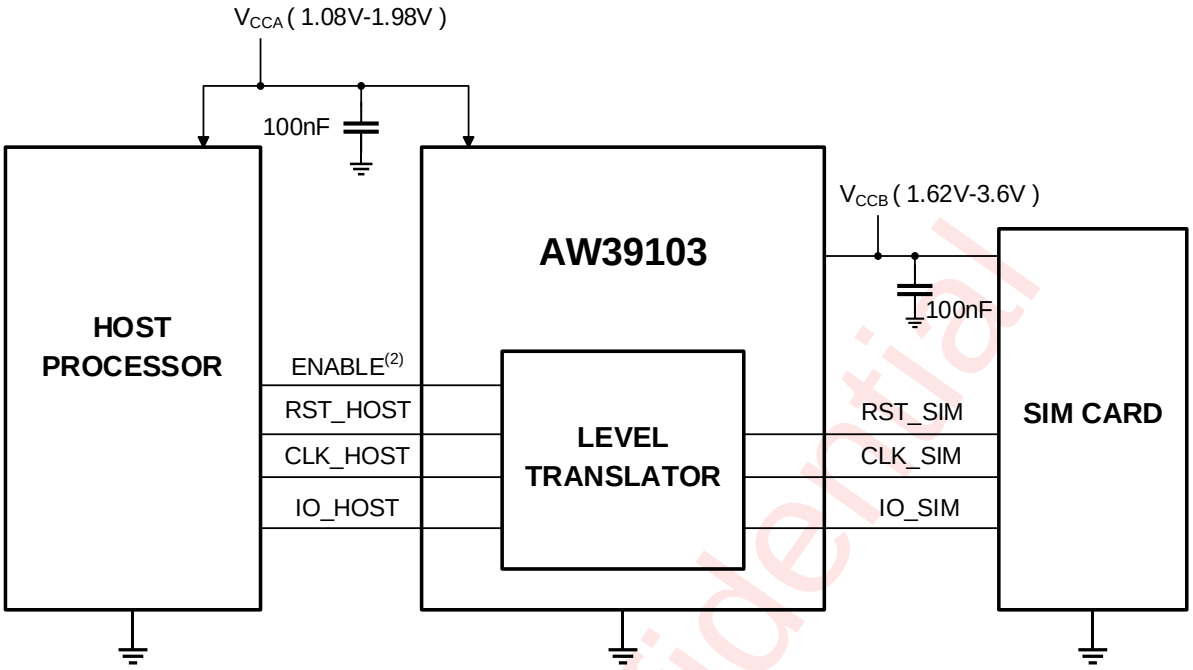


Figure 4 Typical Application Circuit of AW39103

Note:

(1) For typical application circuits, In any case, the A/B Ports Voltage cannot be higher than the V_{CCA}/V_{CCB} voltage;

(2) QFN 1.8×1.4-10L package only

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW39103QNR	-40°C~125°C	QFN 1.8×1.4-10L	UXGY	MSL1	RoHS + HF	4500 units/ Tape and Reel
AW39103FOR	-40°C~125°C	FOWLP 1.060×1.060-9B	Z5	MSL1	RoHS + HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(1)

PARAMETERS		MIN	MAX	UNIT
V_{CCA}	Supply voltage	–0.5	4.0	V
V_{CCB}		–0.5	4.0	
$V_{I(CLK)}$	Input voltage on pin CLK_HOST	–0.5	4.0	V
	Input voltage on pin CLK_SIM	–0.5	4.0	
$V_{I(RST)}$	Input voltage on pin RST_HOST	–0.5	4.0	V
	Input voltage on pin RST_SIM	–0.5	4.0	
$V_{I(IO)}$	Input voltage on pin IO_HOST	–0.5	4.0	V
	Input voltage on pin IO_SIM	–0.5	4.0	
T_{stg}	Storage temperature	–65	150	°C
T_{amb}	Ambient temperature	–40	125	°C
ESD	HBM (Human body mode)(NOTE2)	±2kV		
	CDM (Charged device mode)(NOTE3)	±1kV		
Latch-Up(NOTE4)		+IT: 200mA -IT: 200mA		

NOTE1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.Test method: ESDA/JEDEC JS-001-2023

NOTE3: Test method: ESDA/JEDEC JS-002-2022

NOTE4: Test method:JESD78F

Recommended Operating Conditions

SYMBOL	PARAMETERS	CONDITIONS	MIN	MAX	UNIT
V_{CCA}	Host supply voltage		1.08	1.98	V
V_{CCB}	SIM supply voltage		1.62	3.6	V
V_{IH}	High-level input voltage	IO_HOST,RST_HOST,CLK_HOST	V_{CCA}× 0.7		V
		IO_SIM	V_{CCB}×0.7		V
V_{IL}	Low-level input voltage	IO_HOST,RST_HOST,CLK_HOST	0	V_{CCA} × 0.3	V
		IO_SIM	0	V_{CCB}×0.3	V
Δt/ΔV	Input transition rise or fall rate			200	ns/V

Electrical Characteristics

DC Electrical Characteristics

Operating under recommended conditions, 1.62 V ≤ V_{CCB} ≤ 3.6 V, 1.08 V ≤ V_{CCA} ≤ 1.98 V, Temp = -40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Supplies						
V_{CCA}	HOST supply voltage		1.08		1.98	V
I_{CCA}	HOST supply current	Operating mode, f_{CLK_HOST}=1MHz, EN=V_{CCA}	-	1	5	μA
		Quiescent current, EN=V_{CCA}	-	0.1	1	μA
		Shutdown mode(1), EN=GND			1	μA
V_{CCB}	SIM supply voltage		1.62	-	3.6	V
I_{CCB}	SIM supply current	Quiescent current, EN=V_{CCA}	-	2.5	3.5	μA
Automatic enable feature: V_{CCB}						
V_{CCB_EN}	Enable voltage level	V_{CCA}≥1.0V, V_{CCB} rising edge	1.1	1.45	1.6	V
V_{CCB_DIS}	Disable voltage level	V_{CCA}≥1.0V, V_{CCB} falling edge	1	1.3	1.45	V
ΔV_{CCB_EN}	V_{CCB_EN} hysteresis voltage		-	150	-	mV
Hardware enable pin(1)						
V_{IH_EN}	High-level input voltage	EN pin threshold	0.7•V_{CCA}	-	V_{CCA}+0.3	V
V_{IL_EN}	Low-level input voltage	EN pin threshold	-0.15	-	0.3•V_{CCA}	V
Level shifter						
V_{IH}	High-level input voltage	IO_HOST, RST_HOST, CLK_HOST	0.7•V_{CCA}	-	V_{CCA}+0.3	V
		IO_SIM	0.7•V_{CCB}		V_{CCB}+0.3	V
V_{IL}	Low-level input voltage	IO_HOST, RST_HOST, CLK_HOST	-0.15	-	0.3•V_{CCA}	V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		IO_SIM	-0.15	-	0.3•V_{CCB}	V
R_{PU}(2)	Pull-up resistance	IO_SIM connected to V_{CCB}		5	10	kΩ
		IO_HOST connected to V_{CCA}		5	10	kΩ
V_{OH}	High-level output voltage	RST_SIM, CLK_SIM, IOH = -1 mA	0.85•V_{CCB}	-	V_{CCB}+0.3	V
		IO_SIM, IOH = -10 μA	0.85•V_{CCB}	-	V_{CCB}+0.3	V
		IO_HOST, IOH = -10 μA	0.85•V_{CCA}	-	V_{CCA}+0.3	V
V_{OL}	Low-level output voltage	RST_SIM, CLK_SIM, IOL = 1 mA	0	-	0.12•V_{CCB}	mV
		IO_SIM, IOL= 1 mA	0	-	0.12•V_{CCB}	mV
		IO_HOST, IOL = 1 mA	0	-	0.12•V_{CCA}	mV
R_{pd}	Pull-down resistance	CLK_SIM, RST_SIM, IO_SIM, when EN = 0		400		Ω
EMI filter						
R_S	Series resistance	IO_SIM	-	35	-	Ω
		RST_SIM	-	35	-	Ω
		CLK_SIM	-	35	-	Ω
C_{io}	Input/Output capacitance	IO_SIM	-	10	-	pF
		RST_SIM	-	10	-	pF
		CLK_SIM	-	10	-	pF

Note1: QFN 1.8×1.4-10L package only

Note2: maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Dynamic Characteristics

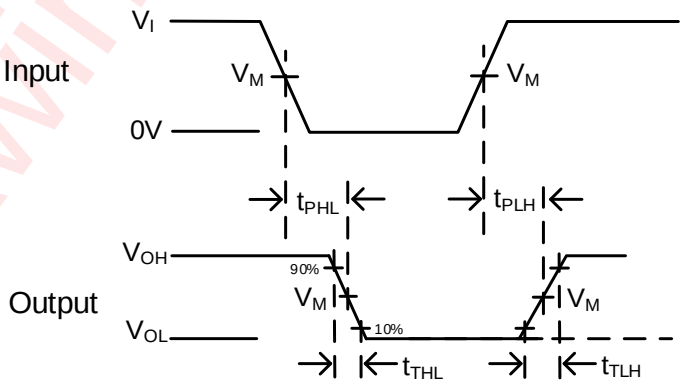
1.65 V ≤ VCCB ≤ 3.6 V, 1.08 V ≤ VCCA ≤ 1.98 V, fclk = fio = 1 MHz, Temp = -40 °C to +125 °C, unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CCA} = 1.8 V, V_{CCB} = 3.0 V, SIM card C_L ≤ 30 pF, host C_L ≤ 10 pF						
t_{pd}(3)	Propagation delay	I/O channel, SIM card side to host side	-	6	12	ns
		All channels, host side to SIM card side	-	6	12	ns
t_t(4)	Transition time		-	4	8	ns
$t_{sk(o)}$	Output skew time	Between channels IO_SIM and CLK_SIM	-	2	-	ns
f_{clk}	Clock frequency	CLK_SIM	-	-	50	MHz
V_{CCA} = 1.2 V, V_{CCB} = 1.8 V, SIM card C_L ≤ 30 pF, host C_L ≤ 10 pF						
t_{pd}(3)	Propagation delay	I/O channel, SIM card side to host side	-	10	20	ns
		All channels, host side to SIM card side	-	10	20	ns
t_t(4)	Transition time		-	4	8	ns
$t_{sk(o)}$	Output skew time	Between channels IO_SIM and CLK_SIM	-	2	-	ns
f_{clk}	Clock frequency	CLK_SIM	-	-	50	MHz

Note3: t_{pd} is the same as t_{PHL} and t_{PLH}.

Note4: t_t is the same as t_{THL} and t_{TLH}.

Test information



Detailed Functional Description

Function table

Supply Voltage		Input	Input/Output		Operational Mode
V_{CCA}	V_{CCB}	EN(1)(2)	Host	SIM Card	
1.08 V to 1.98 V	1.62 V to 3.6 V	H	HOST = SIM Card	SIM Card = HOST	Active
1.08 V to 1.98 V	1.62 V to 3.6 V	L	See the below table, Condition B		Shutdown Mode
GND	1.62 V to 3.6 V	X	See the below table, Condition B		Shutdown Mode
1.08 V to 1.98 V	GND	X	See the below table, Condition A		Shutdown Mode
GND	GND	X	See the below table, Condition A		Shutdown Mode

NOTES:
(1) H = HIGH voltage level; L = LOW voltage level; X = don't care.
(2) V_{IL} and V_{IH} are referenced to V_{CCA}. The EN can be controlled by an external device limit of V_{CCA} + 0.3 V.

Pin condition

Pin condition	Condition A	Condition B
RST_HOST	100 KΩ pull low	100 KΩ pull low
CLK_HOST	100 KΩ pull low	100 KΩ pull low
IO_HOST	5 KΩ pull to V_{CCA}	5 KΩ pull to V_{CCA}
RST_SIM	100 KΩ pull low	400 Ω pull low
CLK_SIM	100 KΩ pull low	400 Ω pull low
IO_SIM	High Z	400 Ω pull low

Embedded Enable – 9 pin and 10 pin if Enable is tied to V_{CCA}

AW39103 integrates the automatic enable function. When V_{CCB} exceeds V_{CCB_EN}, the level translator logic is enabled automatically. If V_{CCB} is lower than V_{CCB_DIS}, the driver of the SIM card and the level translator logic is disabled. Host side IO pin will be configured as a 5KΩ resistor to pull up to V_{CCA}.

When the V_{CCB} is lower than V_{CCB_DIS} but still higher than a MOS threshold (e.g.,0.8V), the NMOS driver transistor in the one-directional drive will be turned off and NMOS controlled by CTL will be turned on, and the 400Ω pull-down resistance will keep the RST/CLK/IO of the SIM card low. In addition, the CLK/RST pins at both ends of the Host and SIM card have 100KΩ pull-down resistances, 400Ω resistance for pull-down discharge when $V_{TH}<V_{CCB}<V_{CCB\_EN}$; and 100KΩ resistance for keeping RST_SIM/CLK_SIM low when $V_{TH}>V_{CCB}$.

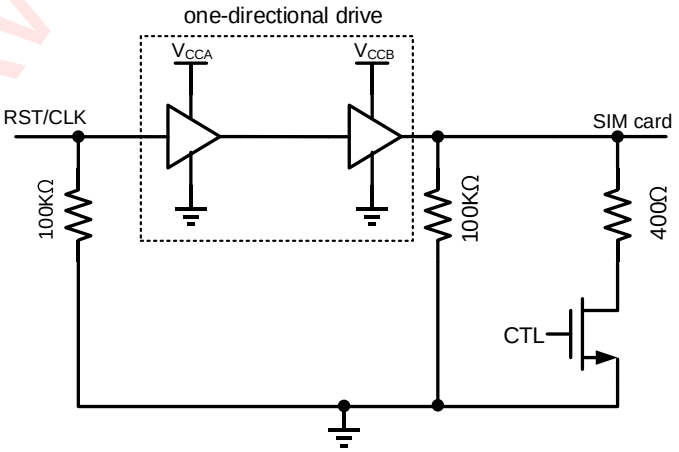


Figure 5. RST/CLK voltage level translation architecture

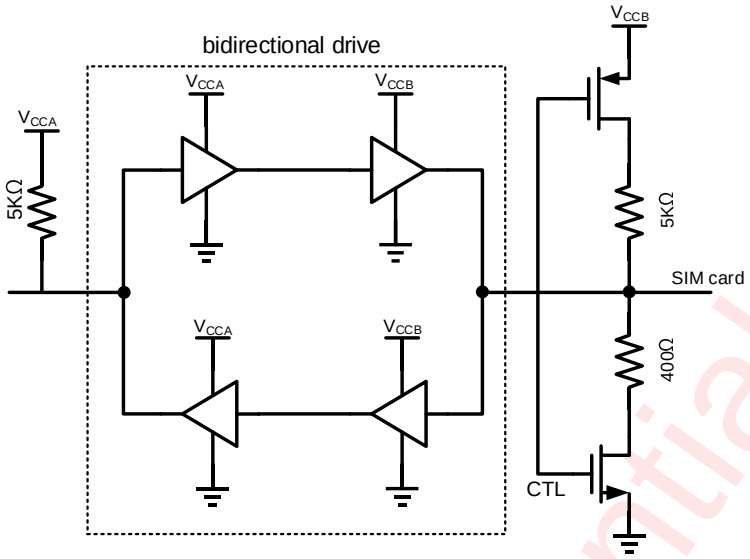


Figure 6. IO voltage level translation architecture

Shutdown Sequence(QFN 1.8×1.4-10L package only)

ISO-7816-3 specifies the sequence in which SIM card signals are turned off to ensure that the SIM card is disabled correctly for power savings. And likewise, the orderly shutdown of these signals during hot swap helps to avoid any improper writing and corruption of data.

When the EN pin is low, the shutdown sequence is initiated by closing the RST_SIM channel, Once the RST_SIM is closed, the CLK_SIM and IO_SIM channels will be closed sequentially one-by-one, An internal pull-down resistance of the SIM card will pull these channels down. The shutdown sequence is completed in a few microseconds. It is important to pull EN down before VCCA and VCCB power supply is low to prevent the shutdown sequence is properly initiated.

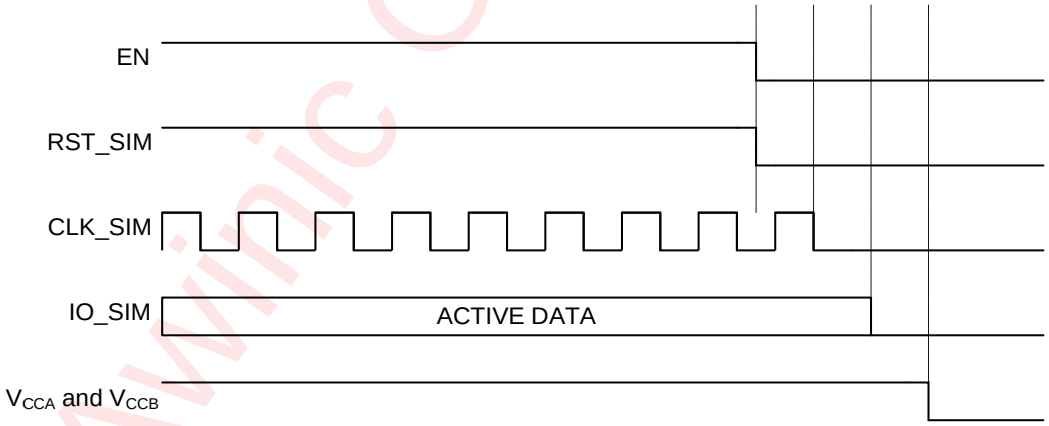


Figure 7. Shutdown sequence for RST_SIM,CLK_SIM,IO_SIM and V_{CCA}/V_{CCB} of AW39103 SIM card translator

Level Shifter

AW39103 does not require additional input signal to control whether the signal flows from HOST to SIM card or from SIM card to HOST. When both sides are in a high state, thetransmission direction can be changed. The control logic authorizes the control of the other side by recognizing the first falling edge. During a rising edge signal, the non-driver side accelerates the slope of the rising edge through a One-shot circuit. As a communication error or some other unforeseen error occurs, both ends are configured as drivers to prevent internal logic locking problems, and IO will return to HIGH level once released from being driven LOW.

The RST and CLK channels have no protection mechanism because they just contain single direction drivers.

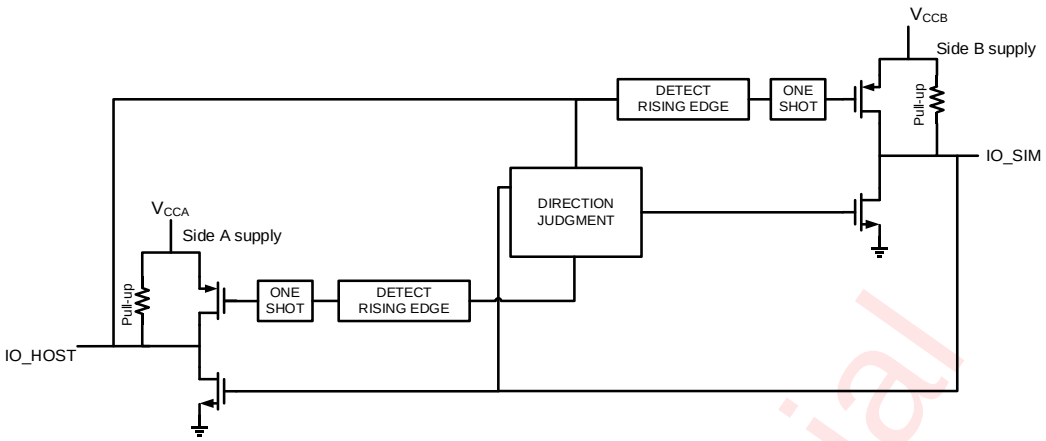
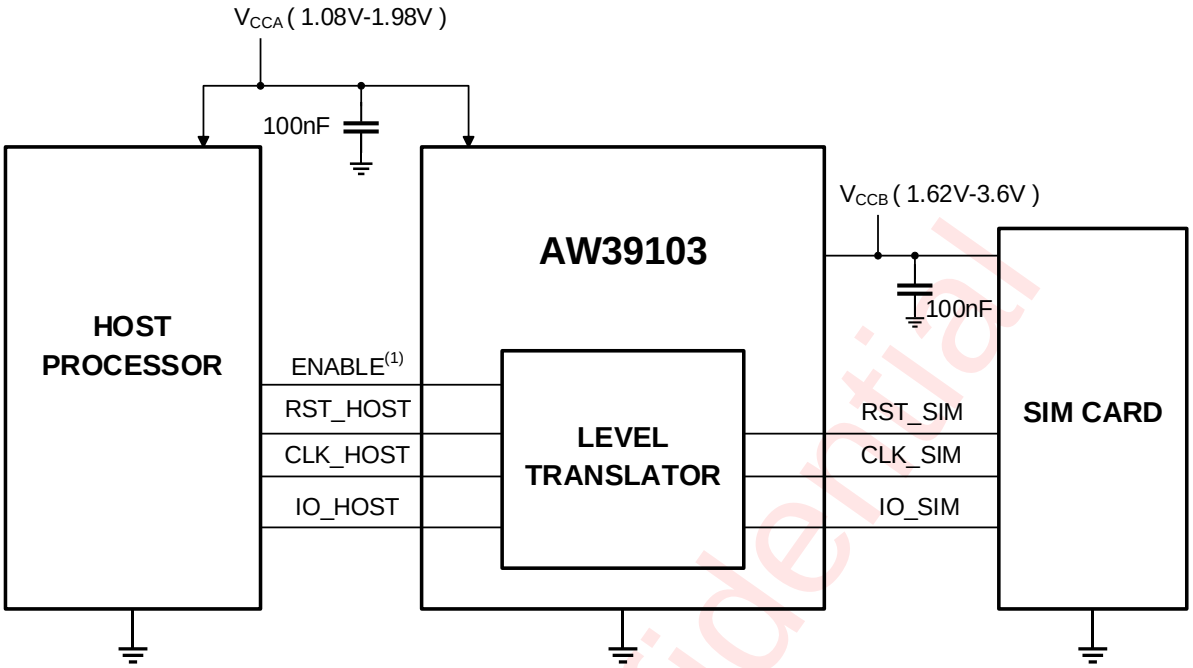


Figure 8. Automatic direstion judgment Structure of level translator

EMI filter

All input/output drivers are equipped with EMI filters to reduce interferences to sensitive mobile communcations.

Application Information



Note1: QFN 1.8×1.4-10L package only

Capacitors Selection

VCCA:

AW39103 advises to use a 1μF or 100nF X5R or X7R ceramic capacitor at V_{CCA} as shown in Typical Application Circuit.

VCCB:

AW39103 advises to use a 1μF or 100nF X5R or X7R ceramic capacitor at V_{CCB} as shown in Typical Application Circuit.

PCB Layout Consideration

1. Input to input, input to output, output to output between the need for ground copper foil isolation, to minimize the ground loop.
2. The power supply of the level shifter should come directly from the same power plane.
3. Bypass capacitors of V_{CCA} and V_{CCB} should be placed as close as possible to V_{CCA} and V_{CCB} pins with a very short PCB trace.
4. The cables on both sides of the Host and SIM card should be as symmetrical as possible and avoid right angles to reduce reflection.

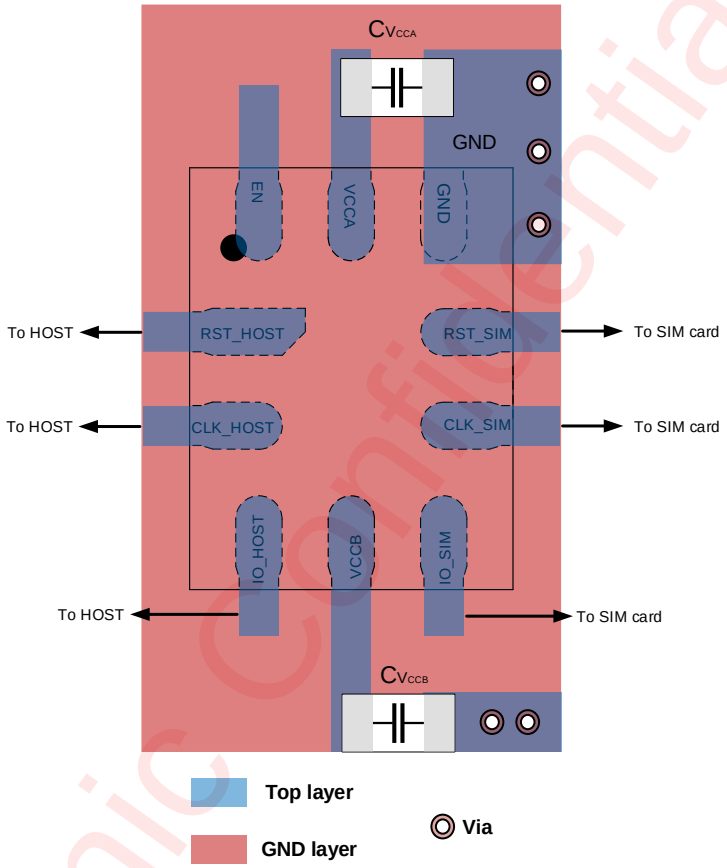


Figure 9. AW39103QNR PCB LAYOUT

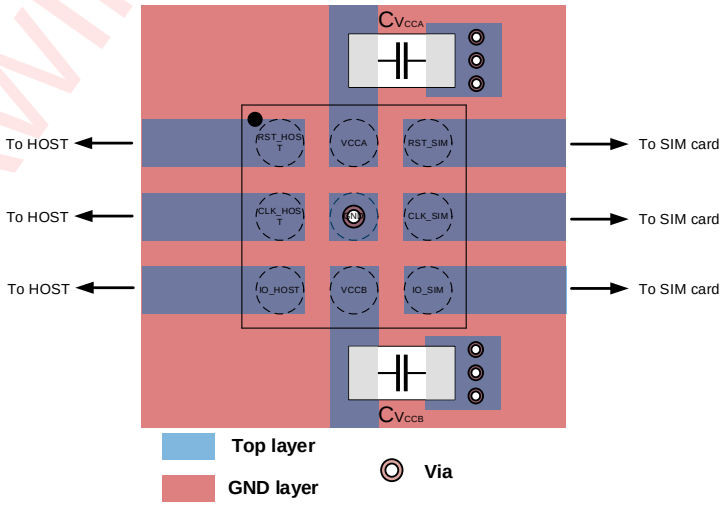
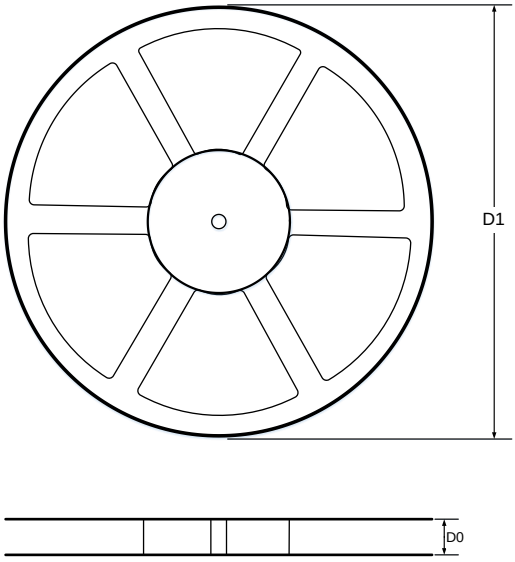


Figure 10. AW39103FOR PCB LAYOUT

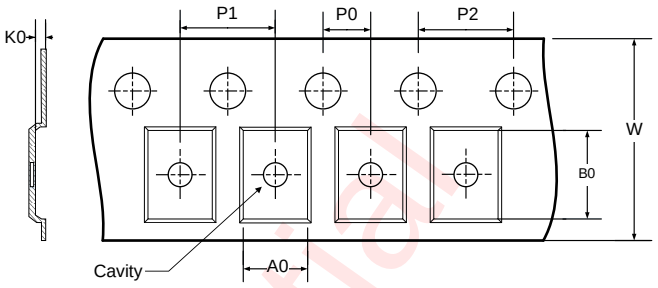
Tape And Reel Information

QFN 1.8×1.4-10L

REEL DIMENSIONS

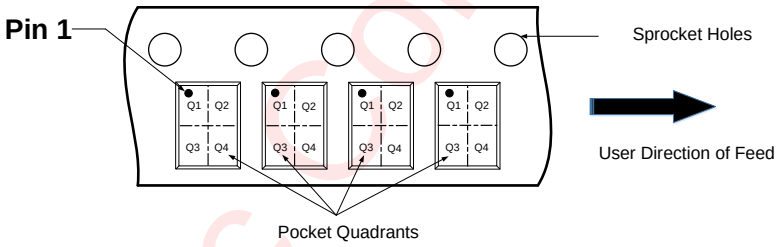


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

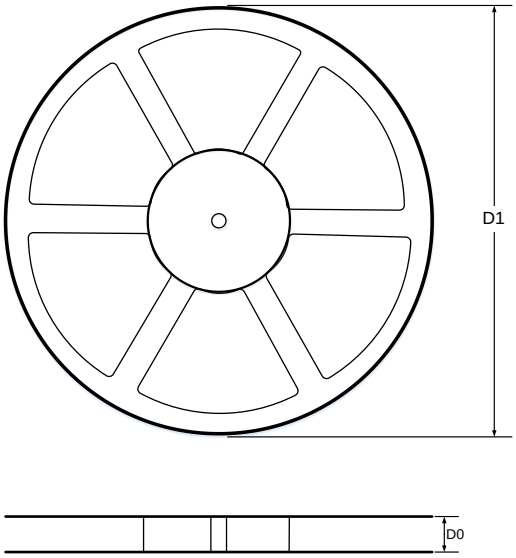
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	8.40	1.58	2.04	0.73	2.00	4.00	4.00	8.00	Q1

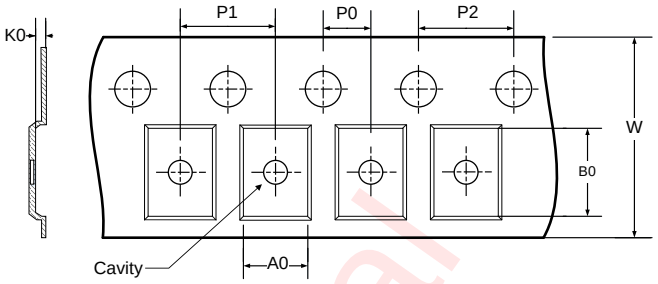
All dimensions are nominal

FOWLP 1.060×1.060-9B

REEL DIMENSIONS

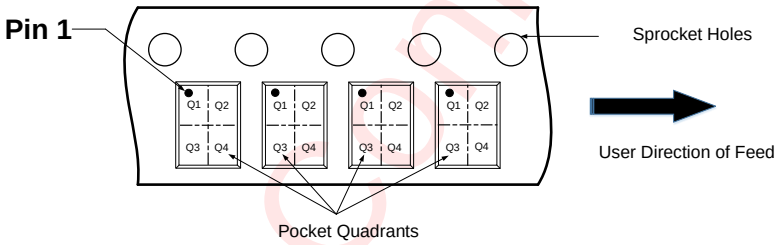


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

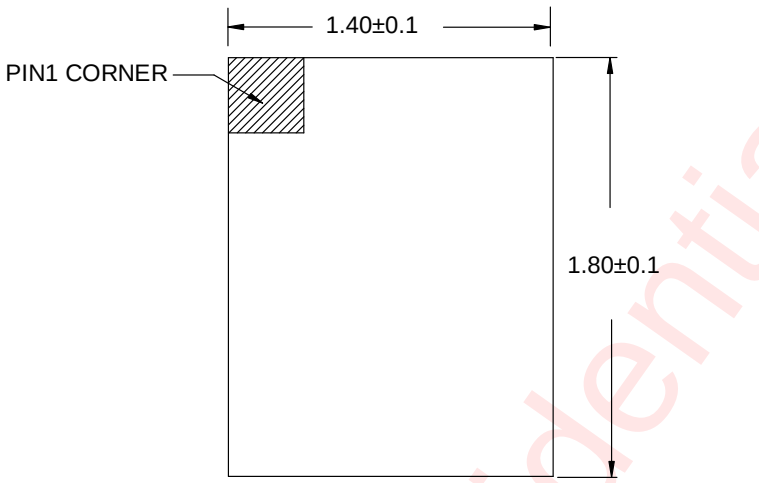
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.18	1.18	0.57	2.00	4.00	4.00	8.00	Q1

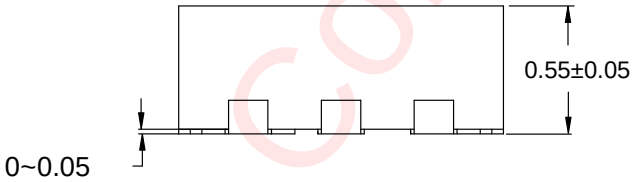
All dimensions are nominal

Package Description

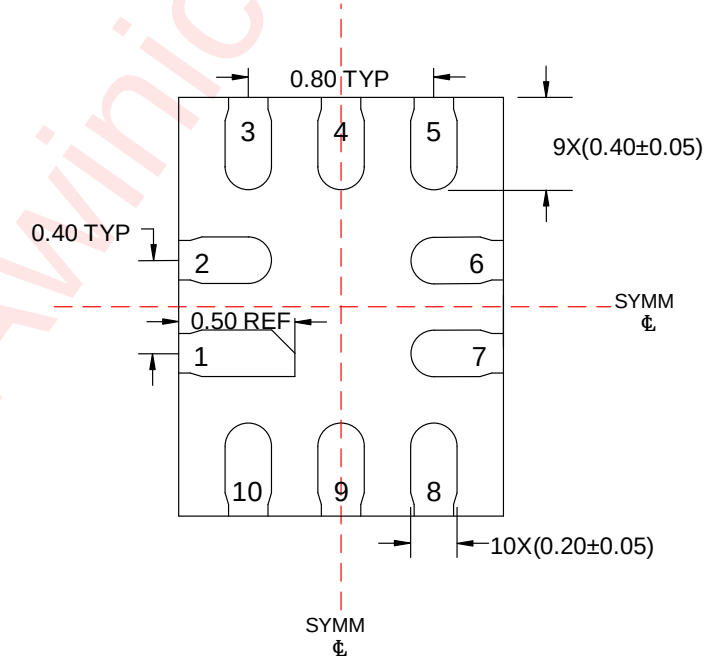
QFN 1.8×1.4-10L



TOP VIEW



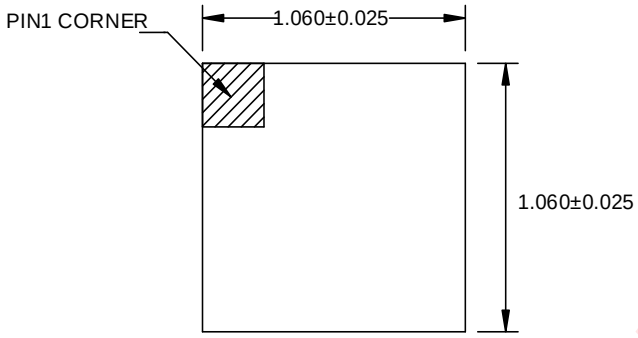
SIDE VIEW



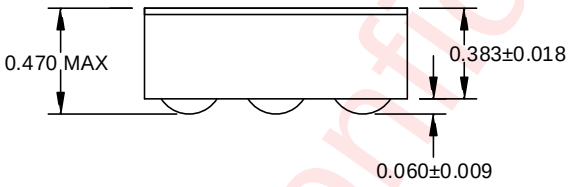
BOTTOM VIEW

Unit:mm

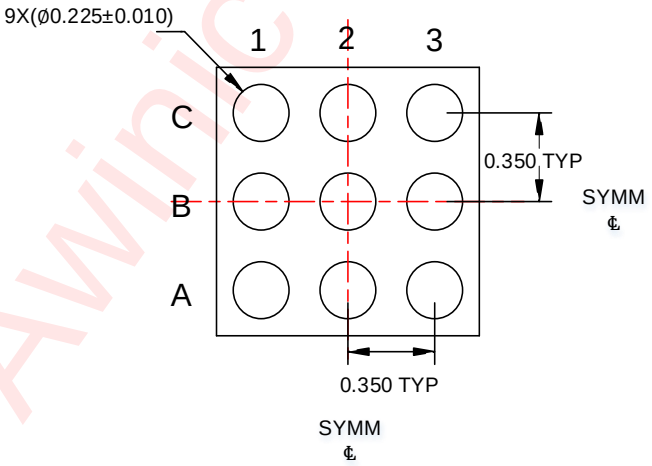
FOWLP 1.060×1.060-9B



TOP VIEW



SIDE VIEW

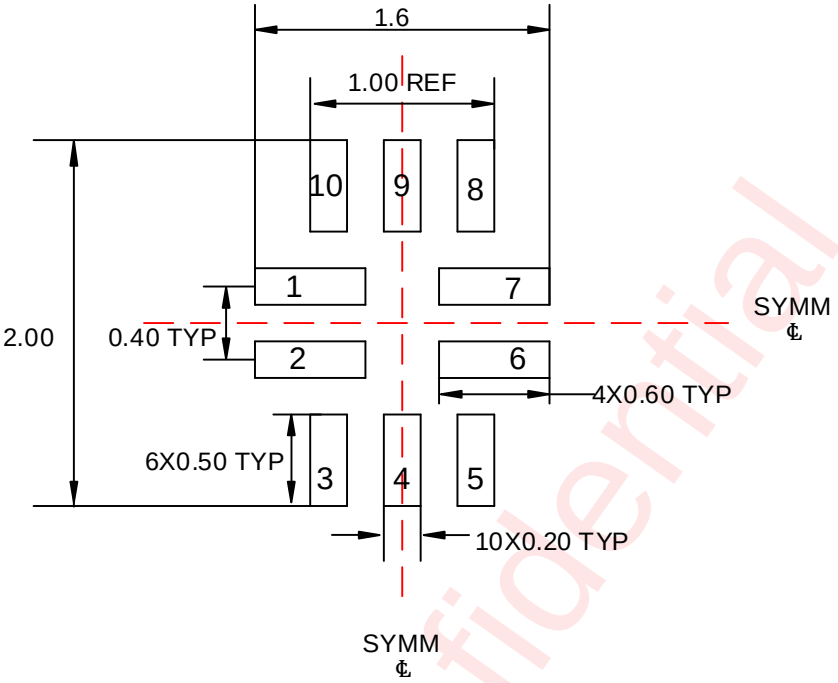


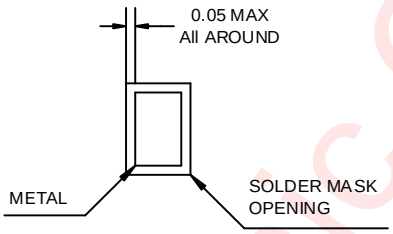
BOTTOM VIEW

Unit：mm

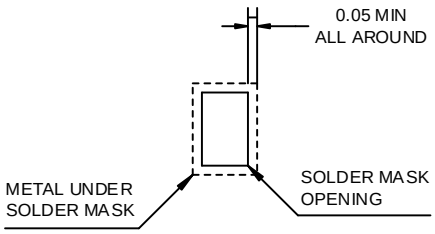
Land Pattern Data

QFN 1.8×1.4-10L





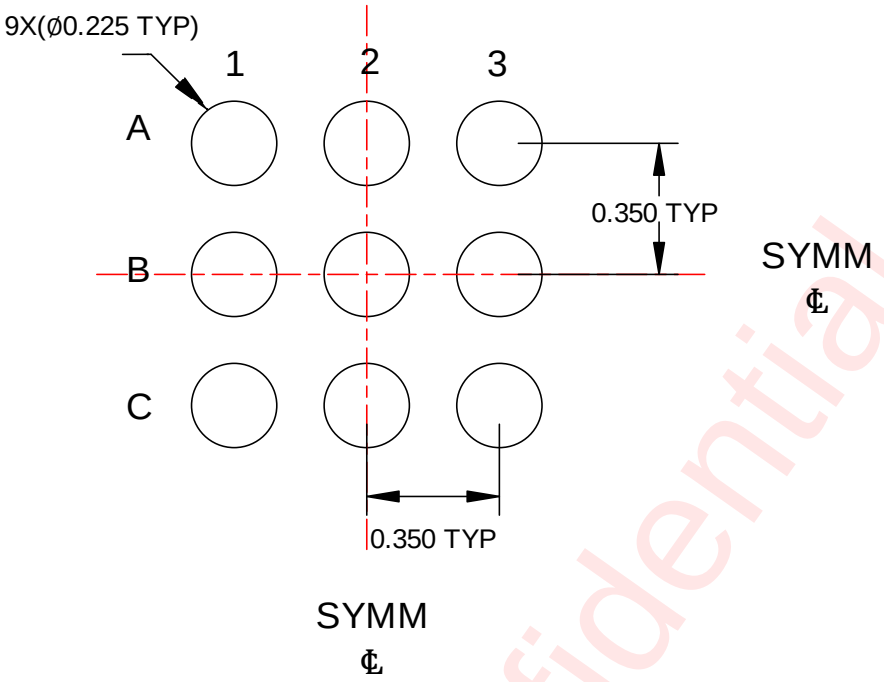
NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit:mm

FOWLP 1.060×1.060-9B



NON-SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Sep. 2025	Officially released.
V1.1	Oct. 2024	Add FOWLP 1.060×1.060-9B package.
V1.2	Nov. 2024	Update Clock frequency to 25 MHz(P1,P8).
V1.3	Jan. 2025	Update DC Electrical Characteristics(P6).
V1.4	Oct. 2025	Update DC Electrical Characteristics(P6-8); Update Functional Block Diagram(P3); Update Package Description of QFN 1.8×1.4-10L package (P16).
V1.5	Nov. 2025	Update Absolute Maximum Ratings(P5); Add Test information(P8).

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