

## Low Noise, RRIO CMOS Op-amps with 8MHz Bandwidth

### Features

- Wide Supply Voltage Range: 1.8V ~ 5.5V
- Low Input Offset Voltage:  $\pm 0.4\text{mV}$
- Slew Rate:  $5\text{V}/\mu\text{s}$
- Low Input Bias Current:  $1\text{pA}$
- Low Broadband Noise:  $13\text{nV}/\sqrt{\text{Hz}}$
- Low Quiescent Current:  $525\mu\text{A}/\text{CH}$
- Rail-to-Rail Input and Output
- Bandwidth: 8MHz
- Sink and Source Current Capability:  $50\text{mA}$
- MSOP - 8L package
- SOT 23 - 8L package

### Applications

- Smart Phones, Tablet PCs
- Consumer Audio-video Equipment
- Headsets/Headphones/Earbuds
- Motion Detectors/Smoke Detectors
- Active Filters
- Low-Side Current Sensing
- Pressure Transmitter
- Process Analytics(Gas, Force, Humidity & PH)

### General Description

The AWS79052 is a dual channel high precision, low-power, low-voltage (1.8V to 5.5V) operational amplifiers with rail-to-rail input and output swing capabilities, which makes it ideal to general-purpose applications. This op amp features very good AC performance with a gain-bandwidth product of 8MHz, slew rate of  $5\text{V}/\mu\text{s}$  and low input voltage noise of  $3.8\mu\text{Vpp}$ , while drawing  $525\mu\text{A}$  per channel (typical) quiescent current. It has an input common-mode voltage range that extends to each supply rail, and its outputs swing to within  $27\text{mV}$  of the supply rails with a  $2\text{k}\Omega$  load.

The AWS79052 provides an appropriate solution for space-constrained applications such as battery powered IoT devices, wearable electronics, and personal electronics where minimum PCB footprint is required. The AWS79052 is available in green small-size MSOP - 8L package and green SOT 23 - 8L package.

### Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AWS79052MPR	MSOP - 8L	3mm × 3mm
AWS79052STR	SOT 23 - 8L	1.6mm × 2.92mm

### Typical Application Circuit

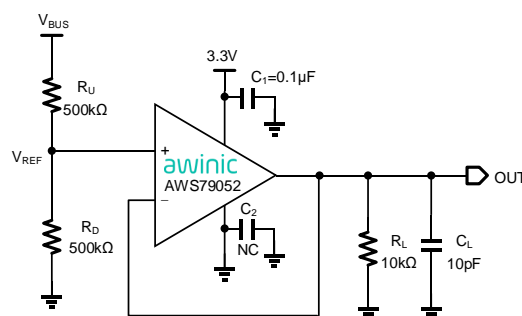
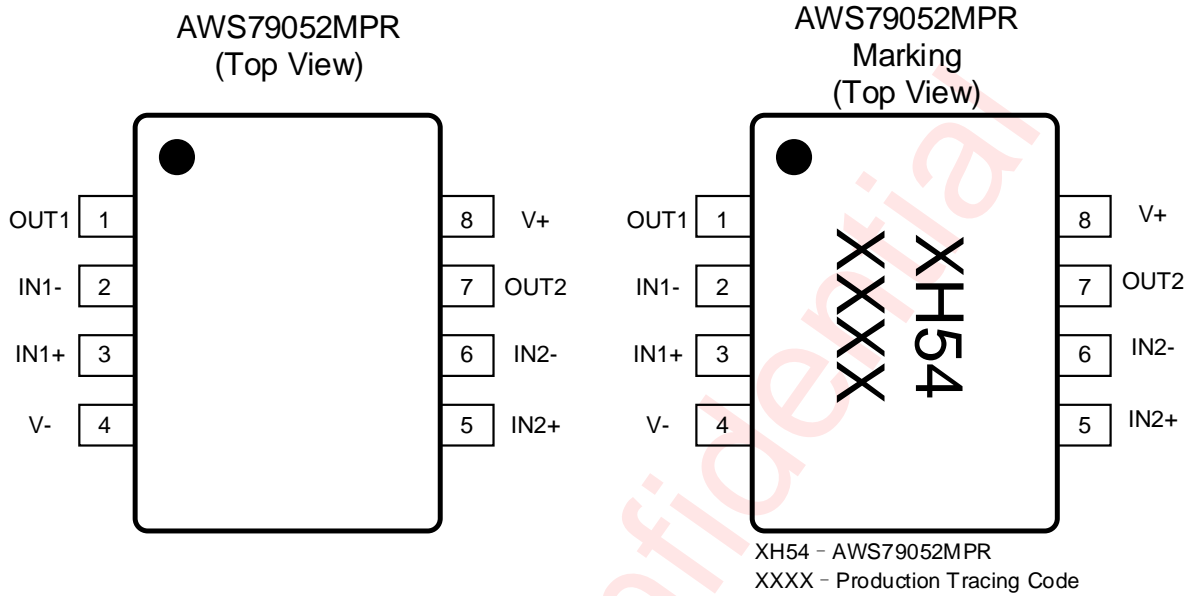


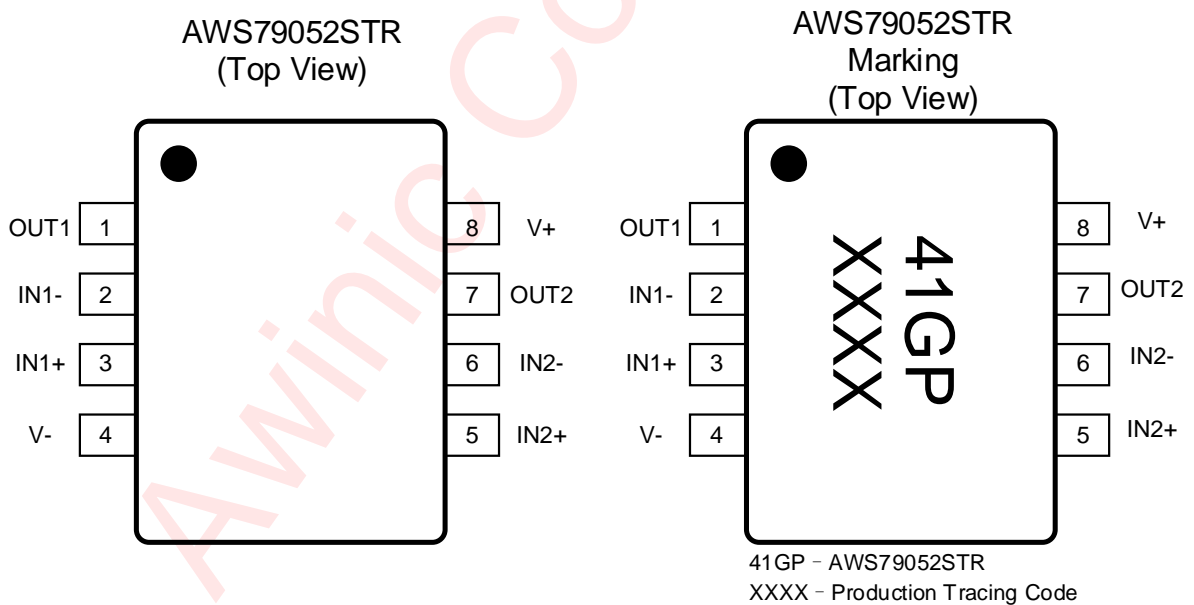
Figure 1 Typical Application of AWS79052

## Pin Configuration And Top Mark

MSOP - 8L



SOT 23 - 8L



**Figure 2 Pin Configuration**

## Pin Definition

No.	NAME	DESCRIPTION
1	OUT1	Channel 1 output
2	IN1-	Channel 1 inverting input
3	IN1+	Channel 1 noninverting input
4	V-	Negative (low) supply or ground (for single-supply operation)
5	IN2+	Channel 2 noninverting input
6	IN2-	Channel 2 inverting input
7	OUT2	Channel 2 output
8	V+	Positive (high) supply

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## Functional Block Diagram

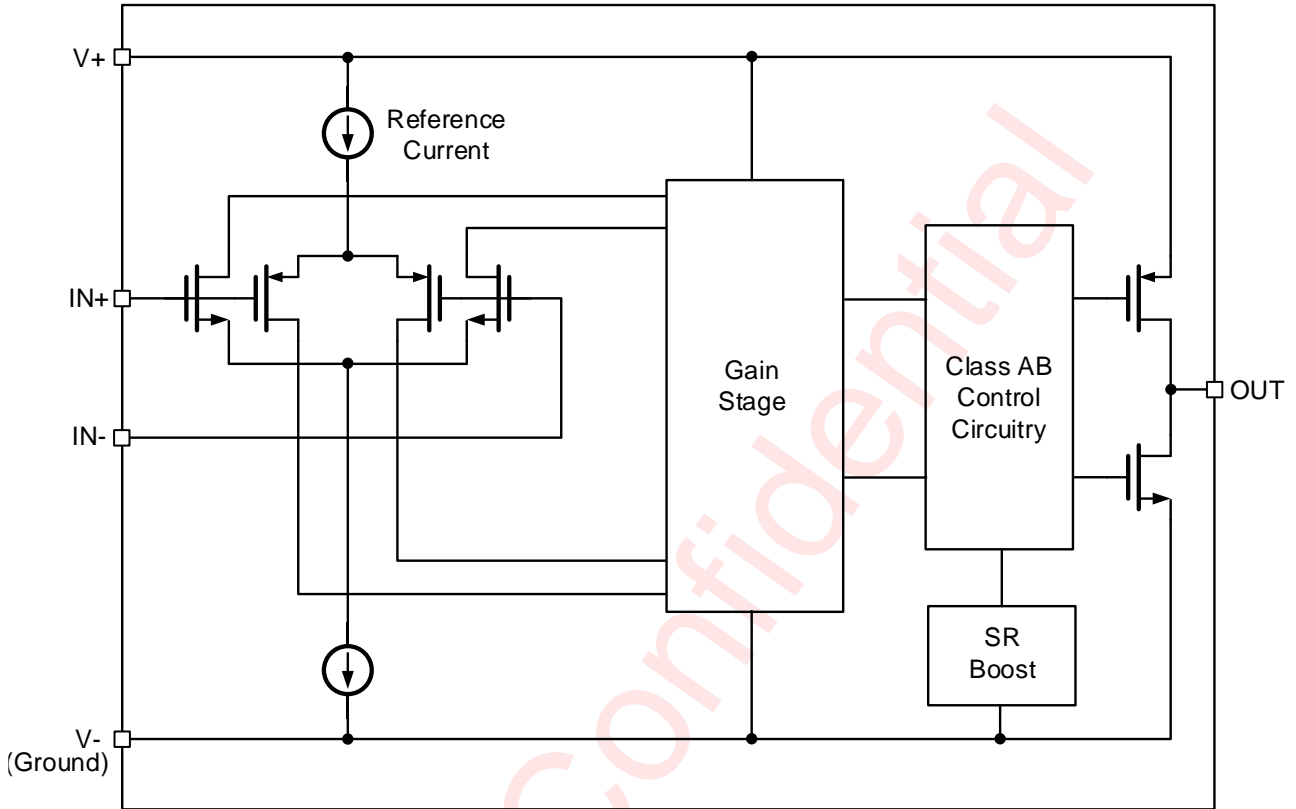


Figure 3 Functional Block Diagram

## Typical Application Circuits

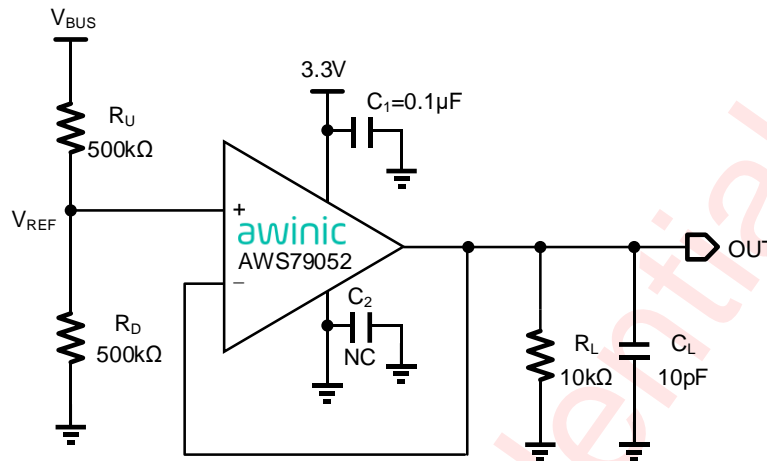


Figure 4 AWS79052 Application Circuit

### Notice for typical application circuits:

1. Bypass capacitors  $C_1/C_2$  are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR,  $0.1\mu\text{F}$  ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces. If negative supply is connected to GND, then negative supply to GND can be disconnected to bypass ceramic.

## Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS79052MPR	$-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$	MSOP - 8L	XH54	MSL3	RoHS+HF	3000 units/ Tape and Reel
AWS79052STR	$-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$	SOT 23 - 8L	41GP	MSL3	RoHS+HF	3000 units/ Tape and Reel

## Absolute Maximum Ratings (NOTE1)

PARAMETERS		RANGE
Supply voltage, $V_S = (V+) - (V-)$		-0.3V to 6.0V
Signal input pins	Common-mode voltage (NOTE 2)	(V-) - 0.5V to (V+) + 0.5V
	Differential voltage (NOTE 2)	-6V to 6.0V
	Current (NOTE 2)	-10mA to 10mA
Output short-circuit (NOTE 3)		Continuous
Operating free-air temperature range $T_A$		-40°C to 125°C
Maximum operating junction temperature $T_{JMAX}$		150°C
Storage temperature $T_{STG}$		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Input pins are diode-clamped to each power supply. Input signals that may extend more than 0.5V beyond the supply rails must be current limited to 10mA or less.

NOTE3: A heat sink may be required to keep the junction temperature below the absolute maximum.

## ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 4)	±4	kV
CDM (NOTE 5)	±1.5	kV
Latch-Up (NOTE 6)	+IT: 400 -IT: -400	mA

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

NOTE5: Test method: ESDA/JEDEC JS-002-2018

NOTE6: Test method: JESD78E

## Thermal Information

THERMAL METRICS		AWS79052		UNIT
		MSOP	SOT	
SYMBOL	PARAMETER	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	199.8	208.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	166.7	103.8	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	114.8	174.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	31.5	79.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	134.7	93.8	°C/W

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## Electrical Characteristics

Unless otherwise noted,  $V_S = (V+) - (V-) = 1.8V$  to  $5.5V$  ( $\pm 0.9V$  to  $\pm 2.75V$ ),  $R_L = 10k\Omega$  connected to  $V_S/2$ ,  $V_{CM} = V_S/2$ , and  $V_{OUT} = V_S/2$ , typical values are at  $V_S = 5V$  and  $T_A = 25^\circ C$ .

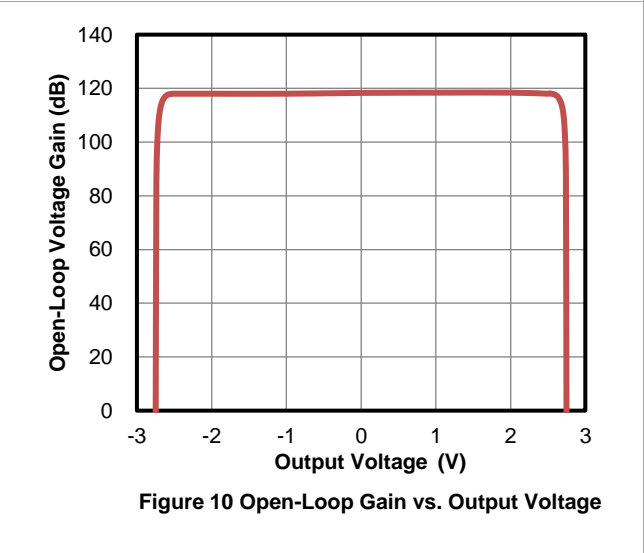
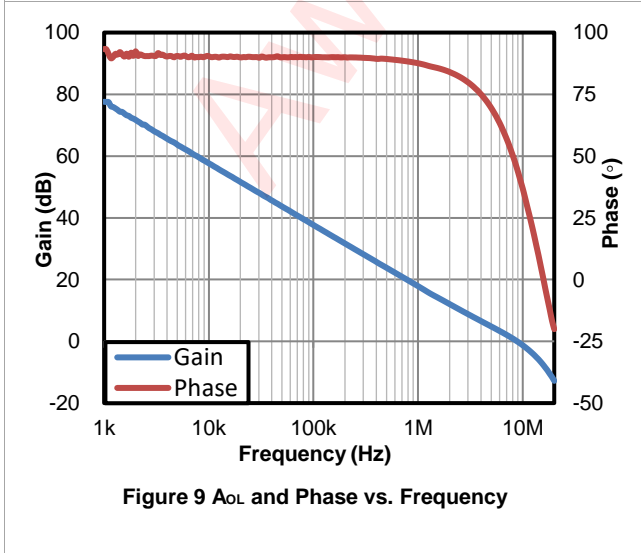
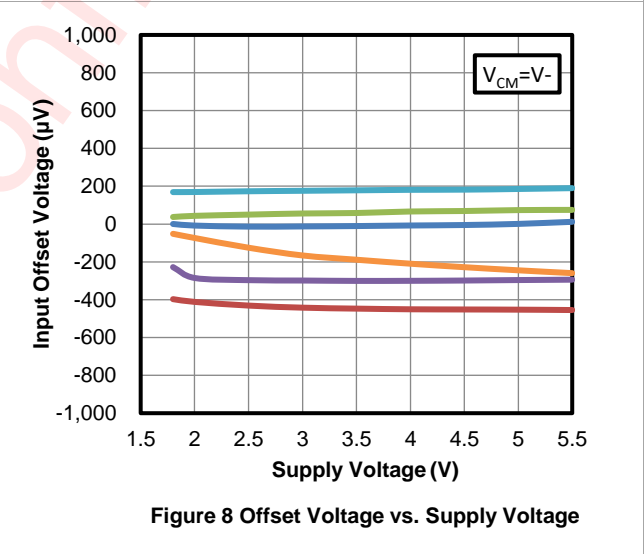
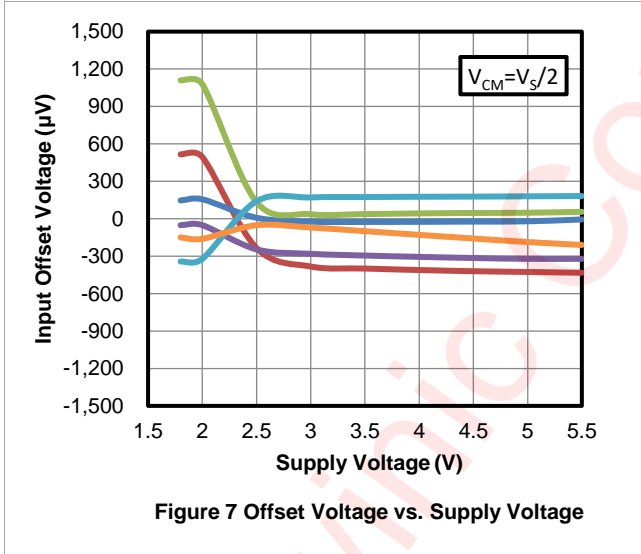
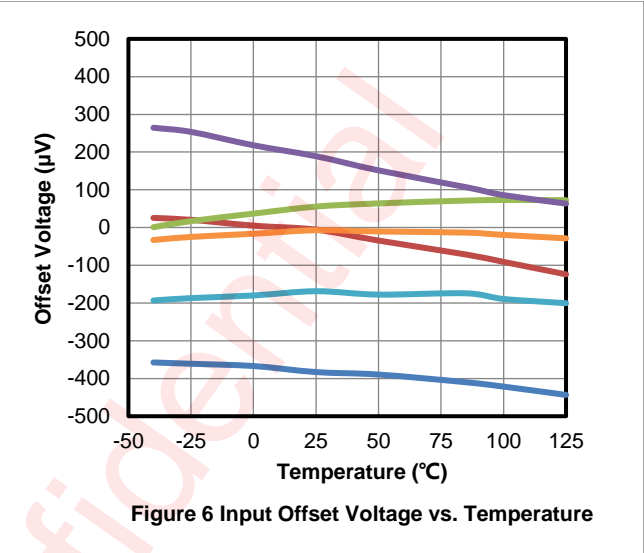
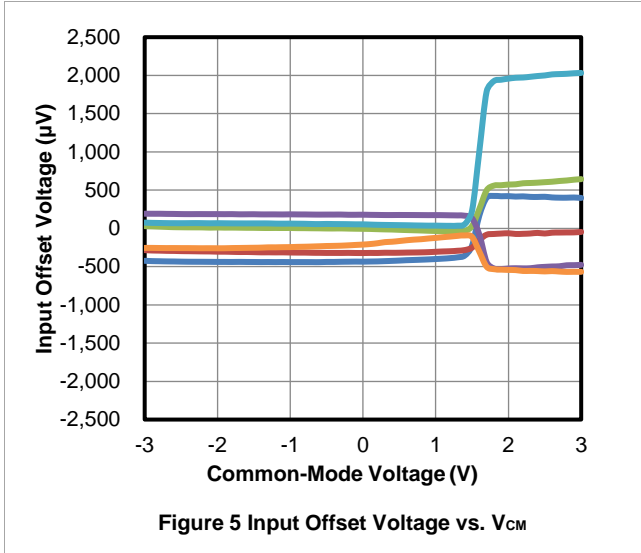
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_S = 5V$		$\pm 0.4$		mV
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ C$ to $125^\circ C$		$\pm 1$		$\mu V/^\circ C$
PSRR	Power-supply rejection ratio	$V_S = 1.8V$ to $5.5V$ , $V_{CM} = V_-$		100		dB
$C_S$	Multiple amplifier channel separation	DC		110		dB
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_{CM} = V_S/2$		$\pm 1$		pA
$I_{OS}$	Input offset current			$\pm 1$		pA
<b>NOISE</b>						
$E_N$	Input voltage noise (peak-to-peak)	$f = 0.1Hz$ to $10Hz$ , $V_S = 5.5V$		3.8		$\mu V_{PP}$
$e_N$	Input voltage noise density	$f = 1kHz$ , $V_S = 5V$		13		$nV/\sqrt{Hz}$
		$f = 10kHz$ , $V_S = 5V$		9		
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range	No phase reversal, rail-to-rail input	(V-) -0.1		(V+) +0.1	V
CMRR	Common-mode rejection ratio	$(V-) - 0.1V < V_{CM} < (V+) - 1.4V$ , $V_S = 1.8V$		94		dB
		$(V-) - 0.1V < V_{CM} < (V+) - 1.4V$ , $V_S = 5.5V$		100		
		$(V-) - 0.1V < V_{CM} < (V+) + 0.1V$ , $V_S = 5.5V$		85		
		$(V-) - 0.1V < V_{CM} < (V+) + 0.1V$ , $V_S = 1.8V$		78		
<b>INPUT CAPACITANCE</b>						
$C_{ID}^{(1)}$	Differential Mode			1		pF
$C_{IC}$	Common Mode			2.5		
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage range		1.8 ( $\pm 0.9$ )		5.5 ( $\pm 2.75$ )	V
$I_Q$	Quiescent current per channel	$V_S = 5.5V$ , $I_O = 0A$		525		$\mu A$

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>OPEN-LOOP GAIN</b>						
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 5.5V, R <sub>L</sub> = 10kΩ, (V <sub>-</sub> ) + 0.05 V < V <sub>O</sub> < (V <sub>+</sub> ) – 0.05V		125		dB
		V <sub>S</sub> = 1.8 V, R <sub>L</sub> = 10kΩ, (V <sub>-</sub> ) + 0.06 V < V <sub>O</sub> < (V <sub>+</sub> ) – 0.06V		115		dB
		V <sub>S</sub> = 1.8V, R <sub>L</sub> = 2kΩ, (V <sub>-</sub> ) + 0.1 V < V <sub>O</sub> < (V <sub>+</sub> ) – 0.1V		115		dB
		V <sub>S</sub> = 5.5V, R <sub>L</sub> = 2kΩ, (V <sub>-</sub> ) + 0.15 V < V <sub>O</sub> < (V <sub>+</sub> ) – 0.15V		130		dB
<b>FREQUENCY RESPONSE CHARACTERISTICS</b>						
GBP	Gain-bandwidth product	V <sub>S</sub> = 5V, G = +1		8		MHz
φ <sub>m</sub>	Phase margin	V <sub>S</sub> = 5V, G = +1		45		°
SR	Slew rate	V <sub>S</sub> = 5V, G = +1		5		V/μs
t <sub>s</sub> <sup>(1)</sup>	Settling time	To 0.1%, V <sub>S</sub> = 5V, V <sub>STEP</sub> = 2V, G = +1, C <sub>L</sub> = 100pF		0.5		μs
THD+N	Total harmonic distortion + noise	V <sub>S</sub> = 5V, V <sub>CM</sub> = 2.5V, V <sub>O</sub> = 0.5V <sub>RMS</sub> , G = +1, f = 1kHz, 80kHz measurement BW		0.0015		%
t <sub>OR</sub>	Overload recovery time	V <sub>S</sub> = 5.5V, V <sub>IN</sub> × gain > V <sub>S</sub>		430		ns
<b>OUTPUT CHARACTERISTICS</b>						
V <sub>OP</sub>	Voltage output swing from positive supply rail	V <sub>S</sub> = 5.5V, R <sub>L</sub> = 10kΩ		5		mV
		V <sub>S</sub> = 5.5V, R <sub>L</sub> = 2kΩ		27		
V <sub>ON</sub>	Voltage output swing from negative supply rail	V <sub>S</sub> = 5.5V, R <sub>L</sub> = 10kΩ		4		mV
		V <sub>S</sub> = 5.5V, R <sub>L</sub> = 2kΩ		20		
I <sub>SC</sub>	Short-circuit current per channel	V <sub>S</sub> = 5.5V		±54		mA
		V <sub>S</sub> = 3.3V		±50		
		V <sub>S</sub> = 1.8V		±13		

(1) Typical value set by simulation only.

## Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_+ = 2.75\text{V}$ ,  $V_- = -2.75\text{V}$ ,  $V_{\text{CM}} = V_S/2$ , and  $V_{\text{OUT}} = V_S/2$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$  unless otherwise noted.



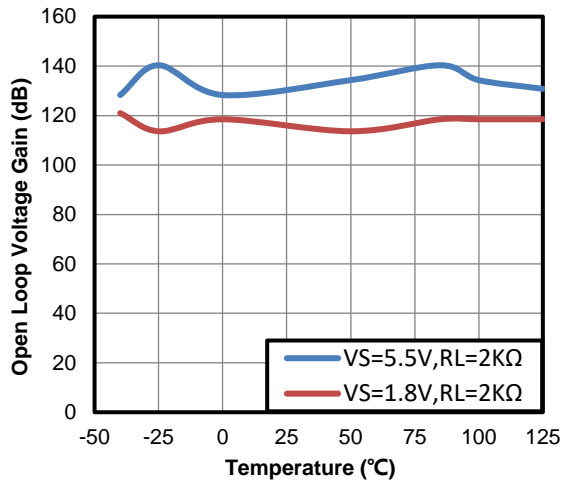


Figure 11 Open Loop Gain vs. Temperature

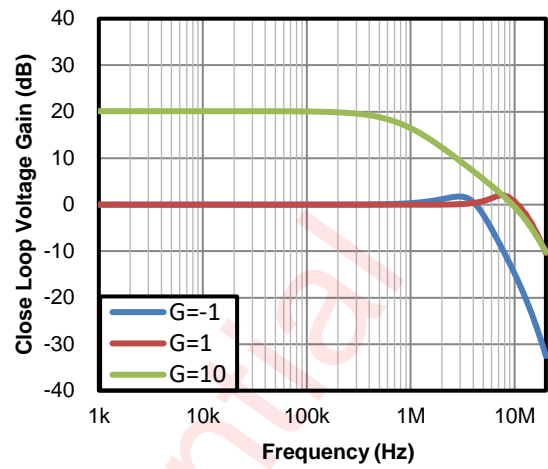


Figure 12 Close Loop Gain vs. Frequency

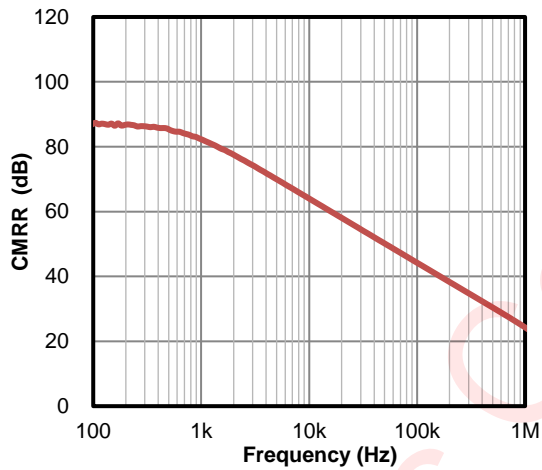


Figure 13 CMRR vs. Frequency

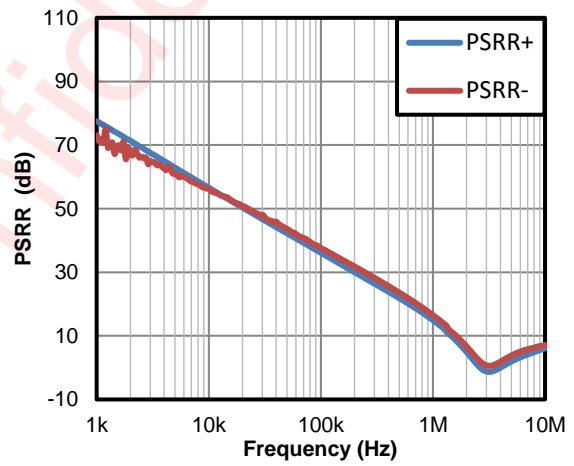


Figure 14 PSRR vs. Frequency

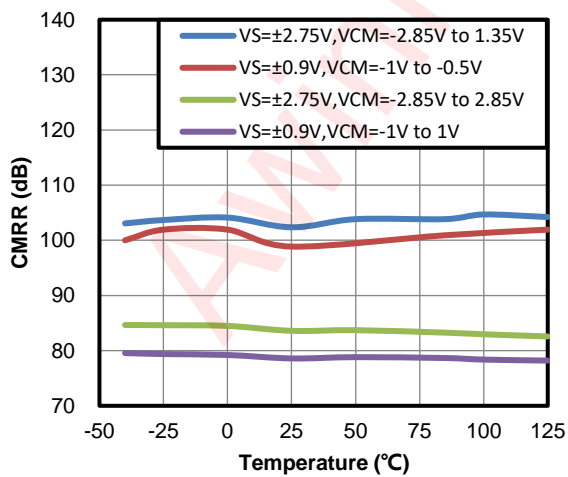


Figure 15 CMRR vs. Temperature

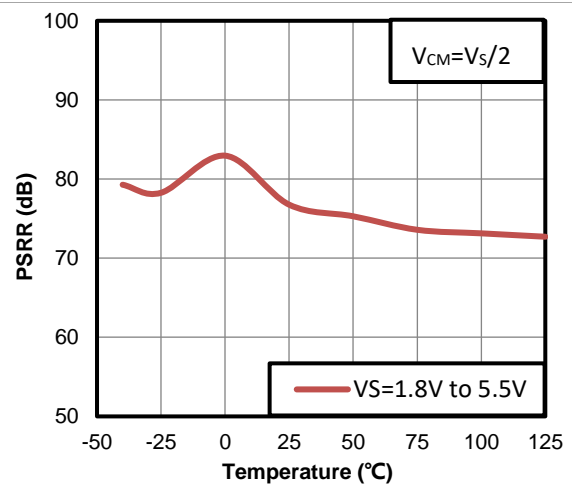


Figure 16 PSRR vs. Temperature

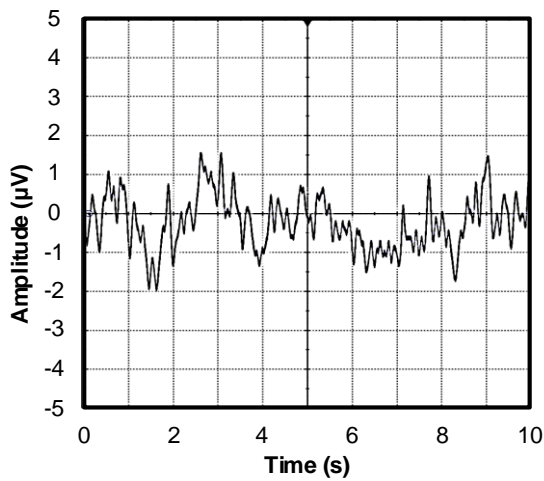


Figure 17 0.1-Hz to 10-Hz Integrated Voltage Noise

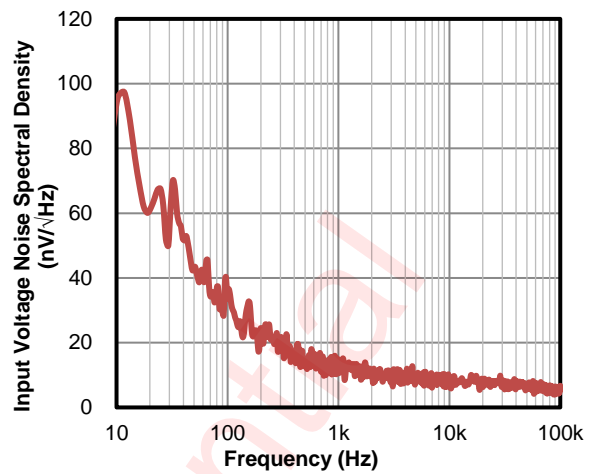


Figure 18 Voltage Noise Spectral Density vs. Frequency

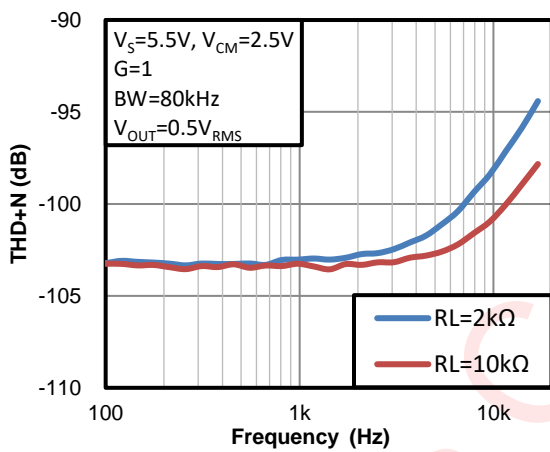


Figure 19 THD + N vs. Frequency

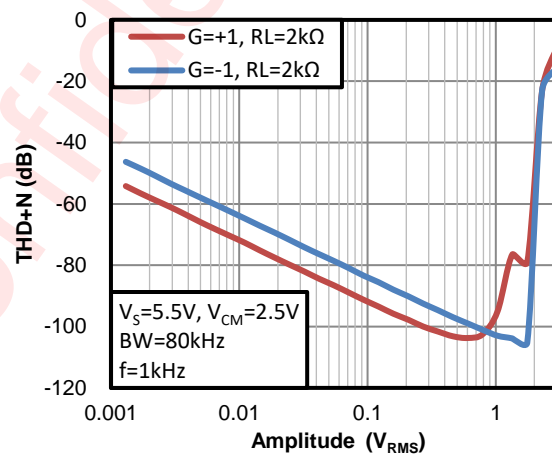


Figure 20 THD + N vs. Amplitude

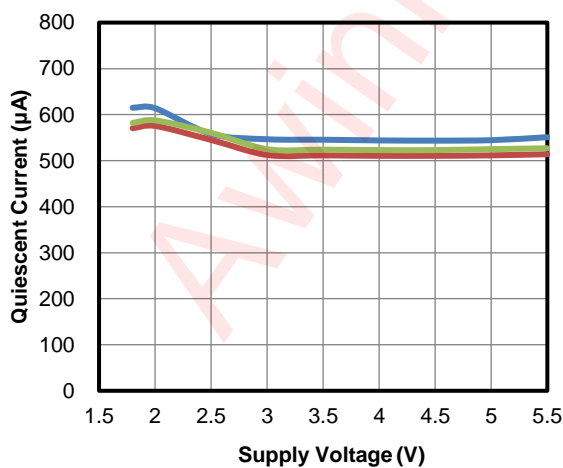


Figure 21 IQ vs. Supply Voltage

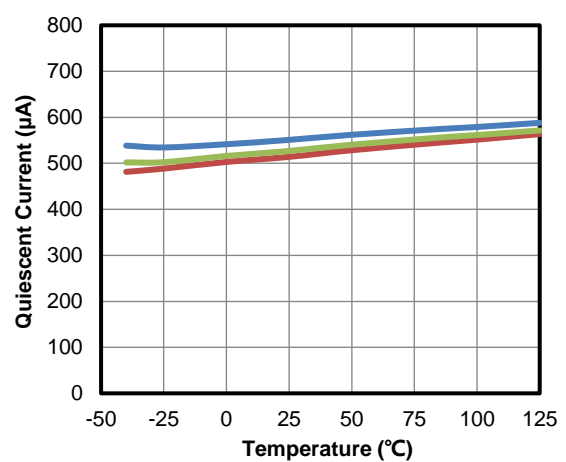


Figure 22 IQ vs. Temperature

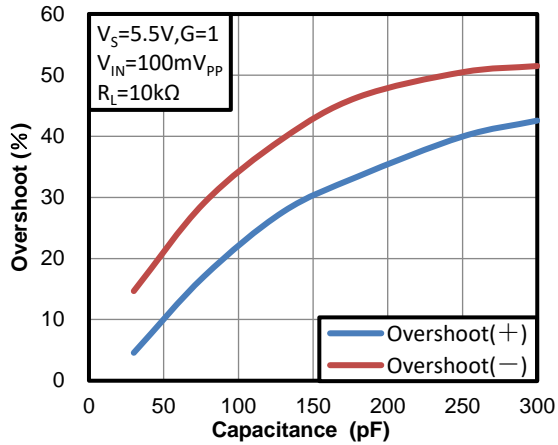


Figure 23 Small Signal Overshoot vs. CL

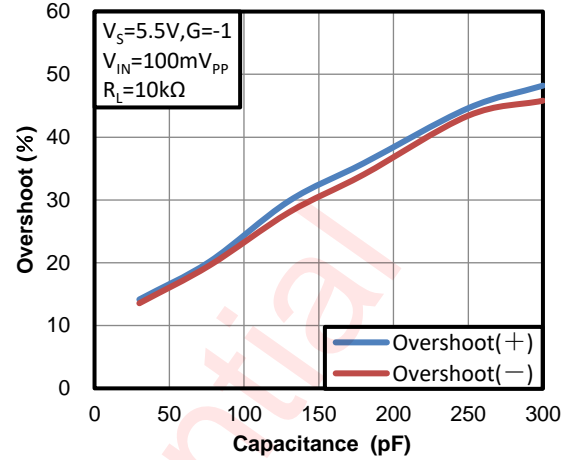


Figure 24 Small Signal Overshoot vs. CL

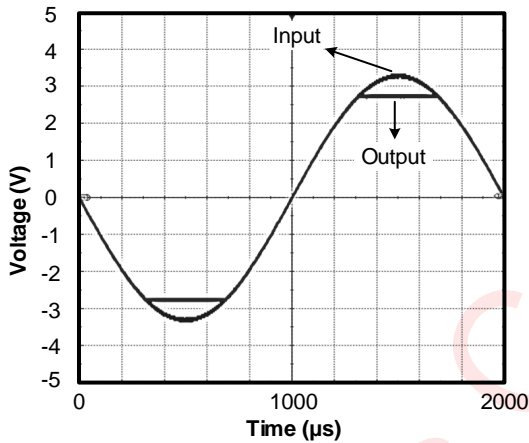


Figure 25 No Phase Reversal

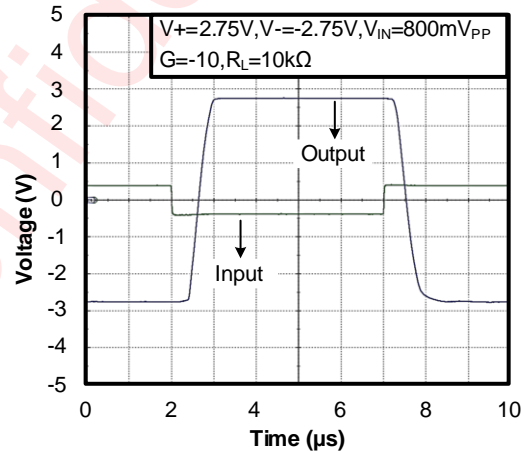


Figure 26 Overload Recovery

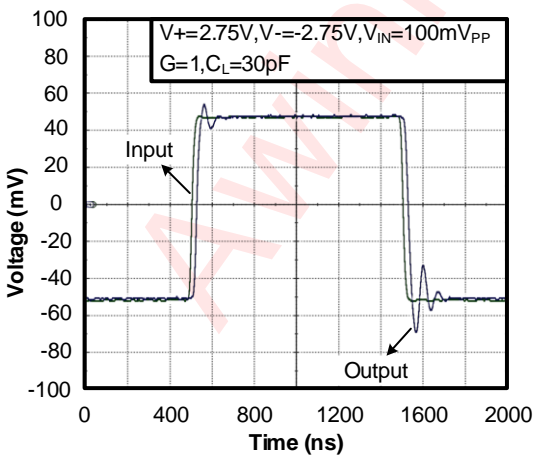


Figure 27 Small Signal Step Response

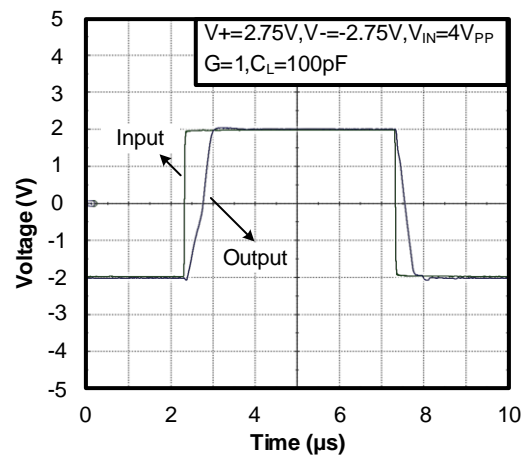


Figure 28 Large Signal Step Response

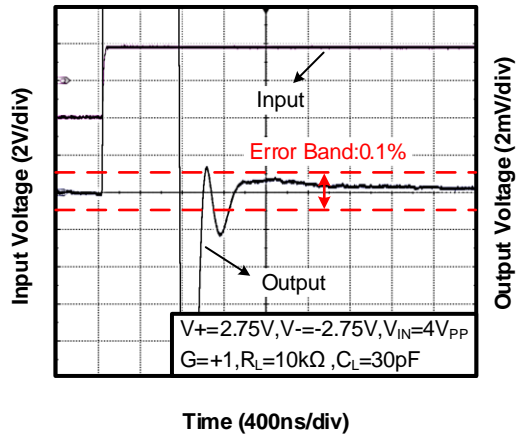


Figure 29 Large Signal Settling Time (Positive)

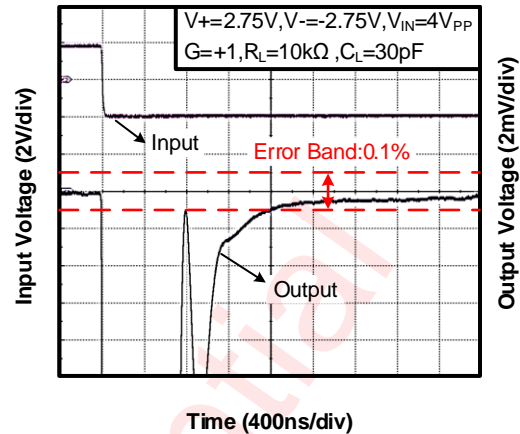


Figure 30 Large Signal Settling Time (Negative)

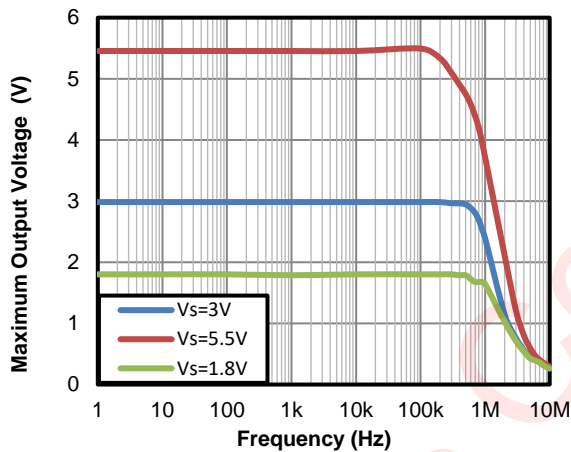


Figure 31  $V_{OUT\_MAX}$  vs. Frequency and  $V_S$

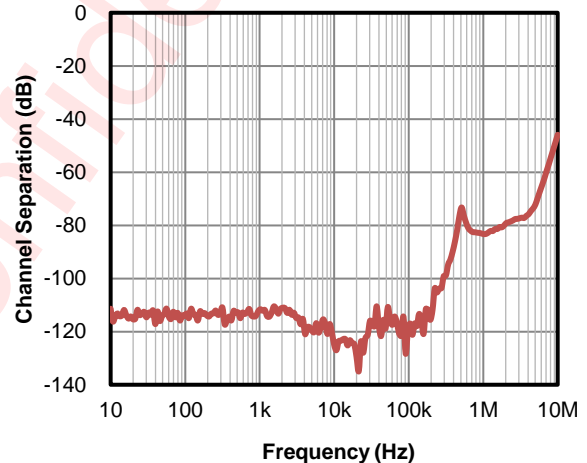


Figure 32 Channel Separation vs. Frequency

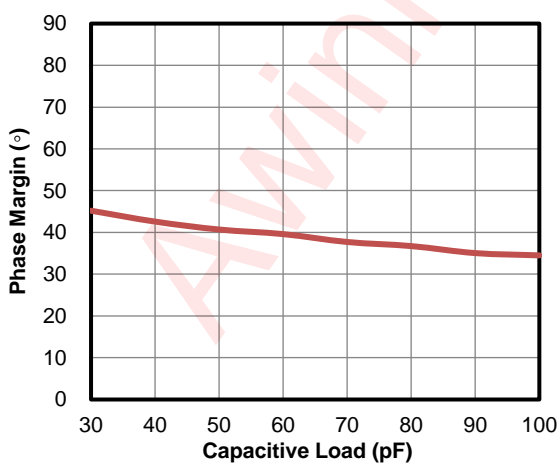


Figure 33 Phase Margin vs. Capacitive Load

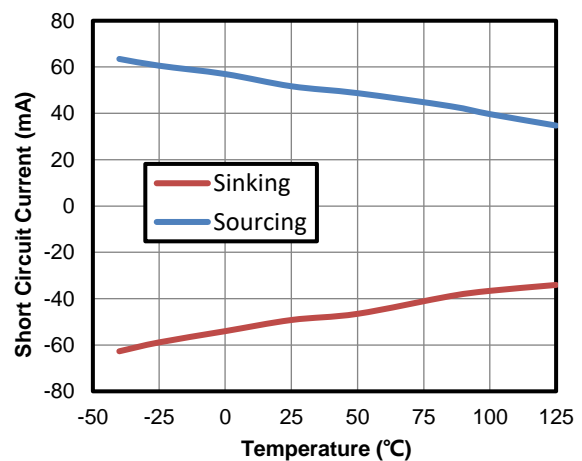


Figure 34 Short Circuit Current vs. Temperature

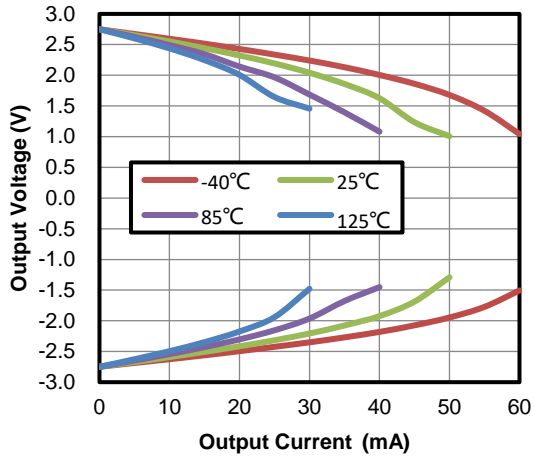


Figure 35 Output Voltage vs. Output Current

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## Detailed Functional Description

The AWS79052 is a dual channel high precision, low-voltage, low-power operational amplifier with rail-to-rail input and output swing capabilities, while drawing 525 $\mu$ A per channel (typical) quiescent current. The device can be unity-gain stable with power supply voltages from 1.8V to 5.5V, which makes it ideal for a wide range of general-purpose applications.

### **Rail-to-Rail Input**

When the input voltage is close to  $V+$ , op-amps with a differential input pair composed of P-channel MOSFETs do not provide a normal output, because a current source enters the linear region and gain is reduced. Similarly, op-amps with a differential input pair composed of N-channel MOSFETs do not provide a normal output when the input voltage is close to  $V-$ . The input voltage range of the AWS79052 can be as high as  $(V+) + 0.1V$  or as low as  $(V-) - 0.1V$  within the full supply voltage range of 1.8V ( $\pm 0.9V$ ) to 5.5V ( $\pm 2.75V$ ). This performance is achieved by using an N-channel input differential pair in parallel with a P-channel differential pair. When input voltage is close to the positive rail, typically  $(V+) - 1.4V$  to  $(V+) + 0.1V$ , the N-channel pair is active, whereas the P-channel pair is active for inputs from  $(V-) - 0.1V$  to approximately  $(V+) - 1.4V$ . Both of the input pairs are on when the input voltage is between typically  $(V+) - 1.2V$  to  $(V+) - 1V$ , which is usually called the transition region. Within this transition region, PSRR, CMRR, offset voltage, and THD can degrade compared to device operation outside this region. Furthermore, the transition region can range from  $(V+) - 1.4V$  to  $(V+) - 1.2V$  on the low end, and up to  $(V+) - 1V$  to  $(V+) - 0.8V$  on the high end with process variations.

### **Rail-to-Rail Output**

A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. Different load conditions change the ability of the amplifier to swing close to the rails. The AWS79052 output stage can drive up to a 2k $\Omega$  load and still swing to within 27mV of the supply rails. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

The rail-to-rail output stage of the amplifier can be modeled as a current source when driving the load toward  $V+$ , and as a current sink when driving the load toward  $V-$ . The limit of this current source/sink varies with supply voltage. The maximum output current is a function of total supply voltage. The output current capability increases as the supply voltage to the amplifier increases. Attention must be paid to keep the junction temperature of the op-amp below 150 $^{\circ}$ C when the output is in continuous short-circuit.

### **Phase Reversal Protection**

Many op amps exhibit a phase reversal when the input is driven beyond its specified input common-mode range, causing the output to reverse into the opposite rail. This condition is most often encountered in noninverting circuits. The AWS79052 has internal phase-reversal protection, therefore, input signals beyond the rails do not cause phase reversal. This performance is shown in Figure 36.

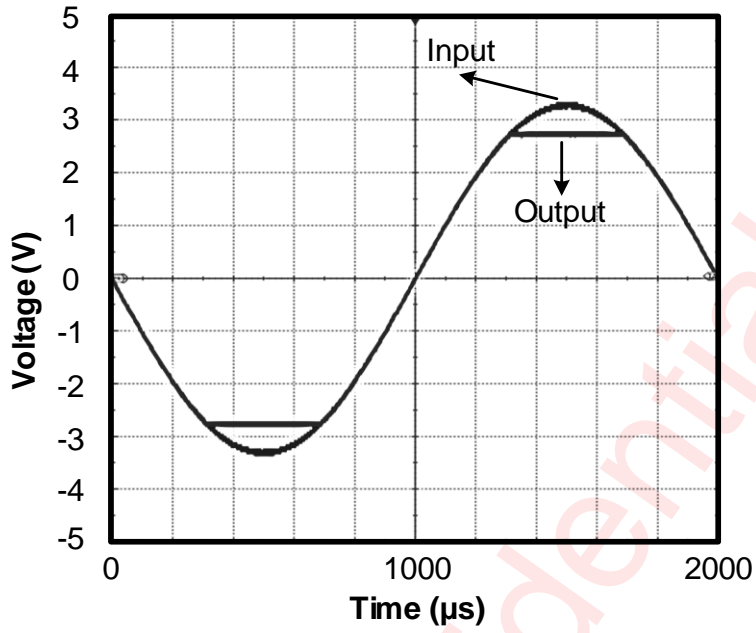


Figure 36 No Phase Reversal

## PCB Layout Consideration

For the optimal performance of the device, good PCB layout practices are needed, here are some guidelines:

1. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1  $\mu\text{F}$  ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces.
2.  $R_i$  is a balance resistor equals to  $R_G \parallel R_F$  to reduce the influence of the input bias current on  $R_G$  and  $R_F$ , which can be shorted when unnecessary.
3. Separate grounding for analog and digital portions of circuitry for better noise suppression. Devote one or more layers on multilayer PCBs to ground planes, which help distribute heat and reduces EMI noise.
4. Run the input traces far away from the  $V_s$  supply or output traces to reduce the parasitic coupling. If not, cross these sensitive traces at a 90 degree instead of being parallel with the noisy trace.
5. The input traces are the most sensitive part of the circuit, so keep the length of input traces as short as possible. Place the external resistors and capacitors as close to device as possible, especially the  $R_F$  and  $R_G$  should be close to the inverting input to minimize the parasitic capacitance.
6. In differential applications, the trace of the inverting input and the non-inverting input should be symmetrical including the same layer, same length, same width and same line spacing.
7. Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process.

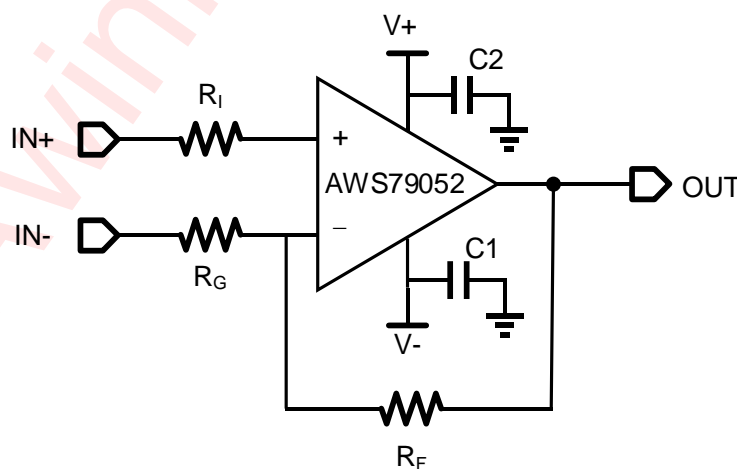
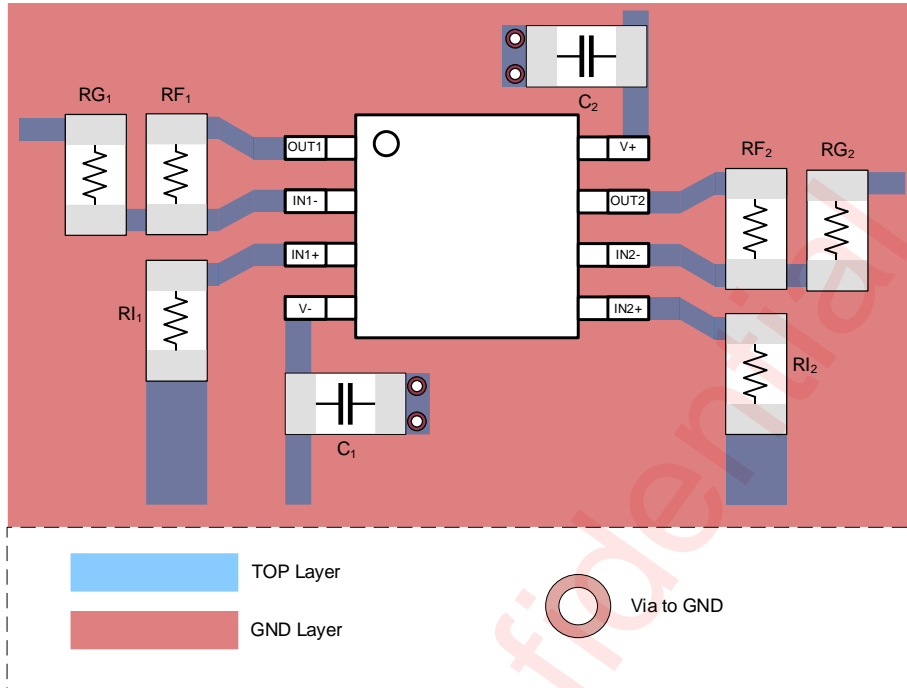


Figure 37 AWS79052 Schematic Example

MSOP - 8L



SOT 23 - 8L

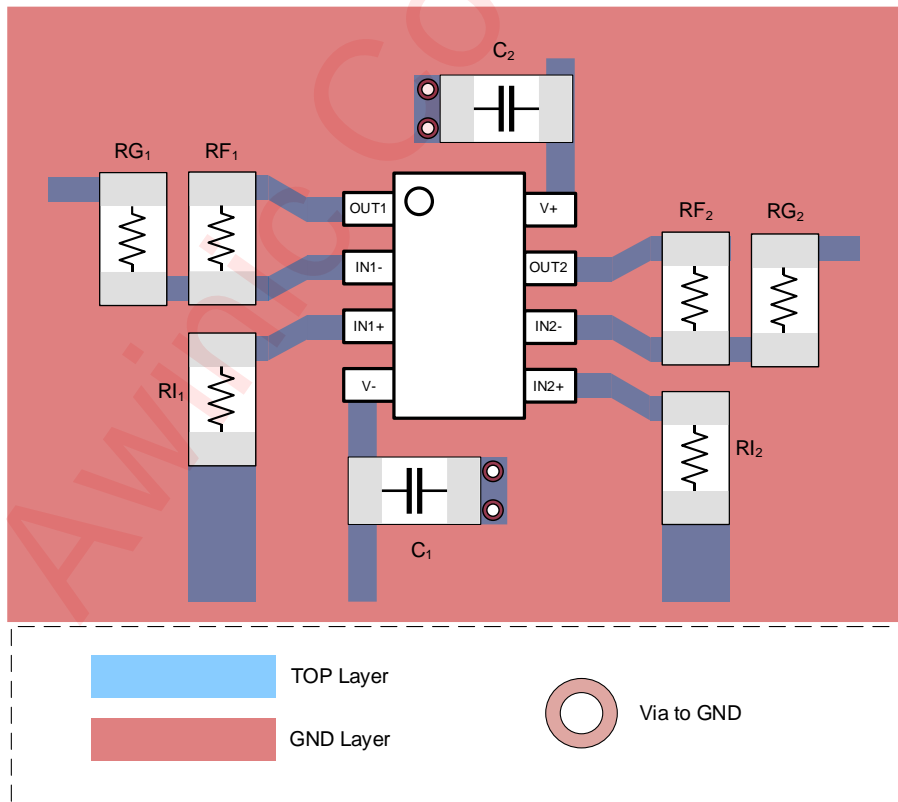


Figure 38 AWS79052 Layout Example

### PCB Surface Leakage Current

In high precision applications where input bias current is critically concerned, the leakage current on PCB surface caused by dust or humidity may badly reduce the output accuracy. In this case, a multi-layer PCB is recommended for routing the input traces under the PCB surface. In addition, the usage of a guard ring can significantly reduce the leakage current to sensitive node. A conductive ring surrounding the inputs should be connected to a low impedance node with the same voltage as the inputs, so this ring will absorb the leakage current from high voltage nodes around the inputs.

For non-inverting gain application, connect the IN+ to the input with traces not touching the PCB surface, for example, routing in second layer in Figure 39. Then surround the IN+ pin with a guard ring which is connected to IN-, thus biasing the guard ring with the same voltage of the common mode input voltage.

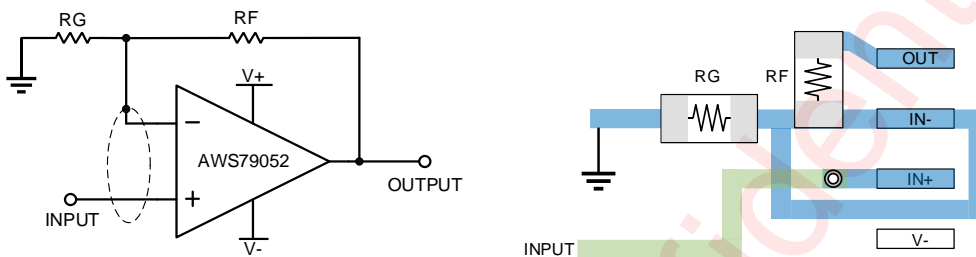


Figure 39 Non-inverting Gain Application Schematic and Layout Example

Similarly, for inverting gain application, connect the IN- to the input with traces not touching the PCB surface, for example, striding over with the input resistor in Figure 40. Then surround the IN- pin with a guard ring which is connected to IN+, thus biasing the guard ring with the reference voltage of AWS79052.

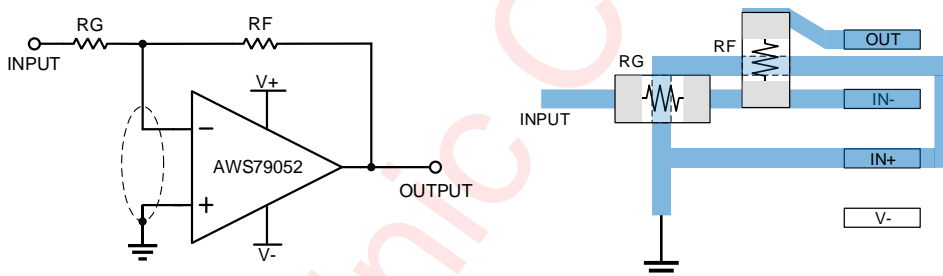
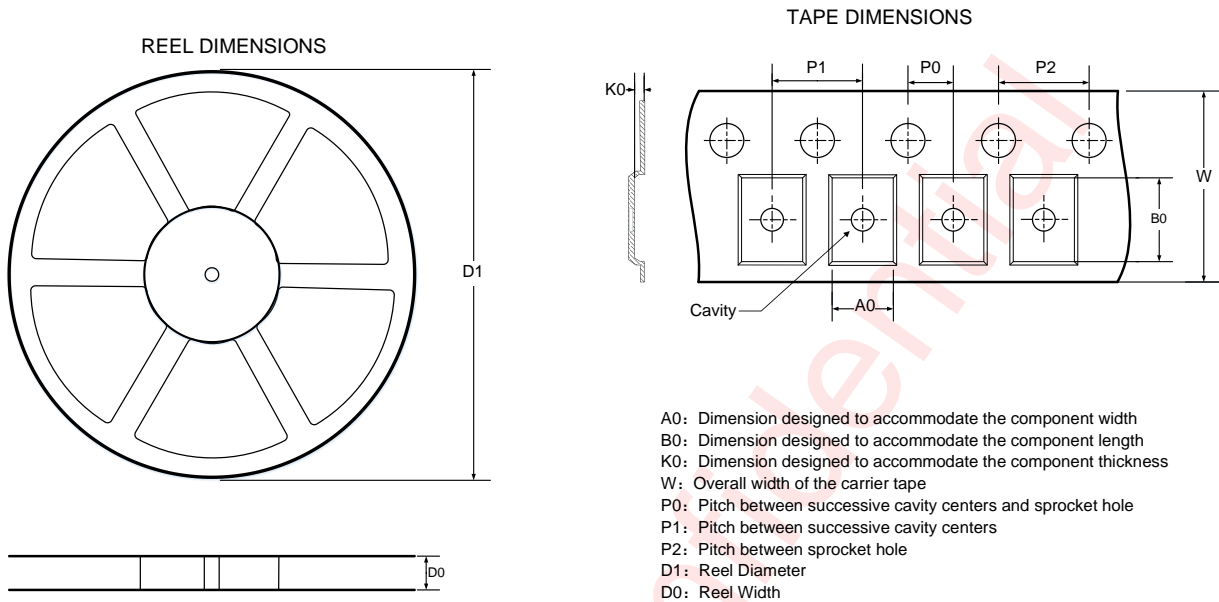


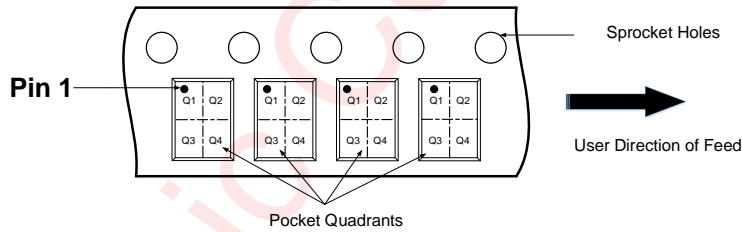
Figure 40 Inverting Gain Application Schematic and Layout Example

## Tape And Reel Information

MSOP - 8L



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



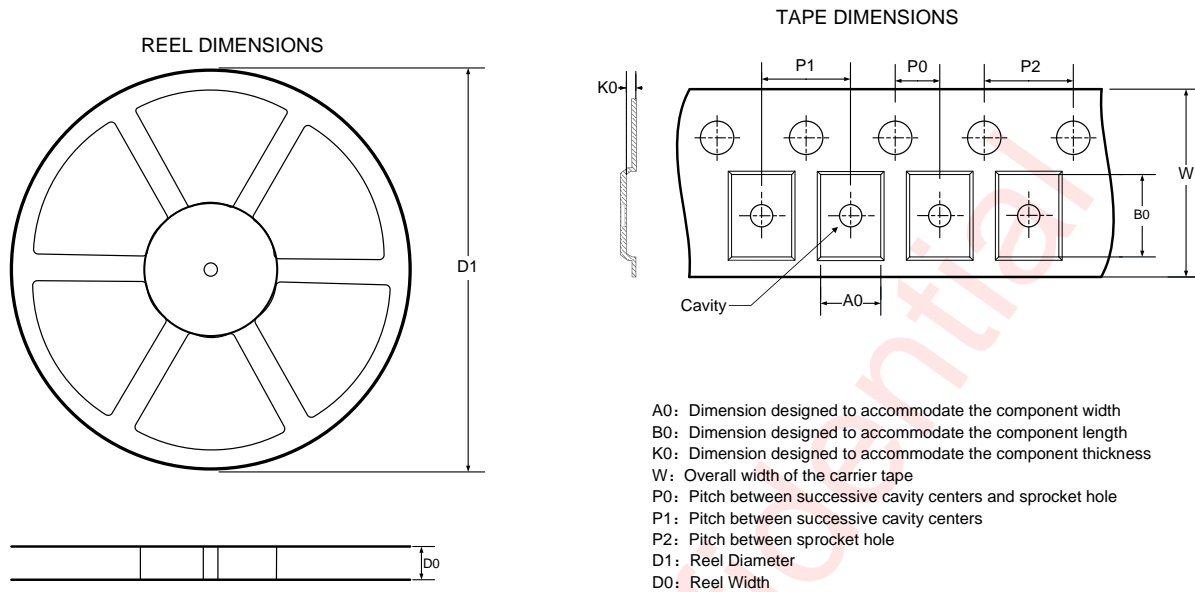
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

### DIMENSIONS AND PIN1 ORIENTATION

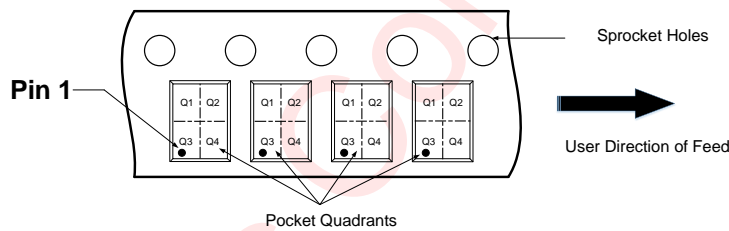
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.25	3.35	1.25	2	8	4	12	Q1

All dimensions are nominal

SOT 23 - 8L



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

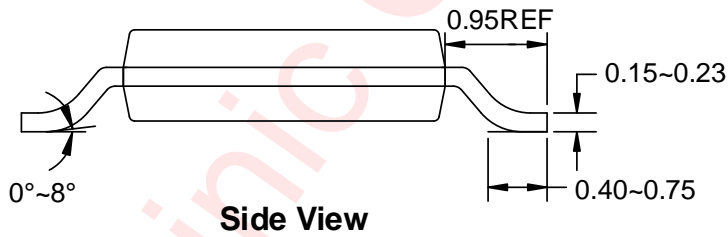
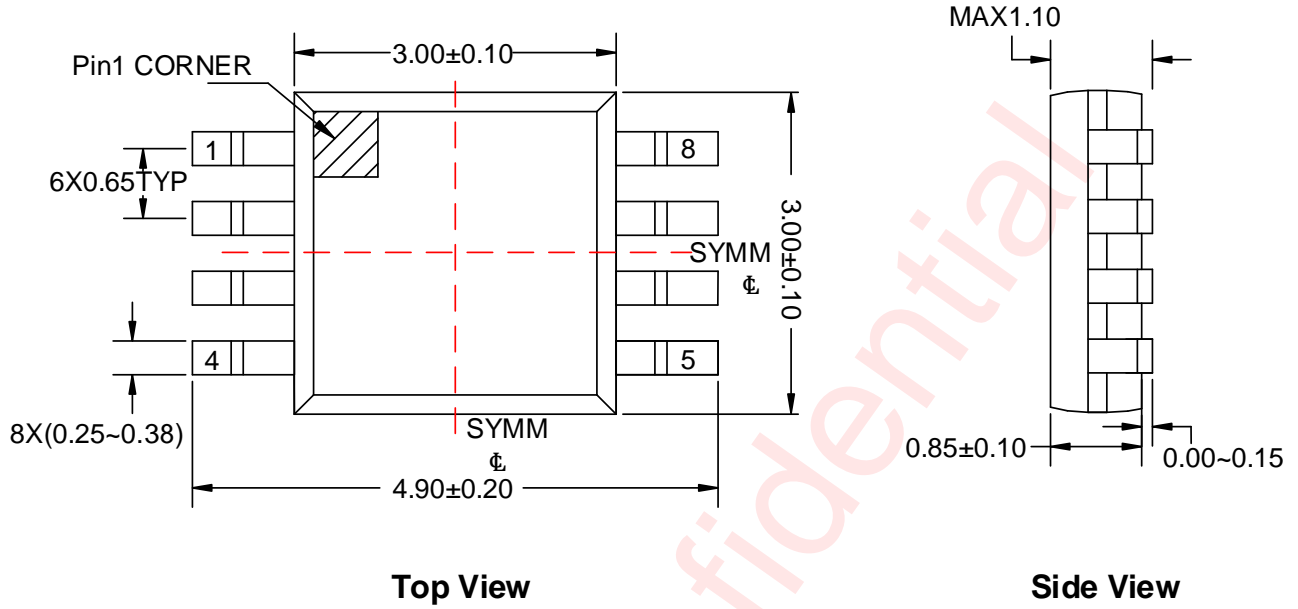
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	3.23	3.17	1.37	2	4	4	8	Q3

All dimensions are nominal

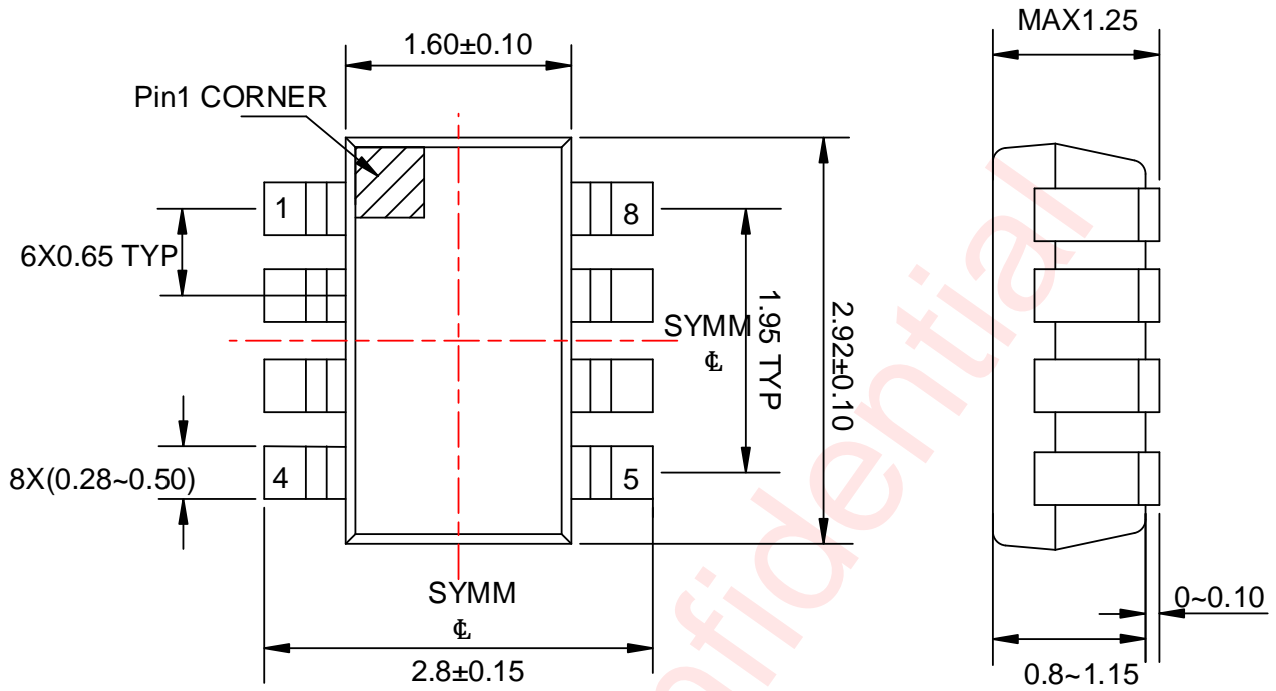
### Package Description

MSOP - 8L



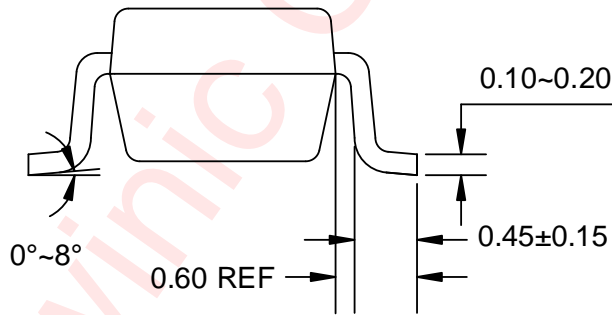
Unit: mm

SOT 23 - 8L



Top View

Side View

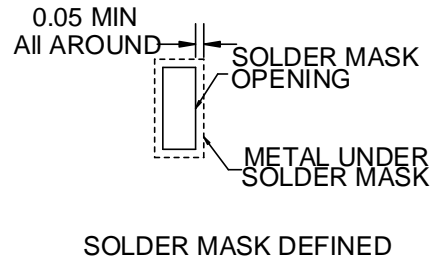
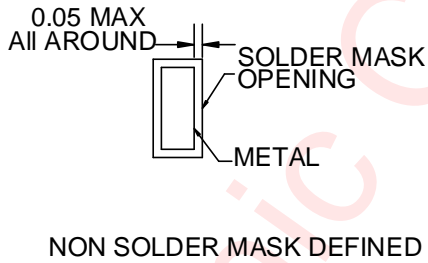
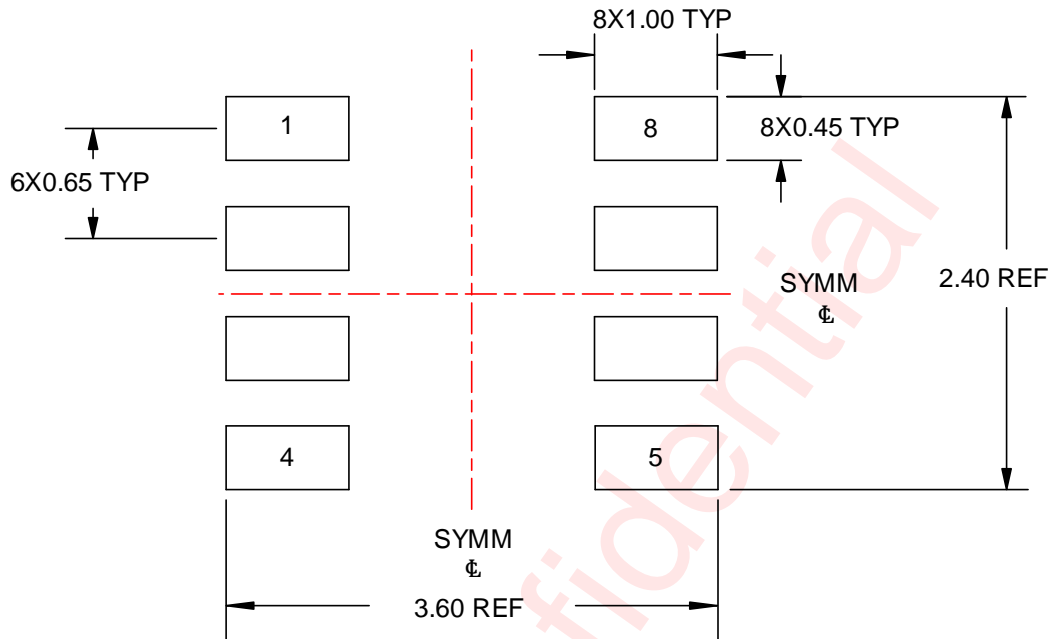


Side View

Unit: mm



SOT 23 - 8L



Unit: mm

## Revision History

Version	Date	Change Record
V1.0	Jun. 2022	Official released
V1.1	Feb.2023	<ol style="list-style-type: none"> <li>1. Added SOT 23 - 8L package information to <i>General Description</i> .(P1)</li> <li>2. Added SOT 23 - 8L pin configuration to <i>Pin Configuration And Top Mark</i> . (P 2)</li> <li>3. Added SOT 23 - 8L information table to <i>Ordering Information</i> .(P5)</li> <li>4. Added SOT 23 - 5L thermal metrics to <i>Thermal Information</i> .(P7)</li> <li>5. Added SOT 23 - 8L layout example of Figure 32 to <i>PCB Layout Consideration</i> .(P19)</li> <li>6. Added SOT 23 - 8L information to <i>Tape And Reel Information</i> .(P22)</li> <li>7. Added SOT 23 - 8L information to <i>Package Description</i> .(P24)</li> <li>8. Added SOT 23 - 8L information to <i>Land Pattern Data</i> .(P26)</li> </ol>
V1.2	Dec.2023	<ol style="list-style-type: none"> <li>1. Update <i>ESD Rating and Latch up</i> .(P6)</li> <li>2. Added typical value of <math>dV_{os}/dT</math> in <i>Electrical Characteristics</i>. (P8)</li> <li>3. Added SOT 23 - 8L and MSOP-8L to <i>Device Information</i>. (P1)</li> </ol>
V1.3	Apr.2025	<ol style="list-style-type: none"> <li>1. Update BODY SIZE(NOM) in <i>Device Information</i>. (P1)</li> <li>2. Update MSOP - 8L information in <i>Package Description</i>. (P23)</li> <li>3. Update SOT23 - 8L information in <i>Package Description</i>. (P24)</li> </ol>

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