

4-Channel High-Performance LDO PMIC With 1.2V I/O

Features

- VIN1 input voltage range: 0.6V to 2.2V
- DVDD1/2 output voltage range: 0.6V~1.8V
- DVDD1/2 dropout voltage: 135mV
($I_{OUT}=1.2A$, 1.2V output)
- DVDD1/2 output drive capability: 1.2A(Typ.)
The max of DVDD1/2 output drive capability can be set to 1.5A by config I²C
- VIN2 input voltage range: 2.5V to 5.5V
- AVDD1/2 output voltage range: 1.2V~4.3V
- AVDD1/2 dropout voltage: 125mV
($I_{OUT}=400mA$, $V_{OUT}=2.8V$)
- AVDD1/2 output drive capability: 400mA(Typ.)
The max of AVDD1/2 output drive capability can be set to 600mA by config I²C
- AVDD1/2 power supply rejection ratio: typical 94dB ($I_{OUT}=50mA$, 2.8V output, freq=1kHz)
- AVDD1/2 noise: typical 9 μ Vrms ($I_{OUT}=30mA$, BW=10Hz to 100KHz)
- Quiescent current: typical: 65 μ A
- Shutdown current: typical: 0.75 μ A
- Available with 1.2V I/O
- Build in 1.9V falling UVLO protection
- Build in OCP, SCP,OTP protection
- Programmable I²C Address
- DFN 2mm × 2mm × 0.75mm-10L package

Applications

Digital camera
Smart phone
Camera module
Silicon-Oxygen Anode Battery

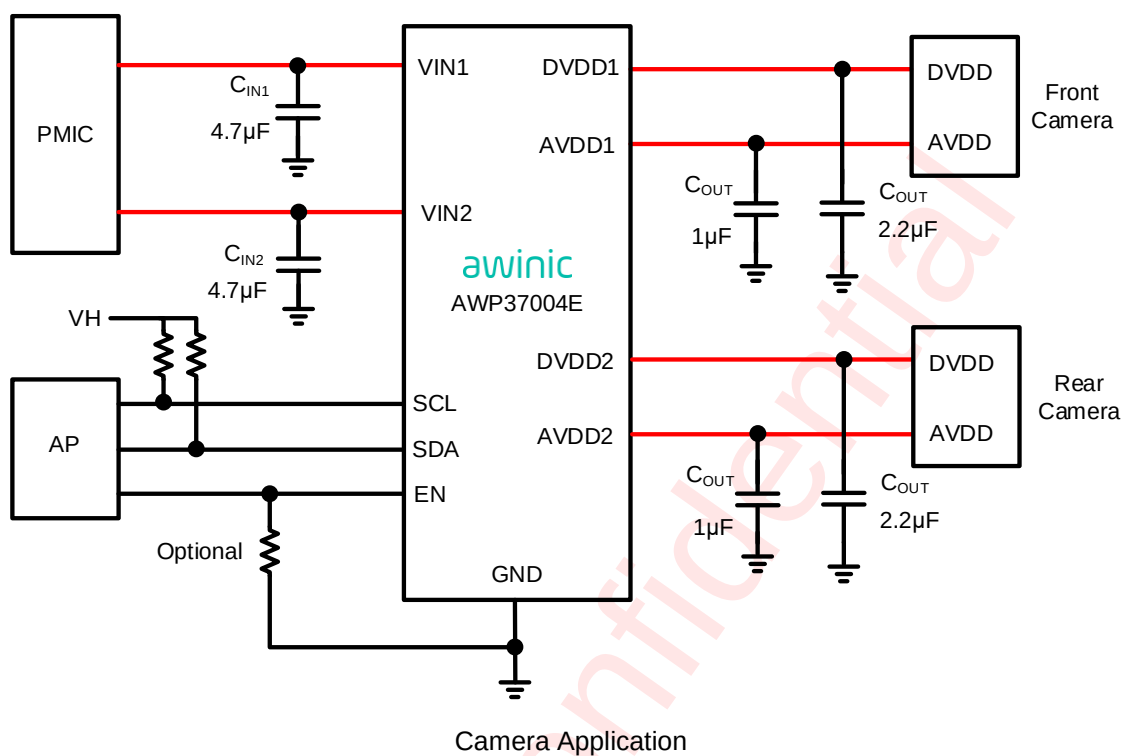
General Description

AWP37004E is a 4-ch integrated LDO PMIC for camera applications include 2-ch DVDD, 2-ch AVDD, with 1MHz high speed I²C interface, the function setting is flexible such as power sequence, output discharge. The chip enable control support EN pin control and I²C control.

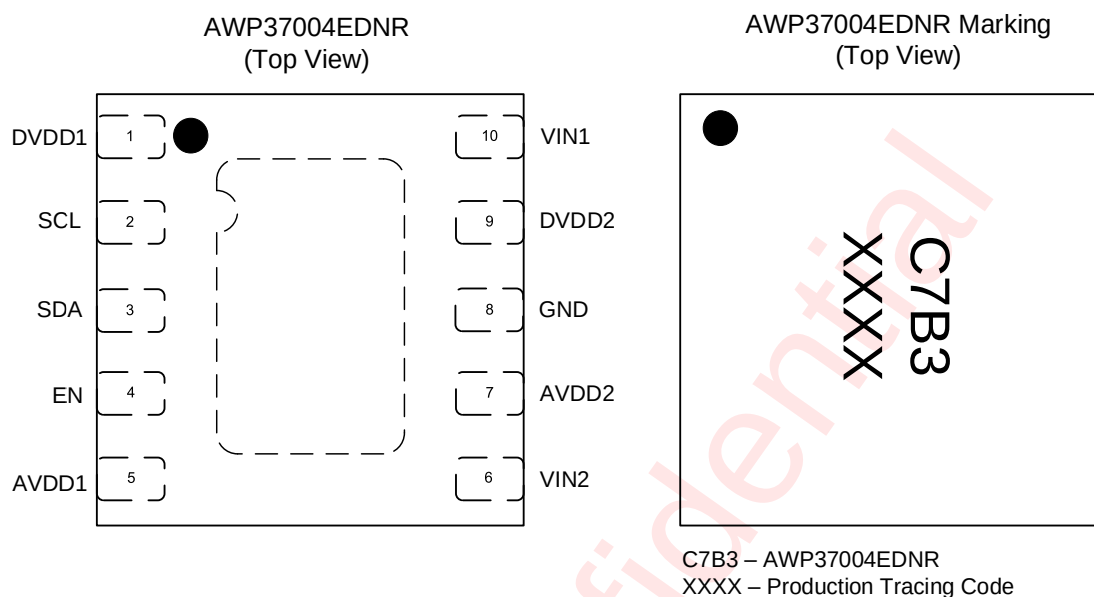
Due to high load current and lower working voltage of DVDD, AWP37004E used N-MOSFET LDO architecture without charge pump for 2-ch DVDD LDO. DVDD LDO input source is VIN1 and VIN2 is the bias voltage. Ultra-low dropout voltage of DVDD LDOs is designed for high efficiency and lower power dissipation purpose.

For the AVDD, AWP37004E used P-MOSFET LDO architecture. The input source is VIN2. Due to high performance requirement of AVDD, AWP37004E's AVDD used special circuit design and optimized pin assignment which is easy for system PCB layout.

Typical Application Circuit



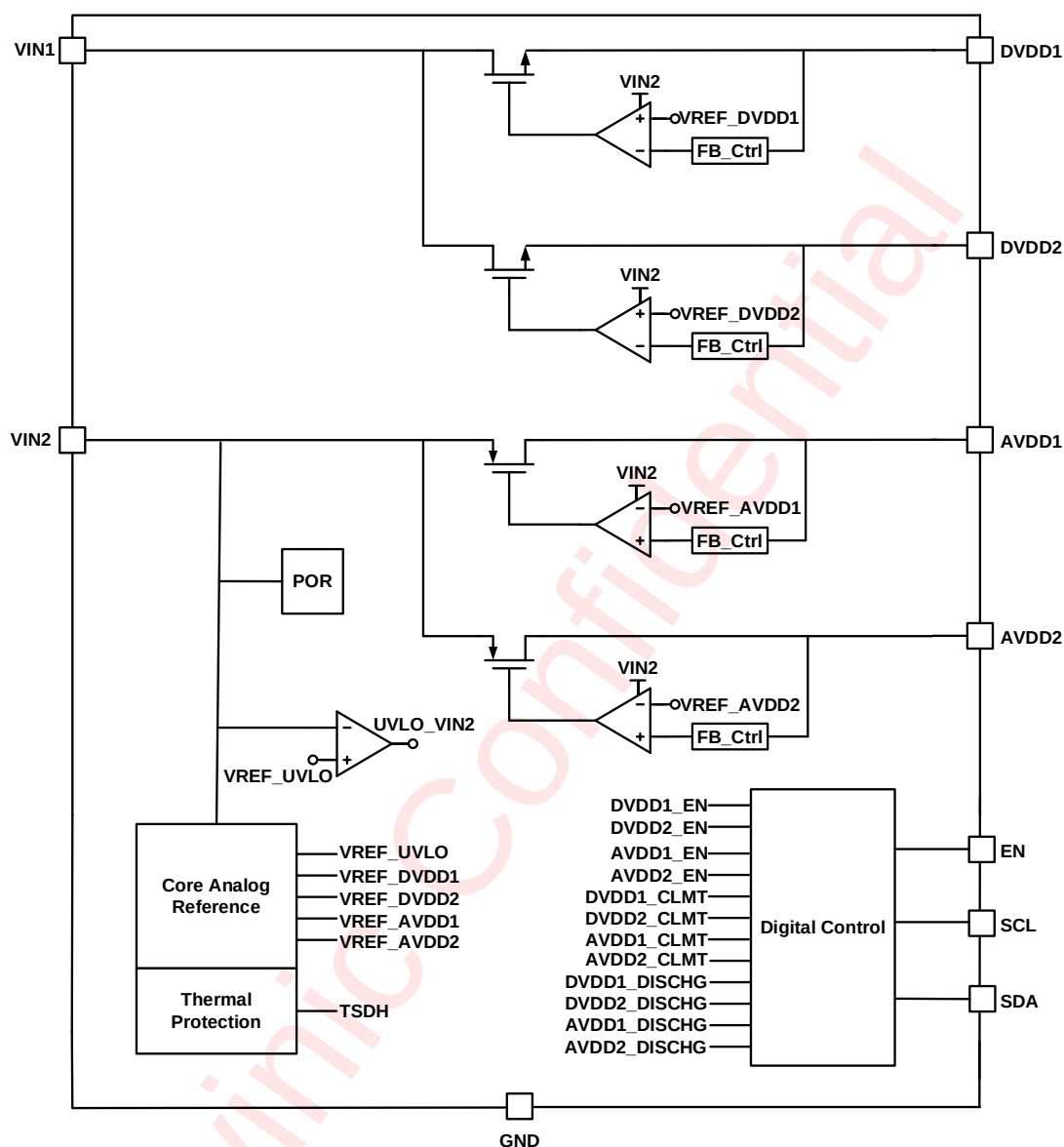
Pin Configuration And Top Mark



Pin Definition

No.	NAME	DESCRIPTION
1	DVDD1	DVDD1 output channel. Connecting a 2.2 μ F or more ceramic capacitor at the output pin.
2	SCL	I ² C data and clock interface.
3	SDA	
4	EN	Enable control pin, tie high to enable the chip, tie low if I ² C control used.
5	AVDD1	AVDD1 output channel. Connecting a 1 μ F or more ceramic capacitor at the output pin.
6	VIN2	DVDD1 and DVDD2 bias input pin, AVDD1 and AVDD2 power supply input pin. Connecting a 4.7 μ F or more ceramic capacitor at the input pin.
7	AVDD2	AVDD2 output channel. Connecting a 1 μ F or more ceramic capacitor at the output pin.
8	GND	Ground pin.
9	DVDD2	DVDD2 output channel. Connecting a 2.2 μ F or more ceramic capacitor at the output pin.
10	VIN1	DVDD1 and DVDD2 power supply input pin. Connecting a 4.7 μ F or more ceramic capacitor at the input pin.

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP37004EDNR	-40°C ~ 85°C	DFN 2mm×2mm -10L	C7B3	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
Input voltage range VIN1 and VIN2	-0.3V to 6.5V
Enable control voltage range	-0.3V to 6.5V
Output voltage range	-0.3V to VIN+0.3V, max. 6.5V
Junction-to-ambient thermal resistance θ_{JA} ^(NOTE2)	88°C/W
Junction-to-board thermal resistance θ_{JB} ^(NOTE2)	8°C/W
Junction-to-case thermal resistance θ_{JC} ^(NOTE2)	120°C/W
Maximum operating junction temperature T _{JMAX}	150°C
Storage temperature T _{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM (Human body model) ^(NOTE3)	±2kV
CDM(Charged device model) ^(NOTE4)	±1.5kV
Latch-Up	
Latch-Up ^(NOTE5)	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2024.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2022.

NOTE5: Test Condition: JESD78F.02-2023.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V _{IN1}	Input voltage	0.6		2.2	V
V _{IN2}	Input voltage	2.5		5.5	V
T _J	Operating free-air temperature range	-40	25	85	°C

Electrical Characteristics

$V_{IN1}=1.35V$, $V_{IN2}=3.3V$, $V_{EN}>0.84V$, $I_{OUT}=1mA$, $C_{IN}=4.7\mu F$, $C_{OUT_AVDD}=1\mu F$, $C_{OUT_DVDD}=2.2\mu F$, $T_A=25^{\circ}C$
(unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Whole device					
I_{SD}	Shutdown Current	$V_{CE}<0.36V$ or shut down by I ² C	0.75	1.5	μA
I_Q	Quiescent Current	$I_{OUT}=0mA$, $V_{EN}>0.84V$ or all channels enabled by I ² C	65	100	μA
V_{ENH}	EN Input Voltage "H"	$-40^{\circ}C \leq T_A \leq 85^{\circ}C$	0.84		V
V_{ENL}	EN Input Voltage "L"	$-40^{\circ}C \leq T_A \leq 85^{\circ}C$		0.36	V
R_{EN}	EN Pull Down Resistance	$V_{EN}=0V$ to 5.5V	10		M Ω
R_{DISC}	Auto Discharge Resistance	$V_{EN}<0.36V$, $I_{OUT}=0mA$, for AVDD	430		Ω
		$V_{EN}<0.36V$, $I_{OUT}=0mA$, for DVDD REG0x02[6]=1	270		Ω
		$V_{EN}<0.36V$, $I_{OUT}=0mA$, for DVDD REG0x02[6]=0	540		Ω
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising	150		$^{\circ}C$
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling	120		$^{\circ}C$
V_{UVLO}	Under Voltage Lock-out	VIN2 Falling	1.9		V
V_{UVLO_HYS}	UVLO Hysteresis	VIN2 Rising	0.1		V
I²C Logic					
V_{IH}	Input Voltage "H"	$-40^{\circ}C \leq T_A \leq 85^{\circ}C$	0.84		V
V_{IL}	Input Voltage "L"	$-40^{\circ}C \leq T_A \leq 85^{\circ}C$		0.36	V

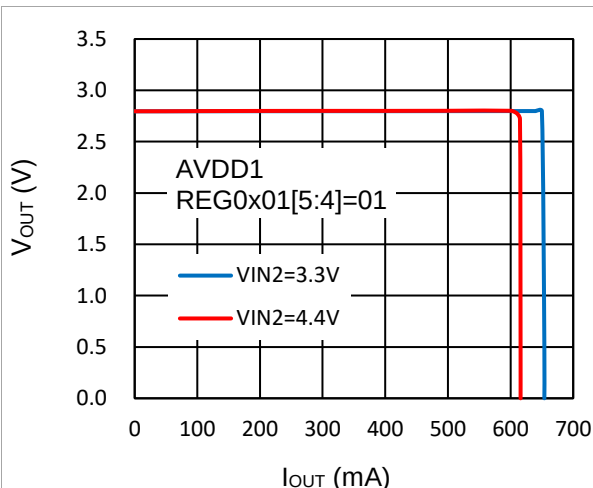
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DVDD1 and DVDD2						
V_{IN1_RANGE}	Input Supply Range		0.6		2.2	V
V_{OUT_ACC}	Output Voltage Accuracy	$T_A=25^{\circ}C$	-1		1	%
V_{OUT_RANGE}	Output Voltage Range		0.6		1.8	V
$V_{OUT_DEFAULT}$	Default Output Voltage			1.2		V
Load_Reg	Load Regulation	$1mA \leq I_{OUT} \leq 1.2A$		1		mV
Line_Reg	Line Regulation	$V_{IN2}=3.3V, 1.25V \leq V_{IN1} \leq 2V, I_{OUT}=1mA$		0.1		mV
		$V_{IN1}=1.35V, 3V \leq V_{IN2} \leq 4V, I_{OUT}=1mA$		0.5		mV
$V_{dropout}$	Dropout Voltage ⁽¹⁾	$I_{OUT}=1.2A, V_{OUT(SET)}=1.2V$ $V_{IN2}=3.3V$		135		mV
PSRR	Power Supply Ripple Rejection	$I_{OUT}=10mA, f=1kHz,$ $V_{IN1}=1.5V+0.1V_{PP}, V_{IN2}=4.4V,$ $V_{OUT(SET)}=1.2V$		76		dB
		$I_{OUT}=10mA, f=1kHz,$ $V_{IN2}=4.4V+0.2V_{PP}, V_{IN1}=1.5V,$ $V_{OUT(SET)}=1.2V$		65		dB
V_N	Output Voltage Noise	$I_{OUT}=30mA,$ $BW=10Hz \text{ to } 100kHz$		90		μV_{rms}
I_{CL}	Output Current Limit	$V_{OUT}=90\% \cdot V_{OUT(SET)}$ DVDD1: REG0x01[1:0]=00 DVDD2: REG0x01[3:2]=00	1000	1360		mA
		$V_{OUT}=90\% \cdot V_{OUT(SET)}$ DVDD1: REG0x01[1:0]=01 (default) DVDD2: REG0x01[3:2]=01 (default)	1200	1500		mA
		$V_{OUT}=90\% \cdot V_{OUT(SET)}$ DVDD1: REG0x01[1:0]=10 DVDD2: REG0x01[3:2]=10	1300	1640		mA
		$V_{OUT}=90\% \cdot V_{OUT(SET)}$ DVDD1: REG0x01[1:0]=11 DVDD2: REG0x01[3:2]=11	1500	1780		mA
I_{SC}	Short Current Limit	$V_{OUT}=0V$		380		mA
VTC	Output Voltage Temperature Coefficient	$-40^{\circ}C \leq T_A \leq 85^{\circ}C$		± 50		ppm/ $^{\circ}C$

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
AVDD1 and AVDD2						
V_{IN2_RANGE}	Input Supply Range		2.5		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy	$T_A=25^{\circ}C$	-1		1	%
V_{OUT_RANGE}	Output Voltage Range		1.2		4.3	V
$V_{OUT_DEFAULT}$	Default Output Voltage			2.8		V
Load_Reg	Load Regulation	$1mA \leq I_{OUT} \leq 400mA$, $V_{OUT(SET)}=2.8V$ $V_{IN1}=1.35V$, $V_{IN2}=3.3V$		2		mV
Line_Reg	Line Regulation	$V_{IN1}=1.35V$, $V_{OUT(SET)}=2.8V$, $3.0V \leq V_{IN2} \leq 4.0V$, $I_{OUT}=1mA$		0.1		mV
$V_{dropout}$	Dropout Voltage ⁽¹⁾	$I_{OUT}=400mA$, $V_{OUT(SET)}=2.8V$		125		mV
PSRR	Power Supply Ripple Rejection	$I_{OUT}=50mA$, $V_{IN2}=4.4V+0.2V_{PP}$, $V_{IN1}=1.5V$, $V_{OUT(SET)}=2.8V$	$f=1kHz$	94		dB
			$f=10kHz$	94		
			$f=100kHz$	77		
			$f=1MHz$	42		
V_N	Output Voltage Noise	$I_{OUT}=30mA$, $BW=10Hz$ to $100kHz$		9		μV_{rms}
I_{CL}	Output Current Limit	$V_{OUT}=90\% \cdot V_{OUT(SET)}$ AVDD1: REG0x01[5:4]=00 AVDD2: REG0x01[7:6]=00	300	400		mA
		$V_{OUT}=90\% \cdot V_{OUT(SET)}$ AVDD1: REG0x01[5:4]=01 (default) AVDD2: REG0x01[7:6]=01 (default)	400	500		mA
		$V_{OUT}=90\% \cdot V_{OUT(SET)}$ AVDD1: REG0x01[5:4]=10 AVDD2: REG0x01[7:6]=10	500	600		mA
		$V_{OUT}=90\% \cdot V_{OUT(SET)}$ AVDD1: REG0x01[5:4]=11 AVDD2: REG0x01[7:6]=11	600	700		mA
VTC	Output Voltage Temperature Coefficient	$-40^{\circ}C \leq T_A \leq 85^{\circ}C$		± 50		ppm/ $^{\circ}C$

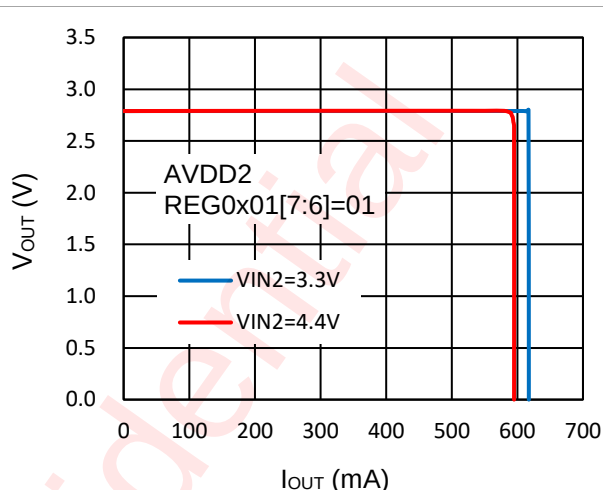
(1) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 98% of its nominal value.

Typical Characteristics

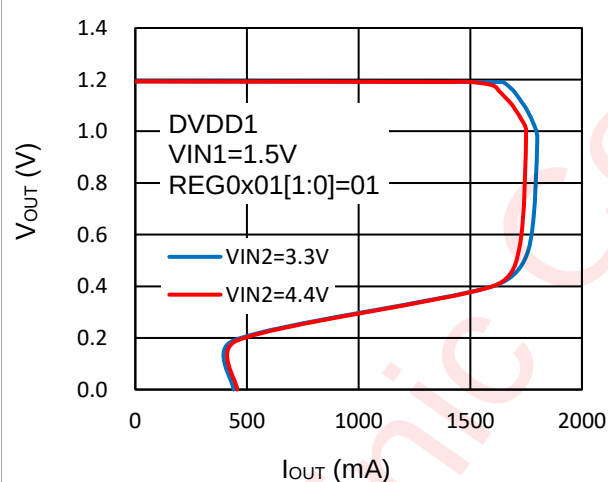
$V_{IN1}=1.35V$, $V_{IN2}=3.3V$, $V_{AVDD1/2}=2.8V$, $V_{DVDD1/2}=1.2V$, $C_{IN}=4.7\mu F$, $C_{OUT_AVDD}=1\mu F$, $C_{OUT_DVDD}=2.2\mu F$, $T_A=25^\circ C$, unless otherwise noted.



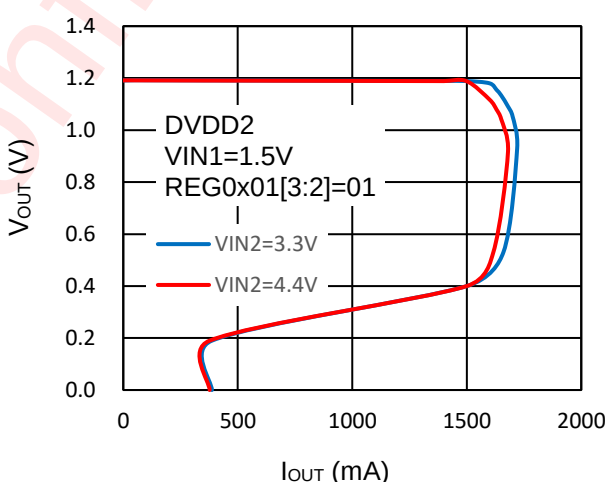
AVDD1 Output Voltage vs Output Current



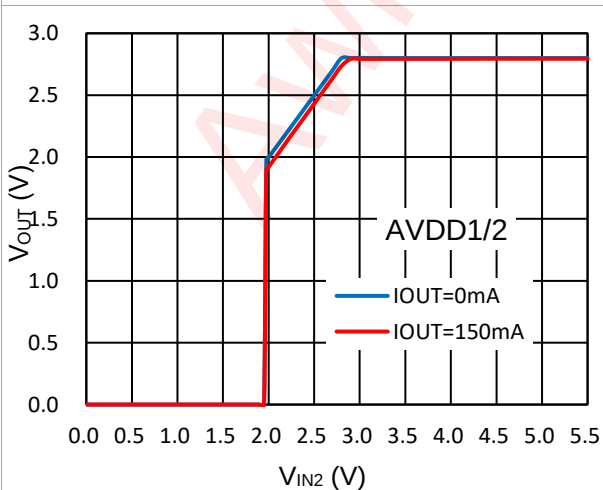
AVDD2 Output Voltage vs Output Current



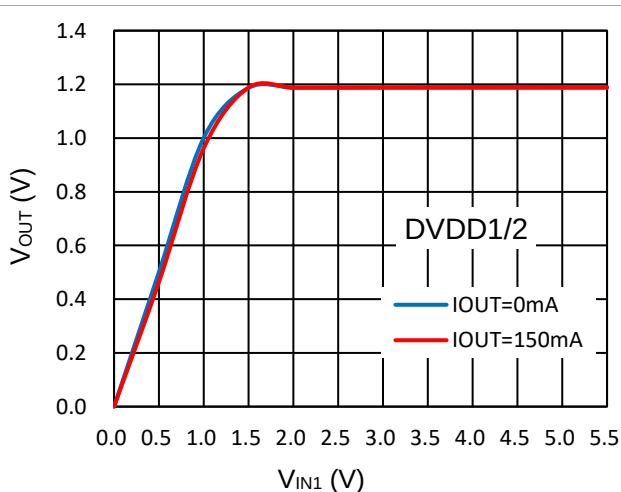
DVDD1 Output Voltage vs Output Current



DVDD2 Output Voltage vs Output Current



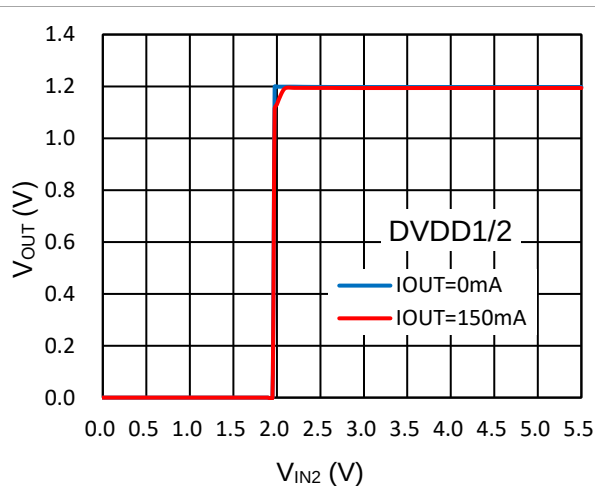
Output Voltage vs Input Voltage



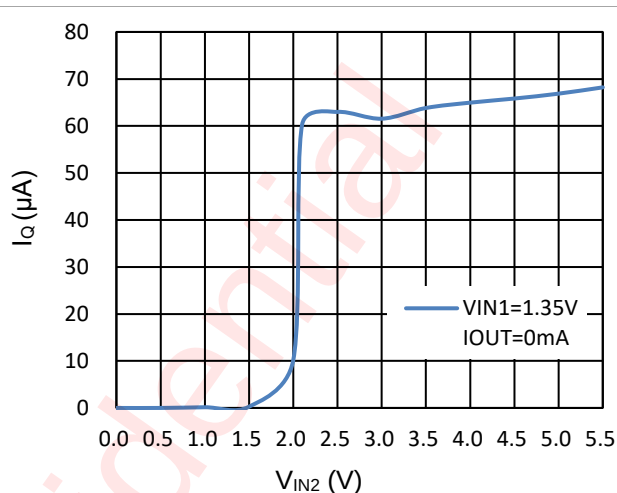
Output Voltage vs Input Voltage

Typical Characteristics (Continued)

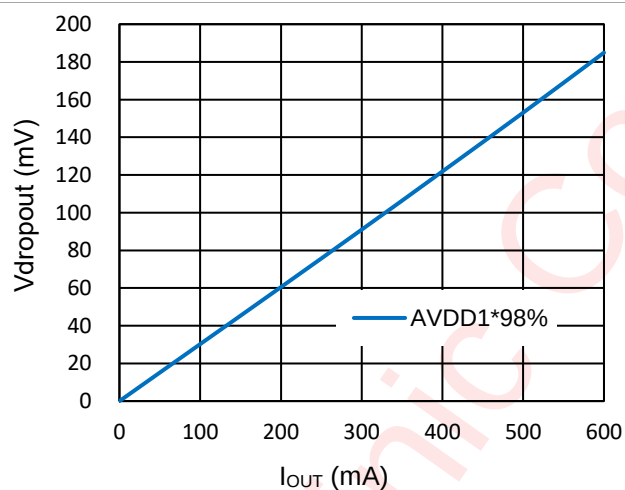
$V_{IN1}=1.35V$, $V_{IN2}=3.3V$, $V_{AVDD1/2}=2.8V$, $V_{DVDD1/2}=1.2V$, $C_{IN}=4.7\mu F$, $C_{OUT_AVDD}=1\mu F$, $C_{OUT_DVDD}=2.2\mu F$, $T_A=25^{\circ}C$, unless otherwise noted.



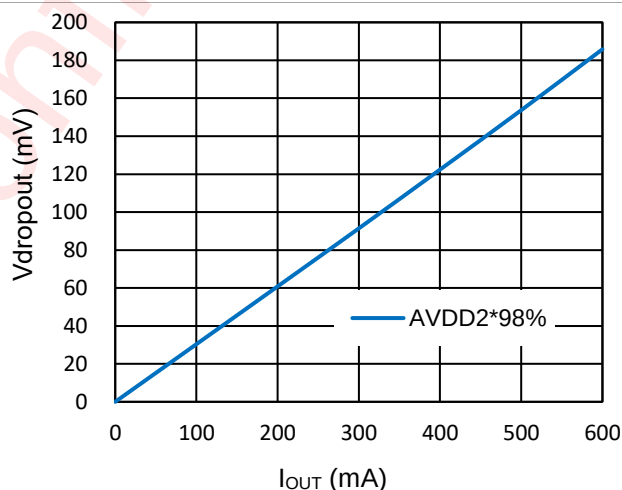
Output Voltage vs Input Voltage



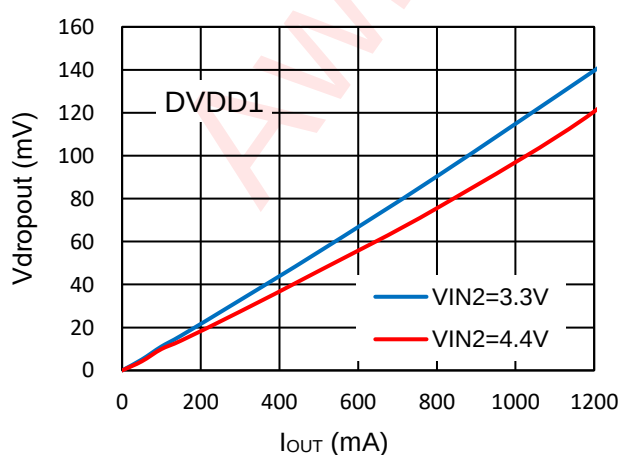
Quiescent Current vs Input Voltage



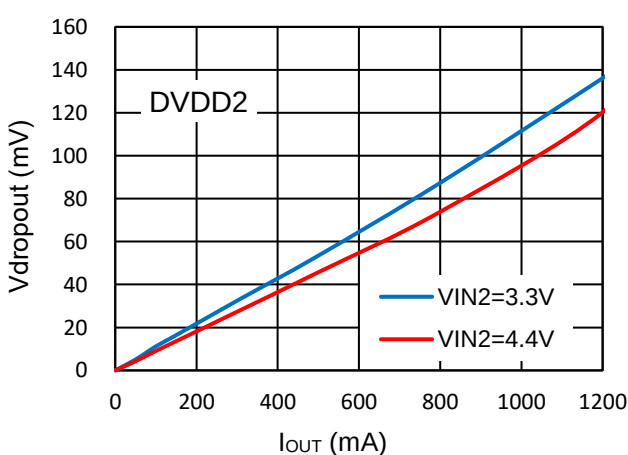
AVDD1 Dropout Voltage vs Output Current



AVDD2 Dropout Voltage vs Output Current



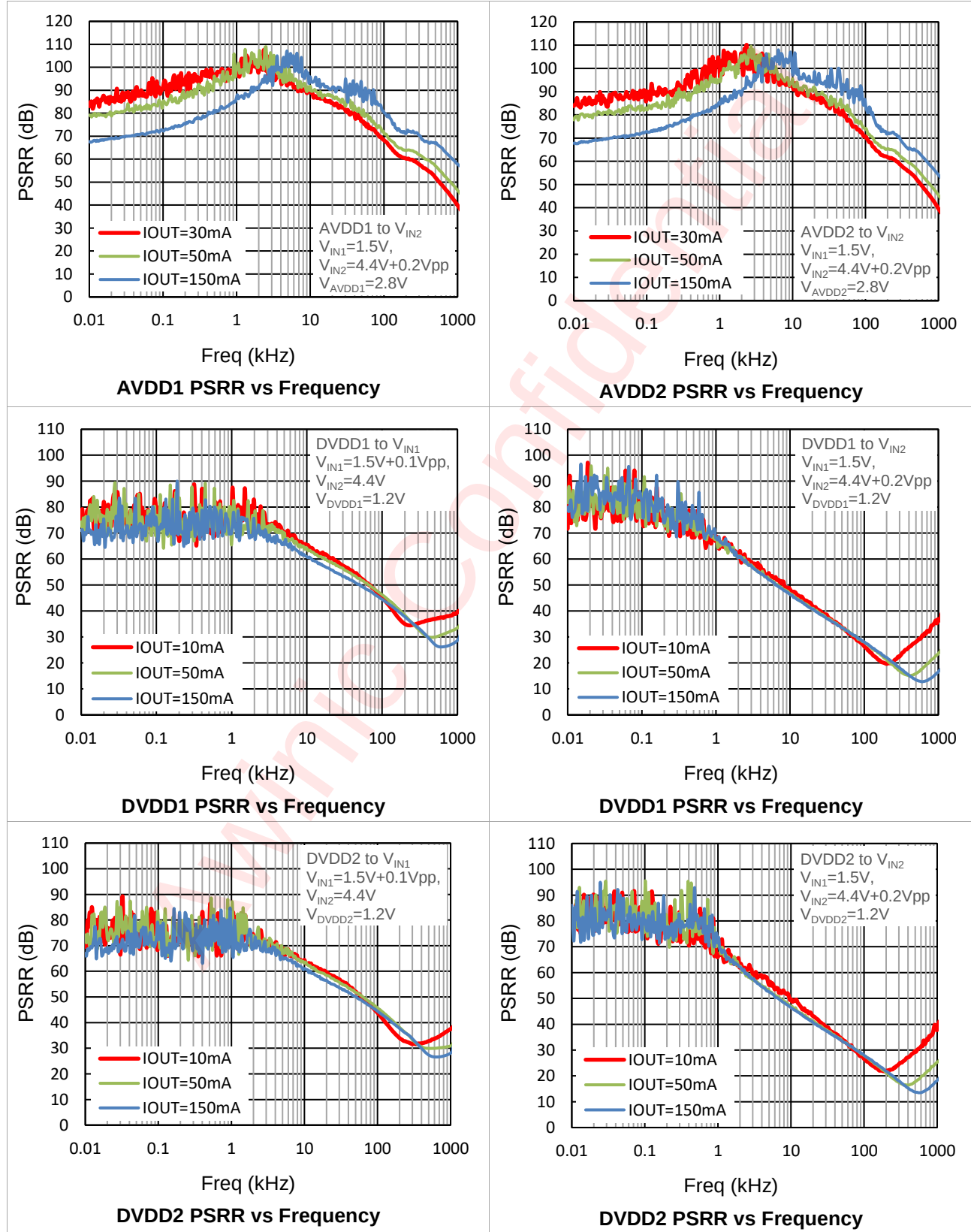
DVDD1 Dropout Voltage vs Output Current



DVDD2 Dropout Voltage vs Output Current

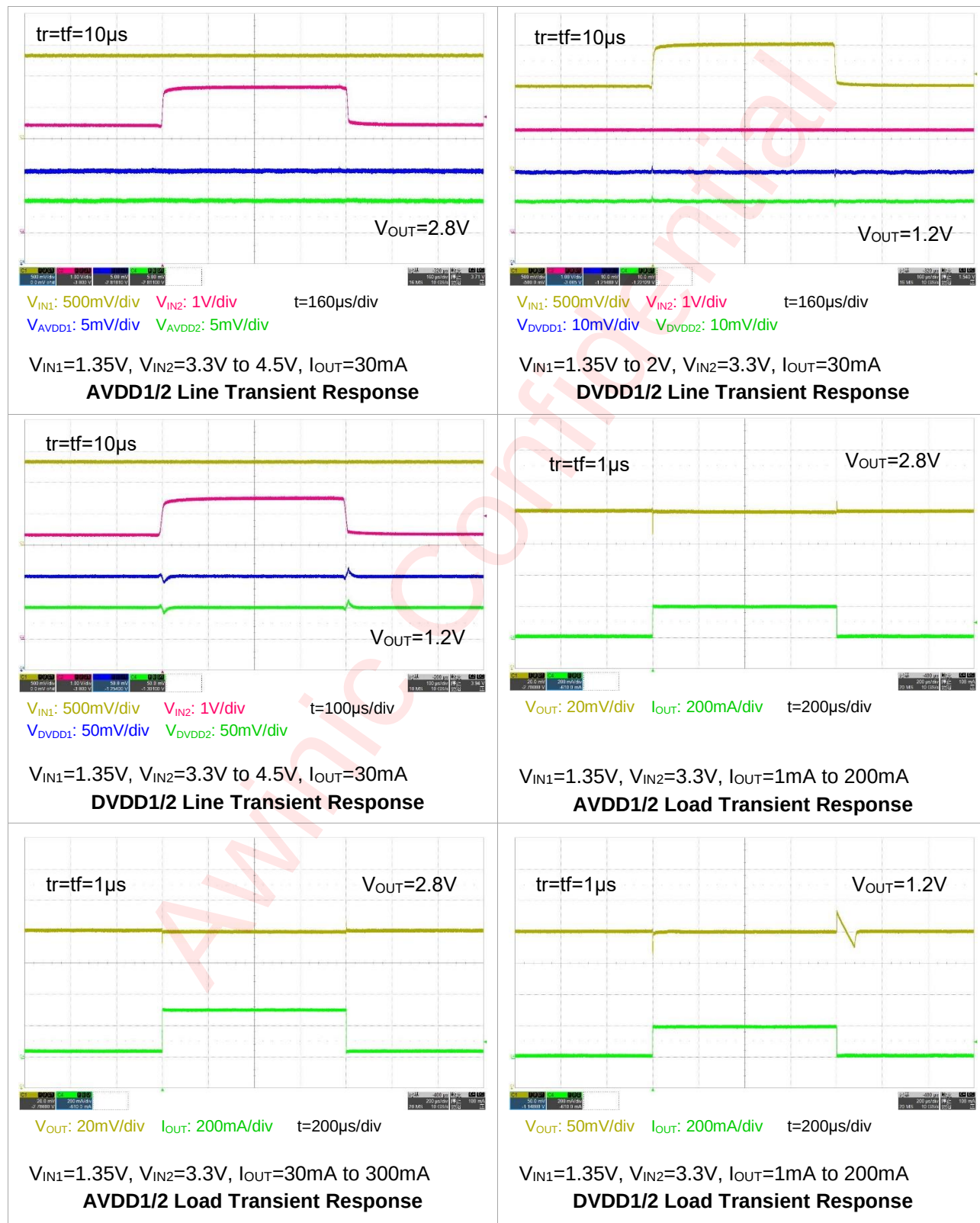
Typical Characteristics (Continued)

$V_{IN1}=1.35V$, $V_{IN2}=3.3V$, $V_{AVDD1/2}=2.8V$, $V_{DVDD1/2}=1.2V$, $C_{IN}=4.7\mu F$, $C_{OUT_AVDD}=1\mu F$, $C_{OUT_DVDD}=2.2\mu F$, $T_A=25^\circ C$, unless otherwise noted.



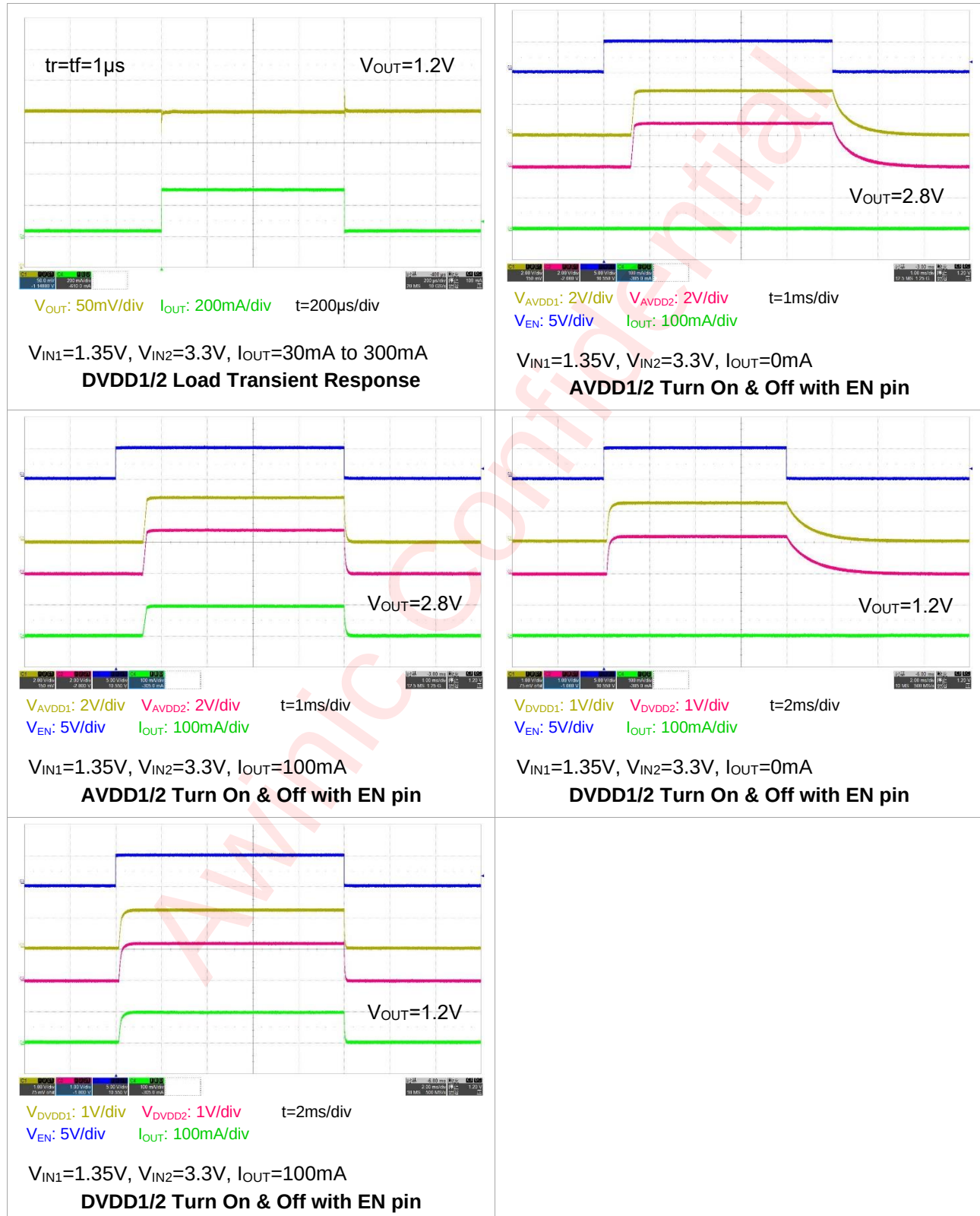
Typical Characteristics (Continued)

$V_{IN1}=1.35V$, $V_{IN2}=3.3V$, $V_{AVDD1/2}=2.8V$, $V_{DVDD1/2}=1.2V$, $C_{IN}=4.7\mu F$, $C_{OUT_AVDD}=1\mu F$, $C_{OUT_DVDD}=2.2\mu F$, $T_A=25^\circ C$, unless otherwise noted.



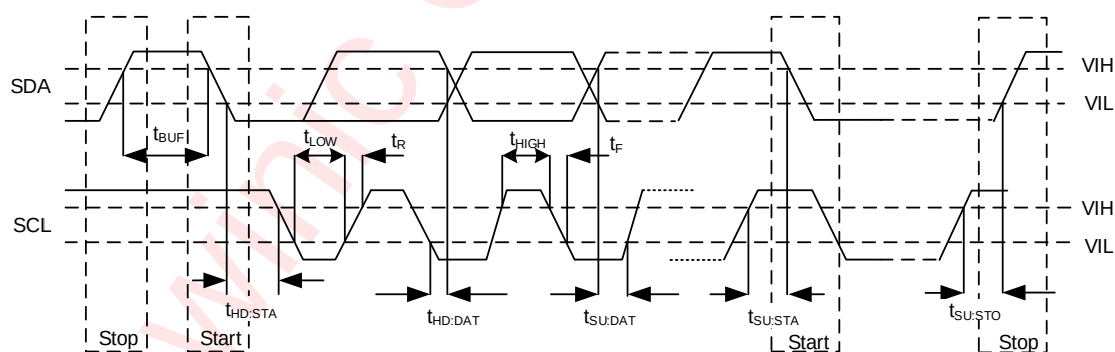
Typical Characteristics (Continued)

$V_{IN1}=1.35V$, $V_{IN2}=3.3V$, $V_{AVDD1/2}=2.8V$, $V_{DVDD1/2}=1.2V$, $C_{IN}=4.7\mu F$, $C_{OUT_AVDD}=1\mu F$, $C_{OUT_DVDD}=2.2\mu F$, $T_A=25^\circ C$, unless otherwise noted.



I²C Interface Timing

PARAMETER		FAST MODE			FAST MODE PLUS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
F _{SCL}	Interface clock frequency	-		400	-		1000	kHz
T _{HD:STA}	(Repeat-start) Start condition hold time	0.6		-	0.26		-	μs
T _{LOW}	Low level width of SCL	1.3		-	0.5		-	μs
T _{HIGH}	High level width of SCL	0.6		-	0.26		-	μs
T _{SU:STA}	(Repeat-start) Start condition setup time	0.6		-	0.26		-	μs
T _{HD:DAT}	Data hold time	0		-	0		-	μs
T _{SU:DAT}	Data setup time	0.1		-	0.05		-	μs
T _R	Rising time of SDA and SCL	-		0.3	-		0.12	μs
T _F	Falling time of SDA and SCL	-		0.3	-		0.12	μs
T _{SU:STO}	Stop condition setup time	0.6		-	0.26		-	μs
T _{BUF}	Time between start and stop condition	1.3		-	0.5		-	μs



Detailed Functional Description

Work Mode

AWP37004E has 4 LDO regulators. Power up/down of each regulator can be controlled by the following three ways. It can be set at the registers DVDDx_SEQ[3:0] & AVDDx_SEQ[3:0] (x=1~2) respectively.

- A. External EN pin toggles from low to high, it will force DVDDx & AVDDx regulators powered up.
- B. Individual on/off control.
- C. Automatic power up/down sequence control.

CHIP ENABLE CONTROL

External EN pin toggles from low to high, it will force DVDDx & AVDDx regulators powered up, output voltage of each LDO is default voltage, and the detailed description is in register DVDDx_VOUT & AVDDx_VOUT.

When external EN pin is low, LDO output can be controlled by an I²C register.

INDIVIDUAL ON/OFF CONTROL

Power-up and shut down of each regulator can be controlled by I²C register. DVDDx_EN & AVDDx_EN are internal signals to enable one regulators. If DVDDx_SEQ[3:0] & AVDDx_SEQ[3:0] set to 4'b0000, that DVDDx & AVDDx channels can be controlled directly by a bit specified in register DVDDx_EN & AVDDx_EN. DVDDx_VOUT[7:0] & AVDDx_VOUT[7:0] can set output voltage of each channel.

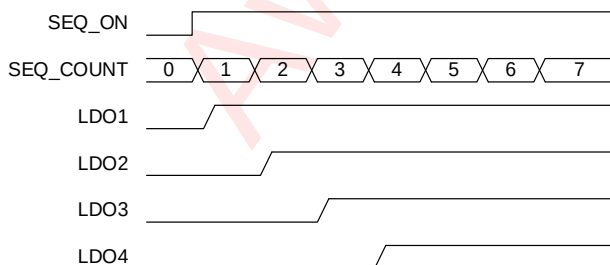
AUTOMATIC POWER UP/DOWN SEQUENCE CONTROL

AWP37004E has 7 SLOTS to which each regulator can be assigned.

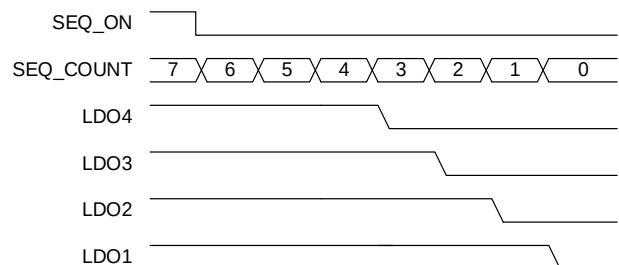
SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7
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They are started by SEQ_ON signal. When SEQ_ON is high. Internal counter SEQ_COUNT[2:0] starts increment from 0 (3'b000) to 7 (3'b111). When SEQ_ON is low, SEQ_COUNT[2:0] decrements from 7 (3'b111) to 0 (3'b000). Regulators assigned to one of SLOTS starts power-up or power-down when SEQ_COUNT[2:0] matches the SLOT number.

Internal logic signal SEQ_ON is asserted by I²C, writing 1'b0 to SEQ_CTRL will set SEQ_ON to '0', while writing 1'b1 to SEQ_CTRL will set SEQ_ON to '1'.



Example of Power-up in the case of DVDDx & AVDDx are assigned to SLOT1 ~ SLOT4 respectively.

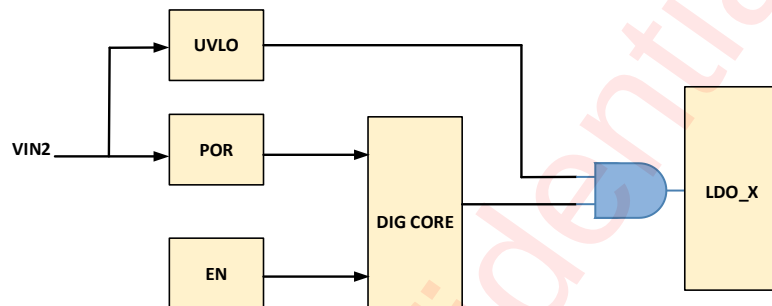


Example of Shut-down in the case of DVDDx & AVDDx are assigned to SLOT1 ~ SLOT4 respectively.

Time Sequence of Chip Enable Control by I²C

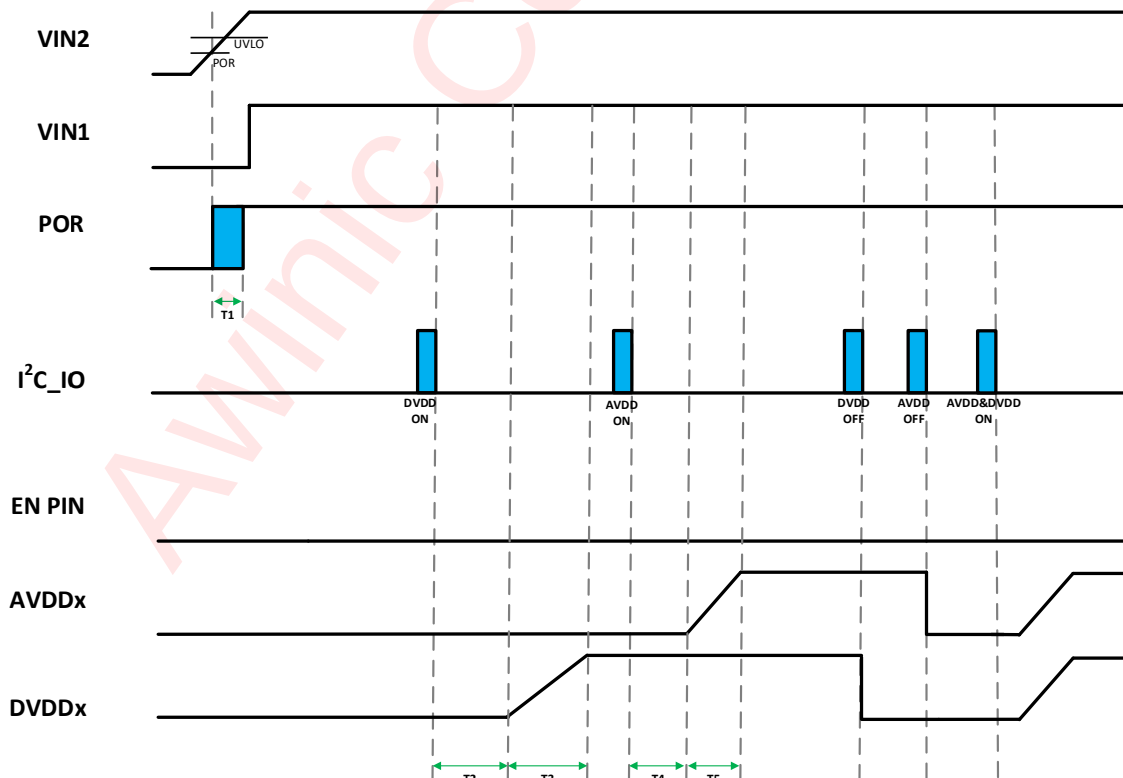
VIN2 serves as the system power supply, providing power to internal fundamental modules. It simultaneously powers the AVDD1 and AVDD2 rails. VIN1 supplies the DVDD1 and DVDD2 rails. After VIN2 powers up, the POR signal is asserted. The digital section requires a T1 delay (500 μ s) to load the efuse status. Once this delay elapses, the I²C communication can be enabled via the EN pin.

EN serves as the I²C enable signal. After EN is asserted low, I²C_IO communication becomes available for configuring the AVDDx and DVDDx settings. When any channel is first enabled, there is a basic module setting time of 250 μ s.



DVDDx: When DVDDx is the first channel to be enabled via I²C configuration, the startup time T2 is 400 μ s. In all other cases, the startup time T2 is 150 μ s. And the time from DVDDx startup to completion is T3 (230 μ s).

AVDDx: When AVDDx is the first channel to be enabled via I²C configuration, the startup time T4 is 530 μ s. In all other cases, the startup time T4 is 280 μ s. And the time from AVDDx startup to completion is T5 (150 μ s).



Note: Once VIN1 powers down, the DVDD channel needs to be turned off by ENCR register(Address 0x0E).

Output Discharge Setting

Set related bits to select output discharge function for Discharge Resistor (DISCR, Address 0x02), 1'b1: Disable, 1'b0: Enable. AWP37004E support 2 modes for Discharge, which controlled by DCE_MODE (bit 7 of DISCR register). It will force enable each LDO Discharge function when DCE_MODE=0. AVDDx & DVDDx Discharge function is controlled by bit 3 ~ bit 0 of DISCR register when DCE_MODE=1.

Output Current Limit

AWP37004E integrates output current limit function, protecting IC from excessive current. When the load is excessively heavy, DVDD limits the current flowing through the IC to a typical 1500mA (default) current, it can be set to max 1780mA by CLMTCR register. AVDD limits the current flowing through the IC to a typical 500mA (default) current, it also can be set to max 700mA by CLMTCR register. This value is specially designed to protect the IC well without affecting the output capacity.

UVLO

When the voltage of VIN2 fall below their UVLO falling threshold(Typ. 1.9V), all LDOs will be shut down, causing a UVLO interrupt. The UVLO status bit will not change until the input voltage rises above its UVLO rising threshold(Typ. 2.0V), and then one or more channels can be opened.

Short Current Limit

AWP37004E integrates a fold-back current limit function to reduce system dissipation during output overload or short to Ground. DVDD1/2 limits the current flowing through the IC to 380mA when its voltage drops below 190mV, with the current limit being released when the voltage recovers to 350mV.

Thermal shutdown

AWP37004E integrates thermal shutdown function, protect IC from excessively high temperature. When the chip temperature exceeds 150°C, AWP37004E detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 120°C. At this moment, the over-temperature protection-state is released, IC resumes to work again. The hysteresis avoids IC's turning off and on frequently around the Thermal Shutdown threshold.

I²C Interface

AWP37004E supports the I²C protocol. The maximum frequency supported by the I²C is 1MHz. The pull-up resistor for the SDA and SCL can be selected from 1kΩ to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I²C, 1kΩ is recommended for 1MHz I²C. Additionally, the I²C device supports continuous reading and writing operations.

DEVICE ADDRESS

The I²C device address is 7-bit (A7~A1), followed by the R/W bit A0 (Read=1/Write=0). Set A0 to "0" for writing and "1" for reading. The default I²C address is 0x28:

A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	W/R

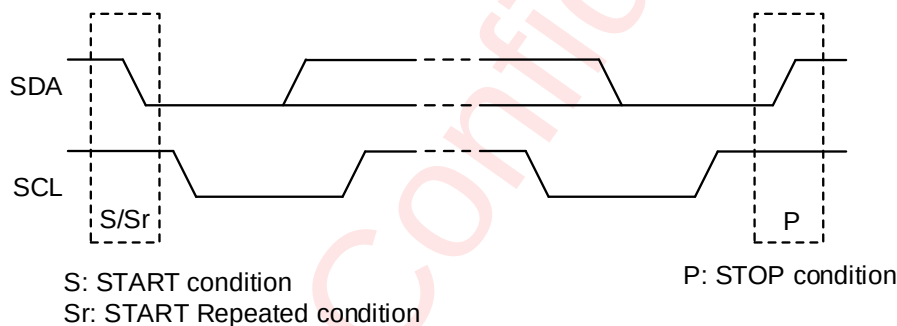
When using multiple AWP37004E, it can be achieved by setting different I²C addresses through I²C Address Register(IIC_ADDR, Address 0x08). When EN pin is low, the IIC_ADDR is read-only. When EN pin is high, the IIC_ADDR is read-write. Therefore, if we set one of the LDOs' EN pin to high, and change the I²C address other than the default address through IIC_ADDR_SEL[1:0], then set the EN pin to low. Set them one by one according to this method, then multiple AWP37004E can be applied in parallel.

IIC_ADDR[1:0]	I ² C Address
2'b00	0x20
2'b01	0x28
2'b10	0x61
2'b11	0x72

I²C START/STOP

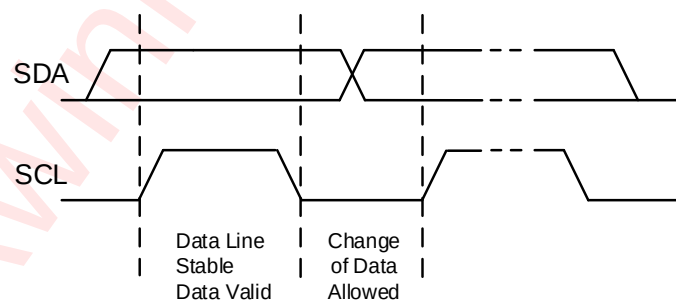
I²C START: SDA changes from high level to low level when SCL is high level.

I²C STOP: SDA changes from low level to high level when SCL is high level.



DATA VALIDATION

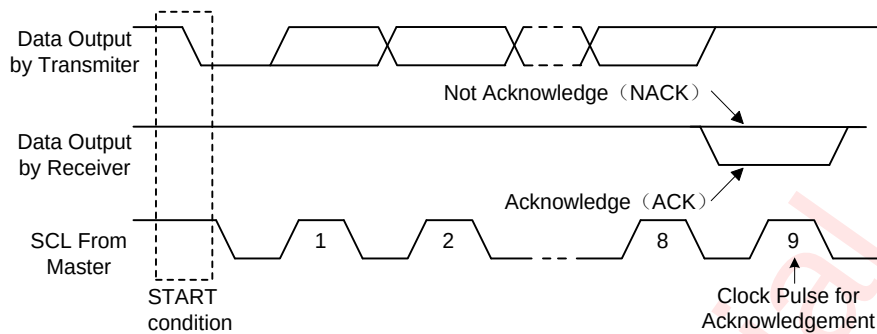
When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.



ACK (ACKNOWLEDGEMENT)

ACK means the successful transition of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C STOP is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.



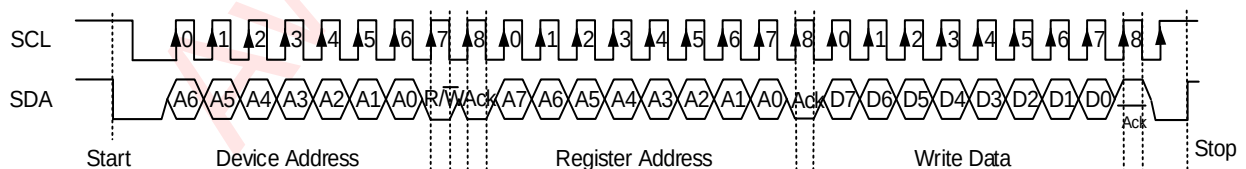
WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

- Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
- Master device sends slave address (7-bit) and the data direction bit R/W = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8-bit).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g).
- Master generates STOP condition to indicate write cycle end.

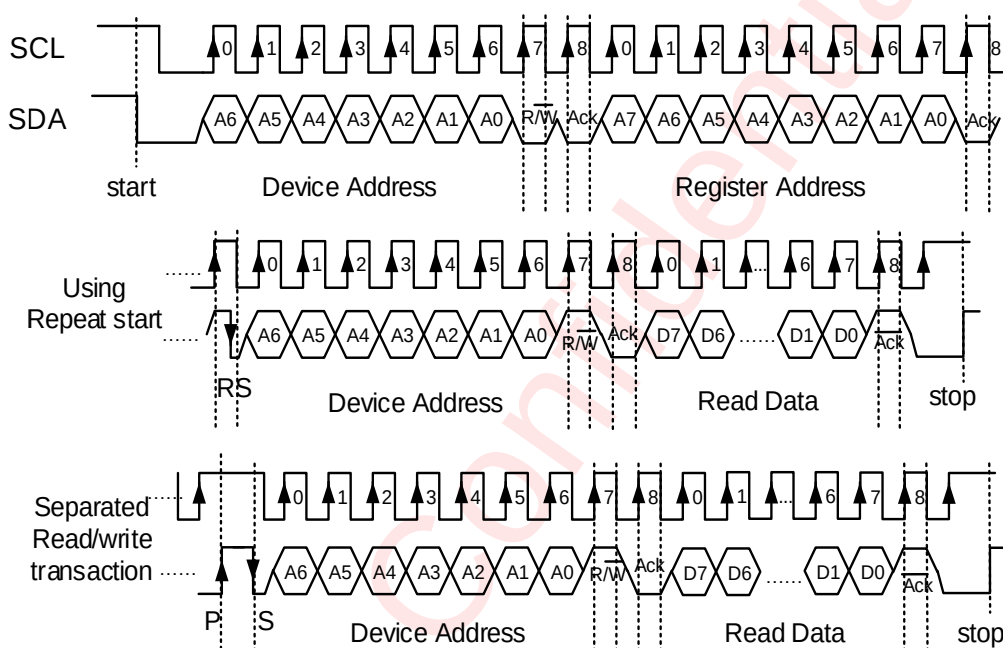


READ CYCLE

In a read cycle, the following steps should be followed:

- Master device generates START condition.
- Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8-bit).

- e) Slave sends acknowledge signal.
- f) Master generates STOP condition followed with START condition or REPEAT START condition.
- g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
- h) Slave device sends acknowledge signal if the slave address is correct.
- i) Slave sends data byte from addressed register.
- j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
- k) If the master device generates STOP condition, the read cycle ends.



Register Description

Ad.	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Init
0x00	CHIP_ID	R	CHIP_ID								0x08
0x01	CLMTCR	R/W	AVDD2_CLMT		AVDD1_CLMT		DVDD2_CLMT		DVDD1_CLMT		0x55
0x02	DISCR	R/W	DCE_MODE	DVDD_DISR			AVDD2_DCE	AVDD1_DCE	DVDD2_DCE	DVDD1_DCE	0x00
0x03	DVDD1_VOUT	R/W	DVDD1_VOUT								0x64
0x04	DVDD2_VOUT	R/W	DVDD2_VOUT								0x64
0x05	AVDD1_VOUT	R/W	AVDD1_VOUT								0x80
0x06	AVDD2_VOUT	R/W	AVDD2_VOUT								0x80
0x08	IIC_ADDR	R/W							IIC_ADDR_SEL		0x01
0x0A	DVDD_SEQ	R/W	DVDD2_SEQ				DVDD1_SEQ				0x00
0x0B	AVDD_SEQ	R/W	AVDD2_SEQ				AVDD1_SEQ				0x00
0x0E	ENCR	R/W					AVDD2_EN	AVDD1_EN	DVDD2_EN	DVDD1_EN	0x00
0x0F	SEQCR	R/W	SEQ_SPEED			SEQ_CTRL	SEQ_ON	SEQ_COUNT			0x00

Register Detailed Description

CHIP_ID: Chip ID (Address 0x00)

Bit	Symbol	R/W	Description	Init
7:0	CHIP ID	R	Indicates the device ID	0x08

CLMTCR: Current Limit Control Register (Address 0x01)

Bit	Symbol	R/W	Description	Init
7:6	AVDD2_CLMT	R/W	AVDD2 current limit control 2'b00: 400mA 2'b01: 500mA 2'b10: 600mA 2'b11: 700mA	0x01

Bit	Symbol	R/W	Description	Init
5:4	AVDD1_CLMT	R/W	AVDD1 current limit control 2'b00: 400mA 2'b01: 500mA 2'b10: 600mA 2'b11: 700mA	0x01
3:2	DVDD2_CLMT	R/W	DVDD2 current limit control 2'b00: 1360mA 2'b01: 1500mA 2'b10: 1640mA 2'b11: 1780mA	0x01
1:0	DVDD1_CLMT	R/W	DVDD1 current limit control 2'b00: 1360mA 2'b01: 1500mA 2'b10: 1640mA 2'b11: 1780mA	0x01

DISCR: Discharge Control Register (Address 0x02)

Bit	Symbol	R/W	Description	Init
7	DCE_MODE	R/W	Discharge mode control: 0: Auto mode, all LDOs' discharge function is enabled 1: Manuel mode, discharge function controlled by DVDDx_DCE & AVDDx_DCE	0x0
6	DVDD_DISR	R/W	DVDD discharge resistance select: 0: 540Ω 1: 270Ω	0x0
5:4	Reserved	R/W	Reserved	0x00
3	AVDD2_DCE	R/W	Discharge function enable of AVDD2 0: Disable 1: Enable	0x0
2	AVDD1_DCE	R/W	Discharge function enable of AVDD1 0: Disable 1: Enable	0x0
1	DVDD2_DCE	R/W	Discharge function enable of DVDD2 0: Disable 1: Enable	0x0
0	DVDD1_DCE	R/W	Discharge function enable of DVDD1 0: Disable 1: Enable	0x0

DVDD1_VOUT: DVDD1 Output Voltage Control Register (Address 0x03)

Bit	Symbol	R/W	Description	Init
7:0	DVDD1_VOUT	R/W	DVDD1 output voltage control $VOUT = 0.6V + DVDD1_VOUT[7:0] \times 0.006V$ 0x00: 0.600V 0x01: 0.606V 0x02: 0.612V ... 0x63: 1.194V 0x64: 1.200V 0x65: 1.206V ... 0xFF: 2.130V	0x64

DVDD2_VOUT: DVDD2 Output Voltage Control Register (Address 0x04)

Bit	Symbol	R/W	Description	Init
7:0	DVDD2_VOUT	R/W	DVDD2 output voltage control $VOUT = 0.6V + DVDD2_VOUT[7:0] \times 0.006V$ 0x00: 0.600V 0x01: 0.606V 0x02: 0.612V ... 0x63: 1.194V 0x64: 1.200V 0x65: 1.206V ... 0xFF: 2.130V	0x64

AVDD1_VOUT: AVDD1 Output Voltage Control Register (Address 0x05)

Bit	Symbol	R/W	Description	Init
7:0	AVDD1_VOUT	R/W	AVDD1 output voltage control $VOUT = 1.2V + AVDD1_VOUT[7:0] \times 0.0125V$ 0x00: 1.2000V 0x01: 1.2125V 0x02: 1.2250V ... 0x7F: 2.7875V 0x80: 2.8000V 0x81: 2.8125V ... 0xFF: 4.3875V	0x80

AVDD2_VOUT: AVDD2 Output Voltage Control Register (Address 0x06)

Bit	Symbol	R/W	Description	Init
7:0	AVDD2_VOUT	R/W	AVDD2 output voltage control $VOUT = 1.2V + AVDD2_VOUT[7:0] \times 0.0125V$ 0x00: 1.2000V 0x01: 1.2125V 0x02: 1.2250V ... 0x7F: 2.7875V 0x80: 2.8000V 0x81: 2.8125V ... 0xFF: 4.3875V	0x80

IIC_ADDR: IIC Address Register (Address 0x08)

Bit	Symbol	R/W	Description	Init
7:2	Reserved	R/W	Reserved	0x00
1:0	IIC_ADDR_SEL	R/W	IIC slave address select: 2'b00: 0x20 2'b01: 0x28 2'b10: 0x61 2'b11: 0x72	0x01

Note: When EN pin is low, the IIC_ADDR is read-only. When EN pin is high, the IIC_ADDR is read-write.

DVDD_SEQ: DVDDx Sequence Control Register (Address 0x0A)

Bit	Symbol	R/W	Description	Init
7:4	DVDD2_SEQ	R/W	DVDD2 sequence slot set 4'b0000: Disable sequence mode 4'bx001: Set sequence slot is 1 4'bx010: Set sequence slot is 2 4'bx011: Set sequence slot is 3 4'bx100: Set sequence slot is 4 4'bx101: Set sequence slot is 5 4'bx110: Set sequence slot is 6 4'bx111: Set sequence slot is 7	0x00
3:0	DVDD1_SEQ	R/W	DVDD1 sequence slot set 4'b0000: Disable sequence mode 4'bx001: Set sequence slot is 1 4'bx010: Set sequence slot is 2 4'bx011: Set sequence slot is 3 4'bx100: Set sequence slot is 4 4'bx101: Set sequence slot is 5 4'bx110: Set sequence slot is 6 4'bx111: Set sequence slot is 7	0x00

AVDD_SEQ: AVDDx Sequence Control Register (Address 0x0B)

Bit	Symbol	R/W	Description	Init
7:4	AVDD2_SEQ	R/W	AVDD2 sequence slot set 4'b0000: Disable sequence mode 4'bx001: Set sequence slot is 1 4'bx010: Set sequence slot is 2 4'bx011: Set sequence slot is 3 4'bx100: Set sequence slot is 4 4'bx101: Set sequence slot is 5 4'bx110: Set sequence slot is 6 4'bx111: Set sequence slot is 7	0x00
3:0	AVDD1_SEQ	R/W	AVDD1 sequence slot set 4'b0000: Disable sequence mode 4'bx001: Set sequence slot is 1 4'bx010: Set sequence slot is 2 4'bx011: Set sequence slot is 3 4'bx100: Set sequence slot is 4 4'bx101: Set sequence slot is 5 4'bx110: Set sequence slot is 6 4'bx111: Set sequence slot is 7	0x00

ENCR: Individual Enable Control Register (Address 0x0E)

Bit	Symbol	R/W	Description	Init
7:4	Reserved	R/W	Reserved	0x00
3	AVDD2_EN	R/W	AVDD2 enable control 0: Disable AVDD2 output when EN pin is low 1: Enable AVDD2 output when EN pin is low	0x0
2	AVDD1_EN	R/W	AVDD1 enable control 0: Disable AVDD1 output when EN pin is low 1: Enable AVDD1 output when EN pin is low	0x0
1	DVDD2_EN	R/W	DVDD2 enable control 0: Disable DVDD2 output when EN pin is low 1: Enable DVDD2 output when EN pin is low	0x0
0	DVDD1_EN	R/W	DVDD1 enable control 0: Disable DVDD1 output when EN pin is low 1: Enable DVDD1 output when EN pin is low	0x0

SEQCR: Sequence Control Register (Address 0x0F)

Bit	Symbol	R/W	Description	Init
7:6	SEQ_SPEED	R/W	The seq_count increment period in sequence mode 2'b00: 2000μs 2'b01: 1000μs 2'b10: 500μs 2'b11: 250μs	0x00
5	Reserved	R/W	Reserved	0x0
4	SEQ_CTRL	R/W	Sequence control when AVDDx/DVDDx slot isn't 0 2'bx0: Shutdown 2'bx1: Power up	0x0
3	SEQ_ON	R	The indication of sequence activation 0: Shutdown 1: Power up	0x0
2:0	SEQ_COUNT	R	The indication of the seq_count 3'b000: No LDO slots active 3'b001: slot 1 active 3'b010: slot 2 active 3'b011: slot 3 active 3'b100: slot 4 active 3'b101: slot 5 active 3'b110: slot 6 active 3'b111: slot 7 active	0x00

Application Information

CAPACITORS SELECTION

IN pin: Input Capacitor C_{IN}

AWP37004E advises to use a 4.7 μ F or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AWP37004E advises to use a 1 μ F or more X5R or X7R ceramic capacitor at AVDD pin as shown in Typical Application Circuit;

AWP37004E advises to use a 2.2 μ F or more X5R or X7R ceramic capacitor at DVDD pin as shown in Typical Application Circuit.

Recommended Components List

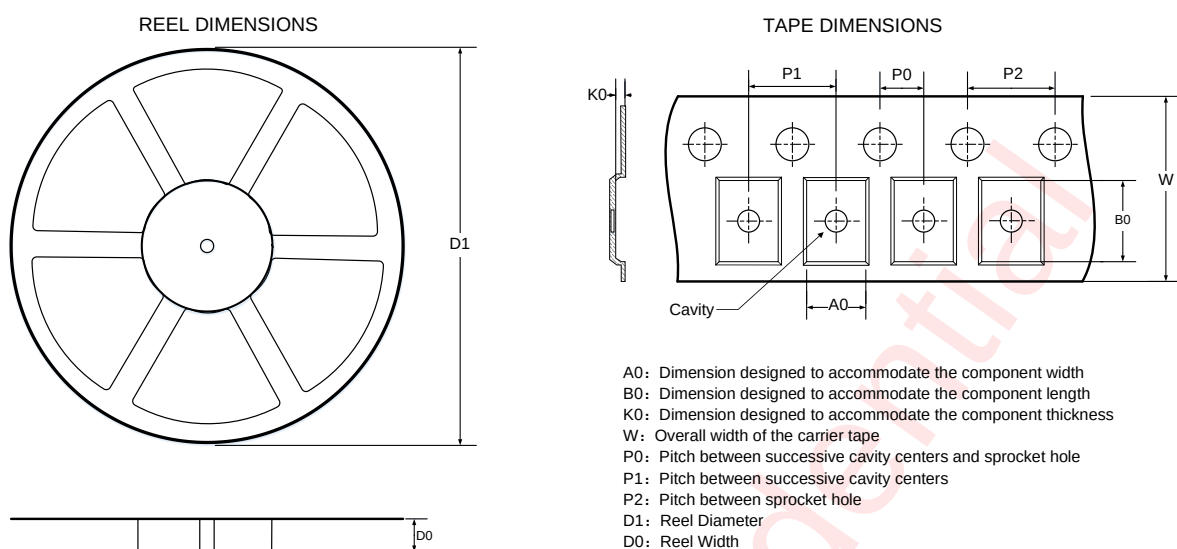
Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	4.7	μ F
C_{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μ F
	GRM153R60J225ME95	6.3V, X5R, 0402	MURATA	2.2	μ F
	GRM153R60J475ME15	6.3V, X5R, 0402	MURATA	4.7	μ F

PCB Layout Consideration

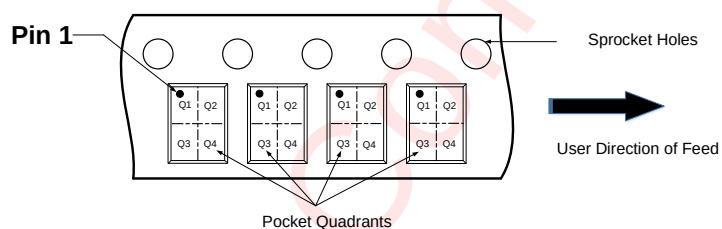
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AWP37004E should be obeyed:

1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



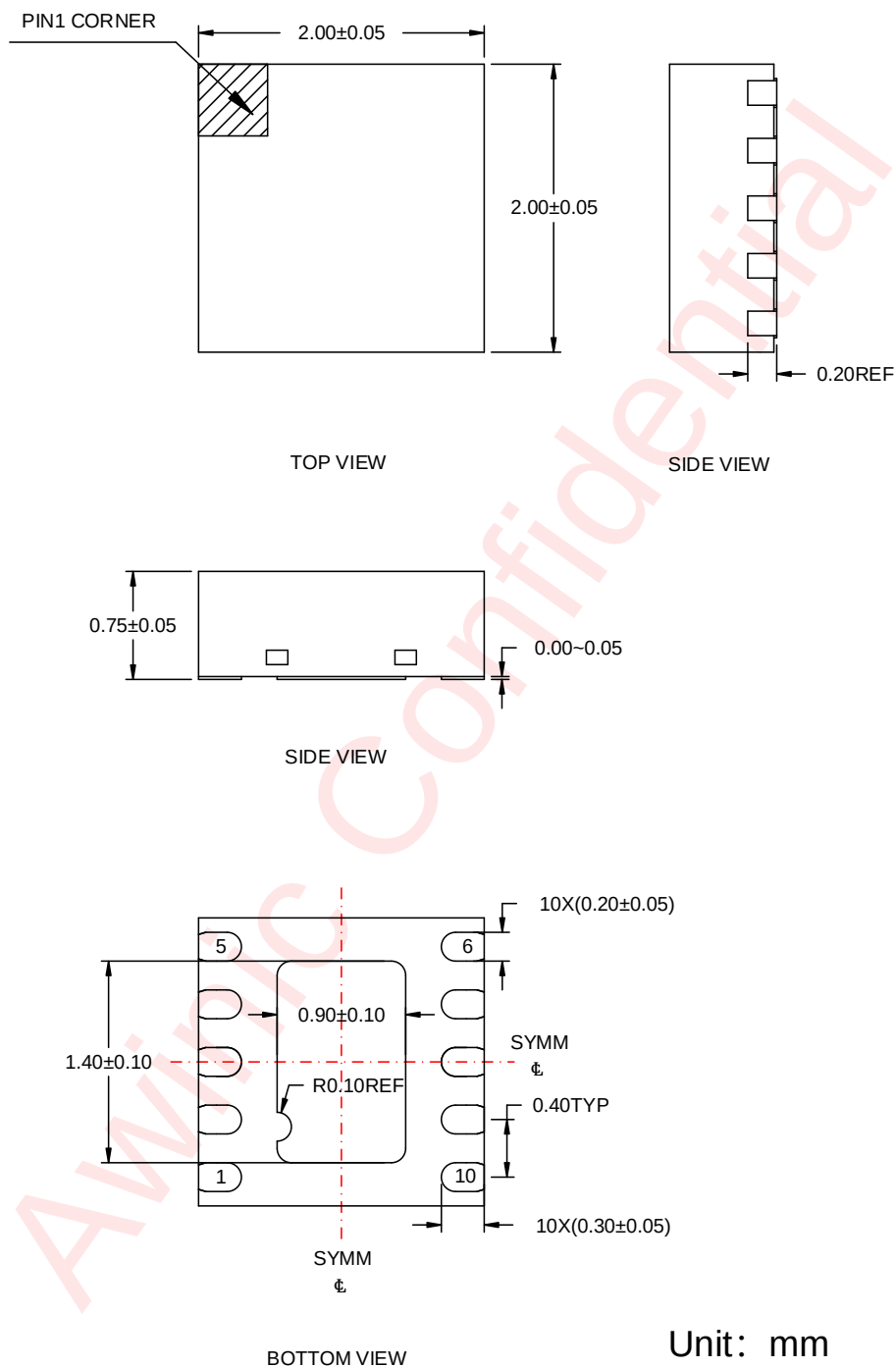
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	2.3	1	2	4	4	8	Q1

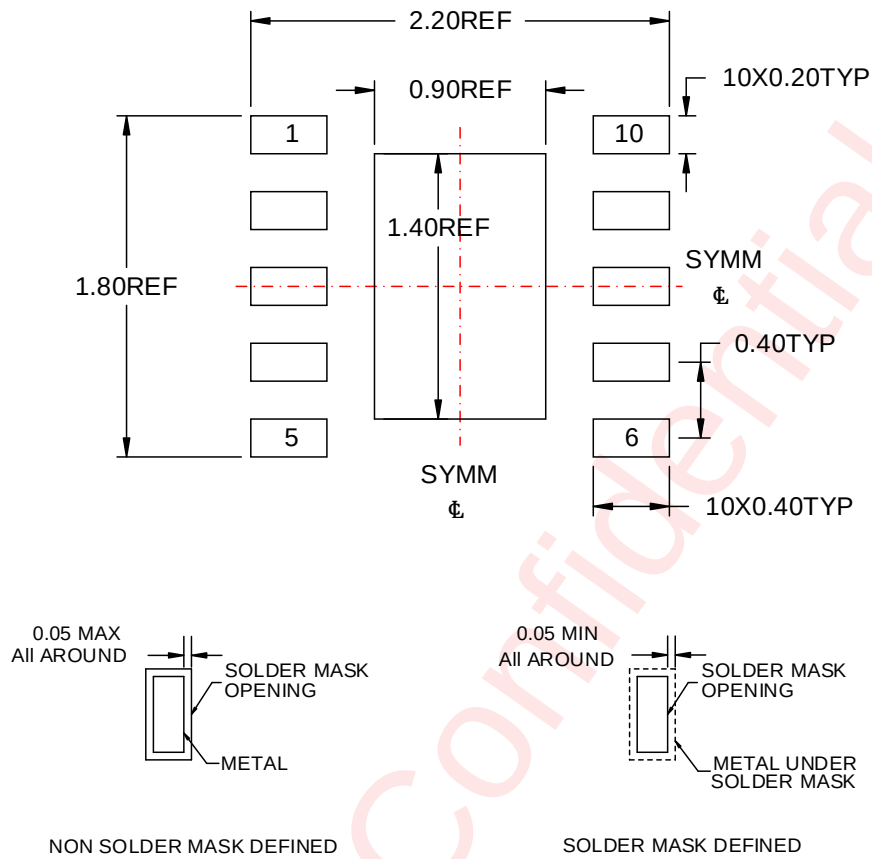
All dimensions are nominal

Package Description



Unit: mm

Land Pattern Data



Unit: mm

Revision History

Version	Date	Change record
V1.0	Jun. 2025	Officially released
V1.1	Nov. 2025	1. Update the Functional Block Diagram.(P4) 2. Update the EC table.(P8) 3. Update the Typical Characteristics.(P9~P10) 4. Update the Detailed Functional Description.(P16~P17)

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