# DRV8840 DC Motor Driver IC

## 1 Features

- Single H-Bridge Current-Control Motor Driver
- 8.2-V to 45-V Operating Supply Voltage Range
- Five Bit Current Control Allows up to 32 Current Levels
- Low MOSFET $R_{DS(on)}$ Typical 0.65 Ω (HS + LS)
- 5-A Maximum Drive Current at 24 V, $T_A$ = 25°C
- Built-In 3.3-V Reference Output
- Parallel Digital Control Interface
- Thermal Enhanced Surface Mount Package
- Protection Features:
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Undervoltage Lockout (UVLO)
  - Fault Condition Indication Pin (nFAULT)

## 2 Applications

- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

## 3 Description

The DRV8840 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has one H-bridge driver, and is intended to drive one DC motor. The output driver block for each consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings. The DRV8840 can supply up to 5-A peak or 3.5-A output current (with proper heatsinking at 24 V and 25°C).

A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable to allow braking or coasting of the motor when disabled.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

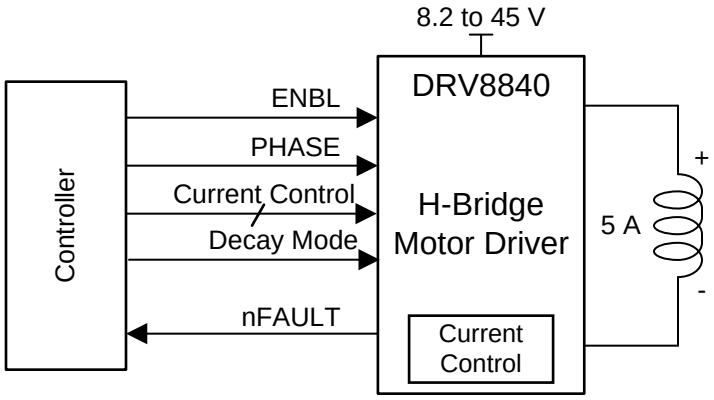
The DRV8840 is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DRV8840 | HTSSOP (28) | 9.70 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematic**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (August 2013) to Revision D | Page |
|---|---|
| • Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Updated *Features* bullets | 1 |
| • Added MIN value for ISENSEx row from –0.3 V to –0.8 V | 4 |


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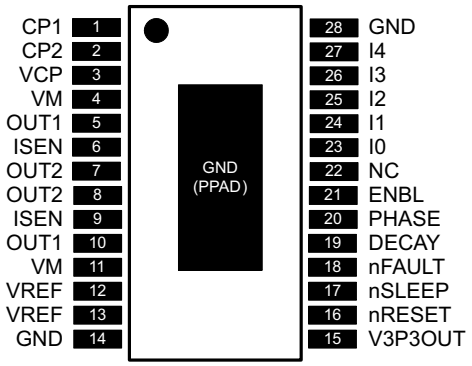
# 5 Pin Configuration and Functions

**PWP Package**
**28-Pin HTSSOP**
**Top View**




## Pin Functions

| PIN | | I/O(1) | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|
| NAME | NO. | | | |
| **POWER AND GROUND** | | | | |
| GND | 14, 28 | — | Device ground | |
| VM | 4, 11 | — | Bridge A power supply | Connect to motor supply (8.2 - 45 V). Both pins must be connected to same supply. |
| V3P3OUT | 15 | O | 3.3-V regulator output | Bypass to GND with a 0.47-µF, 6.3-V ceramic capacitor. Can be used to supply VREF. |
| CP1 | 1 | IO | Charge pump flying capacitor | Connect a 0.01-µF 50-V capacitor between CP1 and CP2. |
| CP2 | 2 | IO | Charge pump flying capacitor | |
| VCP | 3 | IO | High-side gate drive voltage | Connect a 0.1-µF 16-V ceramic capacitor and a 1-MΩ resistor to VM. |
| **CONTROL** | | | | |
| PHASE | 20 | I | Bridge phase (direction) | Logic high sets OUT1 high, OUT2 low. Internal pulldown. |
| ENBL | 21 | I | Bridge enable | Logic high to enable H-bridge. Internal pulldown. |
| I0 | 23 | I | Current set inputs | Sets winding current as a percentage of full-scale. Internal pulldown. |
| I1 | 24 | I | | |
| I2 | 25 | I | | |
| I3 | 26 | I | | |
| I4 | 27 | I | | |
| DECAY | 19 | I | Decay (brake) mode | Low = brake (slow decay), high = coast (fast decay). Internal pulldown and pullup. |
| nRESET | 16 | I | Reset input | Active-low reset input initializes the logic and disables the H-bridge outputs. Internal pulldown. |
| nSLEEP | 17 | I | Sleep mode input | Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown. |
| VREF | 12,13 | I | Current set reference input | Reference voltage for winding current set. Both pins must be connected together on the PCB. |

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

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**Pin Functions (continued)**

| PIN | | I/O[1] | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|
| NAME | NO. | | | |
| **STATUS** | | | | |
| nFAULT | 18 | OD | Fault | Logic low when in fault condition (overtemperature, overcurrent) |
| **OUTPUT** | | | | |
| ISEN | 6, 9 | IO | Bridge ground / Isense | Connect to current sense resistor. Both pins must be connected together on the PCB. |
| OUT1 | 5, 10 | O | Bridge output 1 | Connect to motor winding. Both pins must be connected together on the PCB. |
| OUT2 | 7, 8 | O | Bridge output 2 | Connect to motor winding. Both pins must be connected together on the PCB. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VMx | Power supply voltage | –0.3 | 47 | V |
| | Digital pin voltage | –0.5 | 7 | V |
| VREF | Input voltage | –0.3 | 4 | V |
| | ISENSEx pin voltage[3] | –0.8 | 0.8 | V |
| | Peak motor drive output current, t < 1 µS | Internally limited | | A |
| | Continuous motor drive output current[4] | 0 | 5 | A |
| | Continuous total power dissipation | See *Thermal Information* | | |
| $T_J$ | Operating virtual junction temperature | –40 | 150 | °C |
| $T_A$ | Operating ambient temperature | –40 | 85 | °C |
| $T_{stg}$ | Storage temperature | –60 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.
(3) Transients of ±1 V for less than 25 ns are acceptable.
(4) Power dissipation and thermal limits must be observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_M$ | Motor power supply voltage[1] | 8.2 | 45 | V |
| $V_{REF}$ | VREF input voltage[2] | 1 | 3.5 | V |
| $I_{V3P3}$ | V3P3OUT load current | 0 | 1 | mA |
| $f_{PWM}$ | Externally applied PWM frequency | 0 | 100 | kHz |

(1) All $V_M$ pins must be connected to the same supply voltage.
(2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | DRV8840 PWP (HTSSOP) 28 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 31.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 15.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 5.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 5.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $I_{VM}$ | VM operating supply current | $V_M$ = 24 V, $f_{PWM}$ < 50 kHz | | 5 | 8 | mA |
| $I_{VMQ}$ | VM sleep mode supply current | $V_M$ = 24 V | | 10 | 20 | µA |
| $V_{UVLO}$ | VM undervoltage lockout voltage | $V_M$ rising | | 7.8 | 8.2 | V |
| **V3P3OUT REGULATOR** | | | | | | |
| $V_{3P3}$ | V3P3OUT voltage | IOUT = 0 to 1 mA | 3.2 | 3.3 | 3.4 | V |
| **LOGIC-LEVEL INPUTS** | | | | | | |
| $V_{IL}$ | Input low voltage | | | 0.6 | 0.7 | V |
| $V_{IH}$ | Input high voltage | | 2.2 | | 5.25 | V |
| $V_{HYS}$ | Input hysteresis | | 0.3 | 0.45 | 0.6 | V |
| $I_{IL}$ | Input low current | VIN = 0 | –20 | | 20 | µA |
| $I_{IH}$ | Input high current | VIN = 3.3 V | | 33 | 100 | µA |
| $R_{PD}$ | Internal pulldown resistance | | | 100 | | kΩ |
| **nFAULT OUTPUT (OPEN-DRAIN OUTPUT)** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_O$ = 5 mA | | | 0.5 | V |
| $I_{OH}$ | Output high leakage current | $V_O$ = 3.3 V | | | 1 | µA |
| **DECAY INPUT** | | | | | | |
| $V_{IL}$ | Input low threshold voltage | For slow decay (brake) mode | 0 | | 0.8 | V |
| $V_{IH}$ | Input high threshold voltage | For fast decay (coast) mode | 2 | | | V |
| $I_{IN}$ | Input current | | | | ±40 | µA |
| $R_{PU}$ | Internal pullup resistance | | | 130 | | kΩ |
| $R_{PD}$ | Internal pulldown resistance | | | 80 | | kΩ |
| **H-BRIDGE FETS** | | | | | | |
| $R_{DS(ON)}$ | HS FET on resistance | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 25°C | | 0.1 | | Ω |
| | | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 85°C | | 0.13 | 0.16 | |
| $R_{DS(ON)}$ | LS FET on resistance | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 25°C | | 0.1 | | Ω |
| | | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 85°C | | 0.13 | 0.16 | |
| $I_{OFF}$ | Off-state leakage current | | –40 | | 40 | µA |
| **MOTOR DRIVER** | | | | | | |
| $f_{PWM}$ | Internal current control PWM frequency | | | 50 | | kHz |
| $t_{BLANK}$ | Current sense blanking time | | | 3.75 | | µs |
| $t_R$ | Rise time | | 30 | | 200 | ns |
| $t_F$ | Fall time | | 30 | | 200 | ns |
| **PROTECTION CIRCUITS** | | | | | | |
| $I_{OCP}$ | Overcurrent protection trip level | | 6 | | | A |
| $t_{TSD}$ | Thermal shutdown temperature | Die temperature | 150 | 160 | 180 | °C |
| **CURRENT CONTROL** | | | | | | |
| $I_{REF}$ | VREF input current | VREF = 3.3 V | –3 | | 3 | µA |
| $V_{TRIP}$ | ISENSE trip voltage | VREF = 3.3 V, 100% current setting | 635 | 660 | 685 | mV |
| $\Delta I_{TRIP}$ | Current trip accuracy (relative to programmed value) | VREF = 3.3 V, 5% current setting | –25% | | 25% | |
| | | VREF = 3.3 V, 10% - 34% current setting | –15% | | 15% | |
| | | VREF = 3.3 V, 38% - 67% current setting | –10% | | 10% | |
| | | VREF = 3.3 V, 71% - 100% current setting | –5% | | 5% | |
| $A_{ISENSE}$ | Current sense amplifier gain | Reference only | | 5 | | V/V |


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## 6.6 Typical Characteristics

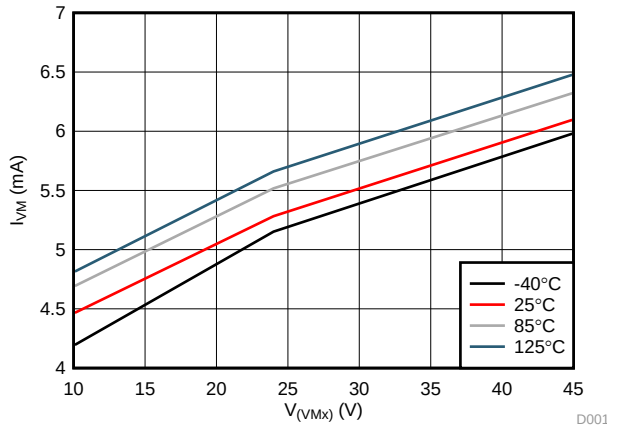


**Figure 1. $I_{VMx}$ vs $V_{(VMx)}$**

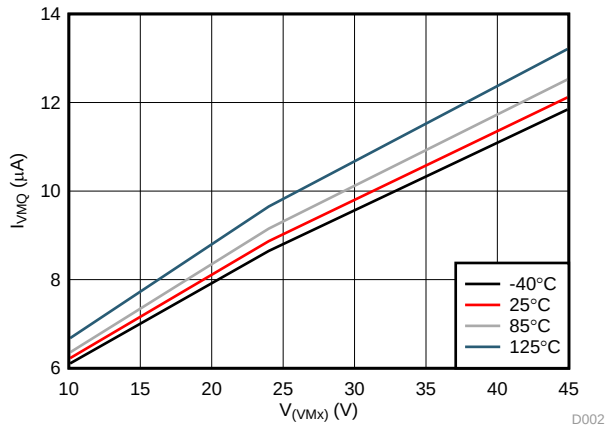


**Figure 2. $I_{VMxQ}$ vs $V_{(VMx)}$**

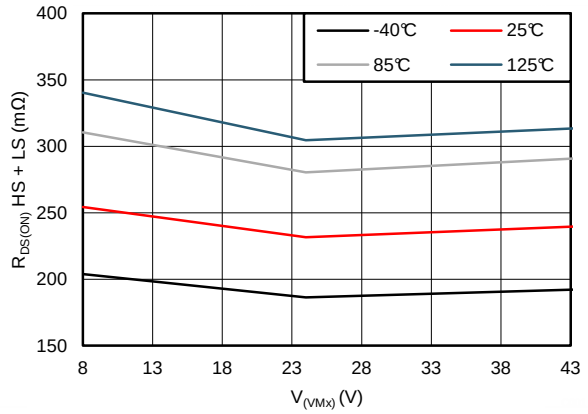


**Figure 3. $R_{DS(ON)}$ vs $V_{(VMx)}$**

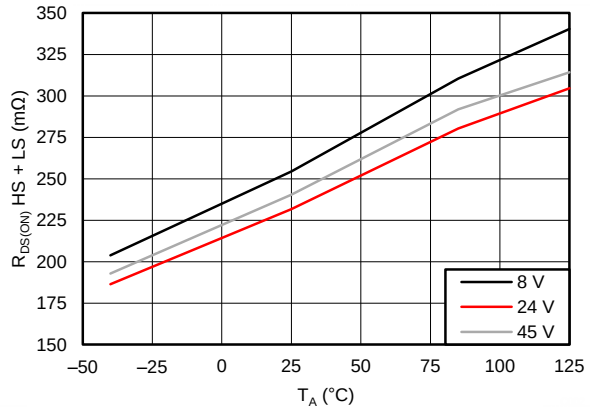


**Figure 4. $R_{DS(ON)}$ vs Temperature**

# 7 Detailed Description

## 7.1 Overview

The DRV8840 is an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device integrates a single NMOS H-bridge, charge pump, current sense, current regulation, and device protection circuitry. The DRV8828 can be powered from a single voltage supply from 8.2 V to 45 V, and is capable of providing a continuous output current up to 5 A.

A simple PHASE/ENBL interface allows for easy interfacing to an external controller. A 5 bit current control scheme allows for up to 32 discrete current levels. The current regulation method is adjustable between slow and fast decay.

Integrated protection circuits allows the device to monitor and protect against overcurrent, undervoltage, and overtemperature faults which are all reported through a fault indication pin (nFAULT). A low power sleep mode is integrated which allows the system to lower power consumption when not driving the motor.


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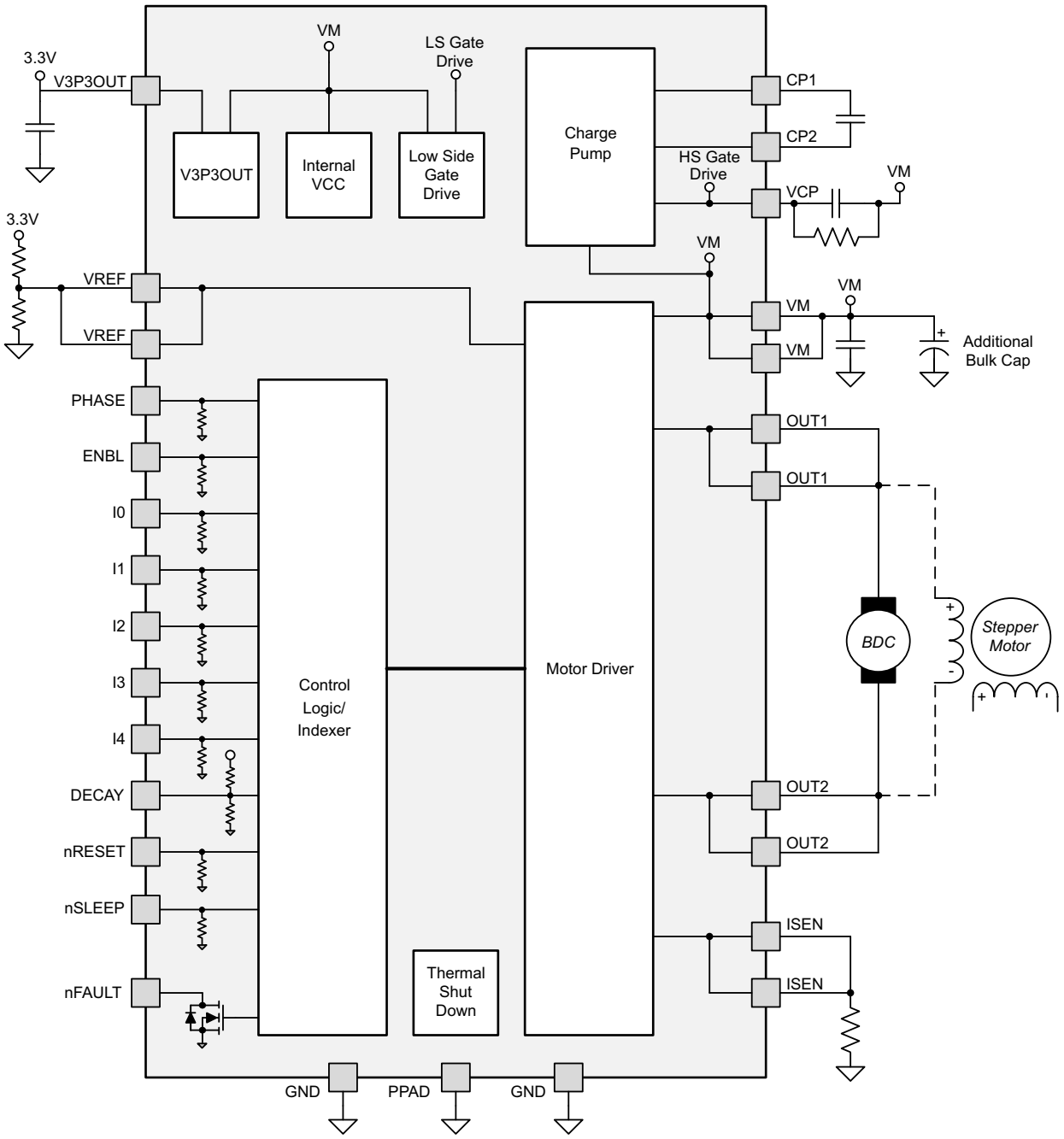
## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 PWM Motor Driver

The DRV8840 device contains one H-bridge motor driver with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 5.

## Feature Description (continued)

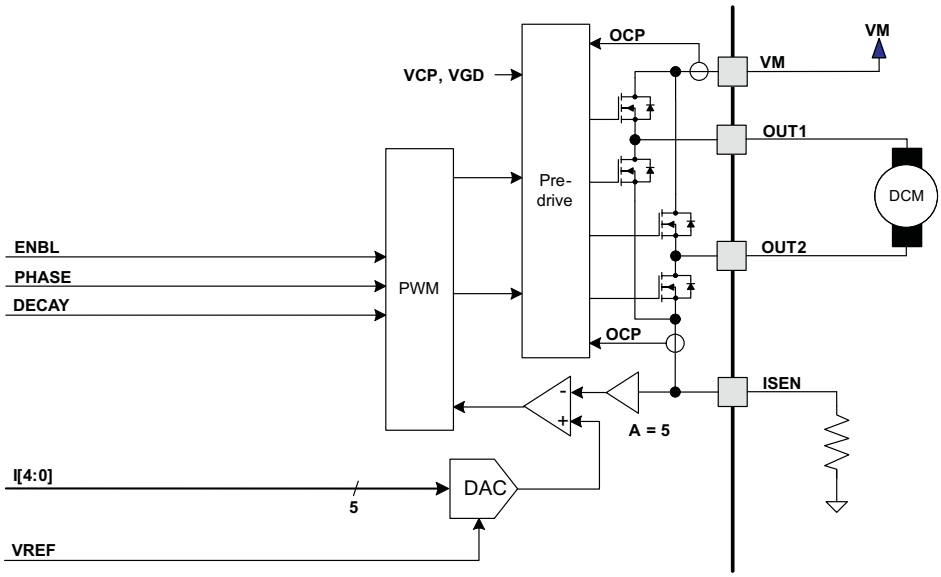



**Figure 5. Motor Control Circuitry**

There are multiple VM, ISEN, OUT, and VREF pins. All like-named pins must be connected together on the PCB.

### 7.3.2 Bridge Control

The PHASE input pin controls the direction of current flow through the H-bridge, and hence the direction of rotation of a DC motor. The ENBL input pin enables the H-bridge outputs when active high, and can also be used for PWM speed control of the motor. Note that the state of the DECAY pin selects the behavior of the bridge when ENBL = 0, allowing the selection of slow decay (brake) or fast decay (coast). Table 1 shows the logic.

**Table 1. H-Bridge Logic**

| DECAY | ENBL | PHASE | OUT1 | OUT2 |
|---|---|---|---|---|
| 0 | 0 | X | L | L |
| 1 | 0 | X | Z | Z |
| X | 1 | 1 | H | L |
| X | 1 | 0 | L | H |

The control inputs have internal pulldown resistors of approximately 100 kΩ.

### 7.3.3 Current Regulation

The maximum current through the motor winding is regulated by a fixed-frequency PWM current regulation, or current chopping. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For DC motors, current regulation is used to limit the start-up and stall current of the motor. Speed control is typically performed by providing an external PWM signal to the ENBLx input pins.

If the current regulation feature is not needed, it can be disabled by connecting the ISENSE pins directly to ground and the VREF pins to V3P3.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the ISEN pin, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the VREF pin, and is scaled by a 5-bit DAC that allows current settings of zero to 100% in an approximately sinusoidal sequence.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The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{REFX}}{5 \times R_{ISENSE}} \quad (1)$$

Example:

If a 0.25-Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current will be 2.5 V / (5 × 0.25 Ω) = 2 A.

Five input pins (I0 - I4) are used to scale the current in the bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The I0 - I4 pins have internal pulldown resistors of approximately 100 kΩ. The function of the pins is shown in Table 2.

**Table 2. Pin Functions**

| I[4..0] | RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT) |
|---|---|
| 0x00h | 0% |
| 0x01h | 5% |
| 0x02h | 10% |
| 0x03h | 15% |
| 0x04h | 20% |
| 0x05h | 24% |
| 0x06h | 29% |
| 0x07h | 34% |
| 0x08h | 38% |
| 0x09h | 43% |
| 0x0Ah | 47% |
| 0x0Bh | 51% |
| 0x0Ch | 56% |
| 0x0Dh | 60% |
| 0x0Eh | 63% |
| 0x0Fh | 67% |
| 0x10h | 71% |
| 0x11h | 74% |
| 0x12h | 77% |
| 0x13h | 80% |
| 0x14h | 83% |
| 0x15h | 86% |
| 0x16h | 88% |
| 0x17h | 90% |
| 0x18h | 92% |
| 0x19h | 94% |
| 0x1Ah | 96% |
| 0x1Bh | 97% |
| 0x1Ch | 98% |
| 0x1Dh | 99% |
| 0x1Eh | 100% |
| 0x1Fh | 100% |

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### 7.3.4 Decay Mode and Braking

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 6 as case 1. The current flow direction shown indicates the state when the xENBL pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 6 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 6 as case 3.

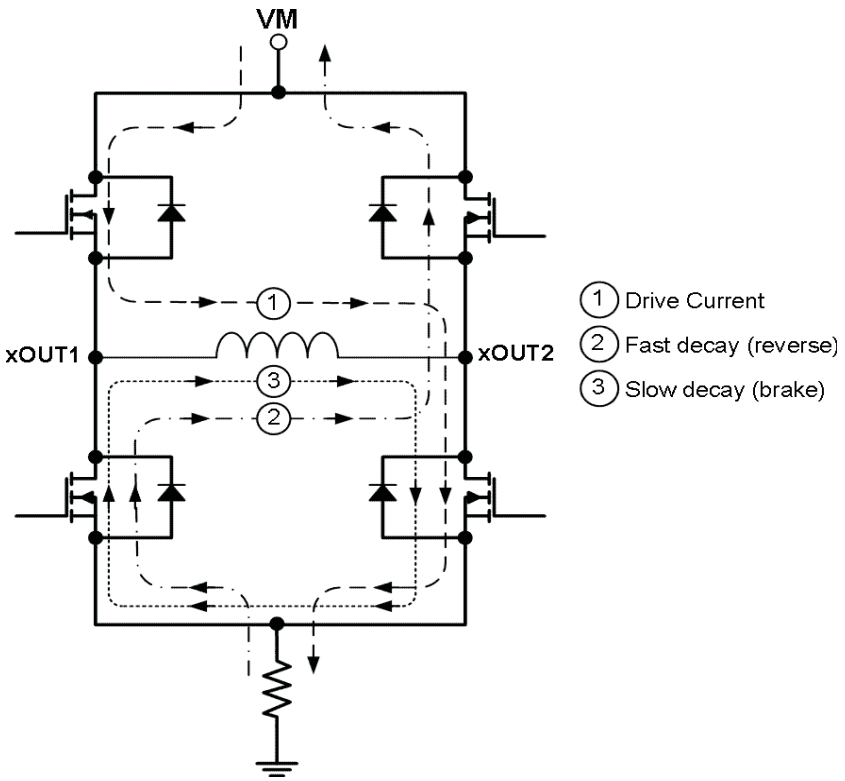


**Figure 6. Decay Mode**

The DRV8840 device supports fast decay and slow decay mode. Slow or fast decay mode is selected by the state of the DECAY pin - logic low selects slow decay, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven.

DECAY mode also affects the operation of the bridge when it is disabled (by taking the ENBL pin inactive). This applies if the ENABLE input is being used for PWM speed control of the motor, or if it is simply being used to start and stop motor rotation.

If the DECAY pin is high (fast decay), when the bridge is disabled fast decay mode will be entered until the current through the bridge reaches zero. Once the current is at zero, the bridge is disabled to prevent the motor from reversing direction. This allows the motor to coast to a stop.

If the DECAY pin is low (slow decay), both low-side FETs will be turned on when ENBL is made inactive. This essentially shorts out the back EMF of the motor, causing the motor to brake, and stop quickly. The low-side FETs will stay in the ON state even after the current reaches zero.


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### 7.3.5 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on time of the PWM.

### 7.3.6 Protection Circuits

The DRV8840 device is fully protected against undervoltage, overcurrent and overtemperature events.

#### *7.3.6.1 Overcurrent Protection (OCP)*

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the $I_{SENSE}$ resistor value or VREF voltage.

#### *7.3.6.2 Thermal Shutdown (TSD)*

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

#### *7.3.6.3 Undervoltage Lockout (UVLO)*

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when $V_M$ rises above the UVLO threshold.

## 7.4 Device Functional Modes

### 7.4.1 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge driver. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational. Note that nRESET and nSLEEP have internal pulldown resistors of approximately 100 kΩ. These signals need to be driven to logic high for device operation.

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The DRV8840 device is used in brushed motor or stepper motor control. The onboard current regulation allows for limiting the motor current through simple pin configurations.

## 8.2 Typical Application

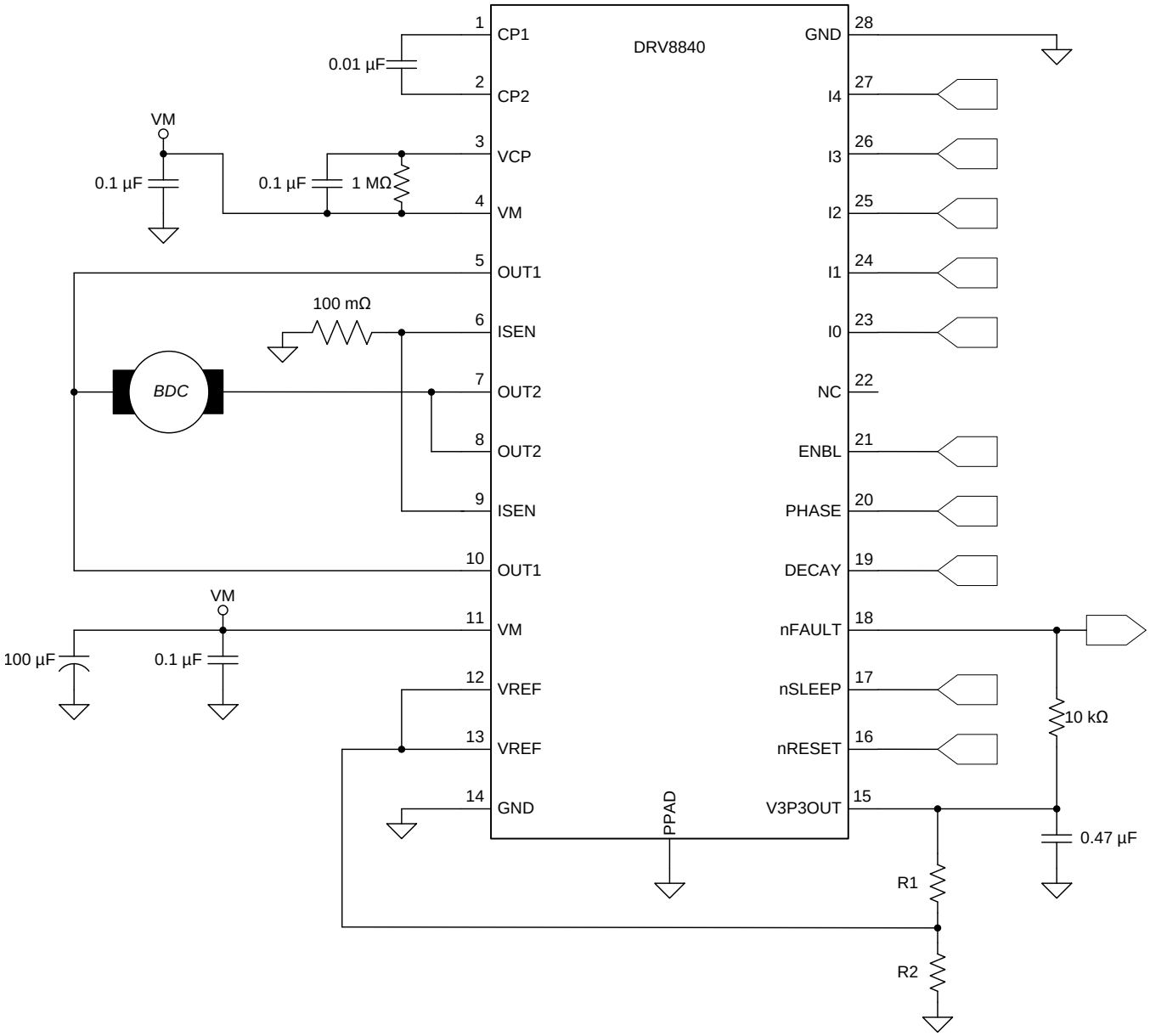


**Figure 7. Typical Application Schematic**


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## Typical Application (continued)

### 8.2.1 Design Requirements

Table 3 shows the design parameters for this application.

**Table 3. Design Parameters**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Supply Voltage | VM | 24 V |
| Motor Winding Resistance | RM | 3.9 V |
| Motor Winding Inductance | LM | 2.9 mH |
| Target Chopping Current | ITRIP | 1.5 A |
| Sense Resistor | RSENSE | 100 mΩ |
| VREF Voltage | VREF | 0.75 V |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Current Regulation*

The maximum current ($I_{TRIP}$) is set by the Ix pins, the VREF analog voltage, and the sense resistor value ($R_{SENSE}$). When starting a brushed DC motor, a large inrush current may occur because there is no back-EMF and high detent torque. Current regulation will act to limit this inrush current and prevent high current on start-up.

$$I_{TRIP} / (5 \times R_{SENSE}) \quad (2)$$

**Example:** If the desired chopping current is 1.5 A:

- Set RSENSE = 100 mΩ
- VREF would have to be 0.75 V
- Create a resistor divider network from V3P3OUT (3.3 V) to set VREF = 0.75 V
- Set R2 = 10 kΩ and set R1 = 3 kΩ

#### *8.2.2.2 Sense Resistor*

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $Irms^2 \times R$. For example, if the RMS motor current is 1.5 A and a 200-mΩ sense resistor is used, the resistor will dissipate $1.5\ A^2 \times 0.2\ \Omega = 0.3$ W. The power quickly increases with greater current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

### 8.2.3 Application Curves

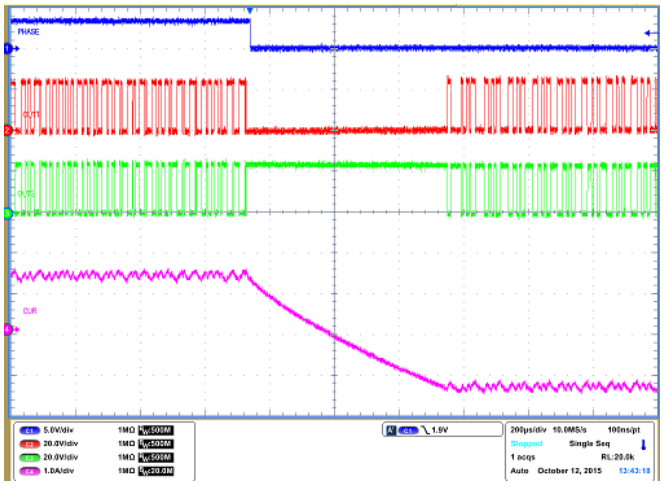


**Figure 8. DRV8842 Current Regulation**

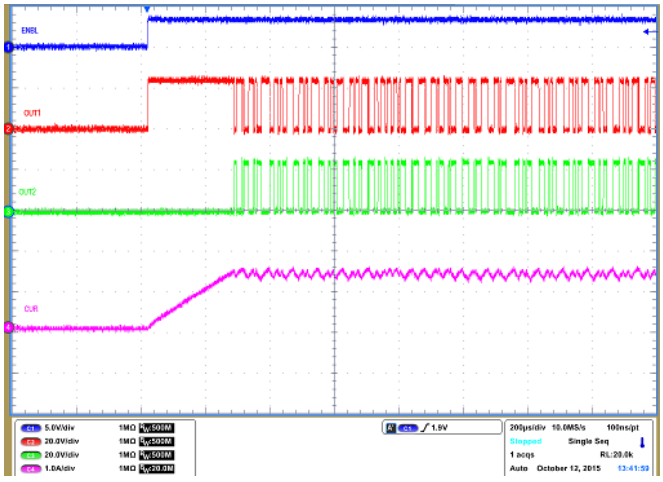


**Figure 9. DRV8842 Direction Change**


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# 9 Power Supply Recommendations

The DRV8840 is designed to operate from an input voltage supply (VM) range from 8.2 V to 45 V. The device has an absolute maximum rating of 47 V. A 0.1-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8840 as possible. In addition, a bulk capacitor must be included on VM.

## 9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be greater than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

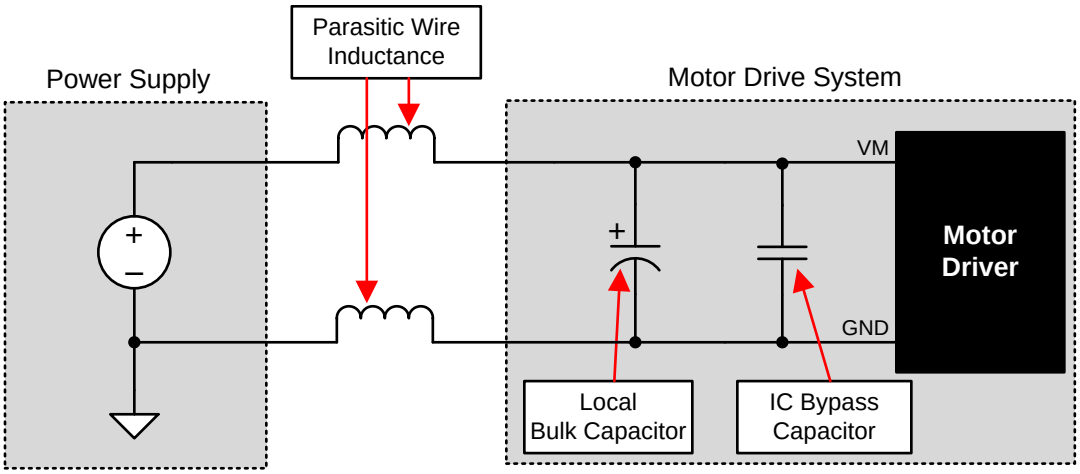


**Figure 10. Setup of Motor Drive System With External Power Supply**

# 10 Layout

## 10.1 Layout Guidelines

Each VM terminal must be bypassed to GND using a low-ESR ceramic bypass capacitors with recommended values of 0.1 µF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.1 µF rated for VM . Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.47 µF rated for 16 V. Place this component as close to the pins as possible. In addition, place a 1 MΩ between VM and VCP.

Bypass V3P3OUT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

The current sense resistor should be placed as close as possible to the device pins to minimize trace inductance between the pin and resistor.

## 10.2 Layout Example

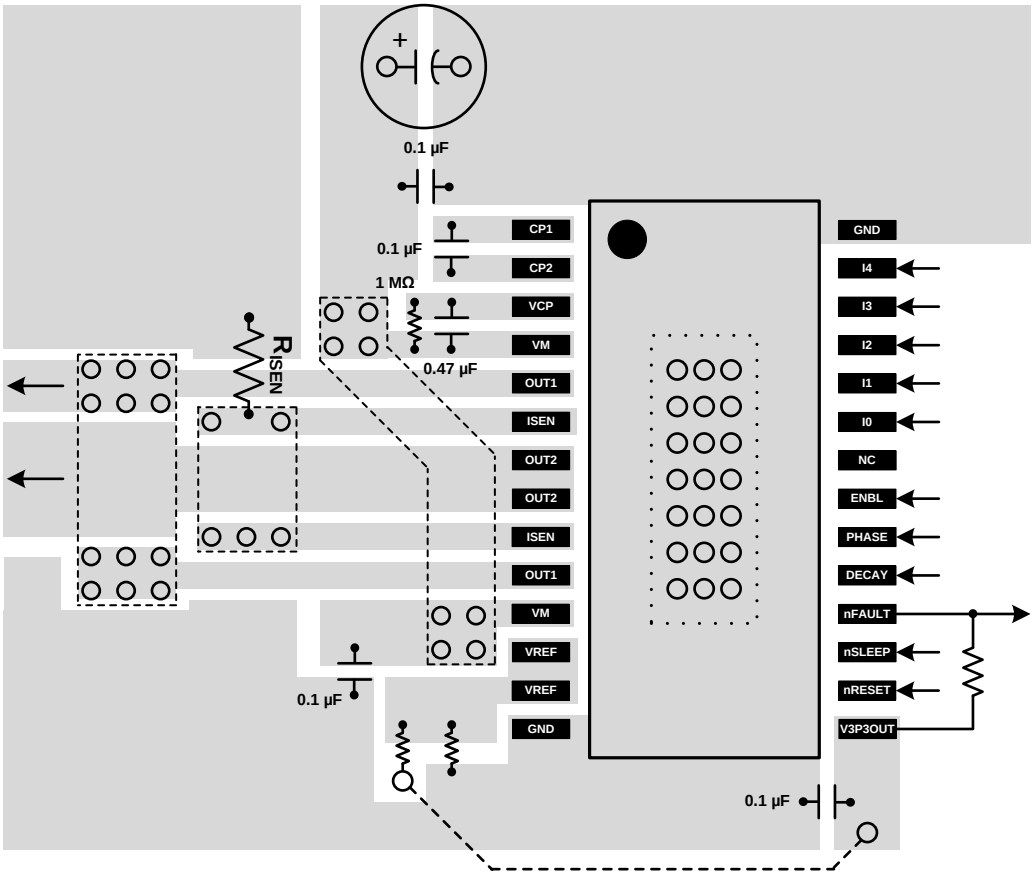


**Figure 11. Example Layout**


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## 10.3 Thermal Considerations

The DRV8840 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### 10.3.1 Power Dissipation

Average power dissipation in the DRV8840 when running a DC motor can be roughly estimated by: Equation 3.

$$P = 2 \times R_{DS(ON)} \times \left(I_{OUT}\right)^2$$

where

- P is the power dissipation of one H-bridge
- $R_{DS(ON)}$ is the resistance of each FET
- $I_{OUT}$ is the RMS output current being applied to each winding. (3)

$I_{OUT}$ is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

### 10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multilayer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see the TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and the TI application brief, *PowerPAD™ Made Easy* (SLMA004), available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

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# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8840PWP | ACTIVE | HTSSOP | PWP | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8840 | Samples |
| DRV8840PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8840 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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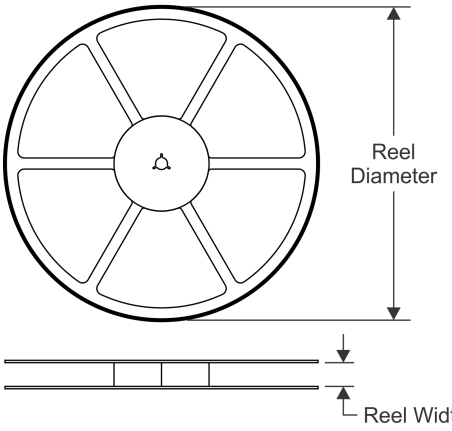
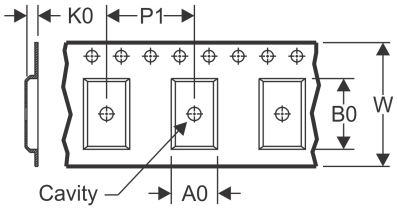
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

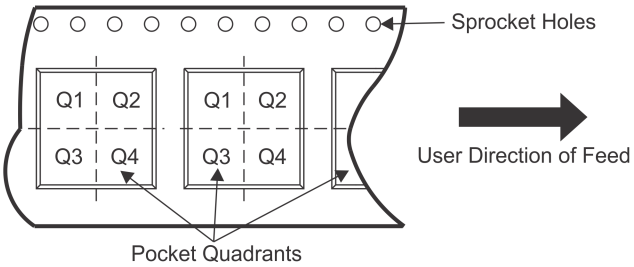



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

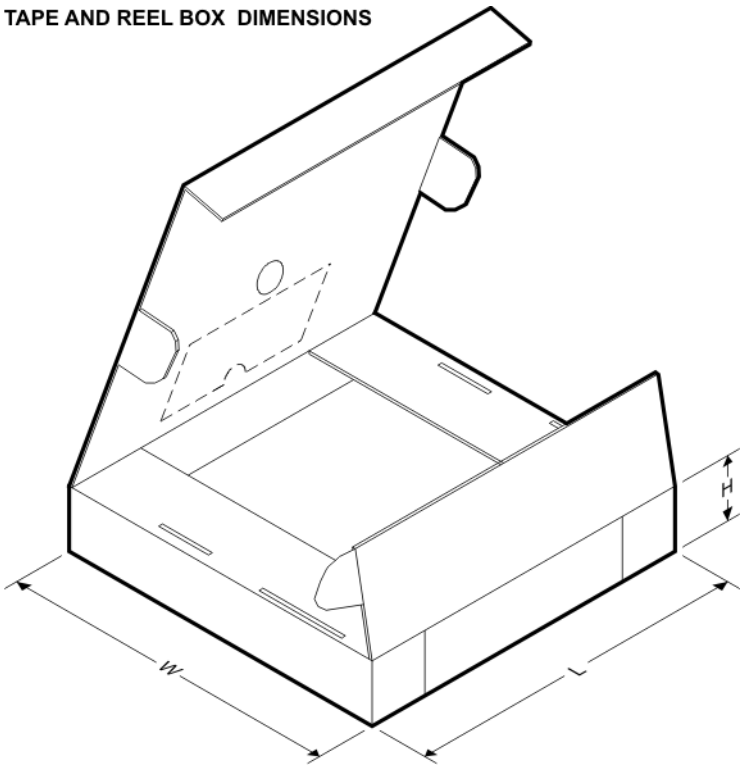
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8840PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8840PWPR | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |

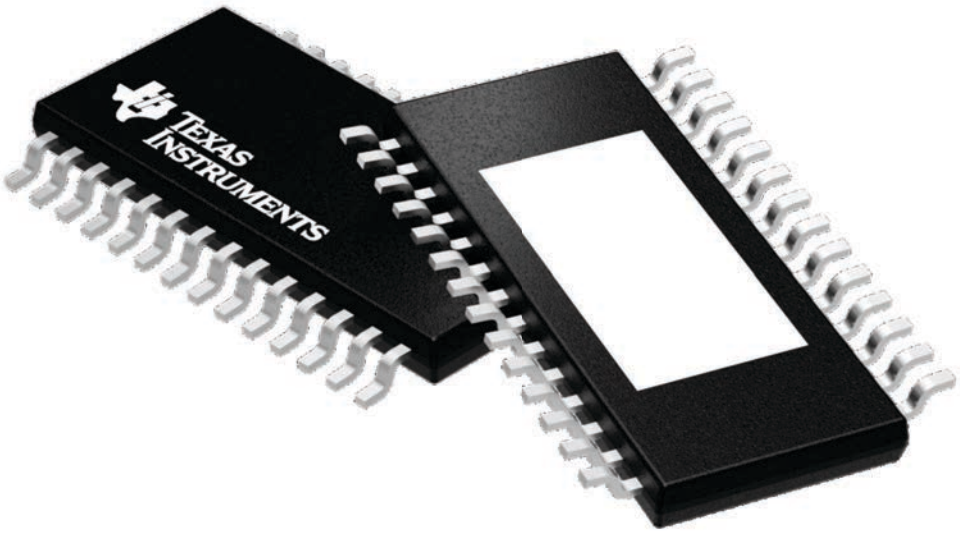
# GENERIC PACKAGE VIEW

## PWP 28

## PowerPAD™ TSSOP - 1.2 mm max height

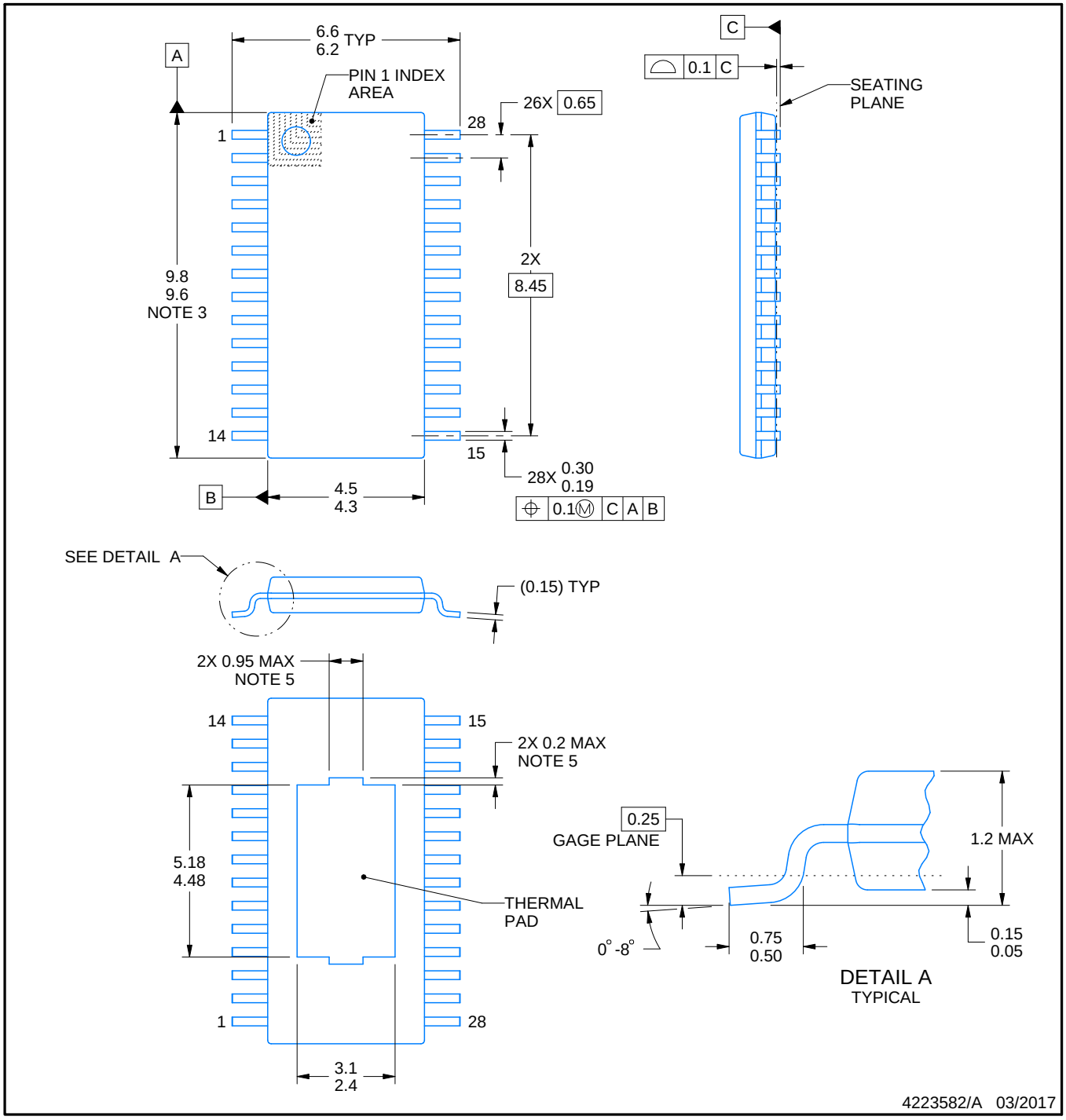
**4.4 x 9.7, 0.65 mm pitch**

SMALL OUTLINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

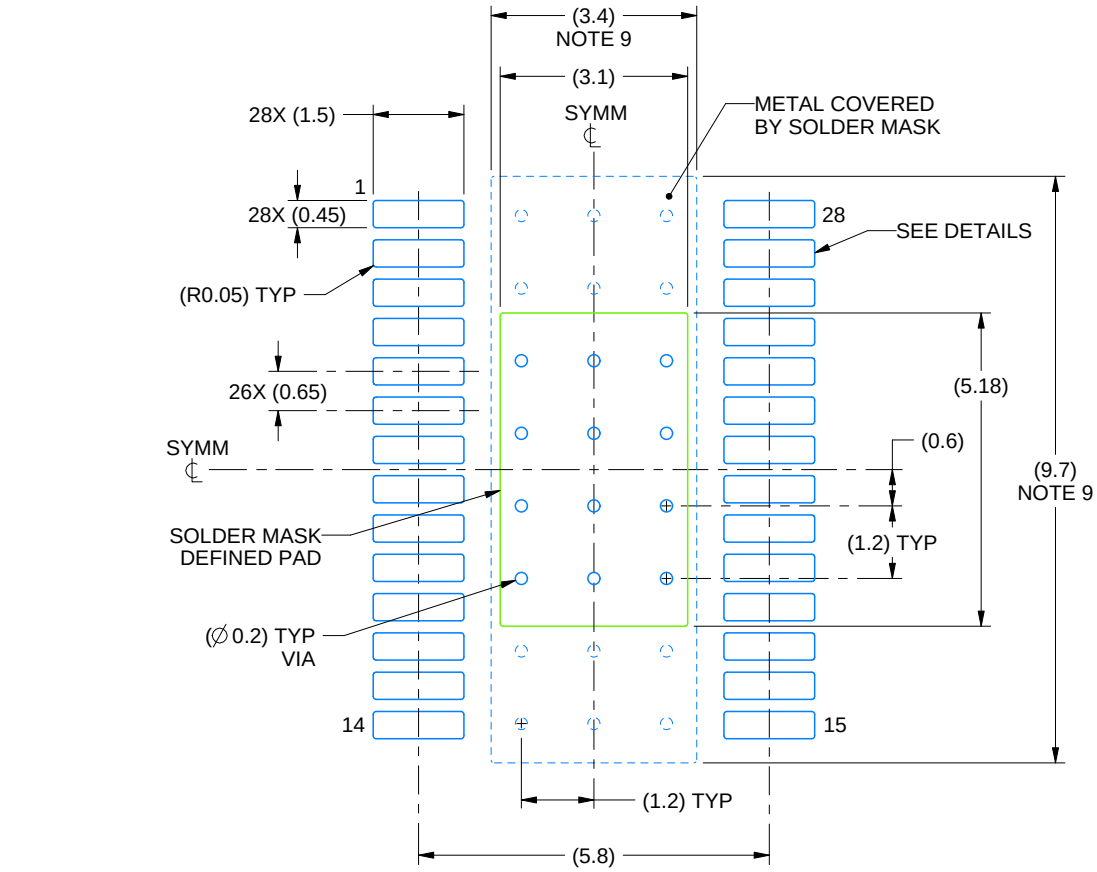
4224765/A



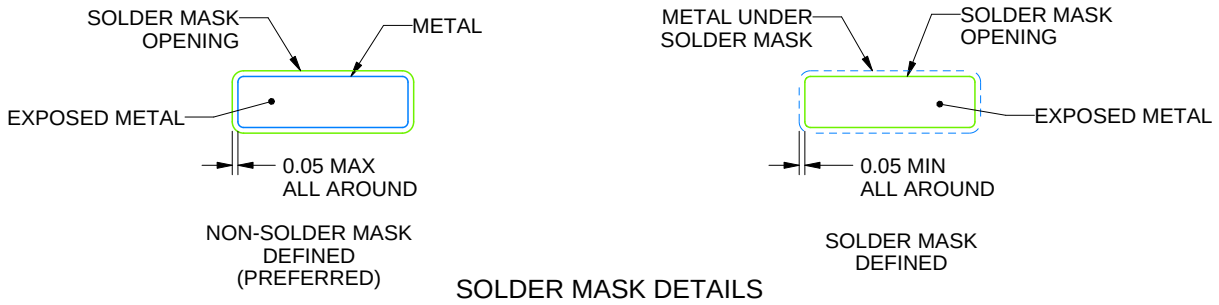

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

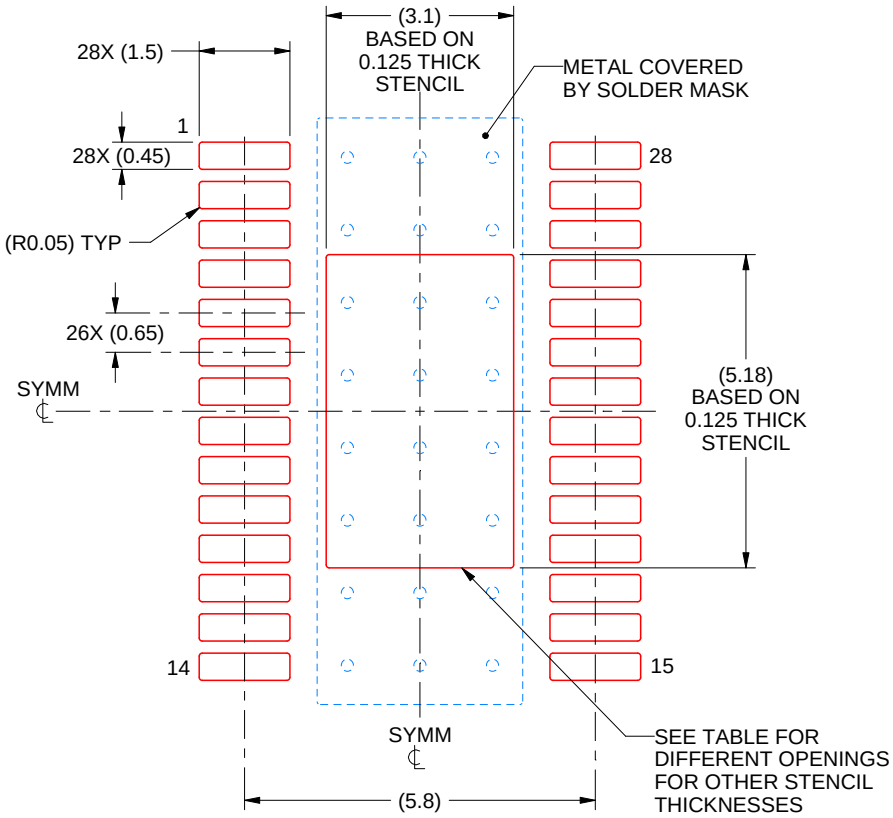



SOLDER MASK DETAILS

4223582/A 03/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.47 X 5.79 |
| 0.125 | 3.10 X 5.18 (SHOWN) |
| 0.15 | 2.83 X 4.73 |
| 0.175 | 2.62 X 4.38 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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