

Over-Voltage Protection Load Switch with Surge Protection

Features

- Highly reliable QFN 1.3mm×1.8mm-12L package
- Surge protection
 - IEC 61000-4-5: > 100V
- Integrated low R_{dson} nFET switch: typical 27mΩ
- 5A continuous current capability
- Default Over-Voltage Protection threshold: 9.98V
- OVP threshold adjustable range: 4V to 24V
- Input system ESD protection
 - IEC 61000-4-2 Contact discharge: ±8kV
 - IEC 61000-4-2 Air gap discharge: ±15kV
- Input maximum voltage rating: 28V_{DC}
- Fast turn-off response: typical 100ns
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO)

Applications

- Smartphones
- Tablets
- Charging Ports

General Description

The AW32919 OVP load switch features surge protection, an internal clamp circuit protects the device from surge voltages up to 100V.

The AW32919 features an ultra-low 27mΩ (typ.) R_{dson} nFET load switch. When input voltage exceeds the OVP threshold, the switch is turned off very fast to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages up to 28V_{DC}.

The default OVP threshold is 9.98V, the OVP threshold can be adjusted from 4V to 24V through external OVLO pin.

The device features an open-drain output \overline{ACOK} , when $V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}$ and the switch is on, \overline{ACOK} will be driven low to indicate a good power input, otherwise it is high impedance.

This device features over-temperature protection that prevents itself from thermal damaging.

Typical Application Circuit

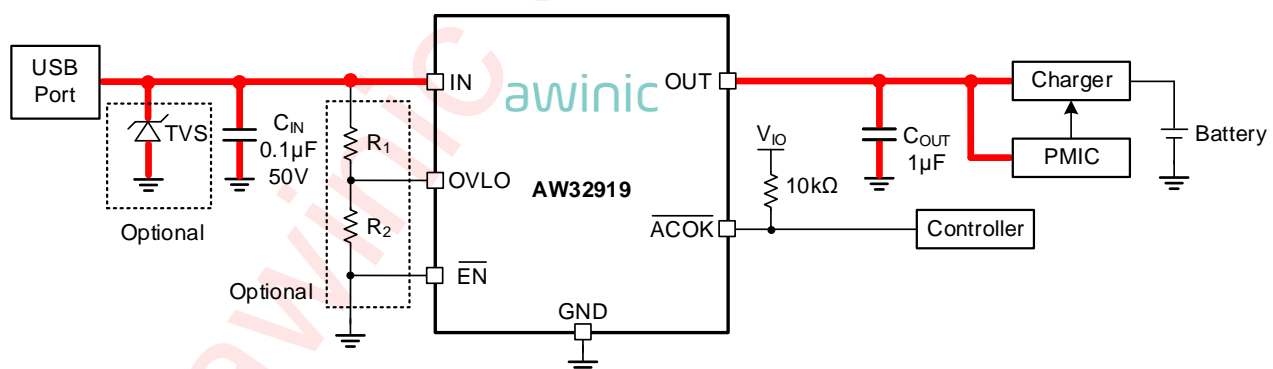


Figure 1 AW32919 Typical Application Circuit

R_1 and R_2 are used for OVP threshold adjustment, to use default OVP threshold, connect OVLO to ground.

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Pin Configuration and Top Mark

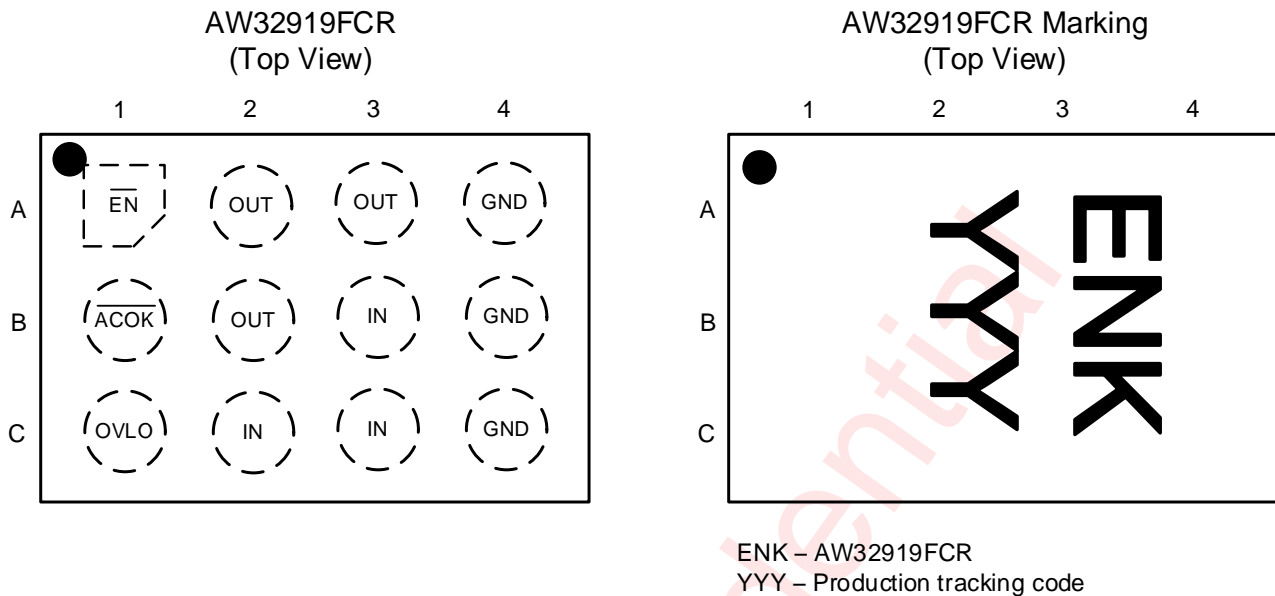


Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
A1	$\overline{\text{EN}}$	Enable pin, active low
B1	$\overline{\text{ACOK}}$	Power good flag, active-low, open-drain output. When $V_{\text{IN_UVLO}} < V_{\text{IN}} < V_{\text{IN_OVLO}}$, $\overline{\text{ACOK}}$ is pulled low, otherwise it's hi-Z state
C1	OVLO	OVP threshold adjustment pin
C2, C3, B3	IN	Switch input and device power supply
A2, A3, B2	OUT	Switch output
A4, B4, C4	GND	Device ground

Functional Block Diagram

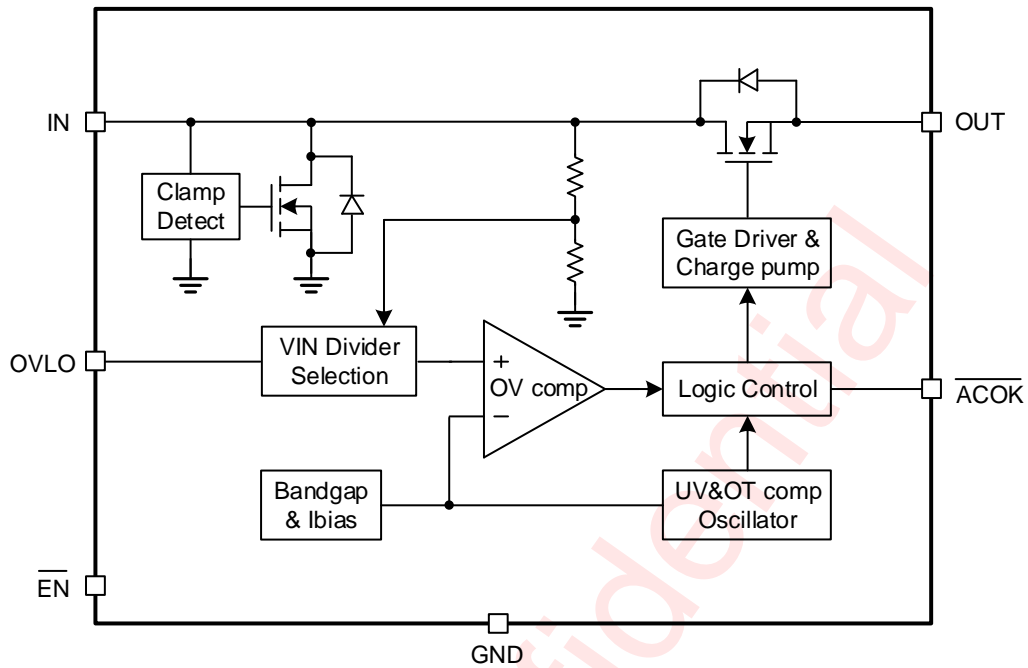


Figure 3 Functional Block Diagram

Typical Application Circuits

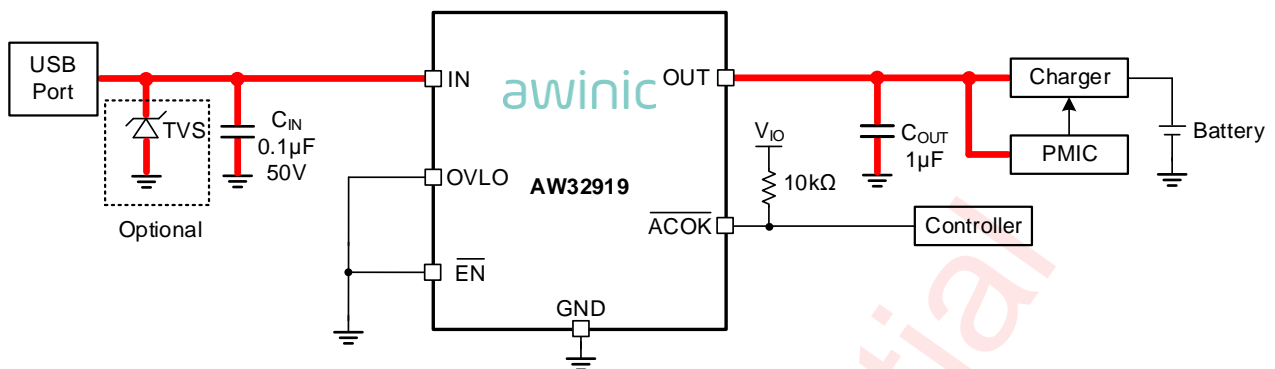


Figure 4 AW32919 Typical Application Circuit(Using Default OVP Threshold)

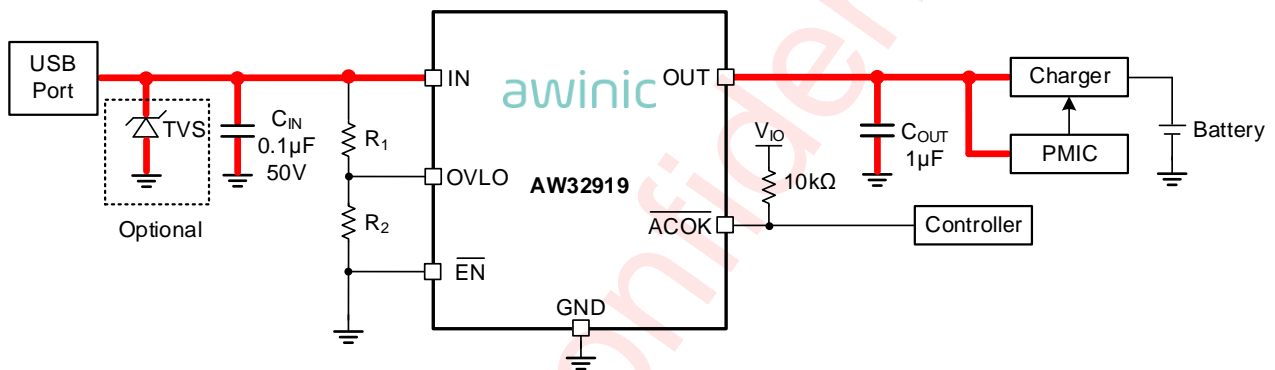


Figure 5 AW32919 Typical Application Circuit(Using External Resistors Set OVP Threshold)

Notice for Typical Application Circuits:

1. If VBUS is required to pass surge voltage greater than 100V, external TVS is needed, the maximum clamping voltage of the TVS should be below 32V.
2. When the default OVP threshold is used, connect OVLO pin to GND directly or through a 0Ω resistor. **OVLO pin cannot be left floating.**
3. If R₁ and R₂ are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision.
4. If $\overline{\text{ACOK}}$ is not used, it can be left floating, or short to GND.
5. C_{IN} = 0.1µF is recommended for typical application, larger C_{IN} is also acceptable. The rated voltage of C_{IN} should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW32919 is used, the rated voltage of C_{IN} should be 50V.
6. C_{OUT} = 1µF is recommended for typical application, larger C_{OUT} is also acceptable. The rated voltage of C_{OUT} should be larger than the OVP threshold. For example, if the OVP threshold is 9.98V, the rated voltage of C_{OUT} should be 16V or higher.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW32919FCR	-40°C – 85°C	QFN 1.3mm×1.8mm -12L	ENK	MSL1	ROHS+HF	4500 units/ Tape and Reel

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Absolute Maximum Ratings ^(NOTE 1)

Symbol	Parameter	Condition	Min.	Max.	Unit
V _{IN}	Input voltage		-0.3	29	V
V _{OUT}	Output voltage		-0.3	See ^(NOTE 2)	V
V _{OVLO}	OVLO voltage		-0.3	6	V
V _{ACOK}	ACOK voltage		-0.3	6	V
V _{EN}	EN voltage		-0.3	6	V
I _{SW}	Continuous current of switch IN-OUT ^(NOTE 3)	Continuous current on IN and OUT pin		5	A
I _{PEAK}	Peak current	Peak input and output current on IN and OUT pin(10ms)		8	A
I _{DIODE}	Continuous diode current	Continuous forward current through the nFET body diode		1.5	A
T _A	Ambient temperature		-40	85	°C
T _J	Junction temperature		-40	150	°C
T _{STG}	Storage temperature		-65	150	°C
T _{LEAD}	Soldering temperature	At leads, 10 seconds		260	°C
Surge	Input surge protection	IEC61000-4-5 test with 2Ω equivalent series resistance	100		V

NOTE1: Conditions out of those ranges listed in “absolute maximum ratings” may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in “recommended operating conditions”. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: 29V or V_{IN}+0.3V, whichever is smaller.

NOTE3: Limited by thermal design.

Thermal Information

Symbol	Parameter	Condition	Value	Unit
R _{θJA}	Thermal resistance from junction to ambient ^(NOTE 1)	In free air	65	°C/W

NOTE1: Thermal resistance from junction to ambient is highly dependent on PCB layout.

ESD and Latch-up Ratings

Symbol	Parameter	Condition	Value	Unit
V _{ESD}	IEC61000-4-2 system ESD on IN pin with 0.1μF C _{IN}	Contact discharge	±8	kV
		Air gap discharge	±15	kV
	Human Body Model	ESDA/JEDEC JS-001-2017	±2	kV
	Charged Device Model	ESDA/JEDEC JS-002-2018	±1.5	kV
I _{Latch-up}	Latch-up	JESD78E	±200	mA

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IN}	Input DC voltage	3		28	V
C _{IN}	Input capacitance		0.1		μF
C _{OUT}	Output load capacitance		1		μF

Electrical Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise noted. Typical values are guaranteed for $V_{IN} = 5\text{V}$, $C_{IN} = 0.1\mu\text{F}$, $I_{IN} \leq 5\text{A}$ and $T_A = 25^{\circ}\text{C}$.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{IN_CLAMP}	Input clamp voltage	$I_{IN} = 10\text{mA}$		32.2		V
R_{dson}	Switch on resistance	$V_{IN} = 5\text{V}$, $I_{OUT} = 1\text{A}$, $T_A = 25^{\circ}\text{C}$		27	37	$\text{m}\Omega$
I_Q	Input quiescent current	$V_{IN} = 5\text{V}$, $V_{OVLO} = 0\text{V}$, $I_{OUT} = 0\text{A}$		91	180	μA
I_{IN_OVLO}	Input current at over-voltage condition	$V_{IN} = 5\text{V}$, $V_{OVLO} = 3\text{V}$, $V_{OUT} = 0\text{V}$		80	160	μA
V_{OVLO_TH}	OVLO set threshold		1.16	1.20	1.24	V
V_{OVLO_RNG}	OVP threshold adjustable range		4		24	V
V_{OVLO_SEL}	External OVLO select threshold	OVLO rising	0.19	0.26	0.33	V
		Hysteresis		0.06		V
I_{OVLO}	OVLO pin leakage current	$V_{OVLO} = V_{OVLO_TH}$	-0.2		0.2	μA
Protection						
V_{IN_OVLO}	OVP trip level	V_{IN} rising	9.78	9.98	10.18	V
		Hysteresis		0.21		
V_{IN_UVLO}	UVLO trip level	V_{IN} rising		2.9	3.0	V
		Hysteresis		0.1		V
T_{SDN}	Shutdown temperature			150		$^{\circ}\text{C}$
T_{SDN_HYS}	Shutdown temperature hysteresis			20		$^{\circ}\text{C}$
Digital Logical Interface						
V_{OL}	\overline{ACOK} output low voltage	$I_{SINK} = 1\text{mA}$			0.4	V
I_{LEAK_ACOK}	\overline{ACOK} leakage current	$V_{IO} = 5\text{V}$, \overline{ACOK} de-asserted	-0.5		0.5	μA
V_{IH}	\overline{EN} input high voltage		1.2			V
V_{IL}	\overline{EN} input low voltage				0.5	V

Electrical Characteristics (Continued)

$T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise noted. Typical values are guaranteed for $V_{IN} = 5\text{V}$, $C_{IN} = 0.1\mu\text{F}$, $I_{IN} \leq 5\text{A}$ and $T_A = 25^{\circ}\text{C}$.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
I_{LEAK_EN}	\overline{EN} leakage current	$V_{EN} = 5\text{V}$	0		2	μA
Timing Characteristics (Figure 6)						
t_{DEB}	Debounce time	From $V_{IN} > V_{IN_UVLO}$ to 10% V_{OUT}		15		ms
t_{START}	Start-up time	From $V_{IN} > V_{IN_UVLO}$ to \overline{ACOK} low		30		ms
t_{ON}	Switch turn-on time	$R_L = 100\Omega$, $C_L = 22\mu\text{F}$, V_{OUT} from 10% V_{IN} to 90% V_{IN}		1		ms
t_{OFF}	Switch turn-off time	$C_L = 0\mu\text{F}$, $R_L = 100\Omega$, $V_{IN} > V_{IN_OVLO}$ to V_{OUT} stop rising, V_{IN} rise at $10\text{V}/\mu\text{s}$		100		ns

Timing Diagram

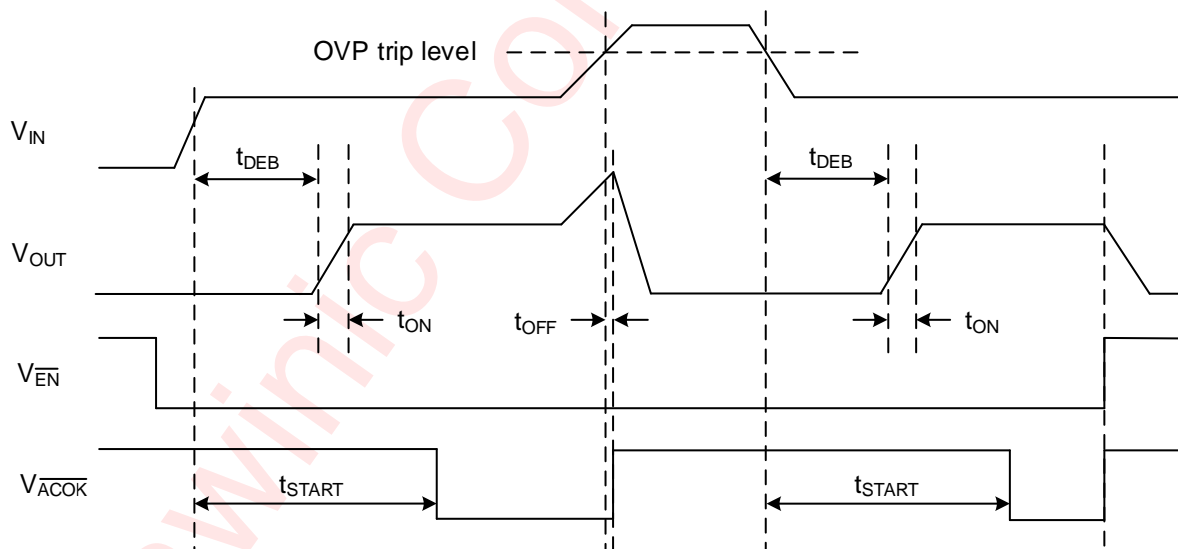


Figure 6 Timing Diagram

Typical Characteristics

$V_{IN} = 5V$, $V_{EN} = 0V$, $V_{OVLO} = 0V$, $C_{IN} = 0.1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ unless otherwise specified.

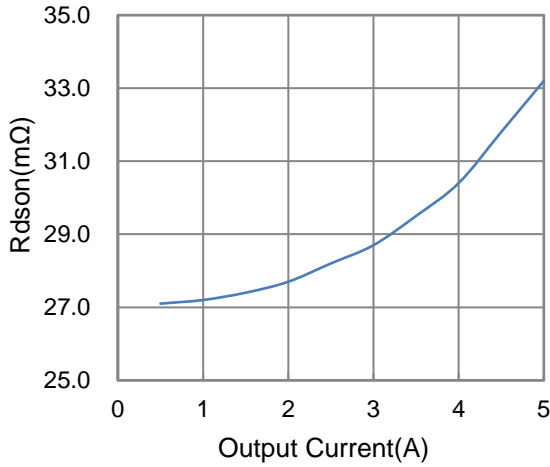


Figure 7 R_{dson} vs. Output Current

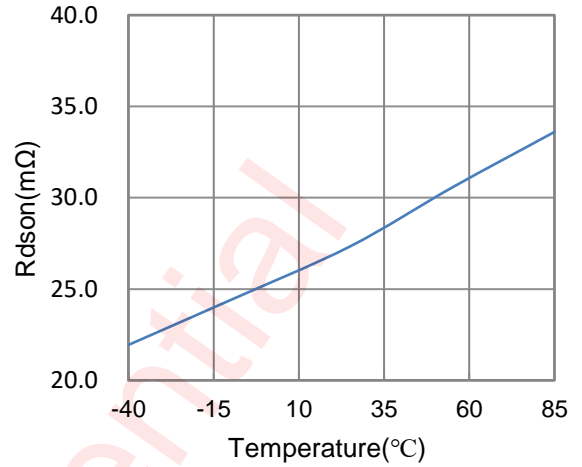


Figure 8 R_{dson} vs. Temp. ($I_{OUT} = 1A$)

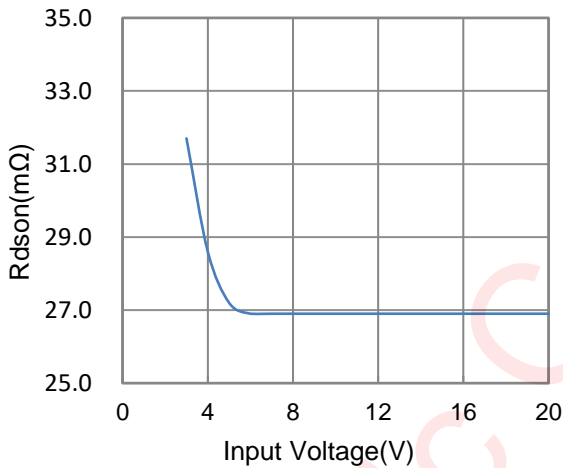


Figure 9 R_{dson} vs. Input Voltage ($I_{OUT} = 1A$)

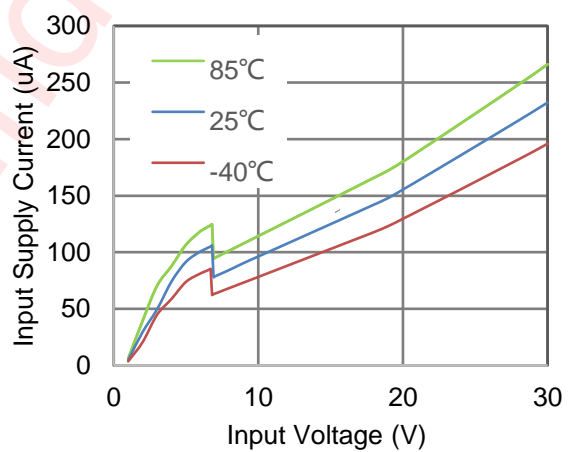


Figure 10 Input Supply Current vs. Supply Voltage

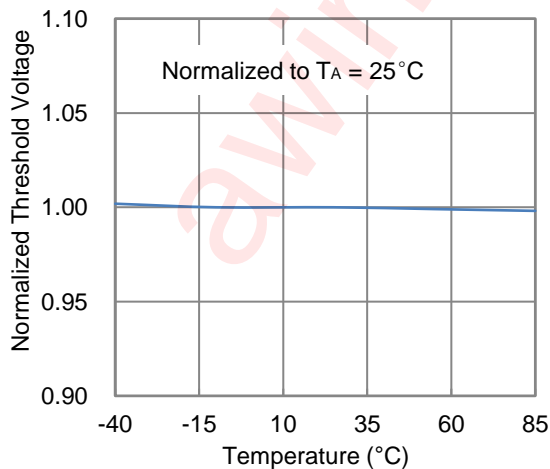


Figure 11 Normalized Internal OVP Threshold vs. Temp.

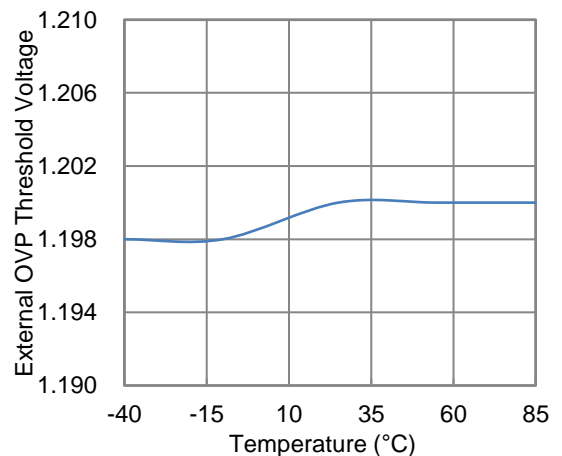


Figure 12 OVLO Set Threshold vs. Temp.

Typical Characteristics (Continued)

$V_{IN} = 5V$, $V_{EN} = 0V$, $V_{OVLO} = 0V$, $C_{IN} = 0.1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ unless otherwise specified.

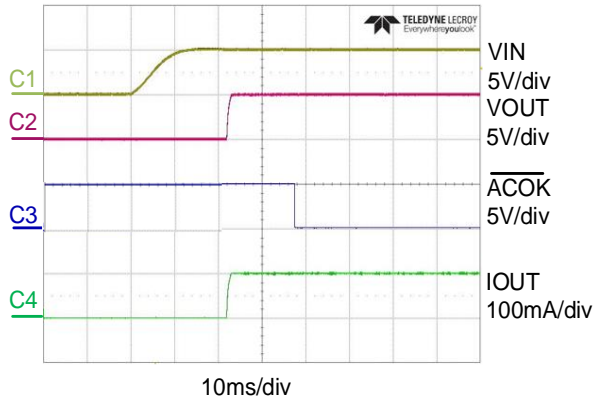


Figure 13 Power-up ($C_{OUT} = 1\mu F$, 100mA load).

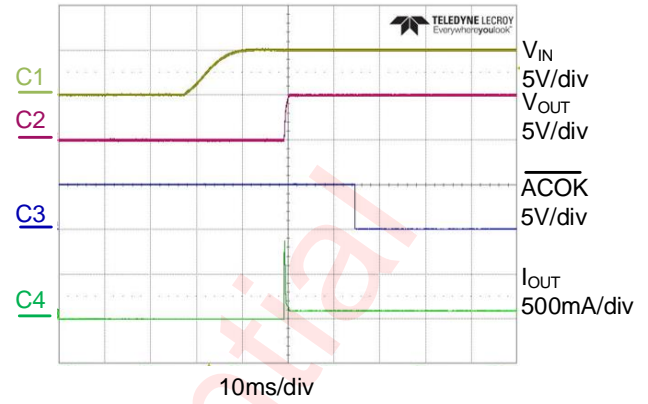


Figure 14 Power-up ($C_{OUT} = 100\mu F$, 100mA load)

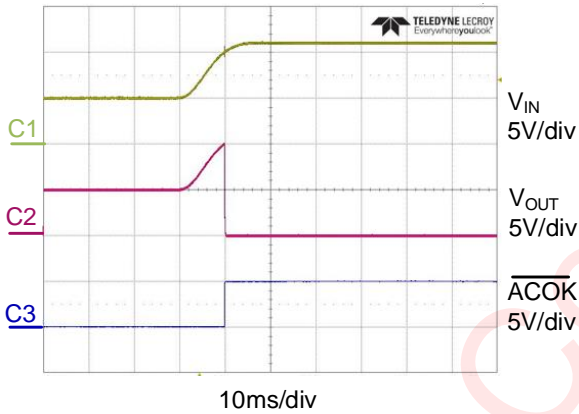


Figure 15 OVP Response

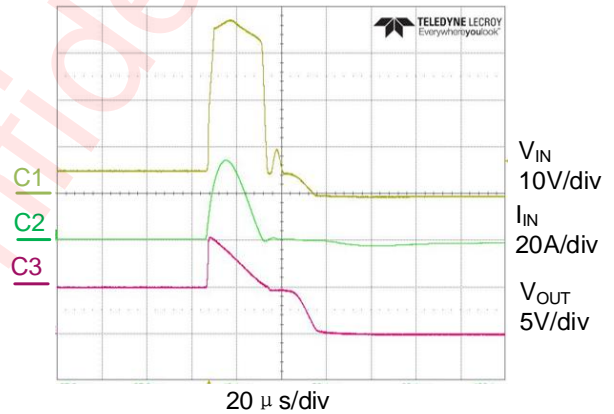


Figure 16 100V Surge Response($R_{OUT}=50\Omega$)

Functional Description

Device Operation

If the AW32919 is enabled and the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on. $\overline{\text{ACOK}}$ will be driven low about 30ms after V_{IN} valid, indicating the switch is on with a good power input. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 100ns. If $\overline{\text{EN}}$ is pulled high, or input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

Surge Protection

The AW32919 integrates a clamp circuit to suppress input surge voltage. For surge voltages between $V_{\text{IN_OVLO}}$ and $V_{\text{IN_CLAMP}}$, the switch will be turned off but the clamp circuit will not work. For surge voltages greater than $V_{\text{IN_CLAMP}}$, the internal clamp circuit will detect surge voltage level and discharge the surge energy to ground. The device can suppress surge voltages up to 100V.

Over-Voltage Protection

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 100ns. The switch will remain off until V_{IN} falls below the OVP falling trip level.

OVP Threshold Adjustment

If the default OVP threshold is used, OVLO pin must be grounded. If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be adjusted as following:

$$V_{\text{IN_OVLO}} = \frac{R_1 + R_2}{R_2} V_{\text{OVLO_TH}}$$

For example, if we select $R_1 = 1\text{M}\Omega$ and $R_2 = 100\text{k}\Omega$, then the new OVP threshold calculated from the above formula is 13.2V. The OVP threshold adjustment range is from 4V to 24V. When the OVLO pin voltage V_{OVLO} exceeds $V_{\text{OVLO_SEL}}$ (0.26V typical), V_{OVLO} is compared with the reference voltage $V_{\text{OVLO_TH}}$ (1.2V typical) to judge whether input supply is over-voltage.

$\overline{\text{ACOK}}$ Output

The device features an open-drain output $\overline{\text{ACOK}}$, it should be connected to the system I/O rail through a pull-up resistor. If the device is enabled and $V_{\text{IN_UVLO}} < V_{\text{IN}} < V_{\text{IN_OVLO}}$, $\overline{\text{ACOK}}$ will be driven low indicating the switch is on with a good power input. If OVP, UVLO, or OT occurs, or $\overline{\text{EN}}$ is pulled high, the switch will be turned off and $\overline{\text{ACOK}}$ will be pulled high.

USB On-The-Go (OTG) Operation

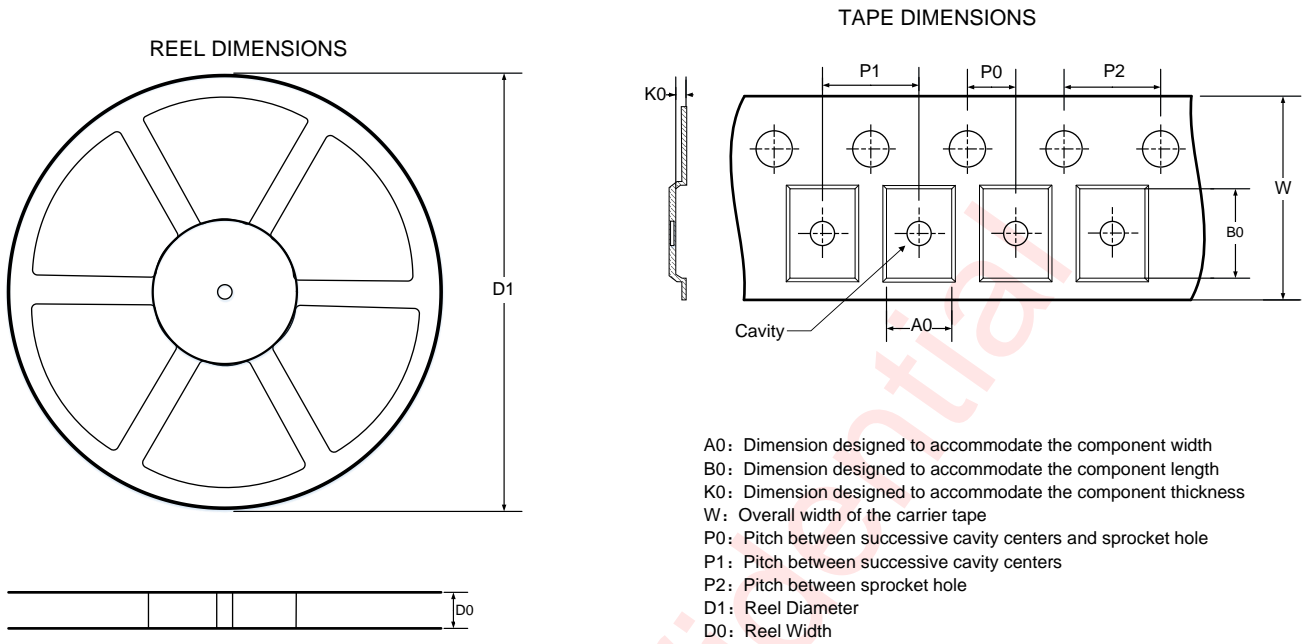
If $V_{\text{IN}} = 0\text{V}$ and OUT is supplied by OTG voltage, the body diode of the load switch conducts current from OUT to IN and the voltage drop from OUT to IN is approximately 0.7V. When $V_{\text{IN}} > V_{\text{IN_UVLO}}$, internal charge pump begins to open the load switch after debounce time (about 15ms). After switch is fully on, current is supplied through switch channel and the voltage drop from OUT to IN is minimum.

PCB Layout Consideration

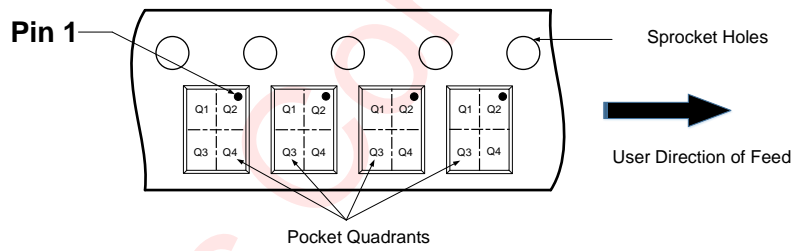
To make fully use of the performance of AW32919, the guidelines below should be followed.

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW32919) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW32919) and close to OUT pin.
2. If external TVS is used, IN pin routing passes through the external TVS firstly, and then connect AW32919.
3. Red bold paths on figure 4 and 5 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.
4. If R_1 and R_2 are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.
5. The power trace from USB connector to AW32919 may suffer from ESD event, keep other traces away from it to minimize possible EMI and ESD coupling.
6. Use rounded corners on the power trace from USB connector to AW32919 to decrease EMI coupling.

Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

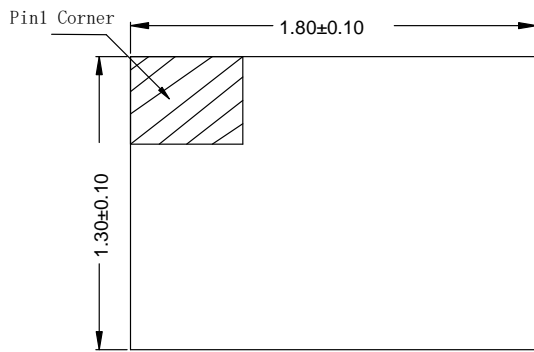


DIMENSIONS AND PIN1 ORIENTATION

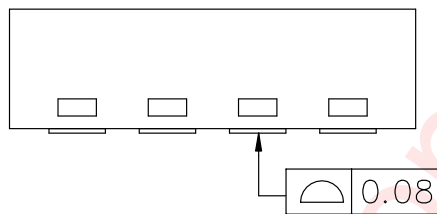
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.58	2.04	0.73	2	4	4	8	Q2

All dimensions are nominal

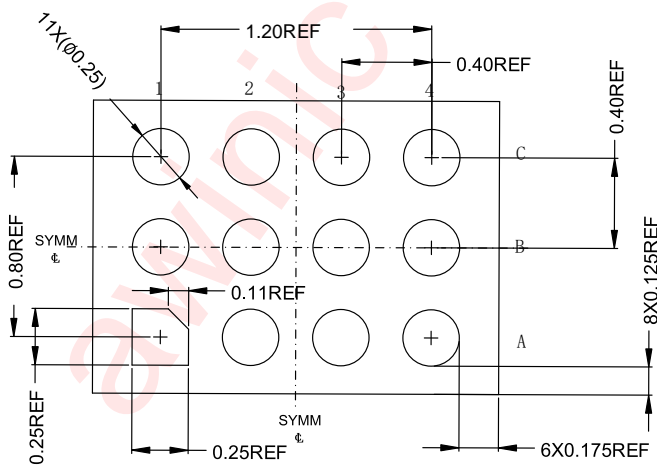
Package Description



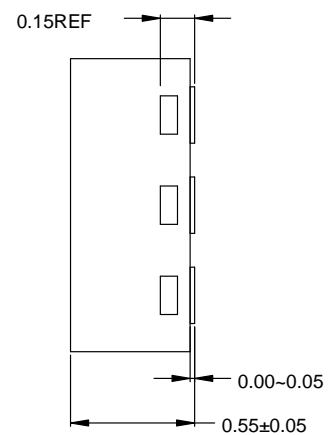
TOP VIEW



SIDE VIEW



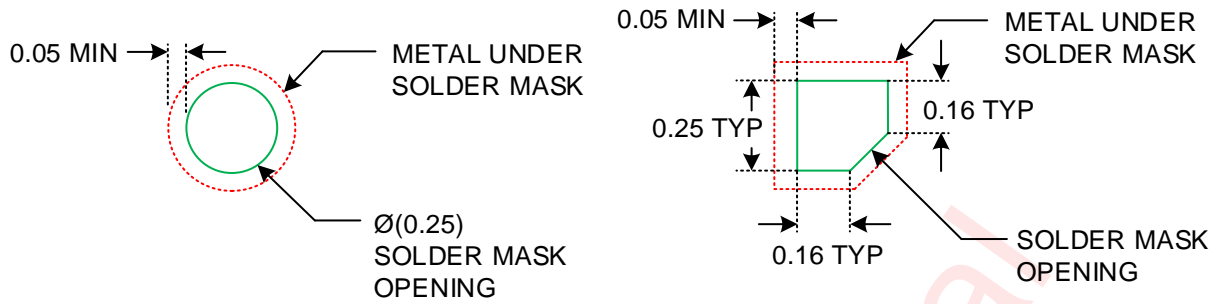
BOTTOM VIEW



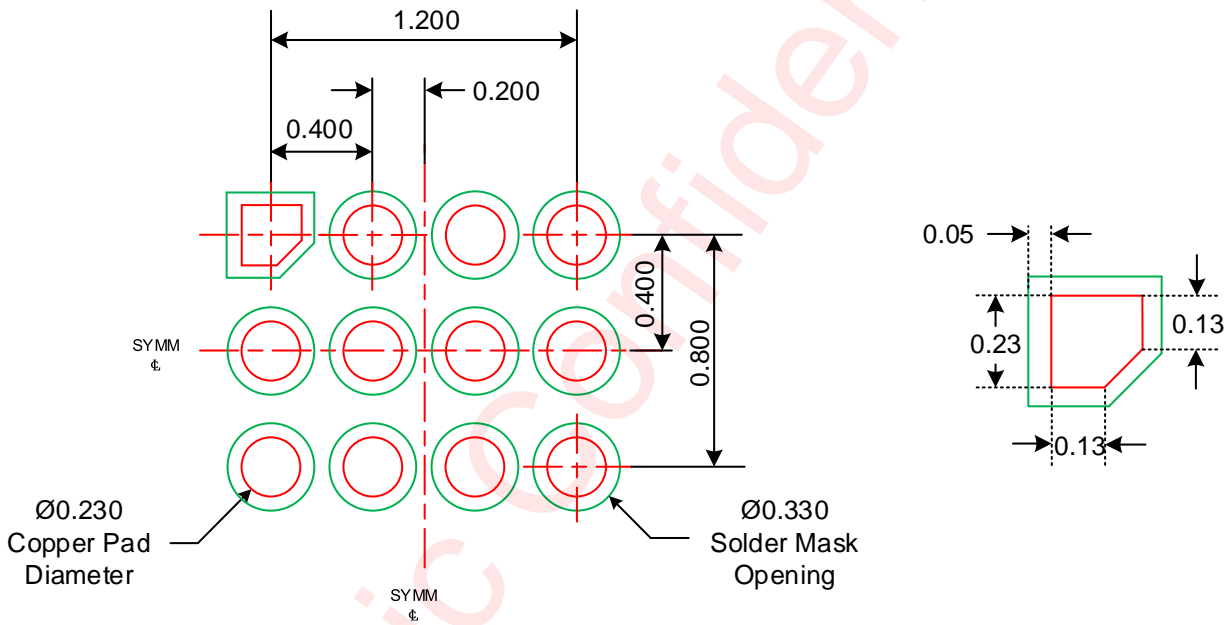
SIDE VIEW

UNIT:mm

Land Pattern Data



Pad Type: Solder Mask Defined



PAD Type: Non-Solder Mask Defined

NOTE:

1. Not to scale
2. Unit: mm.

Revision History

Version	Date	Change Record
V1.0	May 2020	Officially released.

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