Over-Voltage Protection Load Switch with Ideal Diode True Reverse Current

Features

- Wide Input Voltage range from 4V to 24V
- 31V Abs. Max. rating at IN
- 5A continuous current capability
- Integrated ultra-low Ron switch: typical 24 mΩ
- Over-Voltage Protection (OVP)
  - Default 24V with OVLO grounded
  - Adjustable from 4V to 24V with external resistors
- Fast Over-Voltage Protection turn-off response: typical 50ns
- "Ideal Diode" Reverse-Current Protection (RCP) only for AW32105E
- Support OTG (On-The-Go) function only for AW32105P
- Soft-Start for Inrush Current Limit
- Over-Current Protection (OCP)
- Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO)
- Auto-Retry after all faults
- 1.2V and 1.8V Logic Compatible
- FCQFN 2mm×1.5mm×0.55mm-12L, 0.5mm pitch package

Applications

- Desktop, Notebooks, Netbooks, Ultra-Books, Tablets
- Thunderbolt/USB Type-C PD Charging Ports, Docking Stations, Monitors, Accessories

General Description

AW32105E and AW32105P are high input voltage, large current and ultra-low Ron load switch with soft-start, over voltage protection, over current protection, over temperature protection, short circuit protection. AW32105E has reverse current blocking, and AW32105P has OTG function. They are optimized to protect systems with USB Type-C PD ports that sink up to 100W at 20V and withstand up to $31V_{DC}$ on VBUS.

AW32105E has all time Reverse Current Protection regardless of the EN logic level. When disabled, all current flow is blocked. AW32015E has automatic reverse-current blocking feature which acts as an "ideal diode" and isolates VBUS when charging or powering the system via another port. Once the voltage on OUT is higher than IN for RCP trigger voltage, the RCP circuit disables the power switch. Two AW32105E chips can be used in parallel to support dual power inputs connecting to the same charging circuit.

AW32105E and AW32105P are turned off very fast once the input voltage exceeds the OVP threshold to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages to $31V_{DC}$. AW32105E and AW32105P provide a default OVP threshold of 24V typical, and the OVP threshold can be adjusted from 4V to 24V through external OVLO pin.

Device Comparison

Part Number	Enable Pin	Switch Mode
AW32105ELFCR	ENB, Low active	Uni-directional with RCP
AW32105EHFCR	EN, High active	Uni-directional with RCP
AW32105PHFCR	EN, High active	Bi-directional without RCP, support OTG

Typical Application Circuit

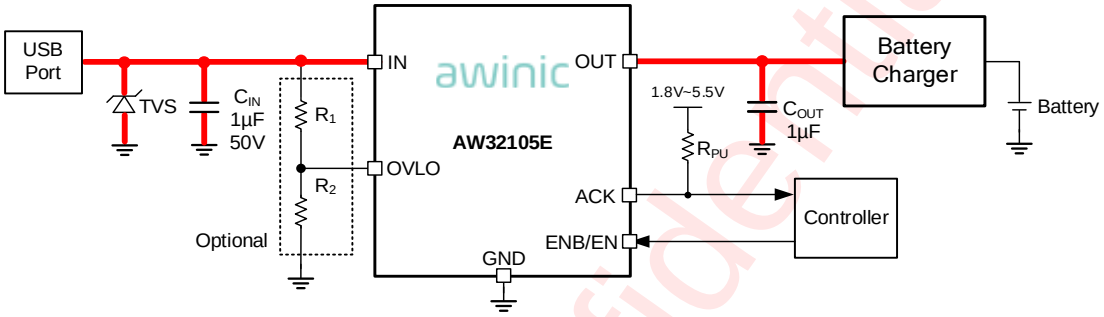


Figure 1 AW32105E Typical Application Circuit

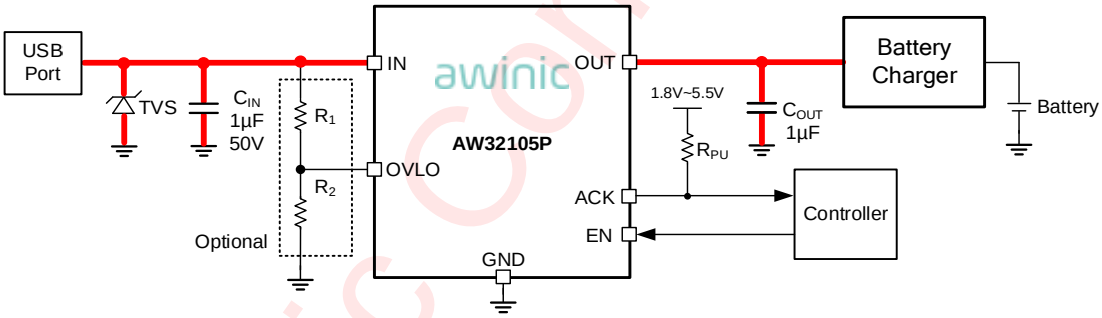


Figure 2 AW32105PH Typical Application Circuit

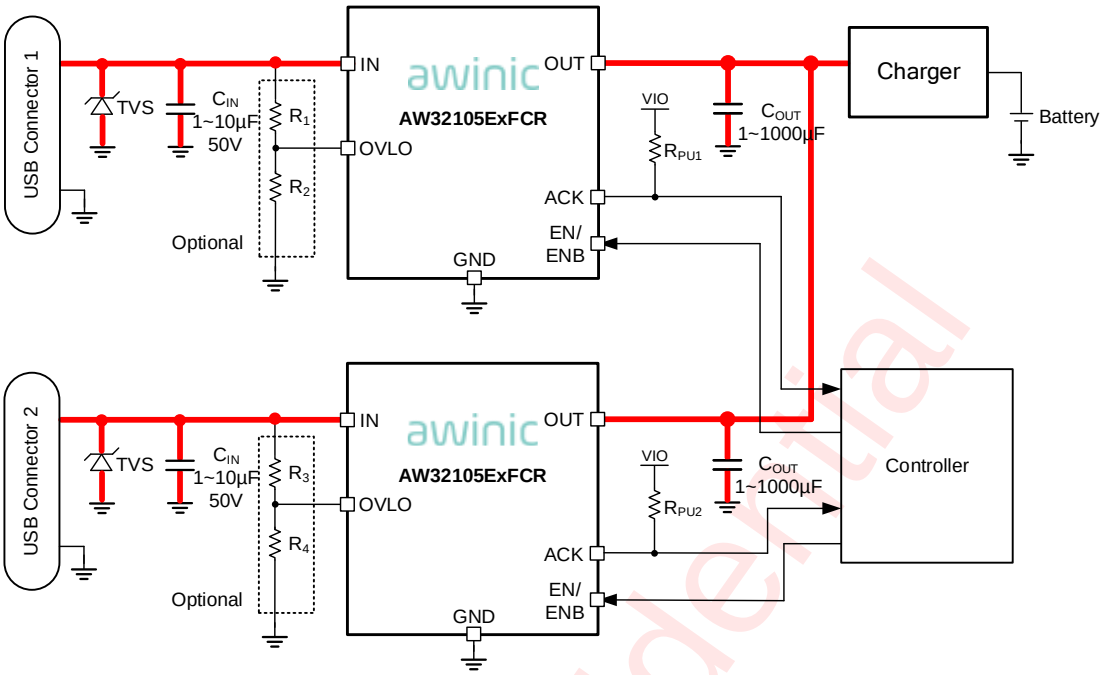


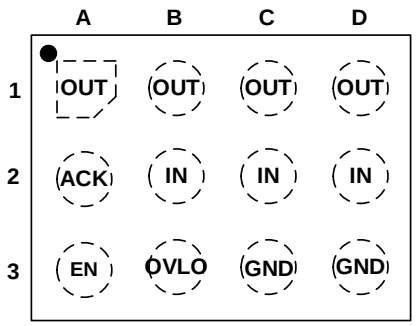
Figure 3 Two AW32105ExFCR in parallel to support dual power inputs

Notice for Typical Application Circuits:

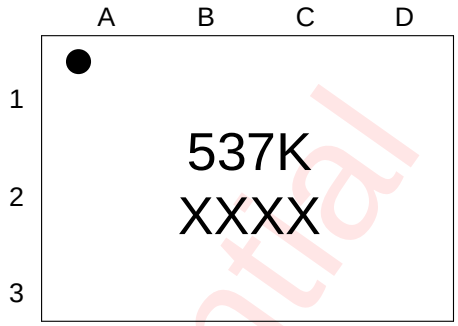
1. If external TVS is needed, the maximum clamping voltage of the TVS should be below 34V.
2. When the default OVP threshold is used, connect OVLO pin to GND directly or through a 0Ω resistor. **OVLO pin cannot be left floating.**
3. If R_1 R_2, R_3 and R_4 are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision.
4. If ACK is not used, it can be left floating, or short to GND.
5. C_{IN} = 1μF is recommended for typical application, larger C_{IN} is also acceptable. The rated voltage of C_{IN} should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW32105E/P is used, the rated voltage of C_{IN} should be 50V.
6. C_{OUT} minimum is recommended to be 1μF. The rated voltage of C_{OUT} should be larger than the OVP threshold. For example, if the OVP threshold is 24V, the rated voltage of C_{OUT} should be 50V.

Pin Configuration

AW32105PHFCR
(Top View)

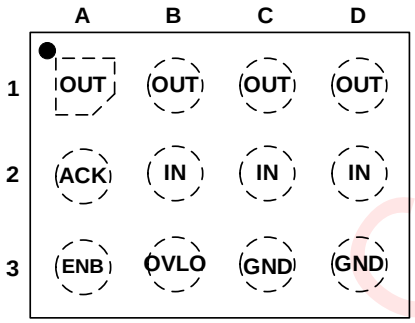


AW32105PHFCR Marking
(Top View)

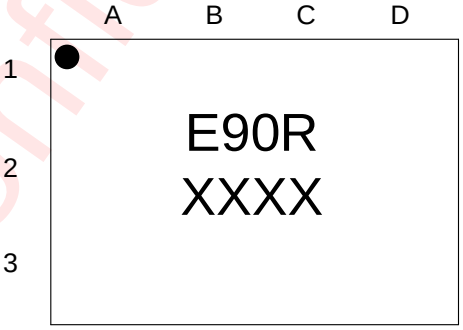


537K - AW32105PHFCR
XXXX - Production Tracing Code

AW32105ELFCR
(Top View)

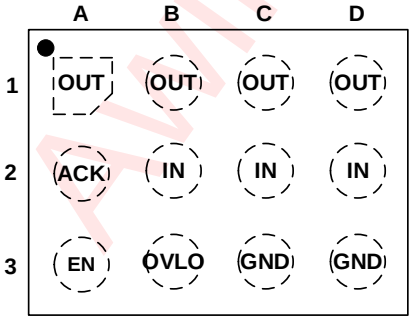


AW32105ELFCR Marking
(Top View)

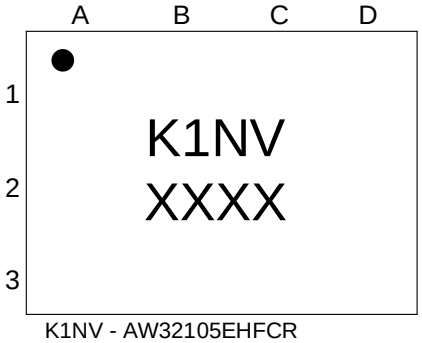


E90R - AW32105ELFCR
XXXX - Production Tracing Code

AW32105EHFCR
(Top View)



AW32105EHFCR Marking
(Top View)



K1NV - AW32105EHFCR
XXXX - Production Tracing Code

Figure 4 Pin Configuration

Pin Definition

Pin	Name	Description
A1, B1, C1, D1	OUT	Power switch output.
B2, C2, D2	IN	Power switch input and device power supply.
A2	ACK	Power good flag, active-low, open-drain output. When $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$, ACK is pulled low, otherwise it's hi-Z state. Connect to GND or leave floating if unused.
A3	ENB	Enable pin, active-low logic input (AW32105EL)
	EN	Enable pin, active-high logic input (AW32105EH, AW32105PH)
B3	OVLO	OVP threshold adjustment pin, connected to GND to use the internally fixed OVLO threshold 24V. Connect external resistors to set an adjustable OVLO threshold from 4V to 24V.
C3, D3	GND	Device ground.

Functional Block Diagram

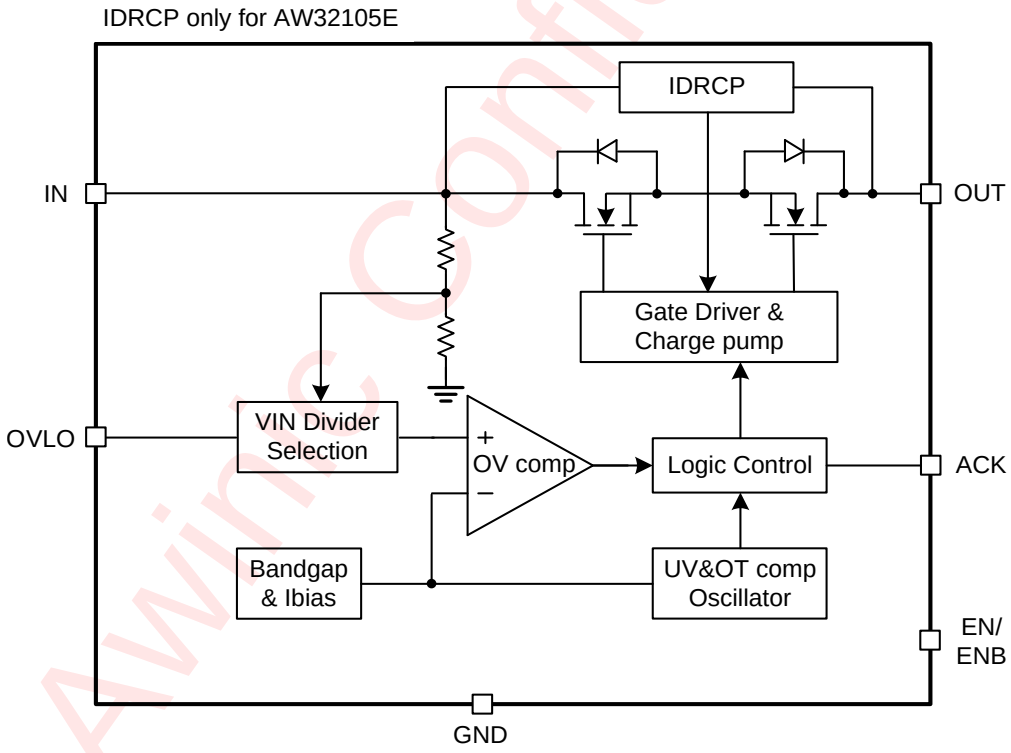


Figure 5 AW32105E/P Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW32105EHFCR	-40°C ~ 85°C	FCQFN 2X1.5-12L	K1NV	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW32105ELFCR	-40°C ~ 85°C	FCQFN 2X1.5-12L	E90R	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW32105PHFCR	-40°C ~ 85°C	FCQFN 2X1.5-12L	537K	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings (NOTE 1)

PARAMETERS	RANGE
Supply voltage range IN	-0.3V to 31V
Supply voltage range OUT, OVLO	-0.3V to 29V
Supply voltage range ACK, EN/ENB	-0.3V to 7V
Continuous current of switch IN-OUT(NOTE2)	5A
Peak switch current on IN and OUT pin(10ms) (NOTE2)	10A
Junction-to-ambient thermal resistance θ_{JA}	80°C /W
Maximum operating junction temperature T_{JMAX}	150°C
Operating free-air temperature range	-40°C to 85°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
Human Body Model (All pins, per ESDA/JEDEC JS-001)	±2kV
Charged Device Model (All pins, per ESDA/JEDEC-JS-002)	±1.5kV
Latch-Up	
Test condition: JESD78F	±200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Limited by thermal design.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage	4		24	V
V_{OUT}	Output Voltage	0		24	V
V_{ACK}	Power Good Flag Output Voltage	0		5.5	V
V_{OVLO}	OVLO Adjust Input Bias Voltage	0		5.5	V
V_{EN}, V_{ENB}	Enable Logic Input Voltage	0		5.5	V
C_{IN}	Input capacitance		1	10	μF
C_{OUT}	Output load capacitance		1	1000	μF

Electrical Characteristics

V_{IN}=5V, V_{EN}=5V, C_{IN}=1μF, C_{OUT}=1μF, T_A = 25°C for typical values (unless otherwise noted).

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{IN}	Input Voltage		4		24	V
R_{ON}	Switch On-Resistance	V_{IN} = 5V, I_{OUT} = 1.5A		24		mΩ
I_Q	IN on-state quiescent current	V_{IN} = 5V, OUT = open		460		μA
		V_{IN} = 20V, OUT = open		600		
	IN on-state quiescent current（AW32105P in OTG Mode）	V_{OUT} = 5V, IN = open		TBD		μA
		V_{OUT} = 20V, IN = open		TBD		
I_{SD}	IN OFF-state quiescent Current	V_{EN}=0V, V_{IN} = 5V, OUT = open		74		μA
		V_{EN}=0V, V_{IN} = 20V, OUT =open		110		
	IN OFF-state quiescent Current（AW32105P in OTG Mode）	V_{EN}=0V, V_{OUT} = 5V, IN = open		TBD		μA
		V_{EN}=0V, V_{OUT} = 20V, IN = open		TBD		
I_{LEAK_IN}	IN OFF-state leakage current	V_{EN}=0V, V_{IN} = 5V, V_{OUT} = 0V		74		μA
		V_{EN}=0V, V_{IN} = 20V, V_{OUT} = 0V		110		
I_{LEAK_OUT}	OUT OFF-state leakage current	V_{EN}=0V, V_{IN} = 0V, V_{OUT} = 5V		94		μA
		V_{EN}=0V, V_{IN} = 0V, V_{OUT} = 20V		136		
I_{OUT_RCP}	Output Supply Current in RCP	V_{EN}=5V, V_{OUT}=5V, V_{IN}=0V		270		μA
I_{IN_OVLO}	Input current at overvoltage condition	V_{IN}=5V, V_{OVLO}=3V, V_{OUT}=0V		230		μA
V_{OVLO_TH}	OVLO set threshold			1.2		V
V_{OVLO_RNG}	OVP threshold adjustable range		4		24	V
V_{OVLO_SEL}	External OVLO select threshold	OVLO rising		0.2		V
		Hysteresis		20		mV
I_{LEAK_OVLO}	OVLO pin leakage current	V_{OVLO} = V_{OVLO_TH}	-0.2		0.2	μA
Protection						
V_{IN_OVLO}	OVP trip level	V_{IN} rising		24		V
		Hysteresis		500		mV

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{IN_UVLO}	UVLO trip level	V_{IN} rising		2.9		V
		Hysteresis		110		mV
V_{trig}	RCP trigger voltage	$V_{trig}=V_{OUT}-V_{IN}$		90		mV
		Hysteresis		110		
V_{RCP}	RCP Droop Regulation Voltage (ideal diode)	$V_{RCP}=V_{IN}-V_{OUT}$, I_{OUT}=100mA		20		mV
t_{RCP_REC}	RCP Fast Recovery Time Note3	V_{OUT} < V_{IN} - 90mV until switch turns back on		10		μs
I_{OCP} (Fast SCP)	Over-Current Threshold Note3			15		A
T_{SDN}	Shutdown temperature Note3			160		℃
T_{SDN_HYS}	Shutdown temperature hysteresis Note3			24		℃
Digital Logical Interface						
V_{OL}	ACK output low voltage	I_{SINK} = 6mA		0.3		V
I_{LEAK_ACK}	ACK leakage current	V_{IO} = 5V, ACK de-asserted	-0.5		0.5	μA
V_{IH}	Input Logic High (EN, ENB)		0.84			V
V_{IL}	Input Logic Low (EN, ENB)				0.54	V
I_{LEAK_EN}	EN leakage current	V_{EN} = 5V, V_{IN}= 0V			1	μA
R_{EN}	EN pull-down resistance （High enable）			1		MΩ
Timing Characteristics (see Figure 7 and Figure 8)						
t_{EN}	Enable Time	From EN to V_{OUT}=10% of V_{IN}; V_{IN} = 5V; C_{OUT} = 100μF, R_L = 100Ω		12		ms
t_{TLH}	V_{OUT} rise time	V_{OUT} from 10% to 90% V_{IN}; CL=100μF, RL=100Ω; V_{IN}=5V		1		ms
		V_{OUT} from 10% to 90% V_{IN}; CL=100μF, RL=100Ω; V_{IN}=20V		2		
t_{OFF_OVP}	OVP Response Time Note3	C_{OUT}=1uF, RL=100Ω; V_{OVLO}=0V, V_{IN}>V_{IN_OVLO} to V_{OUT} stop rising		50		ns
t_{OCP}	OCP Response Time Note3	time from I_{OUT}>I_{OCP} until switch turns off		500		ns

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{START}	Start-up time	EN to ACK low; COUT = 100μF; RL = 100Ω		18		ms
t_{ON}	turn on time	EN to V_{OUT}=90%* V_{IN}, V_{IN}=5V		t_{en}+ t_{TLH}		ms
		EN to V_{OUT}=90%* V_{IN}, V_{IN}=20V		t_{en}+ t_{TLH}		
t_{OFF}	turn off time	EN to V_{OUT}=10%*V_{IN}; V_{IN}=5V, CL=100μF, RL=100Ω		23		ms
		EN to V_{OUT}=10%*V_{IN}; VIN=20V, CL=100μF, RL=100Ω		23		

Note3: guarantee by design

Waveforms and Test Circuits

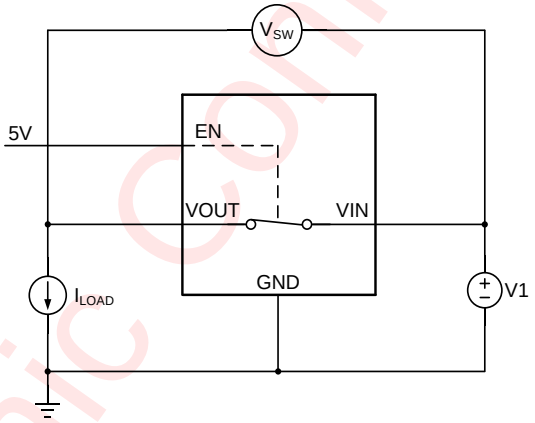


Figure 6 On resistance Measurement Test Circuit

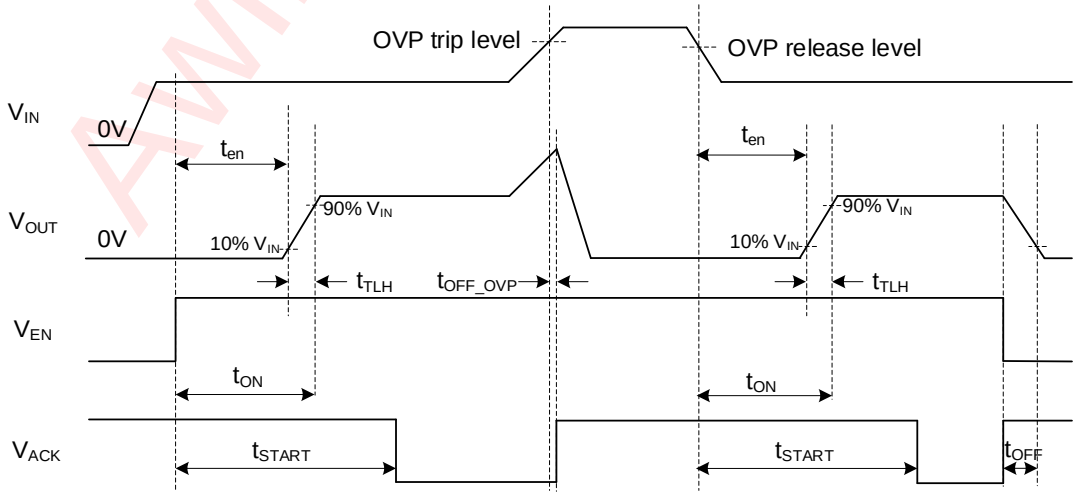
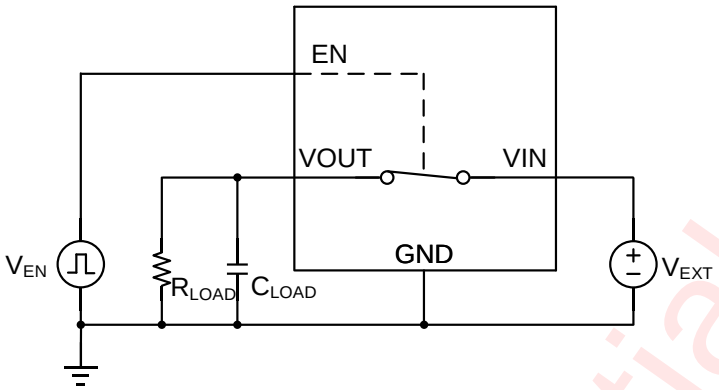


Figure 7 Operating Waveforms and Timing Definitions



Test condition are V_{IN}=4V to 20V, C_{LOAD}=100μF, R_{LOAD}=100Ω, where:

R_{LOAD}=Load resistance.

C_{LOAD}=Load capacitance.

V_{EXT}=External voltage source applied to VIN pin for measurements.

Figure 8 Waveform and Timing Measurements Test Circuit

Typical Characteristics

Ambient temperature is 25°C, V_{IN} =5V, V_{EN}=5V, V_{OVLO}=0V, C_{IN} = C_{OUT}=1μF, unless otherwise noted.

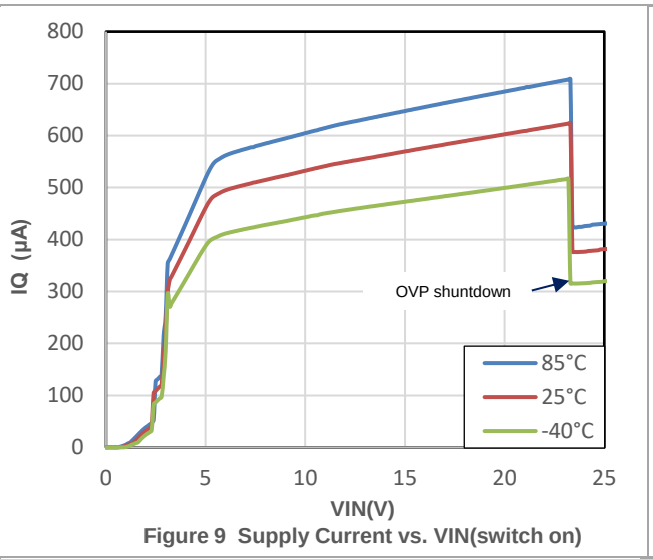


Figure 9 Supply Current vs. VIN(switch on)

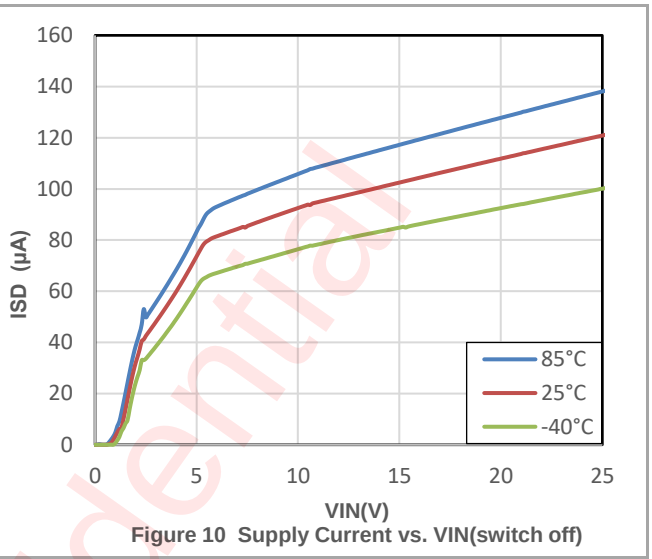


Figure 10 Supply Current vs. VIN(switch off)

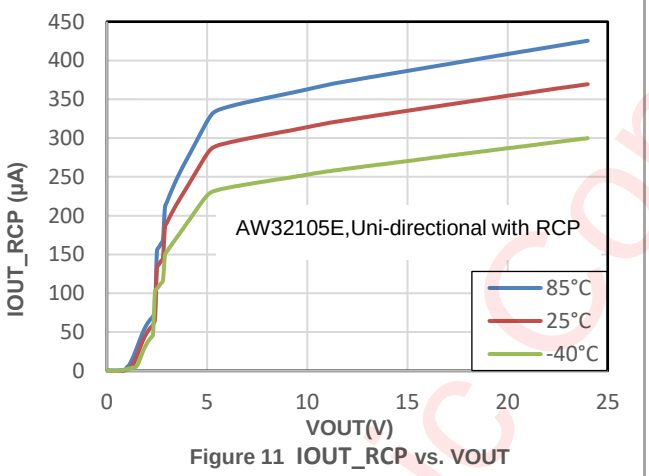


Figure 11 IOUT_RCP vs. VOUT

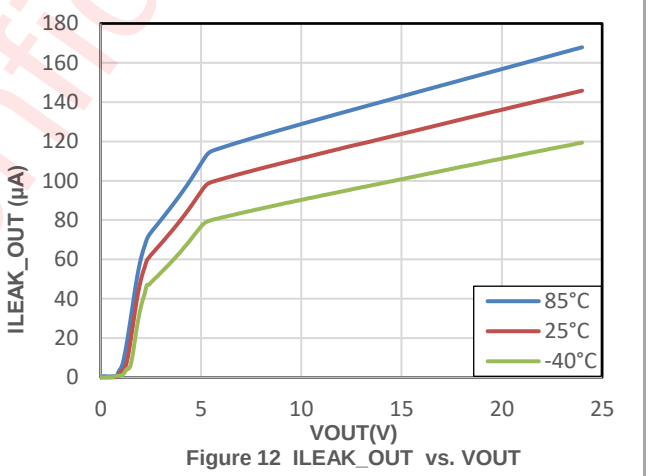


Figure 12 ILEAK_OUT vs. VOUT

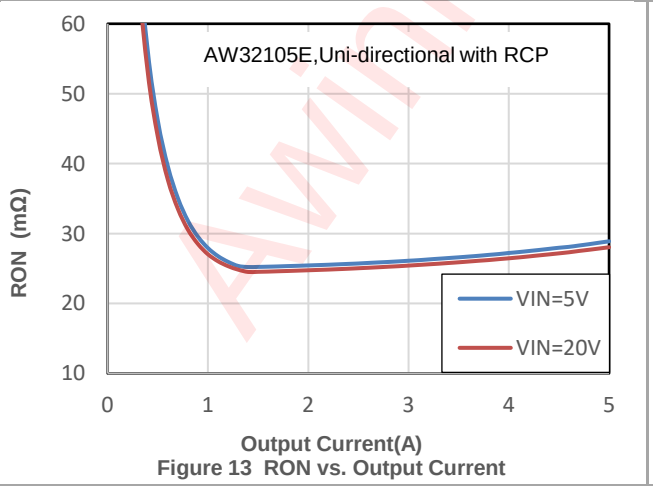


Figure 13 RON vs. Output Current

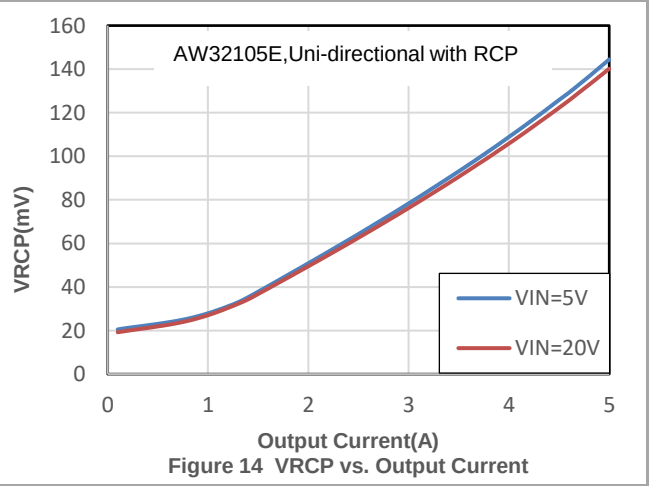


Figure 14 VRCP vs. Output Current

Functional Description

Device Operation

If the AW32105E/P is enabled and the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on. ACK will be driven low about 18ms after VIN valid, indicating the switch is on with a good power input. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 50ns. If EN is pulled low, or ENB is pulled high, or input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

Table1. AW32105EH/PH Function and Logic Table

EN	VIN	VOUT	ACK	Operation Mode
H	$<V_{IN\_UVLO}$	X	Hi-Z	Under-voltage lockout, switch open. (UVLO fault)
H	$V_{IN\_UVLO}<V_{IN}<V_{IN\_OVLO}$	X	L	Enabled, switch closed, charging path on. (Normal on)
H	X	X	Hi-Z	Over-temperature protection, switch open. (OTP fault)
H	$>V_{IN\_OVLO}$	X	Hi-Z	Over-voltage lockout, switch open. (OVP or OVLO fault)
L	X	X	Hi-Z	Disable, switch open. (Normal off)

Table2. AW32105EL Function and Logic Table

ENB	VIN	VOUT	ACK	Operation Mode
L	$<V_{IN\_UVLO}$	X	Hi-Z	Under-voltage lockout, switch open. (UVLO fault)
L	$V_{IN\_UVLO}<V_{IN}<V_{IN\_OVLO}$	X	L	Enabled, switch closed, charging path on. (Normal on)
L	X	X	Hi-Z	Over-temperature protection, switch open. (OTP fault)
L	$>V_{IN\_OVLO}$	X	Hi-Z	Over-voltage lockout, switch open. (OVP or OVLO fault)
H	X	X	Hi-Z	Disable, switch open. (Normal off)

Note: H=logic high level, L=logic low level, Hi-Z=high-impedance(off-state), X= don't care.

Over-Voltage Protection (OVP)

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until V_{IN} falls below the OVP falling trip level.

Under Voltage Lockout (UVLO)

The AW32105E/P has under voltage lockout function which can disable the switch until the input voltage reaches the UVLO threshold (typical 2.9V). The UVLO threshold has a 110mV hysteresis voltage which can prevent the unwanted on/off cycling when there is noise on the input voltage.

Over-Current Protection (OCP)

The AW32105E/P includes output over-current protection (OCP) at 15A that protects the IC from damage when an over-current or short-circuit event suddenly appears. The OCP circuit disables the power switch very quickly. After the hiccup time expires, the chip will check whether the OCP event still exists. If no OCP event and no

other faults are detected under the EN/ENB enable condition, the power switch is re-enabled via the soft-start debounce and ramp time.

Over-Temperature Protection (OTP)

The device has a built-in temperature sensor which monitors the internal junction temperature. When the junction temperature exceeds 160°C, power switch turns off. When the junction temperature falls below the thermal recovery temperature, approximately 136°C, the device auto-recovery after 12ms.

Auto-Retry

The device has a built-in auto-retry function. When any fault causes the switch to open, the device will auto-retry via soft-start debounce and ramp time. If the fault is still detected, the switch will open again, and the auto-retry will repeat.

OTG Mode (AW32105P only)

The AW32105P support OTG mode where both MOSFETs can be turned-on to provide current flow from OUT to IN.

"Ideal Diode" Reverse-Current Protection (RCP, AW32105E only)

The AW32105E includes the Reverse Current Protection (RCP) function, which can prevent the current to flowing through MOSFET when VOUT greater than VIN. Whatever the switch is on or off, the AW32105E always has this function. When VOUT-VIN greater than 90mV, the internal comparator quickly turns off the switch, in order to prevent large reverse current from VOUT to VIN. The switch will return to normal operation once the reverse voltage scenario disappeared.

When the device is ON with no load or under light load conditions, it regulates VOUT to be 20 mV below VIN. As the load current is increasing or decreasing, the device adjusts the MOSFET gate drive to maintain the 20mV drop from VIN to VOUT. As the load current continues to increase the device increases the gate drive until the gate is fully turned on and VIN to VOUT drop is determined by IR drop through the MOSFET.

OVP Threshold Adjustment

If the default OVP threshold is used, OVLO pin must be grounded. If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be adjusted as following:

$$V_{IN\_OVLO} = \frac{R_1+R_2}{R_2} V_{OVLO\_TH}$$

For example, if we select R_1 = 1MΩ and R_2 = 100kΩ, then the new OVP threshold calculated from the above formula is 13.2V. The OVP threshold adjustment range is from 4V to 24V. When the OVLO pin voltage V_{OVLO} exceeds V_{OVLO_SEL} (0.2V typical), V_{OVLO} is compared with the reference voltage V_{OVLO_TH} (1.2V typical) to judge whether input supply is over-voltage.

ACK Output

The device features an open-drain output ACK, it should be connected to the system I/O rail through a pull-up resistor. If the device is enabled and $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$, ACK will be driven low indicating the switch is on with a good power input. If OVP, OCP, UVLO, or OT occur, or EN/ENB is disabled, the switch will be turned off and ACK will be pulled high. The pull up resistor value is recommended to be 10KΩ to 200KΩ.

Application Information

Capacitors Selection

C_{IN} = 1μF, C_{OUT} = 1μF is recommended for typical application, larger C_{IN}, C_{OUT} is also acceptable.

The rated voltage of C_{IN} should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW32105E/P is used, the rated voltage of C_{IN} should be 50V. The rated voltage of C_{OUT} should be larger than the OVP threshold. For example, if the OVP threshold is 24V, the rated voltage of C_{OUT} should be 35V or higher. The recommended value of capacitors and boundary values can refer to the following table:

Capacitor	Typical Value (μF)	Boundary Value (μF)
C_{IN}	1	0.1~10
C_{OUT}	1	0.1~1000

Resistors Selection

The default OVLO voltage is 24V, when using default OVP threshold, it is recommended to connect OVLO to ground or through 0Ω resistor. When R_1 and R_2 are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision. When (R_1+R_2) is larger, the clamping voltage of OUT is smaller. It is recommended to select R_1 = 1MΩ, R_2 can calculate the value according to the required OVP threshold. The calculation formula is as follows: the typical value of V_{OVLO_TH} is 1.2V, and the adjustable range of V_{IN_OVLO} is 4V ~ 24V.

$$V_{IN\_OVLO} = \frac{R_1+R_2}{R_2} V_{OVLO\_TH}$$

The recommended value of resistors and boundary values can refer to the following table:

Resistor	Typical Value (Ω)	Boundary Value (Ω)
R_1	1M	1K~10M
R_2	100K	Determined by R_1

TVS (if used)

First of all, the working voltage of TVS should be determined. TVS with V_{RWM} ≥ 10V can be selected for 5V charging port, TVS with V_{RWM} ≥ 12V can be selected for 9V charging port, and TVS with V_{RWM} ≥ 24V can be selected for 20V charging port. Secondly, it is necessary to meet the requirement of surge protection capability. Assuming that the customer wants to select a TVS with surge voltage rating of 100V, the TVS should meet the requirement of IPP ≥ (100V - 30V) / 2Ω = 35A. When selecting the model of external TVS, the maximum clamping voltage of the TVS should be below 34V. Too high clamping voltage of TVS will cause damage to OVP chip.

PCB Layout Consideration

To make fully use of the performance of AW32105E/P, the guidelines below should be followed.

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer and close to IN pin, and place the output capacitor C_{OUT} on the top layer and close to OUT pin.

2. If external TVS is used, IN pin routing passes through the external TVS firstly, and then connect AW32105E/P.

3. Red bold paths on figure 15 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

4. If R_1 and R_2 are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.

5. The power trace from USB connector to AW32105E/P may suffer from ESD event, keep other traces away from it to minimize possible EMI and ESD coupling.

6. Use rounded corners on the power trace from USB connector to AW32105E/P to decrease EMI coupling.

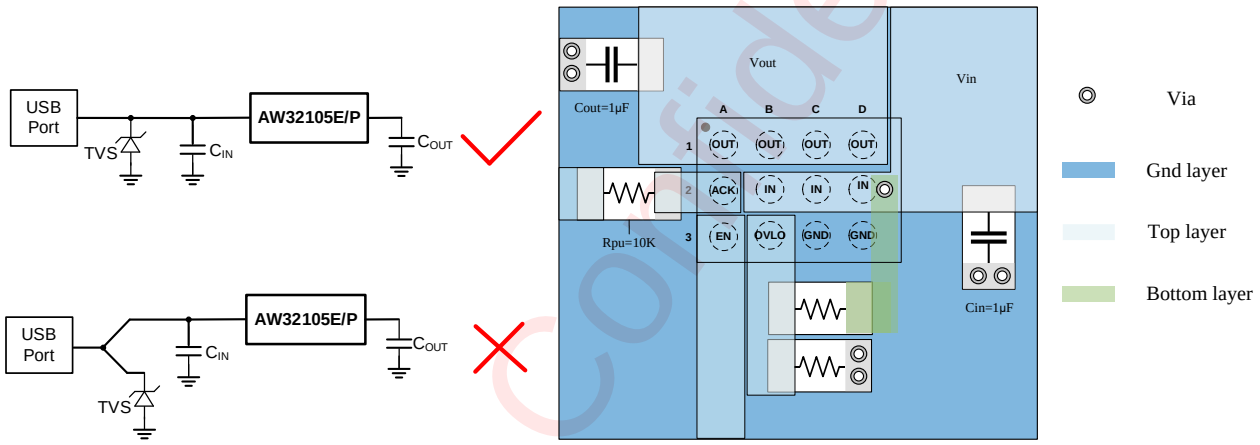
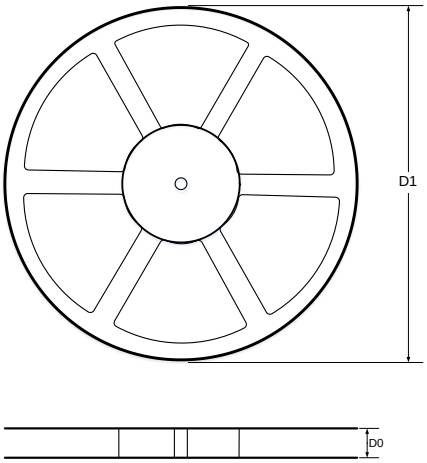


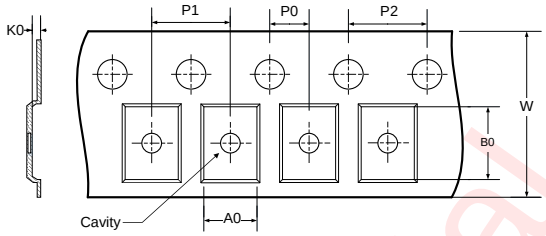
Figure 15 AW32105E/P External Components Placements and PCB Layout Example

Tape And Reel Information

REEL DIMENSIONS

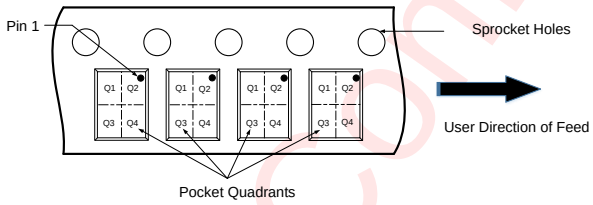


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

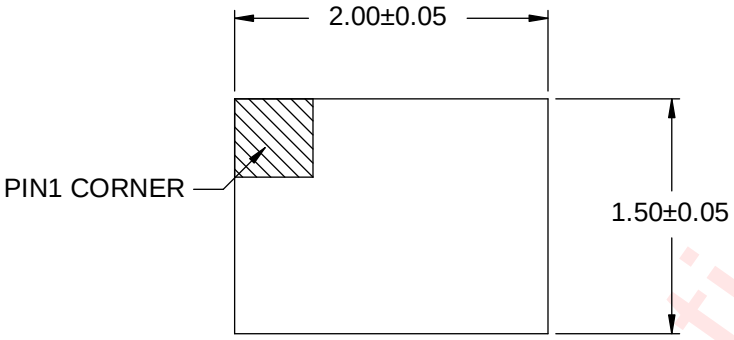


Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

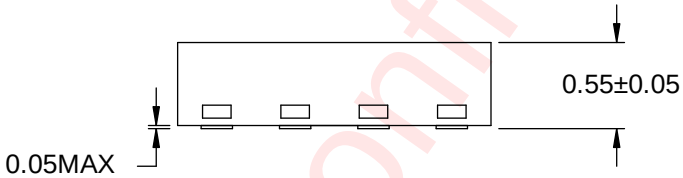
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	8.40	1.70	2.20	0.75	2	4	4	8	Q2

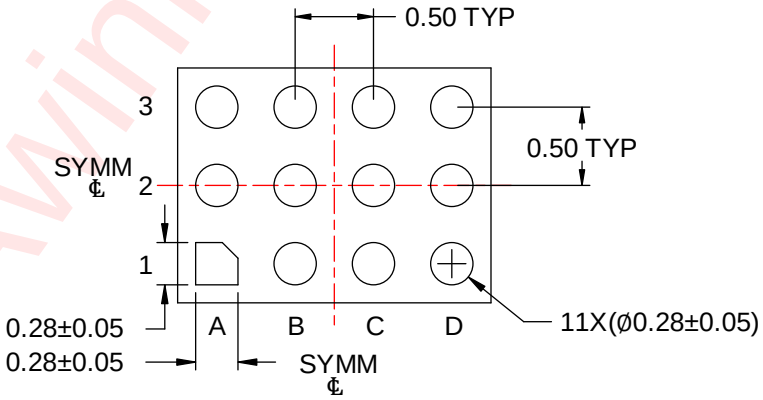
Package Description



Top View



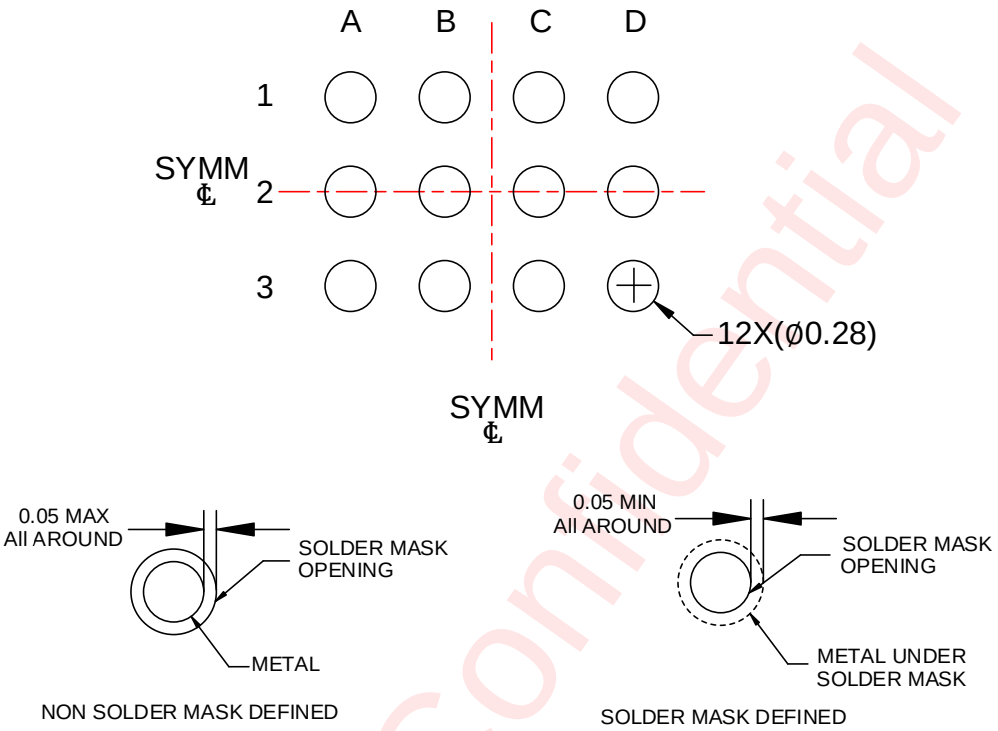
Side View



Bottom View

Unit:mm

Land Pattern Data



Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jan. 2026	Datasheet V1.0 released

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