T117 T117B

±0.1°C/±0.5°C Accuracy, 16bit ADC, Ultra-low Power Consumption, I²C /1-Wire Interface Digital Temperature Sensor Chip

1. Overview

The T117 series are digital-analog mixed signal temperature sensor chips with the highest temperature measuring accuracy of ±0.1°C, requiring no calibration by the user. The principle of temperature sensing is based on the relationship between CMOS semiconductor PN junction temperature and bandgap voltage. After small signal amplification, analog-to-digital conversion, and digital calibration compensation, the temperature chip outputs through a digital bus, featuring high accuracy, good consistency, fast temperature measurement, low power consumption, flexible programmable configuration, and long lifespan.

The chip contains a built-in 16-bit ADC with a resolution of 0.004°C and an ultra-wide operating range of -103°C to +153°C. The chip gurantees 100% testing and calibration before leaving the factory. Calibration coefficients are fitted according to each individualtemperature error characteristics, and the chip automatically performs compensation calculation internally. The chip supports digital I²C communication interface, temperature data memory access, and functional configuration can be achieved through digital protocol instructions. The I²C interface is suitable for high-speed board-level application scenarios, with a maximum interface speed of up to 1MHz.

The chip has a built-in non-volatile E²PROM storage unit for saving the chip ID number, high and low temperature alarm thresholds, temperature calibration correction values, and user-defined information, such as sensor node number, location information, etc.

The chip also has alarm indicator pins, which make it easy for users to expand hardware alarm applications.

2. Features

- Maximum temperature accuracy:±0.1°C/±0.5°C
- Temperature measurement range:-103 ℃ ~+153°C
- Low power consumption: typical standby current 0.01μA, peak current during temperature measurement 0.36mA, average current during temperature measurement 2μA (AVG=8, 1 measurement/s)
- Wide operating voltage range: 1.8V~5.5V
- Temperature sensing resolution:16-bit output 0.004°C
- Configurable temperature conversion time: 15.3ms/8.5ms/5.2ms/2.2ms
- Configurable single/periodic measurement
- Temperature alarm can be set
- Maximum of 112bit additional E²PROM space for storing user information
- Standard I²C interface compatible with digital 1-wire interface
- Heating as self-diagnosis function

3. Applications

- Smart wearables
- Electronic thermometers
- Animal temperature detection
- Medical electronics
- Cold chain logistics, storage
- Smart home
- Thermal meters, gas meters, water meters
- Replacement for PT100/PT1000
- Board level temperature monitoring
- Industrial and agricultural environmental temperature
- Smart appliances
- Consumer electronics
- Temperature measuring instruments

Product information

Part Number	Typical Accuracy	Typical Accuracy Range(℃)	Number of address bits	Package
T117	±0.1℃	+28℃ to +43℃	4	DFN6L
T117Z	±0.1℃	+0℃ to +50℃	4	DFN6L
T117W	±0.1℃	+20℃ to +70℃	4	DFN6L
T117P	±0.1℃	-25℃ to +25℃	4	DFN6L
T117B	±0.5℃	+0℃ to +60℃	4	DFN6L

Note:
Other temperature range accuracy characteristics are described in detail in "7. temperature sensing performance".

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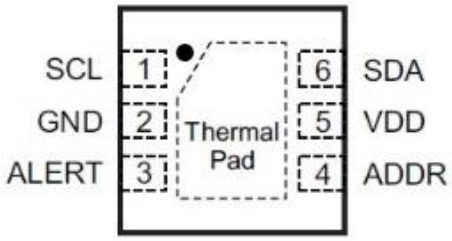
4. Pin Descriptions



(Front View)

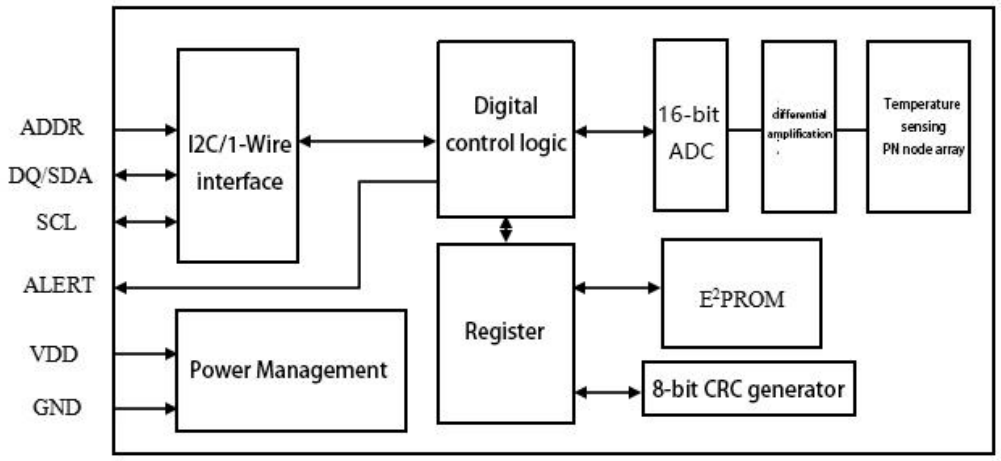
Pin Number	Pin Name	I/O	Description
1	SCL	Input/Output	I^2C Clock Line
2	GND	—	Ground
3	ALERT	Output	Indication of alarm or temperature measurement status , open drain output mode
4	ADDR	Input	I^2Caddress selection:: Connected to GND，0x40 Connected to VDD，0x41 Connected to SDA，0x42 Connected to SCL，0x43
5	VDD	—	Power Supply
6	SDA	Input/Output	I^2C/1-wire Data Line DQ
Heat Sink Pad	NC	—	No Connection or Ground(1)

Note 1: For circuit design, the heat sink pad can be left unconnected or grounded.

1）If mounted on PCB for measuring ambient temperature, it is recommended to connect the heat sink pad to the ground on the PCB.

2)If mounted on PCB or heat sink pad attached to a metal piece for contact temperature measurement, it is recommended not to ground.

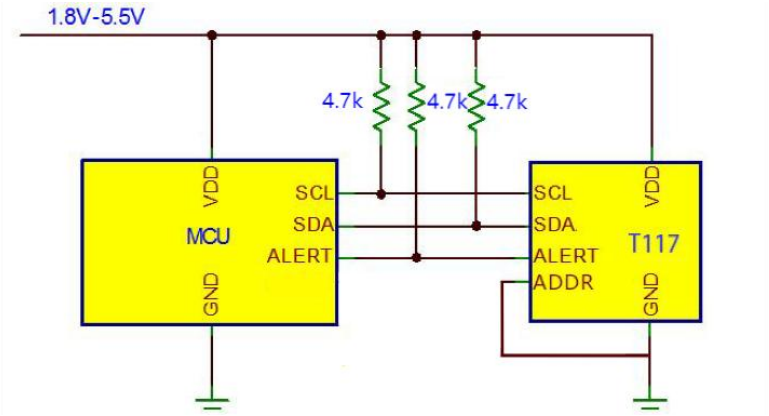
5. System Diagram



The principle diagram of the temperature sensor is shown above. The register includes two bytes of the temperature register, storing the digital output from the sensor. Additionally, the register and extended register provide alarm trigger threshold registers. The configuration register allows users to set the temperature conversion repeatability and continuous measurement frequency. The status register can query the alarm status. Data can be stored in a non-volatile unit, and data will not be lost when the chip is powered off.

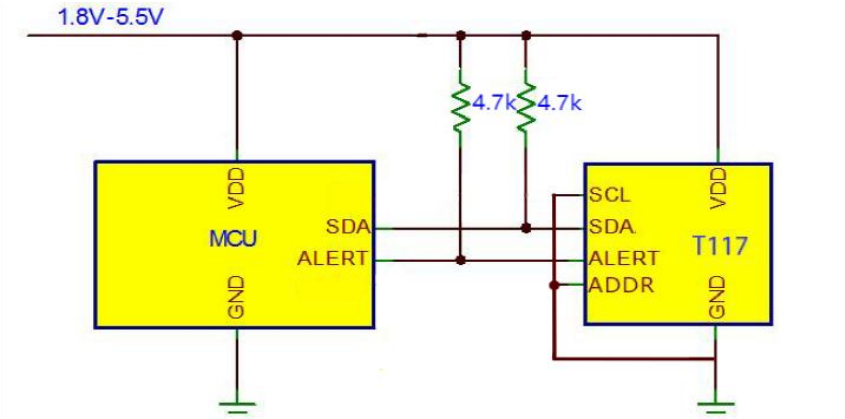
6. Typical Application Circuit

6.1 I²C Protocol Typical Circuit Diagram



The ADDR pins can be connected to GND, VDD, SDA, and SCL, with corresponding I²C communication addresses of 0x40, 0x41, 0x42, and 0x43, respectively.

6.2 1-wire Protocol Typical Circuit Diagram



In 1-wire mode, SCL and ADDR pins cannot be left floating and must be connected to either GND or VDD.

7. Temperature Sensing Performance

Parameter	Symbol	Condition	Min	Typical	Max
Temperature Range	—	—	-103℃	—	+153℃
Temperature error	t_{ERR}	T117	—	—	±0.1℃@+28℃ to +43℃ ±0.5℃@-10℃ to +60℃

		T117Z	—	—	±0.1℃@0℃ to +50℃ ±0.2℃@-10℃ to +60℃ ±0.5℃@-25℃ to +75℃
		T117W	—	—	±0.1℃@+20℃ to +70℃ ±0.2℃@0℃ to +75℃ ±0.5℃@-20℃ to +90℃
		T117P	—	—	±0.1℃@-25℃ to +25℃ ±0.5℃@-55℃ to +55℃
		T117B	—	—	±0.5℃@0℃ to +60℃
		T117 Series	—	±2℃@-103℃ to +153℃	—
Repeatability	—	AVG=1	—	0.02℃	(1)
		AVG=8		0.01℃	—
		AVG=16	—	0.008℃	—
		AVG=32	—	0.007℃	—
Resolution	—	—	—	0.004℃	—
Long Term Drift	—	—	—	—	0.03°C/Year

Note1： The higher the number of averages, the longer the conversion time, but the higher the output accuracy, see Table 9.3-2.

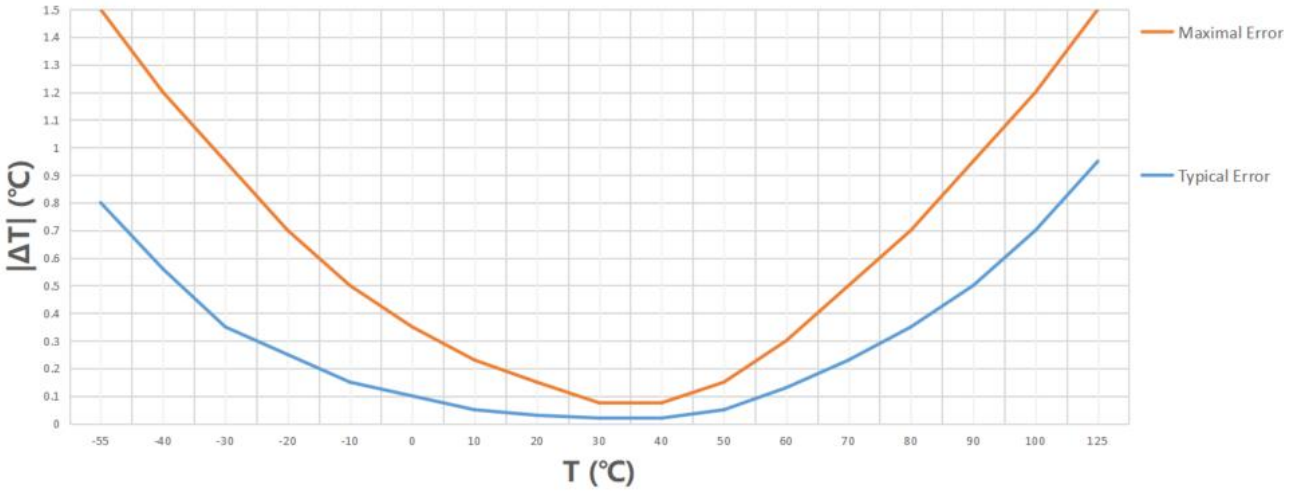


Figure 7-1 T117 Accuracy Error Curve

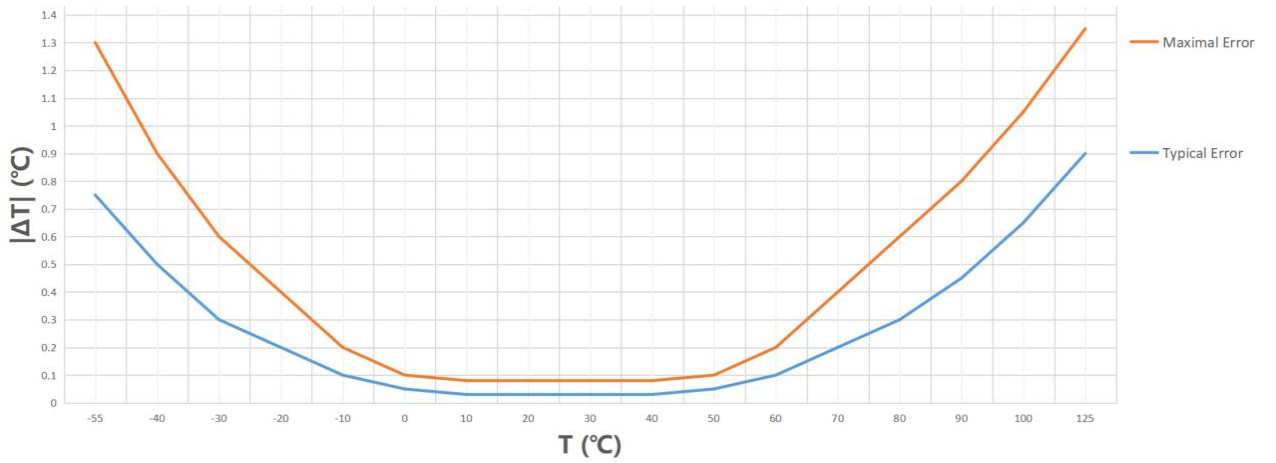


Figure 7-2 T117Z Accuracy Error Curve

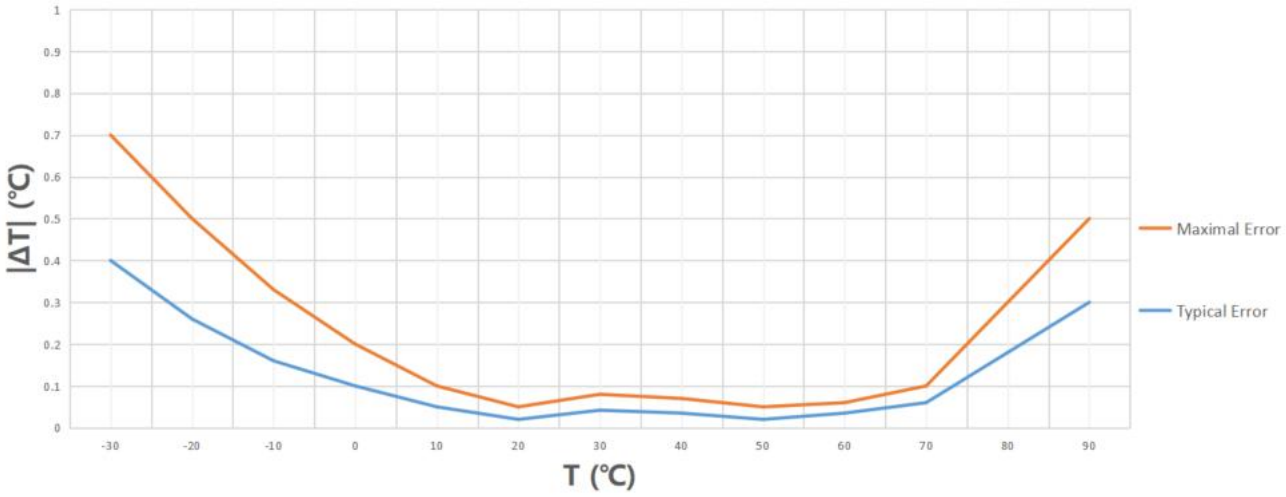


Figure 7-3 T117W Accuracy Error Curve

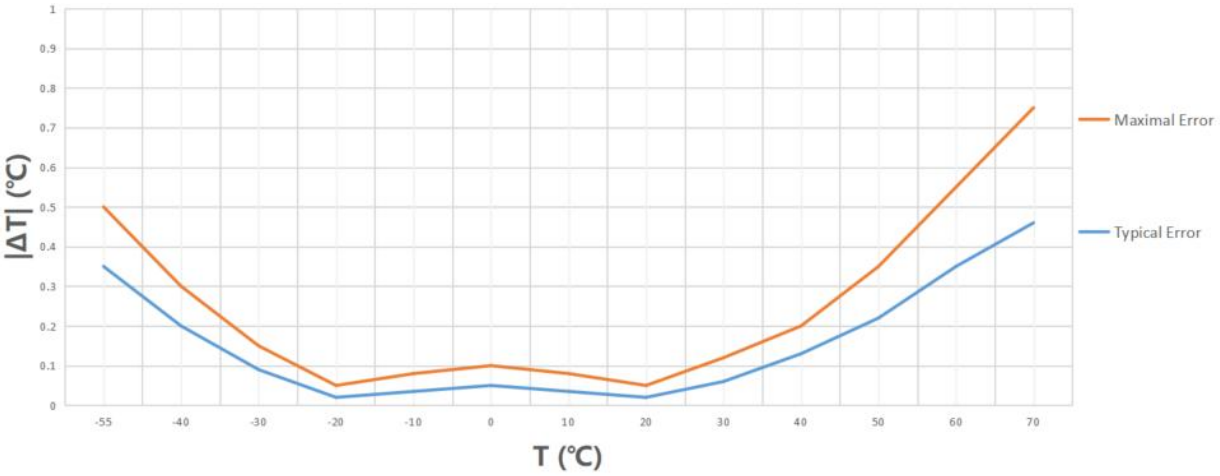


Figure 7-4 T117P Accuracy Error Curve

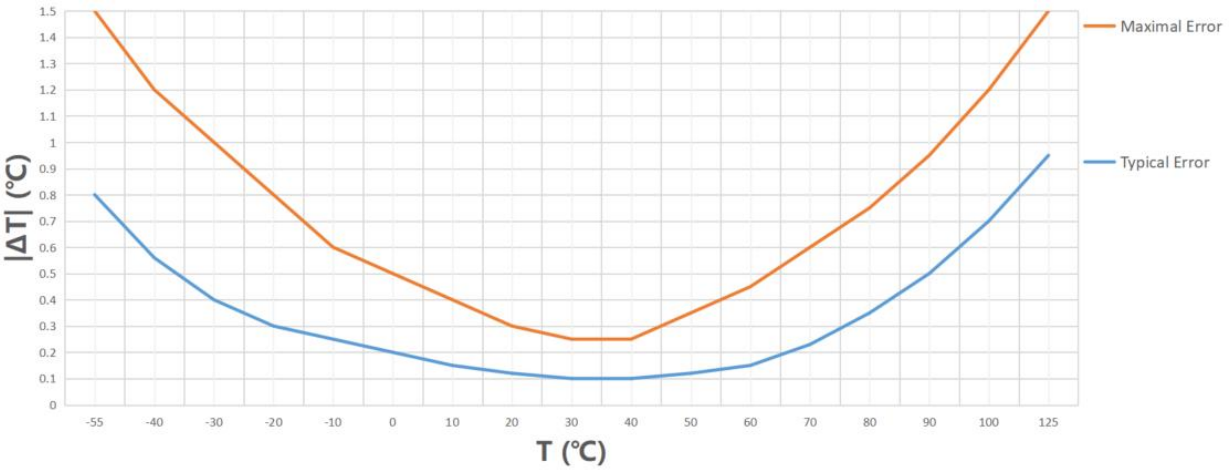


Figure 7-5 T117B Accuracy Error Curve

8. Electrical Specifications

8.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Parameter	Rating	Unit
Supply Voltage VDD	-0.3 to 6	V
Pin Voltage	-0.3 to 6	V
Pin Current	±100	mA
Operating junction temperature	-103 to 153	℃
Storage Temperature Range	-103 to 153	℃
Soldering Temperature	per IPC/JEDEC J-STD-020 specification	
ESD HBM (Human-body model)	±8	kV

8.2 Electrical Characteristics

Typical specifications are at T=25℃ and VDD=3.3V。

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Power Supply							
Operating voltage range	VDD	—	1.8	3.3	5.5	V	Chip pin voltage
Quiescent current	IDD	Idle State (Single Measurement Mode)	—	0.01	—	uA	Idle current in single measurement mode
		Idle State (cycle Measurement	—	50	—	uA	Standby current in cycle

		Mode)					measurement mode
		Active Conversion	—	360	—	uA	Active Conversion
		Average	—	2	—	uA	single measurement mode，AVG=8, 1 measurement/s
Digital input/output							
Input Logic Low	VIL	SCL, SDA	—	—	0.3*VDD	V	
Input Logic High	VIH	SCL, SDA	0.7*VDD	—	—	V	
output Logic low	VOL	IOL = -3 mA	—	—	0.4	V	
Input leakage current	IIN	—	-0.1	—	0.1	uA	
Pull-up resistor	Rup		1	4.7	10	kΩ	

8.3 AC Electrical Characteristics - Non-Volatile Memory

-55℃~+125℃; V_{DD}=1.8V~5.5V

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Write time	t_{WR}	—	—	—	40	ms
E^2PROM Write Cycles	N_{EEWR}	-55°C to+55°C	50000	—	—	cycles
E^2PROM Data Retention	t_{EEDR}	-55°C to +55°C	—	10	—	years

9. Functional Description

Upon powering up the sensor, it enters an idle state awaiting a command from the host to initiate temperature measurement. After the conversion time, the 16-bit temperature data is stored in the temperature register (Temp_lsb/Temp_msb) and is available for reading. The conversion time and average counts setting are related; the more the average counts, the longer the conversion time. For details on average counts and corresponding temperature conversion times, refer to Section 9.3.

9.1 Temperature Output and Conversion Formula

The digital output of the temperature is a 16-bit signed binary code with the LSB resolution of 1/256°C, and S is the sign bit, the data is stored in the Temp_lsb and Temp_msb registers.

Table 9.1 Temperature register（Temp_lsb/Temp_msb）, address 0x00 & 0x01

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
high byte	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8

Low byte	**S**	**2^6**	**2^5**	**2^4**	**2^3**	**2^2**	**2^1**	**2^0**

The conversion relationship between Celsius and Celsius is:

$$T[℃] = \frac{S_T}{256} + 25$$

For example,

25°C corresponds to the register value of 0x00 00

153°C corresponds to the register value of 0x7F FF

-103°C corresponds to the register value of 0x80 00

9.2 Command Registers

The command registers consist of the temperature measurement command register and the E²PROM command register, each comprising two bytes. The Temp_Cmd register includes the measurement mode and heater configuration bits, detailed as follows:

table 9.2-1 temperature measurement command register（Temp_Cmd），address 0x04

Bit	Description	Default Value
7:6	Measurement mode selection (Measurement) 00: Continuous measurement mode 01: Stop measuring 10: Continuous measurement mode, readback value 00 11: Single measurement mode	'01'
5:4	reserve	'00'
3:0	Heater function 1010: Heating function on Others: Heating function off, readback value 0000	'0000'

The chip is in the state of stopping measurement by default after powering up, waiting for the host to send the measurement command. A single measurement only completes one temperature conversion, and the chip will enter the sleep state after completion, unless bit0 of Temp_Cfg is set to 0. Continuous measurement mode will measure the temperature cycle according to bit7~bit5 (MPS) of Temp_Cfg, and the chip won't enter the sleep state in the interval between two conversions, even if bit0 of Temp_Cfg is set to 1. The chip will not go to sleep during the interval between two transitions, even if bit0 of Temp_Cfg is set to 1. In continuous measurement mode, when the host computer writes 01 to bit7~bit6, it will make the chip exit from continuous measurement mode.

The E²PROM command register (E²PROM_Cmd) includes operations for reading and writing to E²PROM and soft reset configurations, as detailed below:

Table 9.2-2 E2PROM command Register (E2PROM_Cmd), Address 0x17

Bit	Default value	Default value
7:0	E²PROM operation 0xB6: Load the value of the E²PROM to the staging memory 0x08: Write the value of the temporary memory to E²PROM 0x6A: System soft reset, while loading the value of E²PROM to the staging registers, all staging registers are restored to their default	'00000000'

	values Other: no operation, readback value 0x00	

9.3 Configuration Register

The configuration register (Temp_Cfg) includes configuration bits for cycle measurement frequency, temperature measurement average number of times, low power mode, etc., as described below:

Table 9.3-1 Configuration Register (Temp_Cfg), Address 0x05

Bit	Description	Default Value
7:5	Measurements per second configuration (MPS) 000: 8 per second 001: 4 per second 010: 2 per second 011: 1 per second 100: 1 time in 2 seconds 101: 1 time in 4 seconds 110: 1 time in 8 seconds 111: 1 time in 16 seconds	'011'
4:3	Temperature measurement average number of configurations (AVG) 00: AVG=1 01: AVG=8 10: AVG=16 11: AVG=32	'01'
2:1	reserve	'00'
0	Low power mode switch (Sleep_en) 0: do not enter low-power mode after executing the instruction 1: Enter low-power mode after executing instructions	'1'

Table 9.3-2 Correspondence between average frequency and conversion time

AVG[1:0]		Number of data	Conversion time t_{CONV}
0	0	1	2.2ms
0	1	8	5.2ms
1	0	16	8.5ms
1	1	32	15.3ms

9.4 Status Register

The Status register (Status) is in read-only mode and contains information such as temperature transition status, alarm status, E^2PROM status, heating status, etc. It is described as follows:

Table 9.4 Status Register, Address 0x03

Bit	Description			Default Value
7	Temperature high line alarm tracking	0: Temperature alarm not triggered	1: Temperature alarm trigger	'0'
6	Temperature low line alarm tracking	0: Temperature alarm not triggered	1: Temperature alarm trigger	'0'

5	Temperature transition state	0: Temperature conversion complete	1: During temperature conversion	'0'
4	E^2PROM status	0: not in read/write state	1: In read/write state	'0'
3	heating state	0: not in heating state	1: In a heated state	'0'
2	Temperature alarm error indication	0: TH is greater than TL	1: TH is less than or equal to TL	'0'
1:0	reserve			'00'

Please note that the flag bit signal indicating the temperature measurement status is stored in the status register (Status). When the temperature measurement is in progress, bit5 of the status register = 1; when the temperature measurement is completed, bit5 of the status register = 0.

9.5 CRC Check Function

The chip includes a CRC data checksum function to improve communication reliability. the CRC value is stored in a specific address byte , which corresponds to the following register combination:
(1) The CRC checksum value of 2 bytes of data from address bytes 0x00 to 0x01 is made as Crc_temp and stored in address byte 0x02;
(2) The CRC checksum value of 8 bytes of data from address bytes 0x03 to 0x0A, done as Crc_scratch, is stored in address byte 0x0B;
(3) The CRC checksum value of 10 bytes of data from address bytes 0x0C to 0x15, done as Crc_scratch_ext, is stored in address byte 0x16.
The computational polynomial for the specific CRC is:

$$CRC = X^8 + X^5 + X^4 + 1$$

This algorithm circuit consists of shift register and iso gate circuit with initial value 0x00 and has the following structure:

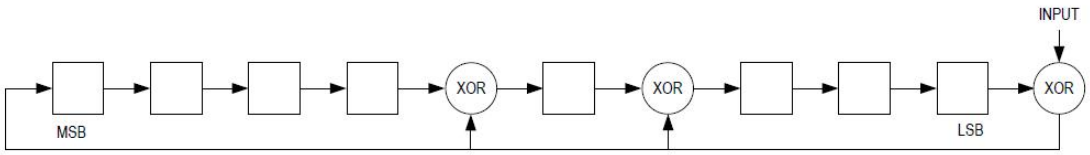


Figure 9.5 CRC generator

I^2C can read (1) one CRC checksum byte and a 1-wire bus can read (1) (2) (3) three CRC checksum bytes. When using the Match ROM command in 1-wire bus mode, the three CRC checksum bytes need to be calculated together by adding the first 7 bytes of the ROM code before the value of registers, corresponding to the following register combination:
(1) The CRC checksum value for the9 bytes of data from address bytes 0x18 to 0x1E, 0x00 to 0x01, as Crc_match_temp, is stored in address byte 0x02;
(2) The CRC checksum value for the 15 bytes of data from address bytes 0x18 to 0x1E, 0x03 to 0x0A, as Crc_match_scratch, is stored in the address byte 0x0B;
(3) The CRC checksum value for the 17 bytes of data from address bytes 0x18 to 0x1E, 0x0C to 0x15, as Crc_match_scratch_ext, is stored in the address byte 0x16.

9.6 Alarm function

Alert mode is used to monitor the ambient temperature and is achieved by configuring the Alert Mode register (Alert_Mode), as well as the Alarm High and Low Threshold registers (Th/Tl). When the

temperature exceeds the preset alarm threshold, the output level of the ALERT pin will change. In addition, the Status register (Status) bit has dedicated bits to indicate the alarm status, as described in section 9.4. The ALERT pin signal can control a switch or be connected to the interrupt pin of a microcontroller. After the sensor issues an alarm, the microcontroller can wake up from sleep mode and perform specified operations.

The Alert-Mode includes configuration bits such as alarm switch, mode selection, polarity selection, port function selection. The specific content of the configuration register is described as follows:

Table 9.6 Alert Mode Register (Alert_Mode), Address 0x06

Bit	Description	Default Value
7	Alarm function switch (Alert_en) 0: Closed 1: Open	'0'
6	Alarm mode (IM) selection 0: Above TH alarm and below TL release alarm 1: Above TH alarm and below TL alarm	'0'
5	Alarm polarity (POL) selection 0: low level effective 1: high level effective	'0'
4	Alarm port output mode (FUNC) selection 0: output temperature alarm sign bit 1: output temperature measurement completion sign bit	'0'
3:0	reserve	'0000'

The alarm threshold registers include the high threshold register (Th) and the low threshold register (Tl), both of which correspond to the resolution of the temperature registers (Temp_lsb/Temp_msb), as described in Section 9.1. The 16-bit signed number of the alarm threshold will be compared with the 16-bit standard output temperature value to determine whether the alarm condition has been met, so the resolution of the temperature alarm threshold is the same as temperature sensing resolution $\Delta T \approx 0.004°C$.

When the alarm function is turned on, the Alert Mode is activated whenever the sensor performs a measurement operation, subsequently, the host can reset the level of the ALERT port by reading the temperature register. If the alarm function needs to be turned off, the host can set bit7 of the Alarm Configuration Register (Alert_Mode) to 1. Additionally, the alarm function can be turned off by setting the Alarm Low Line Setting Value to a value greater than or equal to the Alarm High Line Setting Value (Tl≥Th). The following alarm modes can be realized by changing the alarm mode bit (IM) of the alarm mode register:

(1) Higher than the high limit alarm, lower than the low limit release alarm mode.

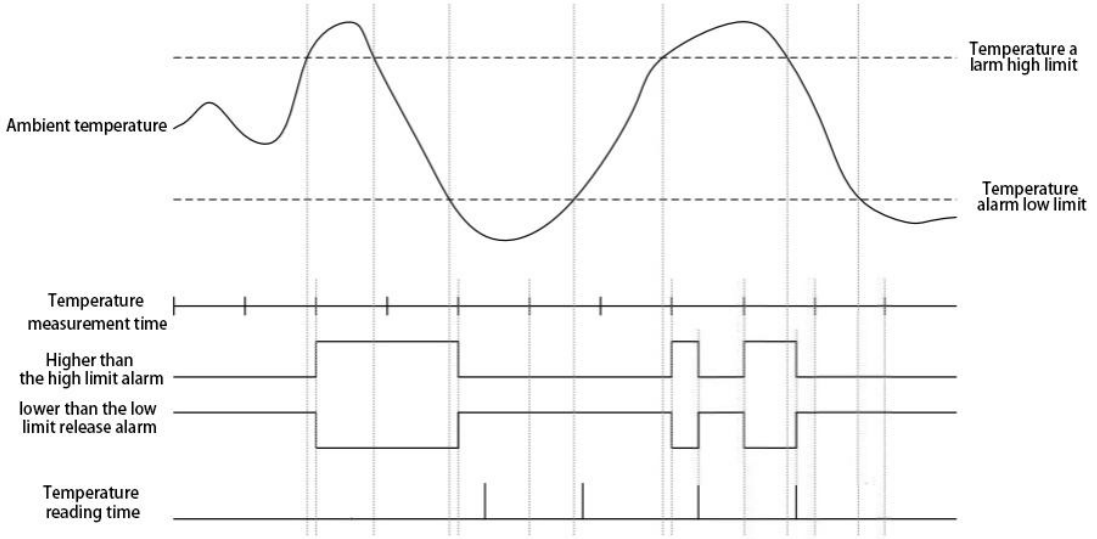


Figure 9 .6-1 Timing diagram for alarm above high limit and de-alarm mode below low limit

This mode corresponds to IM=0, bit7 in the status register (Status) is the same as the flag bit of the above figure for exceeding the high limit alarm, and bit6 is 0.

(2) Above high limit alarm, below low limit alarm mode .

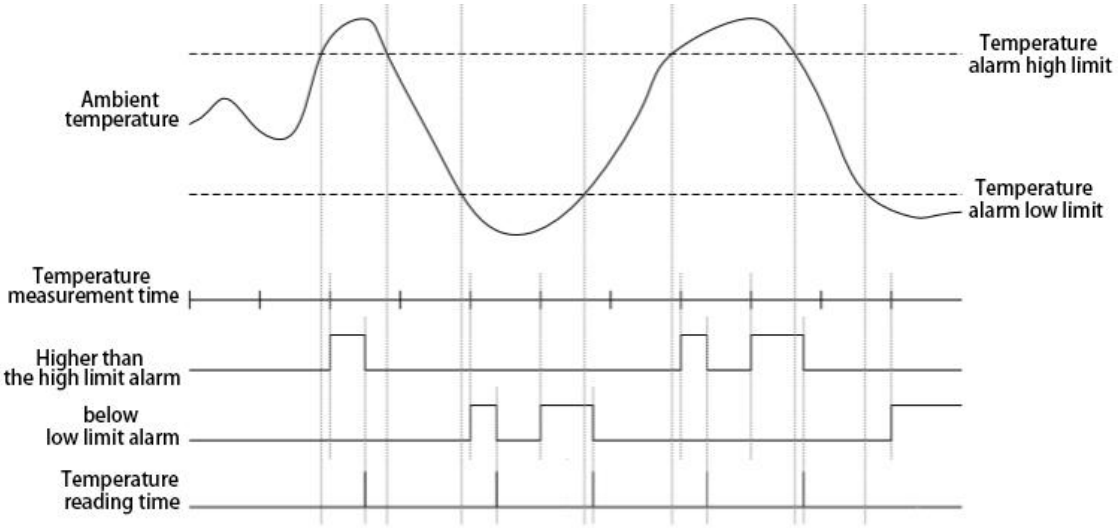


Figure 9 .6-2 Timing Diagram for Alarm Above High Limit, Alarm Below Low Limit Modes

This mode corresponds to IM=1, bit7 in the status register (Status) is the same as the flag bit for exceeding the high limit alarm as shown above, and bit6 is the same as the flag bit for falling below the low limit alarm as shown above.

It should be noted that by configuring bit4 in the Alert-Mode, the signal definition of the ALERT port can be selected:

When the host sets bit4 of the Alert-Mode to 0, the ALERT pin will output a temperature alarm flag bit;

When the host sets bit4 of the Alert-Mode to 1, the ALERT pin will output a temperature measurement completion pulse flag, and the alarm flag will no longer be output.

However, when bit4=1, it only disable the alarm output function of the ALERT port, not the alarm function of the chip. As long as bit7=1 in the Alert-Mode, alarm status information can still be obtained by reading bit7 and bit6 in the status register (Status).

9.7 Heating as a Self-diagnosis Function

The chip is equipped with an internal heating resistor for heating the chip, and the host can read the temperature value before and after heating to determine whether the chip temperature measurement function is normal. The heating power is 7.8mW, and the temperature increase is above 0.1°C. The temperature measurement function is performed by the temperature measurement command register (Temp_cmd). The function is activated and deactivated by bit3~bit0 in the Temperature Command Register (Temp_cmd), and the configuration details are shown in section 9.2.

9.8 Soft Reset

The host can realize the soft reset function of the chip by writing 0x6A to the E^2PROM command register (E^2PROM_Cmd). During soft reset, the register values that have correspondence with E^2PROM will be reloaded, and other register values that do not have correspondence with E^2PROM will be reset to the power-on default values. For the correspondence of specific registers with E^2PROM, please refer to Section 10.

9.9 Parasitic Mode

The chip can be powered by the external power supply on the VDD pin under the 1-wire bus protocol, or it can be powered by the "parasitic" mode, which allows the chip to work without external power supply. The following figure shows the circuit diagram of the chip in parasitic mode, the MCU side of the VDD power supply range of 2.5V-5.5V, the SDA pin is used as a DQ, when DQ is high, it is through the DQ pin "steal" the power supply, DQ is high, some of the charge is stored in the storage capacitor (C) in order to provide power for the chip in the bus for the low time. In parasitic mode, the storage capacitor can supply enough current to the chip as long as the specified capacitance and voltage requirements are met (see DC Characterization and AC Characterization).

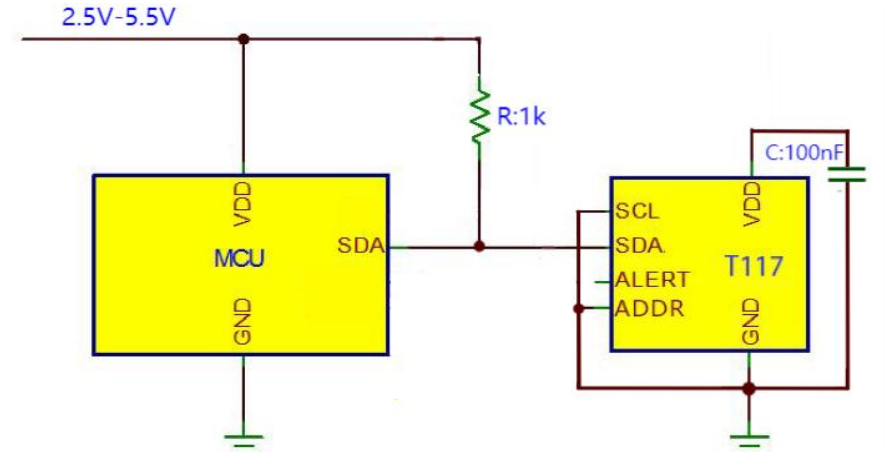


Figure 9 .9 Parasitic Mode Typical Circuit Diagram Diagram

Note: The recommended pull-up resistor resistance value is 1kΩ and the energy storage capacitor is not less than 100nF.

This application is limited to the 1-wire bus protocol, and requires modifying the register value of logical address 0x63 to 0x0A under the condition that the chip VDD is powered by an external power supply.

Table 9.9 Operating Mode Configuration Register (PPM_Cfg), Address 0x63

Bit	Description	Default Value

7:4	reserve	'0000'
3:0	Parasitic mode function switch 1010: Open Other: Closed	'0000'

9.10 Chip ID

The chip ID is 64 bits and is stored in the chip ID register (Romcode) in the format:

Table 9.10 Chip ID Registers (Romcode), Addresses 0x18 ~ 0x1F

Bit	Register Name	Register address	Power on reset default value
7:0	Romcode1	0x18	0x01
15:8	Romcode2	0x19	0x16
16:23	Romcode3	0x1A	Factory value
24:31	Romcode4	0x1B	Factory value
32:39	Romcode5	0x1C	Factory value
40:47	Romcode6	0x1D	Factory value
48:55	Romcode7	0x1E	Factory value
56:63	crc_romcode	0x1F	Factory value

10. Storage System

10.1 Register Table

The sensor's memory is organized as shown in Table 10.1. The memory contains an SRAM register as well as expanded storage non-volatile storage E^2PROM for storing the high and low temperature alarm trigger lines (Th and Tl), the temperature configuration register (Temp_Cfg), the alarm mode register (Alert_Mode), and the 10-byte user programmable region (User_define). Note that the Alarm High (Th) and Alarm Low (Tl) registers can be used as general-purpose memory areas if the sensor's alarm function is not being used. All memory function definitions are described in detail in Section 9.

Table 10.1 Register table and E^2PROM Mapping

Register Name	Bit width	Register address	1-wire bus read	1-wire bus write	E^2PROM address	1-wire bus read	1-wire bus mount E^2PROM	Power on reset default value
Temp_lsb	8	00h	Read temperature (0xBC)	NA	NA	NA	NA	00h
Temp_msb	8	01h		NA	NA	NA	NA	00h
Crc_temp	8	02h		NA	NA	NA	NA	NA
Status	8	03h	Read scratchpad (0xBE)	NA	NA	NA	NA	00h
Temp_Cmd	8	04h		Write config (0x4E)	NA	NA	NA	40h
Temp_Cfg	8	05h			00h	Copy page (0x48)	Recall EE (0xB8) / Recall	69h
Alert_Mode	8	06h			01h			00h
Th_lsb	8	07h			02h			FFh
Th_msb	8	08h			03h			7Fh

Tl_lsb	8	09h			04h		page (0xB6)	00h
Tl_msb	8	0Ah			05h			80h
Crc_scratch	8	0Bh		NA	NA			NA
User_define_0	8	0Ch	Read scratchpad extension (0xDD)	Write scratchpad extension (0x77)	06h			00h
User_define_1	8	0Dh			07h			00h
User_define_2	8	0Eh			08h			00h
User_define_3	8	0Fh			09h			00h
User_define_4	8	10h			0Ah			00h
User_define_5	8	11h			0Bh			00h
User_define_6	8	12h			0Ch			00h
User_define_7	8	13h			0Dh			00h
User_define_8	8	14h			0Eh			00h
User_define_9	8	15h			0Fh			00h
Crc_scratch_ext	8	16h		NA	NA	NA	NA	NA
E^2PROM_Cmd	8	17h	NA	NA	NA	NA	NA	00h
Romcode1	8	18h	Read romcode (0x33)	NA	NA	NA	NA	01h
Romcode2	8	19h		NA	NA	NA	NA	16h
Romcode3	8	1Ah		NA	10h	NA	Recall EE (0xB8)	(1)
Romcode4	8	1Bh			11h			(1)
Romcode5	8	1Ch			12h			(1)
Romcode6	8	1Dh			13h			(1)
Romcode7	8	1Eh			14h			(1)
crc_romcode	8	1Fh		NA	NA			NA

Notes:

(1) This byte is the factory value.

(2) There is also 11 bytes of E^2PROM space inside the chip for analog performance, special function configuration, and information storage, which can be obtained by contacting the manufacturer.

10.2 E^2PROM

The host needs to realize the function trigger of E^2PROM by writing a specific value to the E^2PROM command register (E^2PROM_Cmd). To permanently write data from a register to the E^2PROM, the host must write 0x08 to the E^2PROM command register to accomplish this.The data in the E^2PROM registers are held at power down and automatically loaded into the appropriate register location at power up. Data can also be reloaded by the host writing 0xB6 to the E^2PROM command register. Please note that the write operation to the E^2PROM operates as a 16-byte whole, and you need to make sure that the contents of all 16 registers are correct before making a unified copy.

The operating status of the E^2PROM is reflected in bit4 of the status register (Status): when the E^2PROM read/write is in progress, bit4 of the status register = 1; when the E^2PROM read/write is finished, bit4 of the status register = 0.

10.3 I^2C and 1-wire Bus Commands

This chip supports two communication modes, I^2C and 1-wire bus. Table 10-3 gives the operation methods of the two communication modes corresponding to different functions.

Table 10-3 List of I²C and 1-wire bus Functions

Name	Function	I²C Function Trigger	1-wire bus command
search rom	Search for romcode	-	0xF0
read rom	Read romcode	Read corresponding byte	0x33
match rom	Match rmcode	-	0x55
skip rom	Ignore romcode	-	0xCC
alarm search	Search for Alarm Chips	-	0xEC
convert temperature	measured temperature	Write Temp_Cmd (Address: 0x04)	0x44
read temperature	Read two bytes of the temperature value	Read corresponding byte	0xBC
heat_on	Chip internal heating resistor on	Write Temp_Cmd (Address: 0x04)	0x91
heat_off	Chip internal heating resistor off	Write Temp_Cmd (Address: 0x04)	0x92
soft reset	Reset the entire chip, load E²PROM data to registers, and restore other registers to their initial values on power-up	Write E²PROM_Cmd (Address: 0x17)	0x6A
break	Stop cycle measurement mode	Write Temp_Cmd (Address: 0x04)	0x93
read scratchpad	Read the scratch area	Read corresponding byte	0xBE
write config	Setting the config area	Write the corresponding byte	0x4E
read scratchpad extension	Read the scratch extended region	Read corresponding byte	0xDD
write scratchpad extension	Setting up the scratch extension area	Write the corresponding byte	0x77
copy page	Save register data to E²PROM	Write E²PROM_Cmd (Address: 0x17)	0x48
recall page	Load E²PROM Data to Registers	Write E²PROM_Cmd (Address: 0x17)	0xB6
recall EE	Load all 32 bytes of E²PROM data into registers	Write E²PROM_Cmd (Address: 0x17)	0xB8

11. I²C Bus Protocol

The sensor implements the I²C bus communication interface protocol via the dual SDA and SCL pins, and can support fast modes up to 1 MHz. Each transmission sequence begins with a START condition (S) and ends with a STOP condition (P), as described in the I²C-bus specification.

11.1 I²C Address

Slave I²C address supports extension function, offering 4 configurations, The specific addresses are related to the signal connection of the ADDR pin. The specific correspondences are as follows:"

Slave I²C address	ADDR connection level
01000000	GND
01000001	VDD
01000010	SDA
01000011	SCL

Figure 11.1 the mapping relationship between I²C address and ADDR pin

11.2 Read and Write

I²C bus communication, the host first sends the Slave Address and Write Flag bit (Slave Address + W), followed by the Register Logical Address (Register Address). For read timing, the host then sends the Slave Address and Read Flag bit again (Slave Address + R), and then the slave sends data to the host (Data from Register); for write timing, the host then sends data directly to the slave (Data to Register). Note that the width of the slave address is 7 bits, the write flag bit W = 0, and the read flag bit R = 1. The specific read/write timing diagram is as follows:

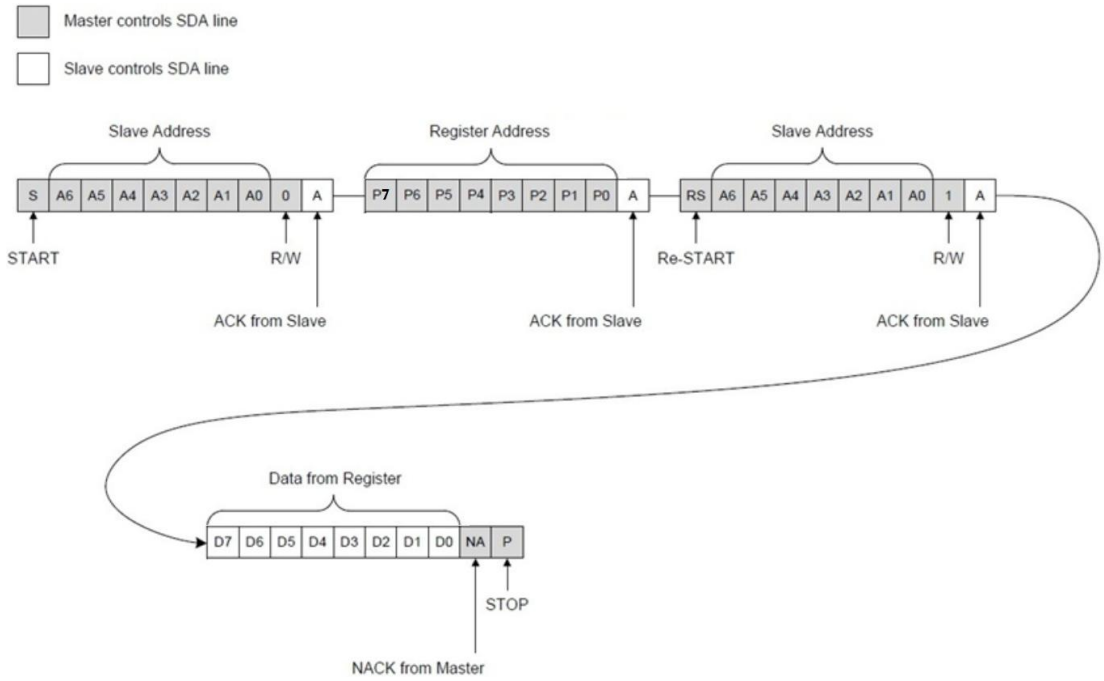


Figure 11.2-1 I²C Read Timings

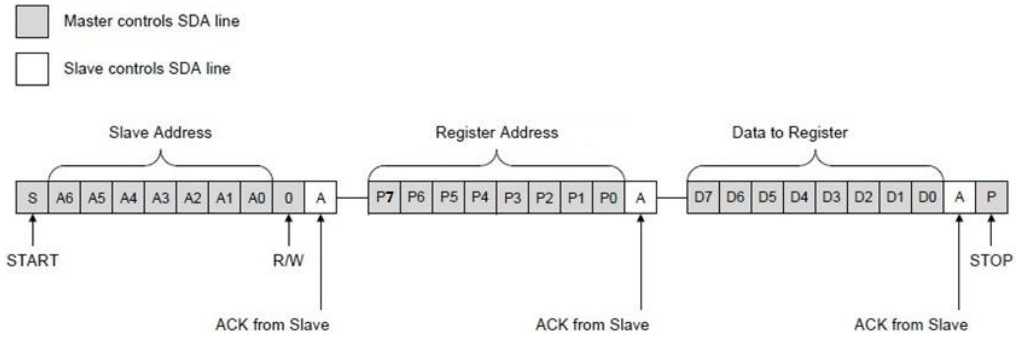


Figure 11.2-2 I²C Write Timings

For the reading of the temperature register low Temp_lsb and high Temp_msb, in order to verify the correctness of the transmitted data, the host can continue to read the Crc_temp register without sending Stop immediately after reading the data in the Temp_msb register, and then send Stop again.

11.3 I²C Timing Characteristics

Table 11.3 I²C Bus Timing Characteristics

Parameters	Symbol	Standard mode		Fast mode		Unit
		MIN	MAX	MIN	MAX	
SCL frequency	f_{SCL}	0	400	0	1000	kHz
SCL low level time	t_{LOW}	1300	—	400	—	ns
SCL high level time	t_{HIGH}	600	—	450	—	ns
Duration of SCL high after SDA pull down at start(restart)	$t_{HD;STA}$	400	—	100	—	ns
Time interval from the start of SCL pull-down to the change in SDA data	$t_{HD;DAT}$	0	0.9	0	—	μs
Time interval from the start of SDA data stabilization to SCL pull-up	$t_{SU;DAT}$	100	—	50	—	ns
SCL high level time before SDA is pulled down at restart.	$t_{SU;STA}$	400	—	150	—	ns
Interval from SCL pull-up to SDA pull-up at stop time	$t_{SU;STO}$	400	—	100	—	ns
Interval between start and stop	t_{BUF}	1300	—	500	—	ns
Time required for SCL/SDA rising edge	t_{RC}	20+0.1 C_b (1)	1000	20+0.1C $_b$ (1)	50	ns
Time required for SCL/SDA falling edge	t_{FC}	20+0.1 C_b (1)	300	20+0.1C $_b$ (1)	100	ns

Note 1：Cb=The total capacitance of the I²C bus，the unit is pF。

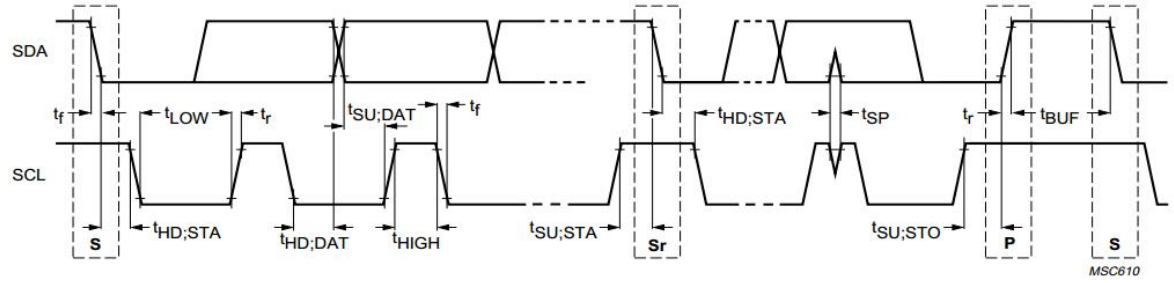


Figure 11.3 I²C Timing Parameters

12. 1-wire Bus System

T117default IO is I²C interface, by writing 10101010 to the mode register Mode_Cfg (0X68), I/O can be changed to a 1-wire interface, at this time the SDA is a 1-wire DQ. After switching modes, you need to send a Copy E²PROM command for power-down preservation, the command can be obtained by contacting the manufacturer.

1-wire bus systems use a single signal line with a master controlling one or more slave devices. Sensors are always slaves. When there is only one slave device on the bus, the system is referred to as a "single-point" system; when there are multiple slave devices on the bus, it is referred to as a

"multipoint" system. All data and command transfers on a 1-wire bus start at the lowest bit. The following description of a 1-wire system is divided into three topics: hardware configuration, transmission sequences, and 1-wire signaling (signal types and timing).

12.1 Hardware Configuration

By definition, a 1-wire bus has only one data line. Each device (master or slave) is connected to the data line through an open-drain or tri-state port. This allows the device to "free" the data line when no data is being transferred, thus making the bus available to other devices.
The internal equivalent circuit of the sensor's 1-wire bus port (DQ pin) is an open drain, as shown in Figure 12.1. The 1-wire bus requires an external pull-up resistor of approximately 4.7 kΩ so that the idle state of the 1-wire bus is high. If for any reason the transmission needs to be paused, the bus must remain idle until the transmission has returned. During recovery, the recovery time between data bits can be infinitely long as long as the 1-wire bus remains in the inactive (high) state. If the bus is pulled low for more than 480 μs, all devices hanging on the bus will be reset.

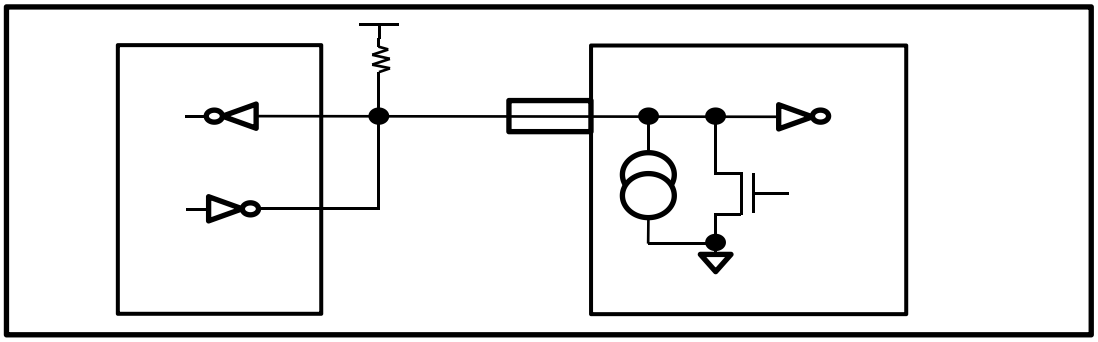


Figure 12.1 1-wire bus hardware configuration

12.2 Transaction Sequences

The transmission sequence for accessing the sensor is as follows:

Step 1 Initialization
Step 2 ROM command (follows any necessary data exchange)
Step 3 Sensor function command (following any necessary data exchange)

It is important to ensure this sequence every time the sensor is accessed, as any steps missing or out of sequence will result in the sensor not responding. The only exceptions to this are the Search ROM [F0h] and Alarm Search [ECh] commands. When these ROM commands are issued, the host must return to step 1 in the sequence.

12.3 Initialization

All execution (processing) over a 1-wire bus begins with an initialization sequence. The initialization sequence consists of a reset pulse issued by the bus controller followed by a presence pulse issued by the slave. The presence pulse lets the bus host know that the slave device is on the bus and ready to operate. The timing of the reset and presence pulses is detailed in the 1-wire bus Signal Timing section.

12.4 ROM Commands

When the bus host detects the presence of a pulse, it can issue ROM commands. These commands operate on a unique 64-bit ROM code for each slave device and allow the host to address specific slaves individually if there are multiple slaves hooked up to a 1-wire bus. These commands also allow

the host to determine how many of what type of devices are on the bus and whether any of the devices meet the alarm conditions. There are five ROM commands, each 8 bits long. The master must issue an appropriate ROM commandcommand before issuing a function command for the sensor.

SEARCH ROM [F0h]

When a system is initialized and powered up, the host must identify the ROM codes of all slave devices on the bus so that the host can determine the number and type of slave devices. The host recognizes the ROM codes through a process of elimination, which requires the host to execute a Search ROM loop (e.g., the Search ROM command follows the data exchange) repeatedly until all slave devices are recognized. If there is only one slave device on the bus, a simple Read ROM (below) command can be used instead of the Search ROM command. After each Search ROM cycle, the bus host can return to step 1 (initial state) of the transfer sequence or follow a function command.

Read ROM [33h]

This command allows the bus host to read the 64-bit ROM code of the sensor. This command can only be used if a single sensor is present on the bus. If there is more than one slave on the bus, a data conflict will occur when all slaves attempt to respond at the same time.

Match ROM [55h]

Matching ROM command, followed by a 64-bit ROM code sequence, allow the bus host to address a specific sensor on a multipoint or single-point bus. Only sensors with an exact match of the 64-bit ROM code sequence will respond to a function command from the master. All other slaves will wait for a reset pulse.

Skip ROM [CCh]

This command allows the host to address all devices on the bus simultaneously without sending any ROM codes. For example, the host can cause all sensors on the bus to perform a temperature conversion at the same time by issuing a Skip ROM command to follow a Convert T [44h] instruction. Note that the Read Scratchpad [BEh] command can only follow the Skip ROM command when a single slave device is hooked up to the bus. In this case, time can be saved by allowing the master to read the slave device without sending the 64-bit device ROM code. If there is more than one slave device on the bus, a Skip ROM command following a Read Scratchpad command will result in a data conflict because multiple devices will attempt to transmit data at the same time.

Alarm Search [ECh]

The flowchart for this command is the same as Search ROM, however, only sensors that have the alarm flag bit set will respond to this instruction. This command allows the host device to know if any sensor has reached a temperature alarm condition at the most recent temperature transition. After each Alarm Search cycle (e.g., the Alarm Search command follows a data exchange), the bus host can return to Step 1 (Initialization) of the transfer sequence or follow a function command. The Operation-Alarm Signals section explains the operation of the alarm flag bits.

12.5 Function Commands

When a bus host addresses a sensor with which it wishes to communicate using a ROM command, the host can issue one of the sensor's function commands. These instructions allow the host to write or read data from the sensor's staging device, initiate temperature conversions, and understand the power supply mode. The sensor's function commands, described below, are summarized in Table 12.5.

CONVERT TEMPERATURE [44h]

This command initiates a temperature conversion. After the conversion, the collected temperature data is stored in the first two bytes of the temperature register, and then the sensor will enter a low power state. The host can issue a read time slot after the Convert Temperature instruction, and then the sensor will respond with a 0 or 1 to indicate that the temperature conversion is in progress or has completed.

READ TEMPERATURE [BCh]

This command allows the host to read the contents of the temperature value register. The data transfer begins at the lowest bit of byte 0x00 and continues traversing the register until byte 0x02 (the temperature cyclic redundancy verification code) is read. all 3 bytes are read, and the sensor enters low power mode by default.

WRITE SCRATCHPAD [4Eh]

This command allows the host to write up to 7 bytes of data to the sensor register. The data transfer begins at the lowest bit of byte 0x04 and continues traversing the register until the highest bit of byte 0xA. All 7 bytes must be written before the host sends a reset signal or the data may be corrupted. (This means that the host can abort the write at any time with a reset).

READ SCRATCHPAD [BEh]

This command allows the host to read the contents of the Scratch register. The data transfer starts at the lowest bit of byte 0x03 and continues traversing the register until byte 0xB (Scratch Cyclic Redundancy Verification Code) is read. 9 bytes are read and the sensor enters low power mode by default. If only a portion of the data in the register is needed, the host can terminate the read at any time by issuing a reset signal.

WRITE SCRATCH_EXTENSION [77h]

This command allows the host to write up to 10 bytes of data to the sensor register. The data transfer begins at the lowest bit of byte 0xC and continues traversing the register until the highest bit of byte 0x15. All 10 bytes must be written before the host signals a reset or the data may be corrupted. (This means that the host can abort the write at any time with a reset).

READ SCRATCH_EXTENSION [DDh]

This command allows the host to read the contents of the Scratch Extension register. The data transfer begins at the lowest bit of byte 0xC and continues through the register until byte 0x16 (the Scratch Extension Cyclic Redundancy Verification Code) is read. 11 bytes are read and the sensor enters a low power mode by default. If only a portion of the data in the register is needed, the host can terminate the read at any time by issuing a reset signal.

COPY PAGE [48h]

This command copies 16 bytes of data from the register to the E^2PROM (see Table 10.1 for correspondence).

RECALL PAGE [B6h]

This command loads 16 bytes of data from the E^2PROM into the register (see Table 10.1 for correspondence). The host device can follow the RECALL PAGE command by posting consecutive read time slots, and then the sensor indicates the status of the load, transmitting a 0 to indicate that the

load is in progress, and a 1 to indicate that the load has ended.

RECALL EE [B8h]

This command loads all 32 bytes of data from the E^2PROM into the register (see Table 10.1 for correspondence). The host device can follow the RECALL EE command by issuing consecutive read time slots, and the sensor will then indicate the status of the load, transmitting a 0 to indicate that the load is in progress, or a 1 to indicate that the load has been completed. This loading operation is performed automatically at power-up, so the sensor will have valid data in its registers immediately after power-up.

Table 12.5 Temperature Sensor Function Command Set

Command	Description	Protocol	Activity on 1-wire bus	Note
Temperature conversion command				
Convert Temperature	Initiate temperature conversion	44h	The sensor transmits the conversion status to the host: if the result of reading the time slot is 0, it is busy; if it is 1, the conversion is finished	
read and write commands				
Read Temperature	Read temperature two bytes + cyclic redundancy check	BCh	Sensor transmits 2 bytes of temperature value + CRC to host computer	
Read Scratchpad	Read all Scratch register contents + cyclic redundancy check	BEh	Sensor transmits 8 bytes + CRC to host computer	(1)
Write Scratchpad	Write Data to Scratch Registers	4Eh	Host transmits 7-byte sensors	(2)
Read scratchpad extension	Read all Scratch extended register contents + cyclic redundancy checksums	DDh	The sensor transmits up to 11 bytes to the host	(1)
Write scratchpad extension	Write Data to Scratch Extended Register Contents	77h	The host transfers 10 bytes of data from the extended staging area to the sensor.	(2)
Break	Stop continuous measurement mode	93h	N/A	
Copy Page	Copy 16 bytes of data from register to E^2PROM	48h	Write E^2PROM time 40ms	
Recall Page	Load 16 bytes of data from E^2PROM to registers	B6h	Sensor transmits call status to host	
Recall EE	Load all 32 bytes of data from E^2PROM to registers	B8h	Sensor transmits call status to host	
Chip related				
Soft Reset	Reset chip, load E^2PROM data to registers, restore other registers to initial values at power-up	6Ah	N/A	
Heat_On	Chip internal heating resistor on	91h	N/A	
Heat_Off	Chip internal heating resistor off	92h	N/A	

Note 1: The host can interrupt data transmission at any time by issuing a reset signal.

Note 2: All bytes must be written before the reset signal is issued.

12.6 Signal Timing of 1-wire Bus

The sensor uses a strict 1-wire communication protocol to ensure data integrity. The protocol defines several signaling types: Reset Pulse, Presence Pulse, Write 0, Write 1, Read 0, Read 1. With the exception of the Presence Pulse, all signaling is initiated by the bus host.

Initialization program - reset and presence pulse

All communication with a sensor begins with an initialization sequence that consists of a reset pulse from the host following a presence pulse from a sensor. Fig. 1 2.6- 1 explains this sequence. When a sensor sends a presence pulse in response to a reset pulse, it indicates to the host that it is hooked up to the bus and is ready to operate. During the initialization sequence, the host sends a reset pulse by pulling the 1-wire bus low for at least 480μs. The bus host then releases the bus into receive mode. When the bus is released, a pull-up resistor pulls the bus high. When the sensor detects this rising edge, it waits 15μs to 60μs then issues a presence pulse by pulling the 1-wire bus low for 60μs to 240μs.

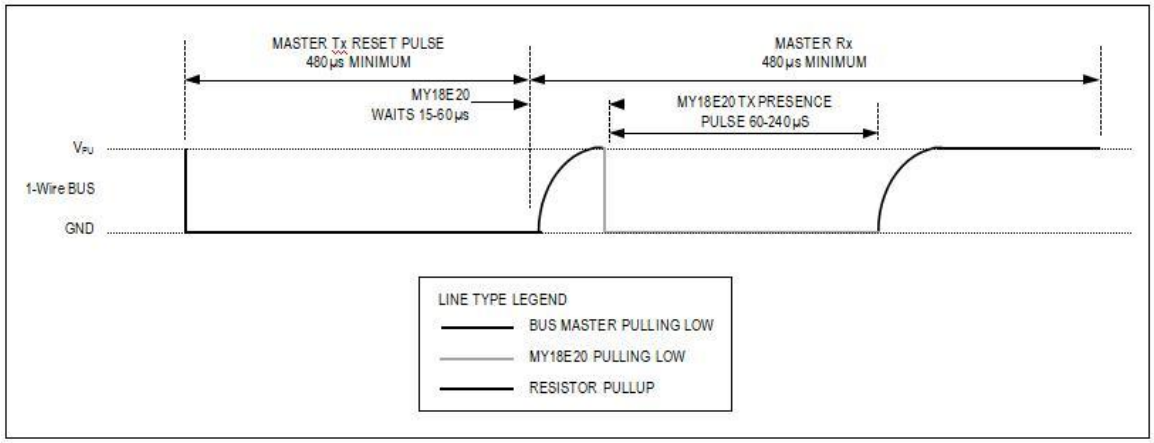


Figure 12.6-1 Initialization Timing

Note: If the chip supply voltage is 1.75V ~ 1.85V, please note that the reset low level (Reset) is extended to 2000μs in order to ensure stable communication.

Read/Write Time Slot

The bus host writes data to the sensor in write time slots and reads data from the sensor in read time slots. Each time slot transfers one data bit on a 1-wire bus.

Write Time Slot

There are two types of write time slots: "Write 1" time slots and "Write 0" time slots. The bus host writes a logic 1 to the sensor via the write 1 time slot and a logic 0 to the sensor via the write 0 time slot. All write slots must last a minimum of 60μs with a recovery time of at least 1μs between writes. Both write time slots are initiated by the host pulling the 1-wire bus low (see Figure 1 2.6- 2).

To generate a write 1 time slot, after pulling the 1-wire bus low, the bus host must release the 1-wire bus within 15μs. After the bus is released, the pull-up resistor pulls the bus high. To generate a Write 0 time slot, after pulling the 1-wire bus low, the bus host must keep the bus low continuously (at least 60μs) for the entire time slot period.

The sensor samples a 1-wire bus in a time window of at least 15μs to 60μs after the host initiates a

write time slot. If the bus is high during this sampling time window, a 1 is written to the sensor. If the bus is low, a 0 is written to the sensor.

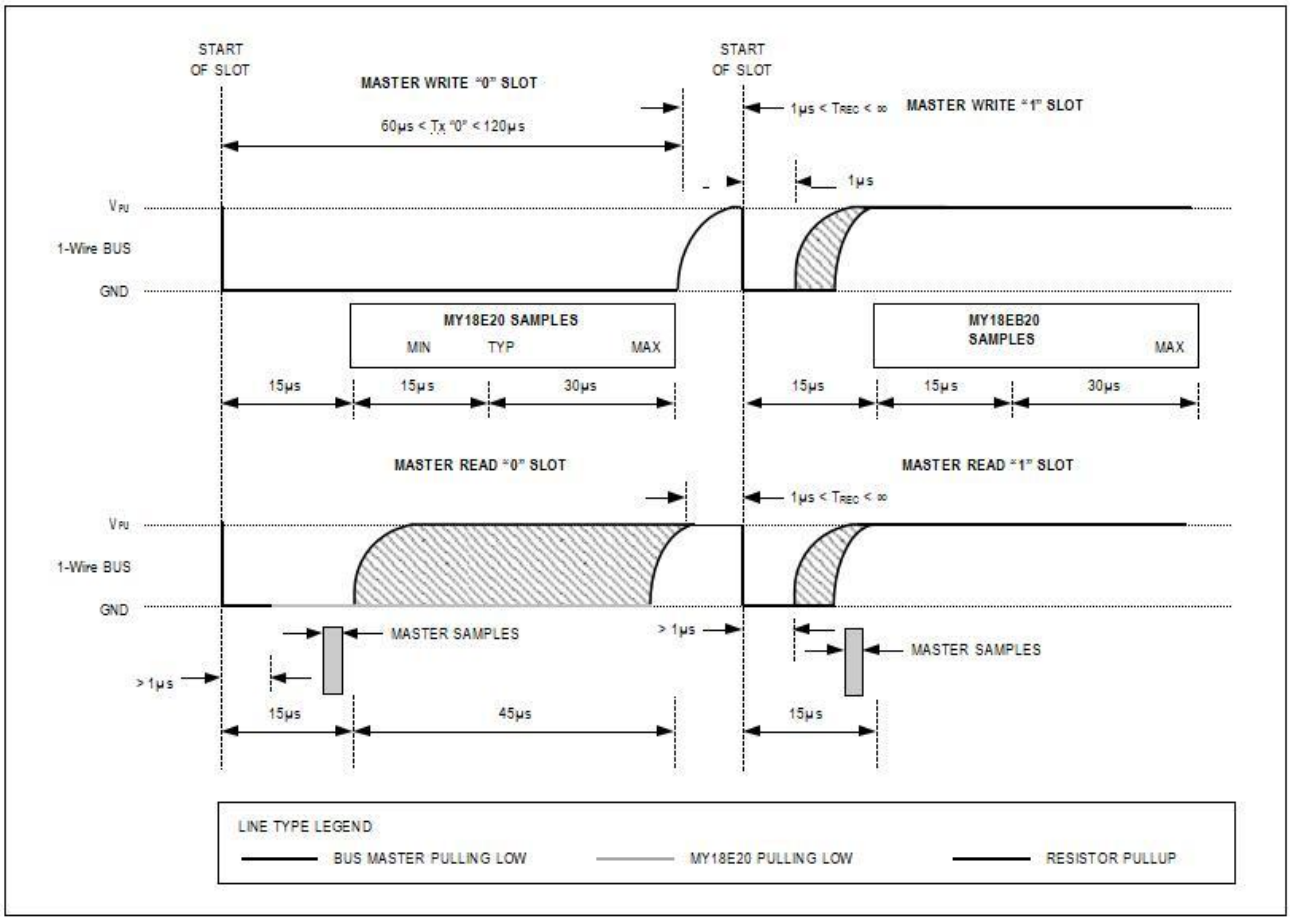


Figure 12.6-2 Read/Write Time Slot Timing

Read Time Slot

The sensor can only transmit data to the host during the time the host issues a Read Scratchpad. All, the host must generate a read time slot immediately after issuing a Read Scratchpad [BEh] command so that the sensor can provide the requested data. Alternatively, the host can generate a read time slot after issuing a Convert T [44h] or Recall EE [B8h] command for operational status. This part of the mechanism is explained in detail in the Sensor Function commands section. All read time slots must last at least 60µs with a recovery time of at least 1µs between writes. read time slots are generated by the host pulling down a 1-wire bus for at least 1µs and then releasing the bus (see Figure 1 2.6-2). After the host initiates a read time slot, the sensor will begin transmitting either a 1 or a 0 on the bus. the sensor sends a 1 by holding the bus high and a 0 by pulling the bus low. when transmitting a 0, the sensor releases the bus at the end of the time slot, after which the bus is pulled back to the high idle state by the pull-up resistor. The sensor's output data is valid for 15µs after the falling edge of the startup time slot. Therefore, the host must release the bus and sample the bus state within 15µs of the start of the time slot. Figure 1 1 2.6-3 illustrates that the sum of t_{INIT} , t_{RC} , and t_{SAMPLE} must be less than 15µs within a read time slot. figure 1 2.6-4 shows that the system's time margin can be maximized by keeping t_{INT} and t_{RC} as short as possible, and by placing the host sampling time at the end of the 15µs period of the read time slot.

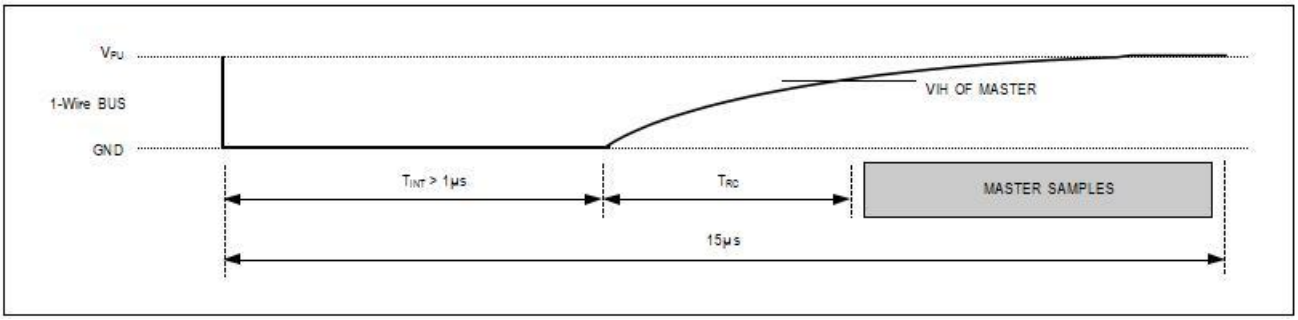


Figure 12.6-3 Detailed Master Read 1 Timing Sequence

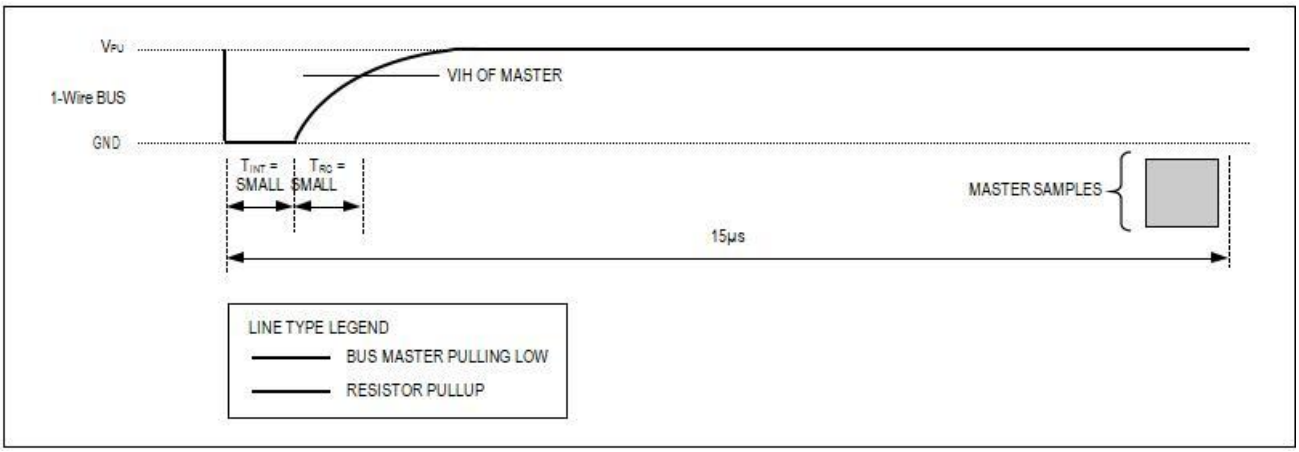


Figure 12 .6-4 Recommended Master Read 1 Timing Sequence

12.7 Temperature Sensor Operation Example 1

In this example there are multiple sensors on the bus. The bus master reads its buffer after initiating a temperature conversion for a particular sensor and then recalculates the cyclic redundancy checksum to validate the data.

Host mode	Data (MSB)	Description
TX	reset	Host sends reset pulse
RX	presence	The sensor responds by the presence of impulses
TX	55h	Host sends Match ROM command
TX	64-bit ROM encoding	The host sends the sensor's ROM code
TX	44h	Host sends Convert T command
	DQ stays high	Mainframe keeps DQ high during temperature transition times
TX	reset	Host sends reset pulse
RX	presence	The sensor responds by the presence of impulses
TX	55h	Host sends Match ROM command
TX	64-bit ROM encoding	The host sends the sensor's ROM code
TX	BCh	Host sends Read Temperature command
RX	3 data bytes	The master reads the entire register including the cyclic redundancy check. The host then recalculates the cyclic redundancy check of the first 2 bytes of data in the register and compares it to the cyclic redundancy check of the read (byte 3). If it matches, the host continues; otherwise, the entire read operation is repeated.

12.8 Temperature Sensor Operation Example 2

In this example there is only one sensor on the bus. The host writes data including Tha_Set_lsb, Tla_Set_lsb, Tha_Set_msb, and Tla_Set_msb to the sensor register. The host then copies the contents of the staging and extended staging registers to the E^2PROM.

Host mode	Data (MSB)	Description
TX	reset	Host sends reset pulse
RX	presence	The sensor responds by the presence of impulses
TX	CCh	Host sends Skip ROM command
TX	4Eh	Host sends Write Scratchpad command
TX	7 bytes	Host sends 7 data bytes to the staging area (including Tha_Set_lsb, Tla_Set_lsb, Tha_Set_msb and Tla_Set_msb-)
TX	reset	Host sends reset pulse
TX	presence	The sensor responds by the presence of impulses
TX	CCh	Host sends Skip ROM command
TX	48h	Host sends Copy Page0 command
TX	DQ stays high	Host keeps DQ high for at least 40ms during copy operation

12.9 1-wire Bus Timing Characterization

Parameters	Symbol	Conditions	MIN	TYP	MAX	Unit
slot length	t_{SLOT}	See Notes	60		120	μs
recovery time	t_{REC}	See Notes	1	5		μs
Write 0 low level time	t_{LOW0}	See Notes	60	60	120	μs
Write 1 low level time	t_{LOW1}	See Notes	1	5	15	μs
Read Data Valid Time	t_{RDV}	See Notes		5	15	μs
Reset Low level Time	t_{RSTL}	See Notes	480	960		μs
Presence detection high level time	t_{PDHIGH}	See Notes	15	30	60	μs
Presence detection low level time	t_{PDLOW}	See Notes	60	115	240	μs

Note: See Figure 12.9 below for more information on time slots.

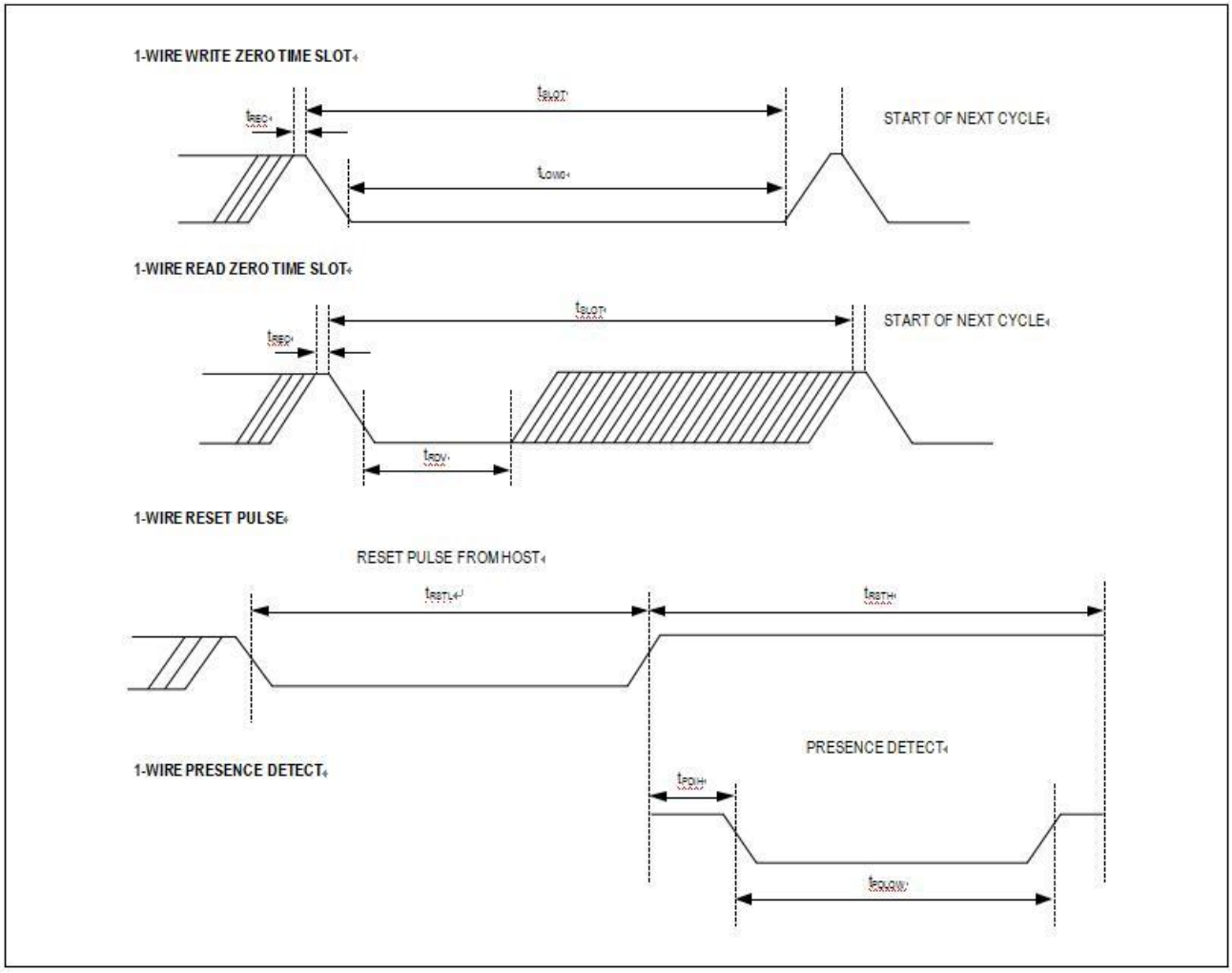
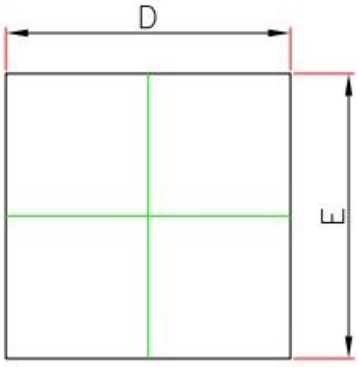
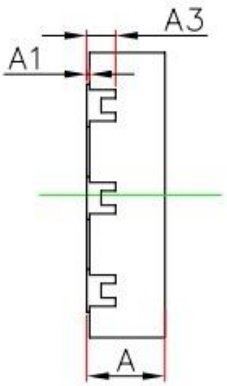


Figure 12.9 Time slot diagram

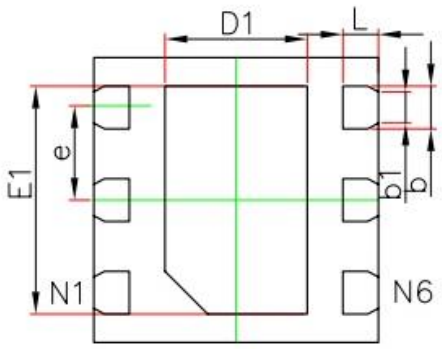
13. Packaging Diagram



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008 REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E1	1.500	1.700	0.059	0.067
b	0.250	0.350	0.010	0.014
b1	0.220 REF.		0.009 REF.	
e	0.650 BSC.		0.026 BSC.	
L	0.174	0.326	0.007	0.013

Figure 13 Package Drawing of DFN4L (1.6X1.2X0.55mm)