24MHz 32-bit General Automotive MCU

Features

- AECQ-100 Grade 2: -40~105℃
- 24MHz 32-bit MCU
- 4kB LDROM, 60kB Flash, 16kB SRAM
- 100k SPS 14-bit SAR ADC
  10 chanels differential input
- CRC32 and High-speed divider
- 2 x 32-bit timer,
- 2 watch-dog
- 1MHz I^2C
- UART
- 16 GPIOs
- Power-on reset, Low voltage detection
- Low voltage reset and temperature detection
- Support In-System Programming (ISP) & In-Circuit Programming (ICP)
- Low power mode
- QFN 5.0mmX5.0mmX0.75mm-40L package

General Description

AW32F001QNR -Q1 is a 24MHz 32-bit general automotive MCU. It has embedded 60k byte program flash (APROM), 4k byte boot program space LDROM, 16k byte SRAM. It integrated timers, watchdogs, 1 AFE module, 1 I^2C module, 1 UART module and 1 GPIO module.

AW32F001QNR-Q1 support ISP (In-System Programming) and ICP (In-Circuit Programming). System startup interval is configurable, and it can be configured to boot from ROM, LDROM or SRAM.

Applications

Automotive

Typical Application Circuit

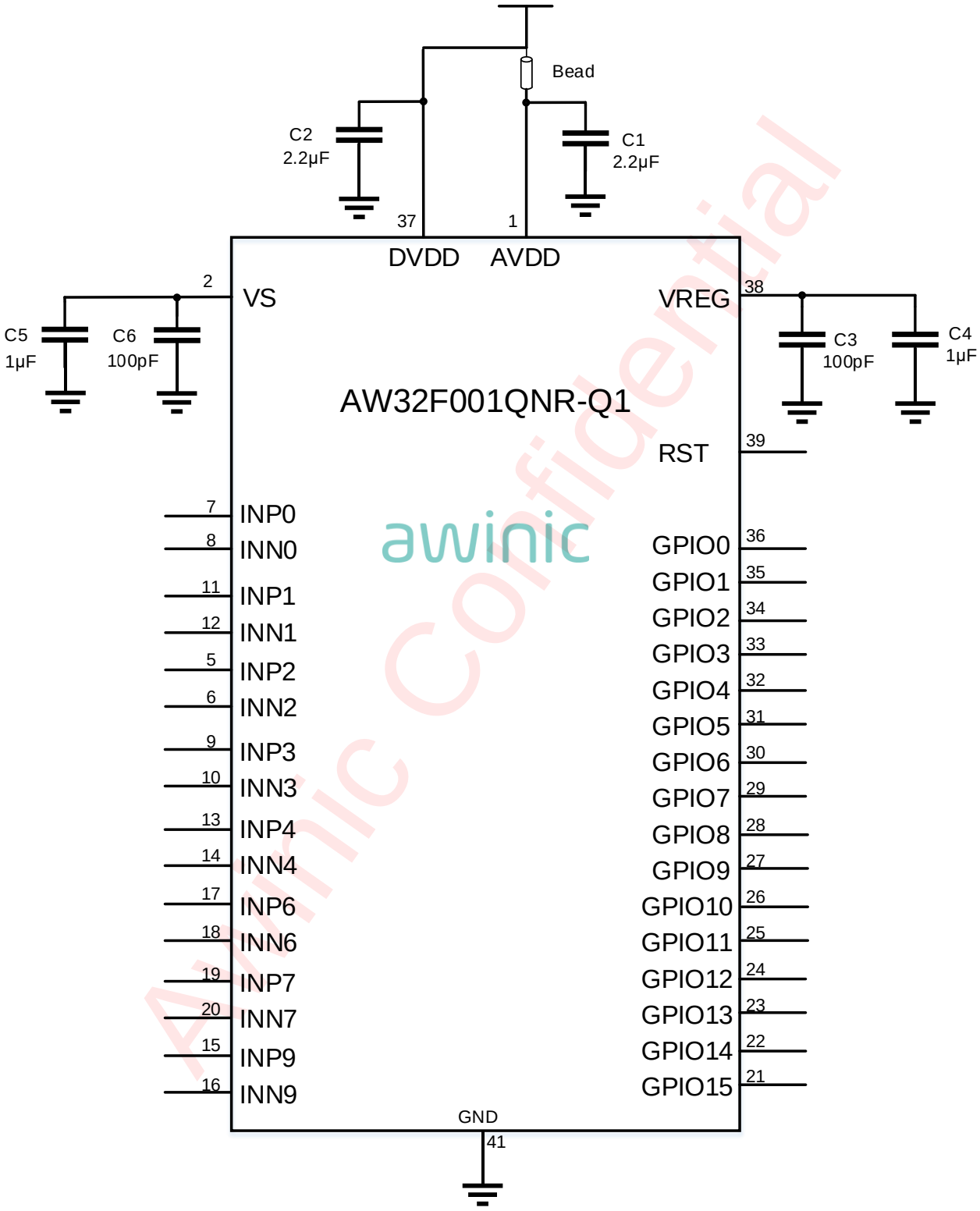
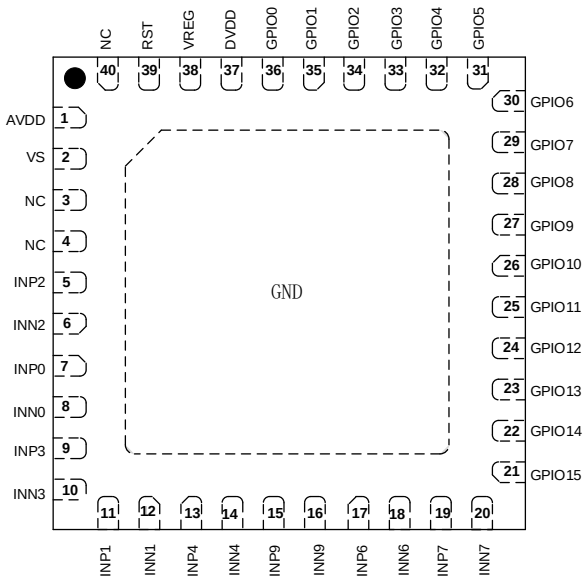


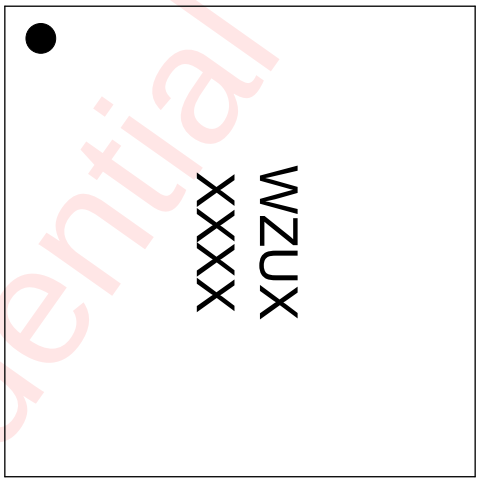
Figure 1 AW32F001QNR-Q1 Typical Application Circuit

Pin Configuration And Top Mark

AW32F001QNR-Q1
(Top View)



AW32F001QNR-Q1 Marking
(Top View)



WZUX - AW32F001QNR-Q1
XXXX - Production Tracing Code

Figure 2 AW32F001QNR-Q1 Pin Configuration and Top Mark

Pin Definition

No	NAME	DESCRIPTION
1	AVDD	Analog power
2	VS	VS Regulated output, needs to be connected to 1μF capacitor
3	NC	Not Connected
4	NC	Not Connected
5	INP2	AFE2 Positive Input
6	INN2	AFE2 Negative Input
7	INP0	AFE0 Positive Input
8	INN0	AFE0 Negative Input
9	INP3	AFE3 Positive Input
10	INN3	AFE3 Negative Input
11	INP1	AFE1 Positive Input
12	INN1	AFE1 Negative Input
13	INP4	AFE4 Positive Input
14	INN4	AFE4 Negative Input
15	INP9	AFE9 Positive Input
16	INN9	AFE9 Negative Input
17	INP6	AFE6 Positive Input
18	INN6	AFE6 Negative Input
19	INP7	AFE7 Positive Input
20	INN7	AFE7 Negative Input
21	GPIO15	GPIO15, push-pull output / SW DEBUG DATA
22	GPIO14	GPIO14, push-pull output / SW DEBUG CLK
23	GPIO13	GPIO13, open-drain output / I^2C DATA/ UART0 RXD
24	GPIO12	GPIO12, open-drain output / I^2C CLK/ UART0 TXD
25	GPIO11	GPIO11, open-drain output / UART0 TXD / AFE11 Positive Input
26	GPIO10	GPIO10, open-drain output / UART0 RXD / AFE11 Negative Input
27	GPIO9	GPIO9, open-drain output
28	GPIO8	GPIO8, open-drain output / AFE10 Positive Input
29	GPIO7	GPIO7, open-drain output / AFE10 Negative Input
30	GPIO6	GPIO6, open-drain output / External clock input pin

31	GPIO5	GPIO5, open-drain output
32	GPIO4	GPIO4, open-drain output
33	GPIO3	GPIO3, push-pull output / VS3 output
34	GPIO2	GPIO2, push-pull output / VS2 output
35	GPIO1	GPIO1, push-pull output / VS1 output
36	GPIO0	GPIO0, push-pull output / VS0 output
37	DVDD	Digital power
38	VREG	LDO output pin, needs to be connected to 1μF capacitor
39	RST	Reset input, active high
40	NC	Not Connected
41	GND	Ground

Functional Block Diagram

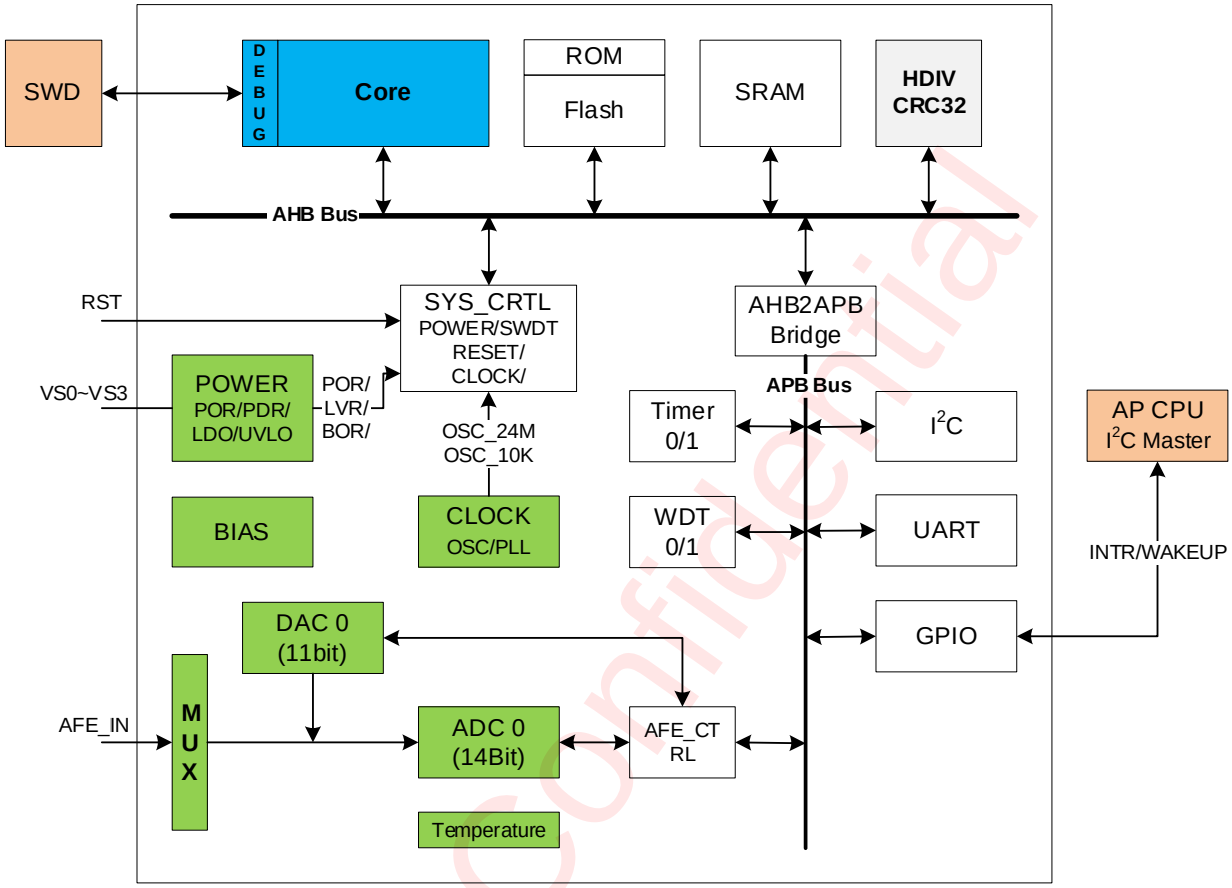


Figure 3 AW32F001QNR-Q1 Function Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW32F001QNR-Q1	-40℃~105℃	WBQFN 5.0mmX5.0mmX 0.75mm-40L	WZUX	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

Parameter	Range
Supply Voltage AVDD	-0.3V to 6.0V
Supply Voltage DVDD	-0.3V to 6.0V
INP, INN, GPIO	-0.3V to VDD+0.3V
Digital power supply VREG	-0.3V to 1.65V
Package Thermal Resistance θ_{JA}	60°C/W
Ambient Temperature Range	-40°C to 105°C
Maximum Junction Temperature T_{JMAX}	150°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature(Soldering 10 Seconds)	260°C
ESD Rating (NOTE 2 3)	
HBM(Human Body Model)	±2000V
CDM(Charge Device Model)	±1500V
Latch-up	
Test Condition: AEC_Q100-004-Rev-C	+IT: 200mA -IT: -200mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE 2：The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: AEC-Q100-002-RevE.

NOTE 3：Charge Device Model test method: AEC-Q100-011-RevD.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD	Analog supply voltage	2.5	3.3	5.5	V
DVDD	Analog supply voltage	2	3.3	5.5	V
C_{AVDD}	Input capacitance		2.2		μF
C_{DVDD}	Input capacitance		2.2		μF
C_{VS1}	VS Decoupling capacitor	1			μF
C_{REG1}	VREG Decoupling capacitor	1			μF
T_A	Operating free-air temperature range	-40	25	105	°C

Electrical Characteristics

AVDD=3.3V, DVDD=3.3V, RST=0, TA=25°C for typical values (unless otherwise noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
AVDD	Analog supply voltage		2.5		5.5	V
DVDD	Digital supply voltage		2		5.5	V
V_{IH}	Logic input high level		1.35			V
V_{IL}	Logic input low level				0.39	V
V_{OL}	Logic output low level	I_{OUT}=0.8mA			0.4	V
V_{OH}	Logic output high level	I_{OUT}=0.8mA	AVDD-0.4			V
I_{SD}(1)	Shutdown current	RST =3.3V		0.03	2	μA
I_{LP1}	Power down mode supply current	POR+LOSC Turn on		3		μA
I_{LP2}	Deep sleep mode supply current	POR+LOSC+LDO Turn on		7		μA
I_{LP3}	Sleep mode supply current	CPU Power consumption in sleep mode		1.2		mA
I_Q	Quiescent current			4.5		mA
T_{SD}	Over temperature protection threshold			160		℃
T_{SDR}	Over temperature protection recovery threshold			130		℃
24MHz HOSC						
F_{HOSC}	HOSC working frequency			24		MHz
R_{HOSC}	HOSC Accuracy		-2		2	%
35kHz LOSC						
F_{LOSC}	LOSC working frequency			35		kHz
R_{LOSC}(3)	LOSC Accuracy		-15		15	%
14bit SAR ADC						
V_{ADIN}(3)	Input voltage		0		AVDD	V
V_{REF}	ADC Reference voltage			AVDD		V
F_{ADC}	Conversion rate			100		ksps
DAC						
R_{DAC}	Resolution			12		bit
M_{DAC}	Monotonic			11		bit
V_{EOSI}(3)	Equivalent offset calibration range		- 540		+540	mV
LDO						
V_{REG}	LDO output voltage		1.35	1.5	1.65	V

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
C_{REG}	LDO Decoupling capacitor		1			μF
VS						
V_S(3)	VS output voltage		2.4		3.1	V
C_{VS}	VS Decoupling capacitor		1			μF
I_{VSH}(2)	High supply surrent of VS turns on			100		mA
UVLO						
V_{UV}	Undervoltage detection voltage			2.3		V
V_{UVH}	Under-voltage protection hysteresis voltage			100		mV
POR						
V_{POR}	Power-on reset voltage			1.6		V
TS						
T_R	Temperature detection range		-40		85	℃
R_{TS}(3)	Temperature detection accuracy		-3		3	℃

(1) Does not include reset leakage

(2) High supply current pulse of VS turns on less than 60μs

(3) Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

I²C Interface TIMING

Parameter			Super-fast mode			UNIT
No.	Symbol	Name	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency		400	1000	kHz
2	t_{LOW}	SCL Low level Duration	0.5			μs
3	t_{HIGH}	SCL High level Duration	0.3			μs
4	t_{RISE}	SCL, SDA rise time			0.1	μs
5	t_{FALL}	SCL, SDA fall time			0.1	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.3			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.3			μs
8	$t_{SU:STO}$	Stop condition setup time	0.3			μs
9	t_{BUF}	the Bus idle time START state to STOP state	0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

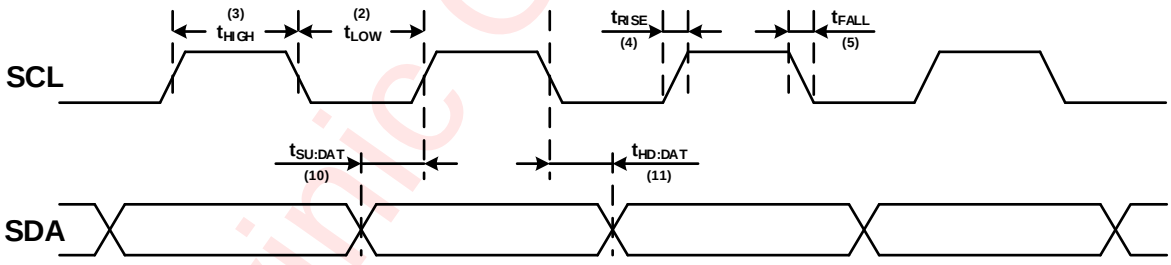


Figure 4 SCL and SDA timing relationships in the data transmission process

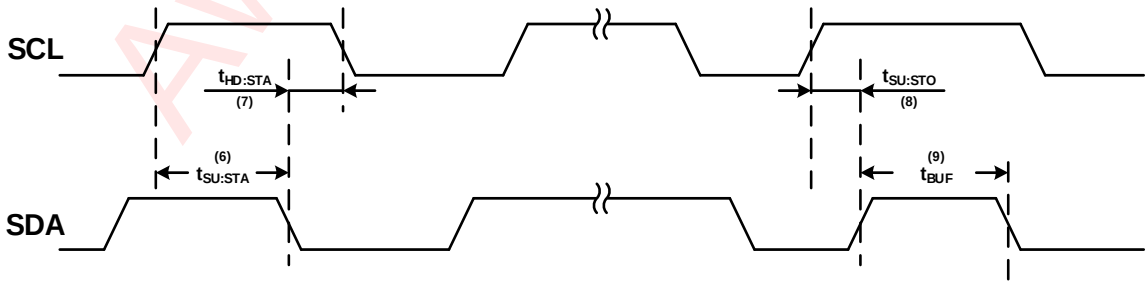


Figure 5 The timing relationship between START and STOP state

I²C Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 32-bit and register data is 32-bit. Note that I²C also support 8-bit data transfer. Writing

process of I²C is showed as below picture.

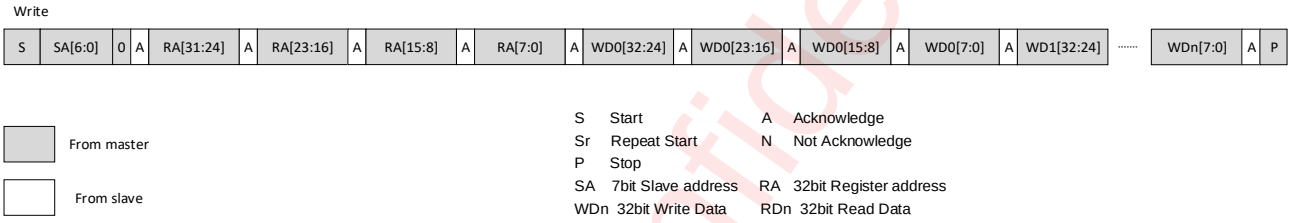


Figure 6 I²C Write Byte Cycle

I²C Read Cycle

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is showed as below picture

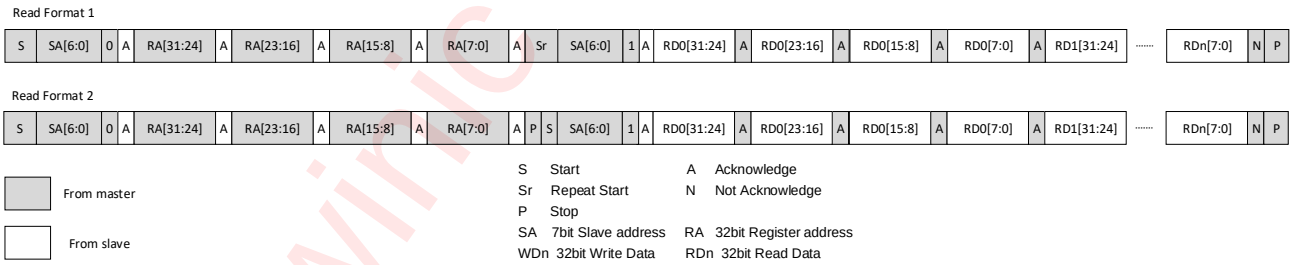


Figure 7 I²C Read Byte Cycle

Detailed Functional Description

Low-power Modes

Hardware low-power power management and low-power policy control are integrated in AW32F001QNR-Q1. This chip can be woken up by the 5V SWDT interrupt in low-power mode. This chip can also be woken up by I²C interrupt, GPIO interrupt, UART interrupt, timing interrupt and watchdog interrupt in DEEP SLEEP mode.

Power on and Power down Sequence

The power on and power down sequence of this device is illustrated in the following figure:

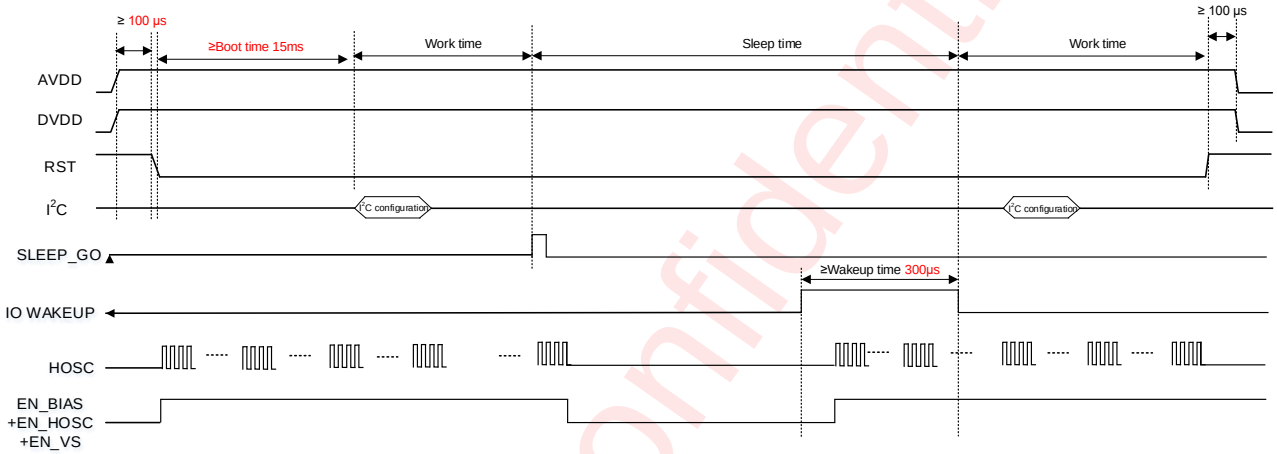


Figure 8 Power On and Power Down Sequence

24MHz 32-bit MCU

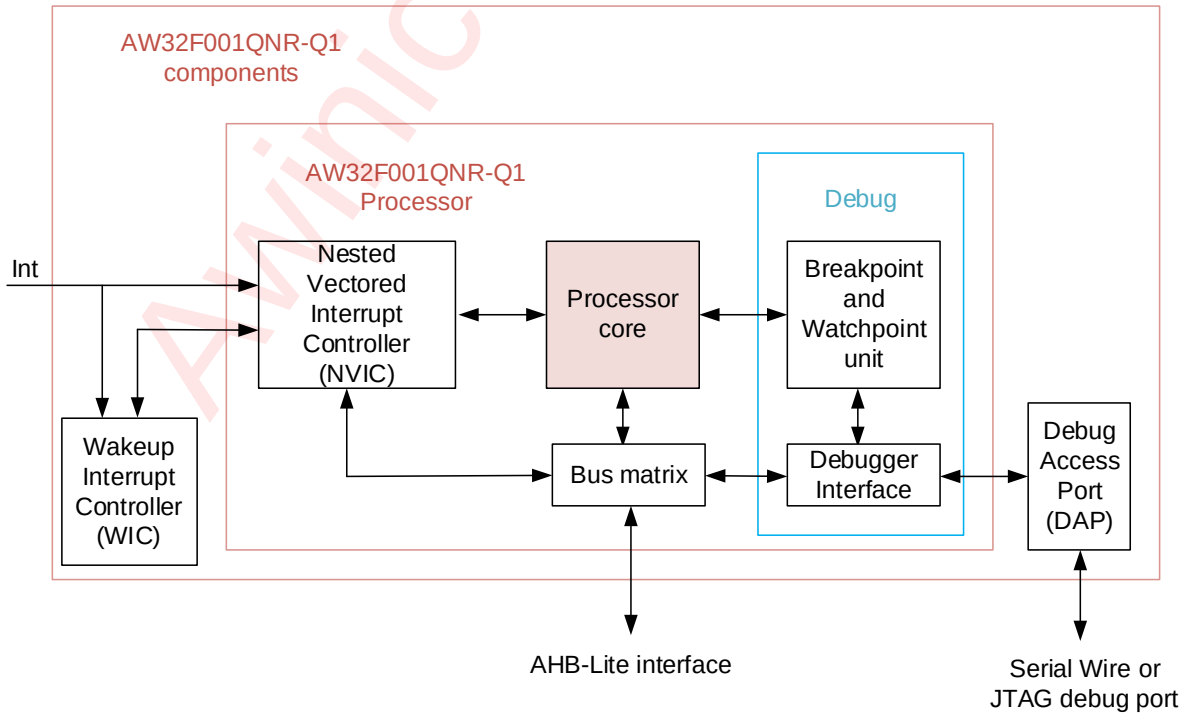


Figure 1 AW32F001QNR-Q1 core

The processor of AW32F001QNR-Q1 is a 32-bit multi-level configurable RISC processor.It has AMBA-AHB-Lite interface and Nested Vectored Interrupt Controller(NVIC),with optional hardware debugging function,can execute.This processor supports two operation modes Thread mode Handler mode.When an exception occurs,the processor enters Handler mode.Exception return can only occur in Handler mode.When reset,the processor will enter Thread mode, the processor can also enter Thread mode when an abnormal return.

Flash

AW32F001QNR-Q1 integrates 60kbytes Flash Memory and Flash controller based on AHB bus, supports multiple erasing, can realize Flash whole piece, block erasing, single word, multi-word programming, the maximum support for single programming 64 bytes. Flash content can be read directly through the AHB bus.

The AW32F001QNR-Q1 integrates 60kbytes Flash Memory and Flash controller based on AHB bus. The Flash can be erased multiple times, and it can be erased whole, block. The Flash supports single word, multi-word programming, the maximum support for single programming 64 bytes. The Flash can be read directly through the AHB bus.

AW32F001QNR-Q1 Core Features

The system supports little-endian data access and provides a single instruction 32-bit hardware multiplier.

NVIC provides 32 external interrupts with 4-level interrupt priority. There is a dedicated non-maskable interrupt NMI. The system supports level and pulse interrupt trigger. Interrupt wakeup register WIC, support ultra-low power sleep mode.

Debug: there are 4 hardware breakpoints, 2 observation points, program count sampling register for non-invasive code analysis, single-step vector capture capability.

Bus interface: The system provides a single 32-bit AMBA-3, AHB-lite system interface that integrates all system peripherals and memory and Single 32-bit slave port supporting DAP (Debug Access Port).

- Low gate count processor with the following features
  - Thumb-2 technology
  - 24-bit systick timer
  - 32-bit hardware divider
  - Supports little-endian data access
  - Deterministic, fixed delay interrupt handling capability
  - Abnormal mode (C-ABI) compatible with C application binary interface, allowing users to implement interrupt handling with pure C language functions
  - Use wait for interrupt (WFI), wait for event instruction (WFE), or directly enter low-power sleep mode when returning from interrupt
- NVIC characteristics
  - 32 external interrupt inputs, each with 4 priority levels
  - Non-maskable interrupt input
  - Supporting level and pulse trigger interrupt
  - Interrupt wake controller (WIC), supporting ultra-low power sleep mode
- Bus interface
  - Single 32-bit AMBA-3, AHB-Lite system interface provides convenient integration for all system peripherals and memory
  - Single 32-bit slave port supporting DAP (Debug Access Port)
- Debug

- 4 hardware breakpoints
- 2 observation points
- Program count sampling register for non-intrusive code (PCSR)
- Single step and vector capture capabilities

System Memory Map

The chip provides 4G byte addressing space, only supports little-endian data format, unified addressing of ROM, SRAM and controller registers.

Flash memory space		
0x0100_1000 – 0x0100_FFFF	FLASH_BA	FLASH Memory space (60kB)
LDROM memory space		
0x0100_0000– 0x0100_0FFF	LDROM_BA	LDROM Memory space (4kB)
ROM memory space		
0x1000_0000– 0x1000_0FFF	ROM_BA	ROM Memory space (4kB)
SRAM memory space		
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory space (16kB)
AHB controller memory space (0x5000_0000 – 0x502F_FFFF)		
0x5000_0000 – 0x5000_1FFF	GCR_BA	System Management Control Register
0x5000_2000 – 0x5000_23FF	PWR_BA	Power Management Unit Register (Contains SWDT function register)
0x5000_2400 – 0x5000_27FF	RST_BA	Reset management unit register
0x5000_2800 – 0x5000_2BFF	CLK_BA	Clock management unit register
0x5000_C000 – 0x5000_DFFF	FMC_BA	Flash Memory control register
0x5000_E000 – 0x5000_FFFF	RMC_BA	SRAM Memory control register
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware divider control register
0x5002_4000 – 0x5002_7FFF	CRC_BA	CRC control register
APB controller memory space (0x4000_0000 – 0x401F_FFFF)		
0x4000_0000 – 0x4000_0FFF	WDT0_BA	Watchdog0 control register
0x4000_1000 – 0x4000_1FFF	WDT1_BA	Watchdog1 control register
0x4000_3000 – 0x4000_3FFF	UART0_BA	UART0 control register
0x4000_4000 – 0x4000_4FFF	TMR0_BA	Timer 0 control register
0x4000_5000 – 0x4000_5FFF	TMR1_BA	Timer 1 control register
0x4000_6000 – 0x4000_6FFF	I^2C_BA	I^2C Interface control register
0x4000_8000 – 0x4000_8FFF	AFE0_BA	AFE0 control register

0x4000_9000 – 0x4000_9FFF	GPIOA_BA	GPIOA control register
System control space (SCS) (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System timer control register (SysTick)
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers (External interrupt control register)
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System control register

System Interruption

AW32F001QNR-Q1 provides an interrupt controller for managing exceptions, NVIC, and is closely connected with the processor.

AW32F001QNR-Q1 provides an interrupt controller as a complete part of the exception model, named it nested vector interrupt controller.

NVIC supports 4-level discrete interrupt priority. When any interrupt request is received, the start address of the ISR register is taken from the interrupt vector table in memory. NVIC automatically saves the processing status to the stack and saves value of the registers "PC, PSR, LR" , RO ~ R3, R12 ".

At the end of the ISR, NVIC will restore the value of the relevant register from the stack, and then perform normal operations, so it takes a small amount of time to process the interrupt request.

The base address of the vector table is 0x00000000. The vector table includes the initial value of the stack after reset and the entry address of all exception handling situations and the order of the vector numbers for handling exceptions.

NVIC supports "Tail chaining" to handle interrupts. After an interrupt is processed, there is no need to resume the scene and the next one is processed immediately. This can reduce the interrupt waiting time and improve the efficiency of interrupt processing.

NVIC also supports "late arrival" to handle interrupts. If the current interrupt is saving the context and has not entered the interrupt processing function, a higher priority interrupt occurs, NVIC will handle the higher priority interrupt, and do not need to save again Context, which can improve real-time.

number and priority of interrupt vector

Exception Name	number	priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Set aside	4~10	Set aside
SVCall	11	Configurable
Set aside	12~13	Set aside
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16~47	Configurable

Exception number	IRQ number	Exception name	Source of anomaly	Interrupt description	Wake up deep sleep mode
1~15			System abnormality		
16	0	UVLO	UVLO	Undervoltage interrupt	No
17	1	TMR0_INT	TMR0	Timer 0 interrupt	Yes
18	2	TMR1_INT	TMR1	Timer 1 interrupt	Yes
19	3	UART0_INT	UART0	UART0 interrupt	Yes
20	4	I^2C_INT	I^2C	I^2C interrupt	Yes
21	5	AFE0_INT	AFE0	AFE0 interrupt	No
22	6	AFE0_CMP0_INT	AFE0_CMP0	AFE0 interrupt	No
23	7	AFE0_CMP1_INT	AFE0_CMP1	AFE0 interrupt	No
24	8	GPIOA_INT	GPIOA	GPIOA interrupt	Yes
25	9	RMC_INT	RMC	RAM Parity failed interrupt	No
26	10	FMC_INT	FMC		No
27	11	WDT0_INT	WDT0	Watchdog 0	Yes
28	12	SWDT_INT	SWDT	Smart watchdog	Yes
29	13	WDT1_INT	WDT1	Watchdog 1	Yes

Clock

The functions of the clock management unit module (CMU) mainly include: detecting whether the clock is OK according to the clock enable; after the alternative clock is OK, one of the external pin clock, the internal low-speed clock, and the internal high-speed clock is selected as the internal system clock according to the selector.

The CMU will also enable the clock gate control of the system clock, cpu clock and peripheral clock according to the low power consumption mode

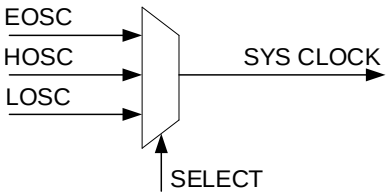


Figure 2 Clock

Reset

Select chip reset, digital system reset (MCU reset), CPU reset, peripheral module reset according to hard reset and register configuration

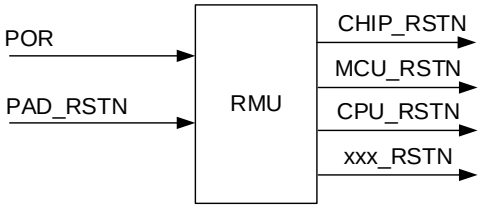


Figure 3 Reset

Analog Front End (AFE)

The AFE module includes one 12-bit DAC and one 14-bit ADC

- 14-bit SAR ADC,13-bit accuracy guarantee
- 12 external AFE inputs, 4 internal inputs (VS, VS/2, TEMP, GND)
- 16 channels
- 100kHz SPS
- Support the conversion result of 2's complement format / unsigned format / original format
- Provide multiple working modes
  1. Single conversion mode : Complete a conversion on the designated channel
  2. Single cycle scan mode : Complete a conversion on all designated channels
  3. Finite cycle scan mode1 : Each channel switches to the next channel after a specified number of conversions
  4. Finite cycle scan mode2 : Each channel converts once and then enters the next channel in turn, converting a specified number of times in total
  5. Infinite scan mode : Continuously execute single-cycle scan mode until software stops A/D conversion
  6. Burst Mode : Continue on a single designated channel and store the results in FIFO in sequence
- The conversion result can be compared with the specified value, the user can set whether to generate an interrupt when matching
- Built-in 12-bit DAC for offset voltage calibration

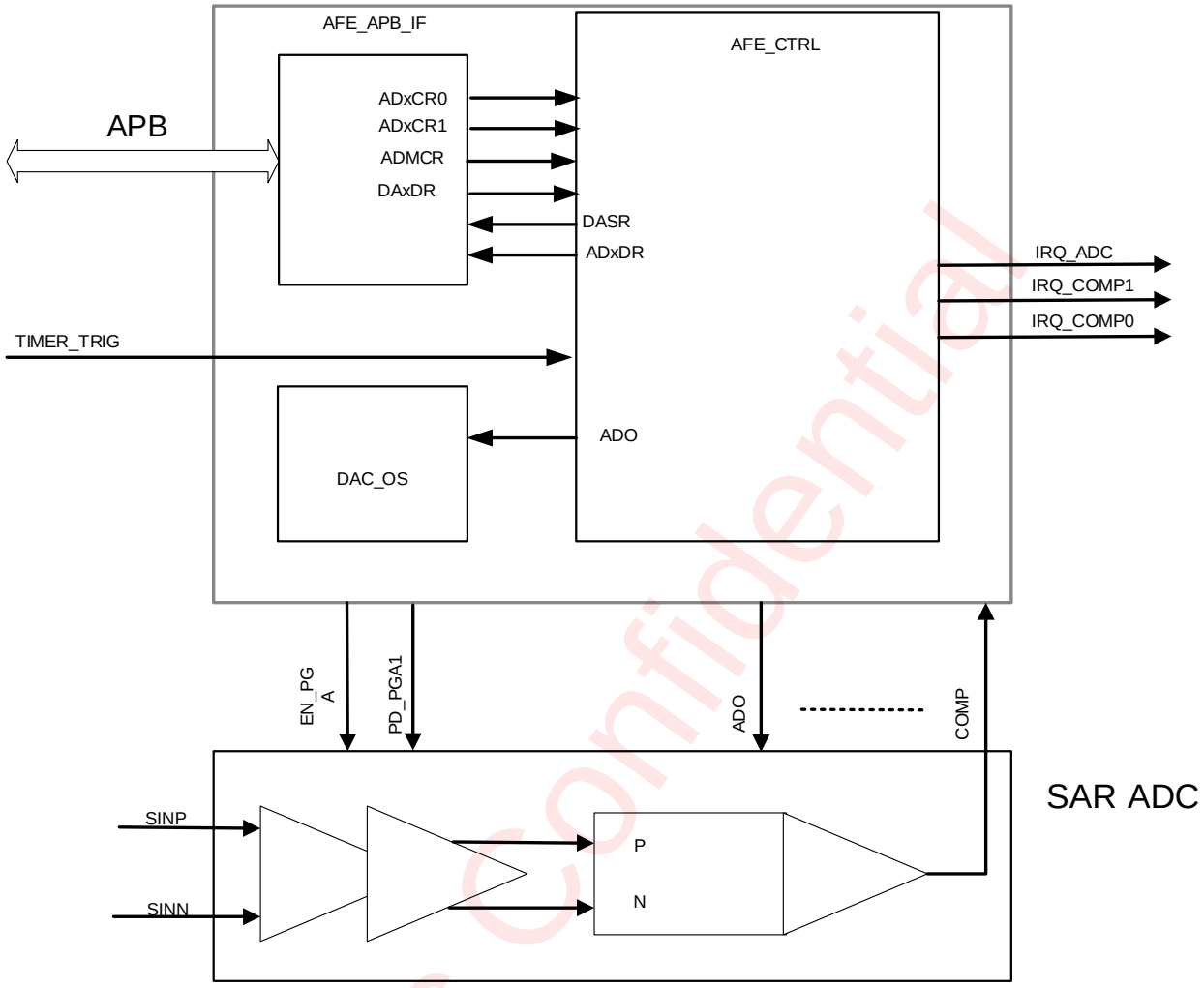


Figure 4 AFE

General-Purpose Inputs/Outputs (GPIOs)

AW32F001QNR-Q1 has a maximum of 16 GPIO pins, each GPIO pin can be configured independently by the software as input, output. GPIO0~3 and GPIO14~15 pins can be configured as push-pull or open-drain output, GPIO4~13 pins can be only open-drain output. GPIO can be configured to multiplex analog channel input, I²C interface, UART interface, SWD debug interface, VS switch output. When doing general IO, software programmable output data content, software programmable identify input data and programmable receive data to generate interrupts.

I²C Bus

The AW32F001QNR-Q1 includes a 1.8V I²C interface that can operate in multimaster or slave mode. The I²C communication process is implemented by hardware and interacts with the CPU through FIFO and interrupts. Each I²C module has an 8-byte sending FIFO and an 8-byte receiving FIFO built in.

I²C interface supports Standard mode, Fast mode (Fm), and Fm+. Up to 800kHz rate communication is supported.

Universal Asynchronous Receiver/Transmitter (UART)

AW32F001QNR-Q1 integrates hardware UART, supports normal speed UART, and supports automatic process control. The UART interface controller can convert the data received by the peripheral according to the UART transmission protocol, and convert the data sent from the CPU.

Timers

The AW32F001QNR-Q1 has two 32-bit timers, each with an independent clock source, and can choose internal 32kHz, 24MHz, and HCLK as the clock source. The current value of the timer can be read by the timer data register (TDR). The timer has 3 working modes: single pulse mode, cycle mode, continuous counting mode.

Smart Watchdogs

A Smart watchdog timer (Smart WDT) and two 32-bit watchdog timers with internal clock are integrated in the AW32F001QNR-Q1. The WDT supports waking up the CPU in sleep mode or deep sleep mode or power down mode. It can be chose to reset or shut down the CPU when a timeout occurs.

Cyclic Redundancy Check (CRC) Calculation Unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

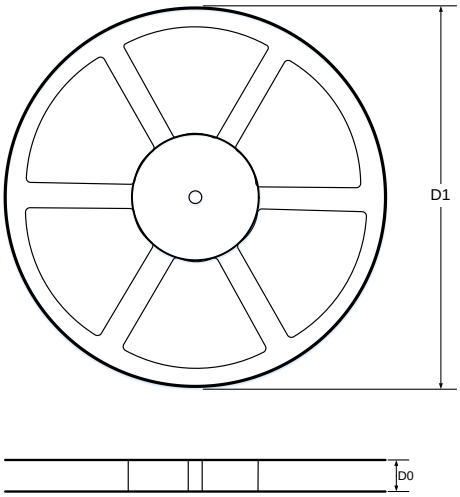
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps to compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

Serial Wire Debug Port (SW-DP)

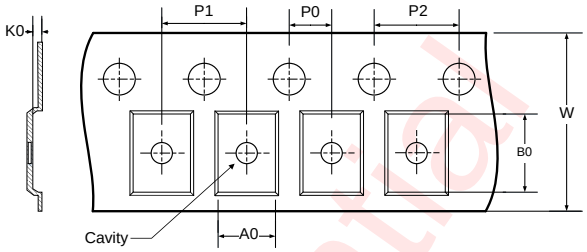
An SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Tape And Reel Information

REEL DIMENSIONS

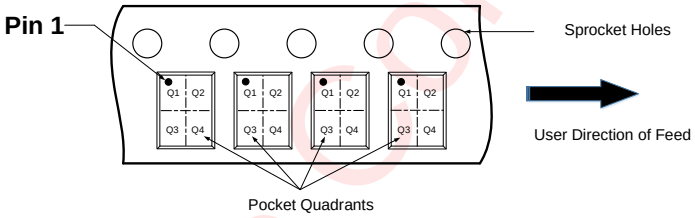


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



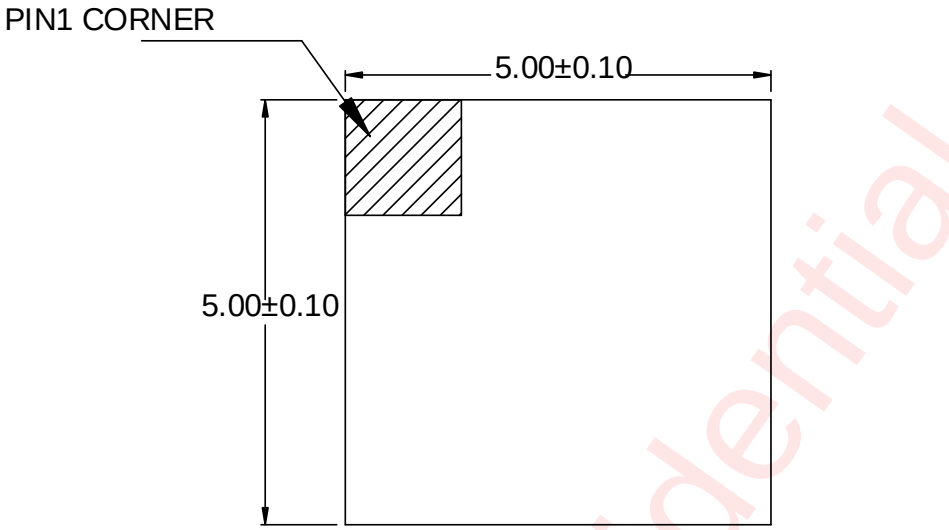
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

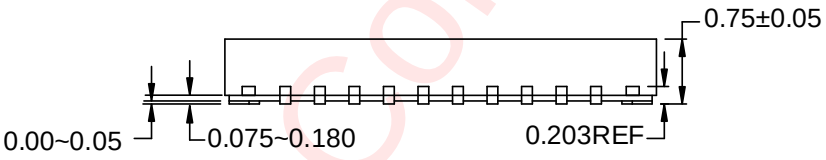
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.25	5.25	1.1	2	8	4	12	Q1

All dimensions are nominal

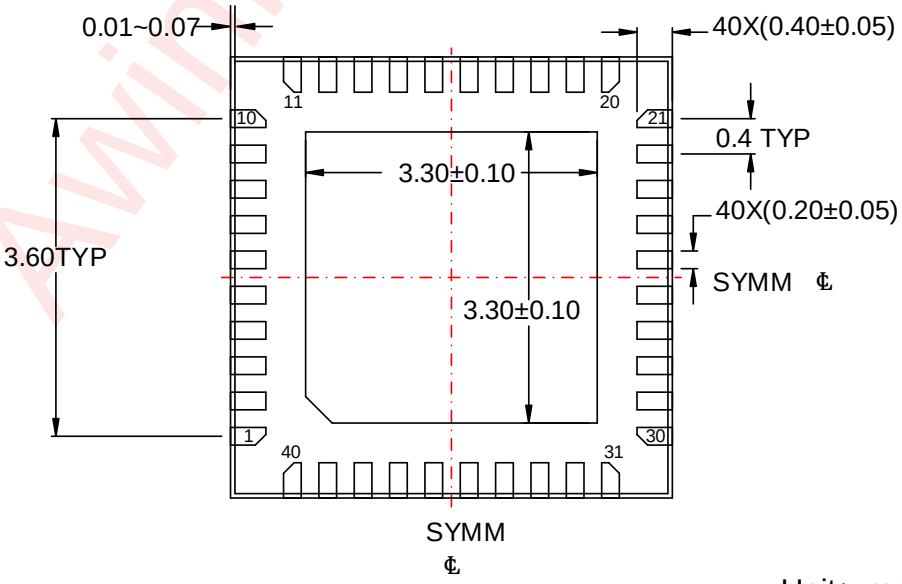
Package Description



TOP VIEW



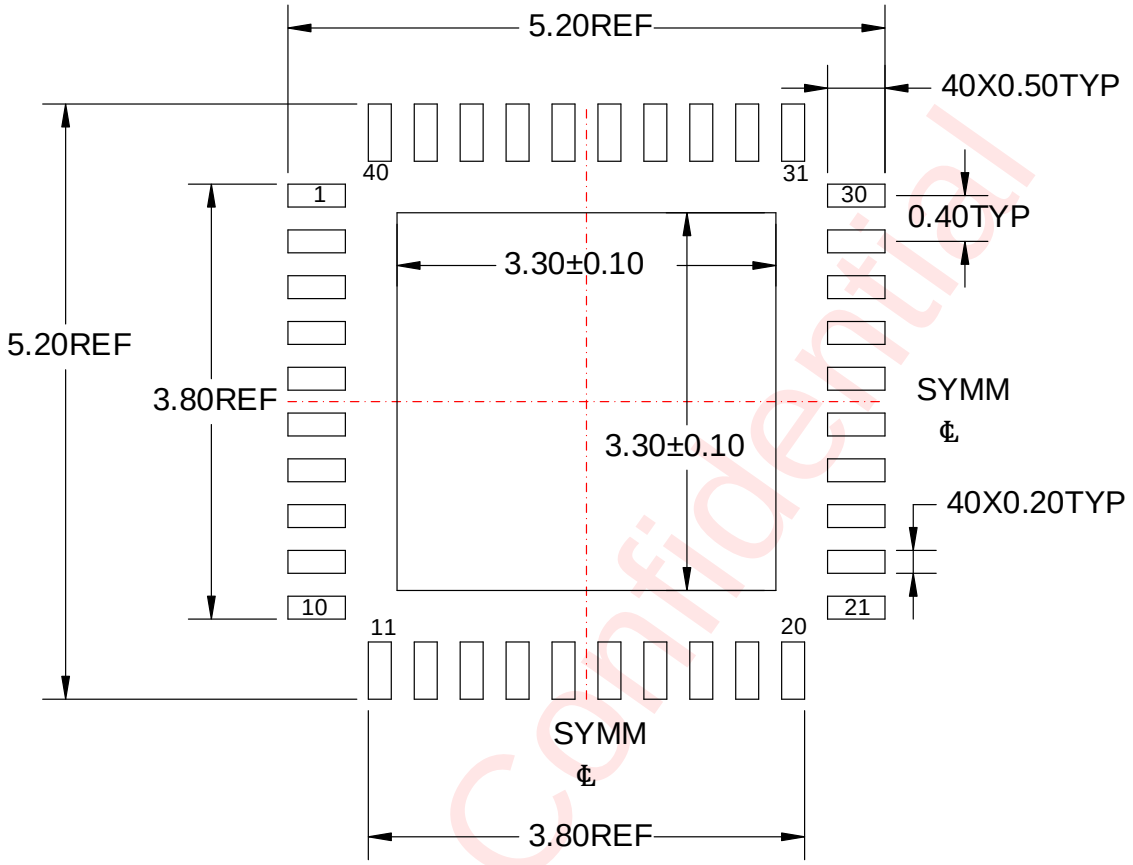
SIDE VIEW

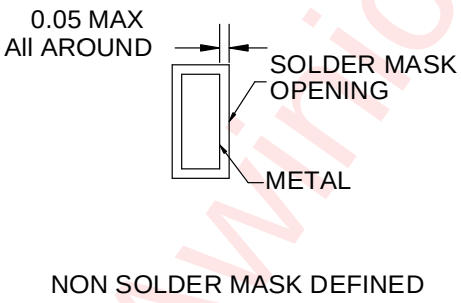


Unit：mm

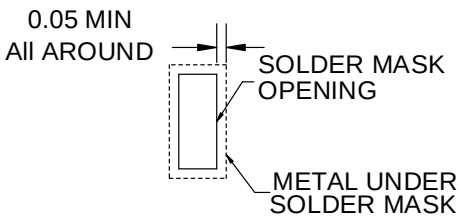
BOTTOM VIEW

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2021	Officially released.
V1.1	Nov. 2024	Update description of GENERAL DESCRIPTION. (P1)
V1.2	Jul. 2025	Update Electrical Characteristics(P9)

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