钍地半导体
Tudi Semiconductor

# Product Specification

## TUDI-ULQ2004A

高电压大电流达林顿晶体管阵列

网址 www.sztdbdt.com

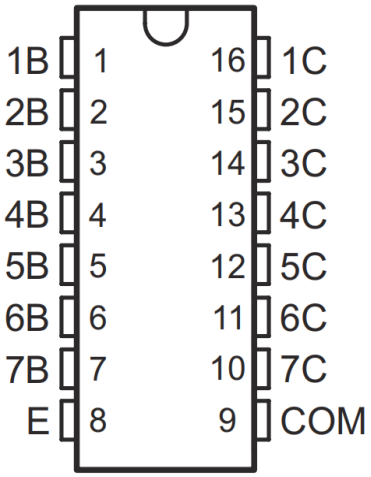
**用芯智造·卓越品质**

**semiconductor device manufacturer**

- Design
- research and development
- production
- and sales

## 特性

- ●符合汽车应用要求
- ●ESD 保护超过 200V（使用机器放电模型，C = 200pF，R = 0）
- ●500mA 额定集电极电流（单路输出）
- ●高电压输出：50V
- ●输出钳位二极管
- ●可兼容各类逻辑的输入
- ●继电器驱动器应用




16-Pin SOIC

## 应用

- ●继电器驱动器
- ●步进电机驱动器和有刷直流电机驱动器
- ●灯驱动器
- ●显示屏驱动器（LED 和气体放电元件）
- ●线路驱动器
- ●逻辑缓冲器

## 说明

ULQ200xA-Q1 器件为高电压大电流达林顿晶体管阵 列，均由 7 个 NPN 达林顿对组成，这些达林顿对具有 高压输出，带有用于开关感性负载的共阴极钳位二极 管。单个达林顿对的集电极电流额定值为 500mA。将达林顿对并联可以实现更大的电流。

ULQ2003A-Q1 的每个达林顿对都具有一个 2.7kΩ 的 串联基极电阻，可直接与 TTL 或 5V CMOS 器件一起 运行。ULQ2004A-Q1 具有一个 10.5kΩ 串联基极电 阻，可直接从使用 6V 至 15V 电源电压的 CMOS 器件 上运行 。 ULQ2004A-Q1 所需的输入电流低于 ULQ2003A-Q1 的输入电流。

表 **4-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1B | I | Channel 1 through 7 Darlington base input. |
| 2 | 2B | | |
| 3 | 3B | | |
| 4 | 4B | | |
| 5 | 5B | | |
| 6 | 6B | | |
| 7 | 7B | | |
| 8 | E | — | Common emitter shared by all channels (typically tied to ground). |
| 9 | COM | — | Common cathode node for flyback diodes (required for inductive loads). |

表 **4-1. Pin Functions**（续）

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 10 | 7C | O | Channel 1 through 7 Darlington collector output. |
| 11 | 6C | | |
| 12 | 5C | | |
| 13 | 4C | | |
| 14 | 3C | | |
| 15 | 2C | | |
| 16 | 1C | | |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CE}$ | Collector-emitter voltage | | | 50 | V |
| | Clamp diode reverse voltage(2) | | | 50 | V |
| $V_I$ | Input voltage(2) | | | 30 | V |
| | Peak collector current | See 图 8-2 | | 500 | mA |
| $I_{OK}$ | Output clamp current | | | 500 | mA |
| | Total emitter-terminal current | | | -2.5 | A |
| $P_D$ | Continuous total power dissipation | | See 节 5.8 | | |
| $T_A$ | Operating free-air temperature | ULQ200xAT | -40 | 105 | °C |
| | | ULQ200xAQ | -40 | 125 | |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±500 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CE}$ | Collector-emitter voltage | 0 | 50 | V |
| $T_J$ | Junction temperature | -40 | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | ULQ2003A-Q1, ULQ2004A-Q1 | ULQ2003A-Q1 | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | DYY (SOT) | |
| | | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 87.9 | 112.9 | 119.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 49.4 | 49.2 | 56.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.1 | 58.1 | 52.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 11.9 | 9.1 | 2.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 48.6 | 57.6 | 51.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Electrical Characteristics, ULQ2003AT and ULQ2003AQ

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{I(on)}$ | On-state input voltage | $V_{CE}$ = 2 V, see 图 6-8 | $I_C$ = 200 mA | | | | 2.7 | V |
| | | | $I_C$ = 250 mA | | | | 2.9 | |
| | | | $I_C$ = 300 mA | | | | 3 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $I_I$ = 250 μA, $I_C$ = 100 mA, see 图 6-7 | | ULQ2003AT | | 0.9 | 1.2 | V |
| | | | | ULQ2003AQ | | 1 | 1.3 | |
| | | $I_I$ = 350 μA, $I_C$ = 200 mA, see 图 6-7 | | ULQ2003AT | | 1 | 1.4 | |
| | | | | ULQ2003AQ | | 1 | 1.5 | |
| | | $I_I$ = 500 μA, $I_C$ = 350 mA, see 图 6-7 | | ULQ2003AT | | 1.2 | 1.7 | |
| | | | | ULQ2003AQ | | 1.2 | 1.8 | |
| $I_{CEX}$ | Collector cutoff current | $V_{CE}$ = 50 V, $I_I$ = 0, see 图 6-1 | $T_A$ = 25°C | | | | 100 | μA |
| | | | $T_A$ = 105°C, ULQ2003AT | | | | 165 | |
| $V_F$ | Clamp forward voltage | $I_F$ = 350 mA, see 图 6-6 | | | | 1.7 | 2.2 | V |
| $I_{I(off)}$ | Off-state input current | $V_{CE}$ = 50 V, $I_C$ = 500 μA, see 图 6-3 | | | 30 | 65 | | μA |
| $I_I$ | Input current | $V_I$ = 3.85 V, see 图 6-4 | | | | 0.93 | 1.35 | mA |
| $I_R$ | Clamp reverse current | $V_R$ = 50 V, $T_A$ = 25°C, see 图 6-5 | | | | | 100 | μA |
| $C_i$ | Input capacitance | $V_I$ = 0, f = 1 MHz | | | | 15 | 25 | pF |

## 5.6 Electrical Characteristics, ULQ2004AT

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{I(on)}$ | On-state input voltage | $V_{CE}$ = 2 V, see 图 6-8 | $I_C$ = 125 mA | | | 5 | V |
| | | | $I_C$ = 200 mA | | | 6 | |
| | | | $I_C$ = 275 mA | | | 7 | |
| | | | $I_C$ = 350 mA | | | 8 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $I_I$ = 250 μA, $I_C$ = 100 mA, see 图 6-7 | | | 0.9 | 1.1 | V |
| | | $I_I$ = 350 μA, $I_C$ = 200 mA, see 图 6-7 | | | 1 | 1.3 | |
| | | $I_I$ = 500 μA, $I_C$ = 350 mA, see 图 6-7 | | | 1.2 | 1.6 | |
| $I_{CEX}$ | Collector cutoff current | $V_{CE}$ = 50 V, $I_I$ = 0, see 图 6-1 | $T_A$ = 25°C | | | 50 | μA |
| | | | $T_A$ = 105°C | | | | |
| | | $V_{CE}$ = 50 V, see 图 6-2 | $I_I$ = 0 | | | 100 | |
| | | | $V_I$ = 1 V | | | 500 | |
| $V_F$ | Clamp forward voltage | $I_F$ = 350 mA, see 图 6-6 | | | 1.7 | 2.1 | V |
| $I_{I(off)}$ | Off-state input current | $V_{CE}$ = 50 V, $I_C$ = 500 μA, see 图 6-3 | | 50 | 65 | | μA |
| $I_I$ | Input current | $V_I$ = 5 V, see 图 6-4 | | | 0.35 | 0.5 | mA |
| | | $V_I$ = 12 V, , see 图 6-4 | | | 1 | 1.45 | |
| $I_R$ | Clamp reverse current | $V_R$ = 50 V, see 图 6-5 | $T_A$ = 25°C | | | 50 | μA |
| | | | $T_A$ = 105°C | | | 100 | |
| $C_i$ | Input capacitance | $V_I$ = 0, f = 1 MHz | | | 15 | 25 | pF |

## 5.7 Switching Characteristics, ULQ2003A and ULQ2004A

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | See 图 6-9 | | 1 | 10 | μs |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | See 图 6-9 | | 1 | 10 | μs |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 50 V, $I_O$ = 300 mA, see 图 6-10 | $V_S$ – 500 | | | mV |

## 5.8 Dissipation Ratings

| PACKAGE | $T_A$ = 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 85°C POWER RATING | $T_A$ = 105°C POWER RATING | $T_A$ = 125°C POWER RATING |
|---|---|---|---|---|---|
| D | 950 mW | 7.6 mW/°C | 494 mW | 342 mW | 190 mW |

## 6 Parameter Measurement Information

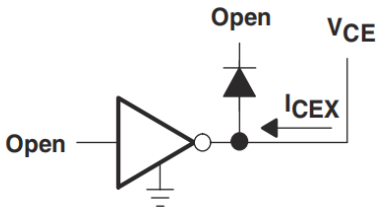



图 6-1. $I_{CEX}$ Test Circuit

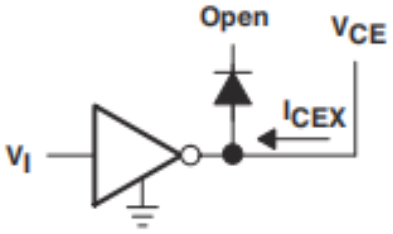



图 6-2. $I_{CEX}$ Test Circuit

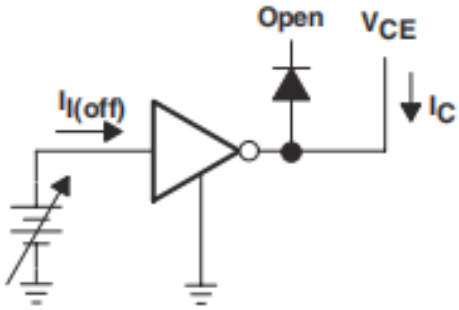



图 6-3. $I_{I(off)}$ Test Circuit

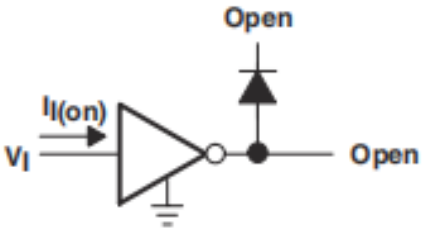



图 6-4. $I_I$ Test Circuit

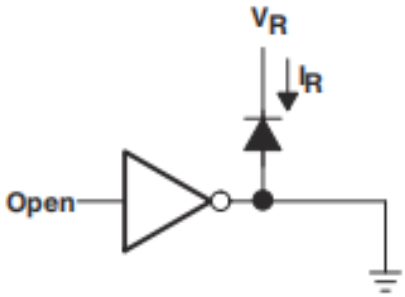



图 6-5. $I_R$ Test Circuit

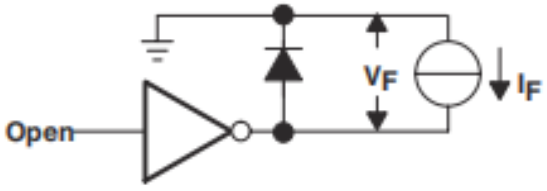
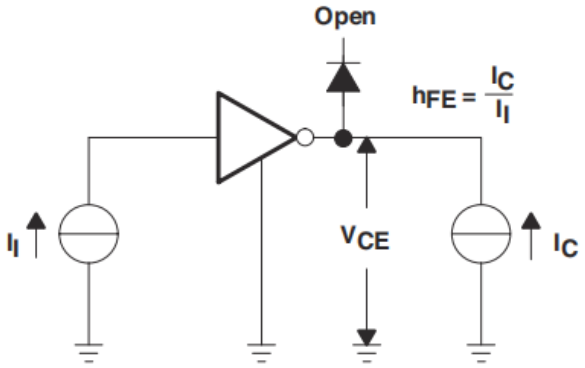



图 6-6. $V_F$ Test Circuit




A. $I_I$ is fixed for measuring $V_{CE(sat)}$, variable for measuring $h_{FE}$.

图 6-7. $h_{FE}$, $V_{CE(sat)}$ Test Circuit

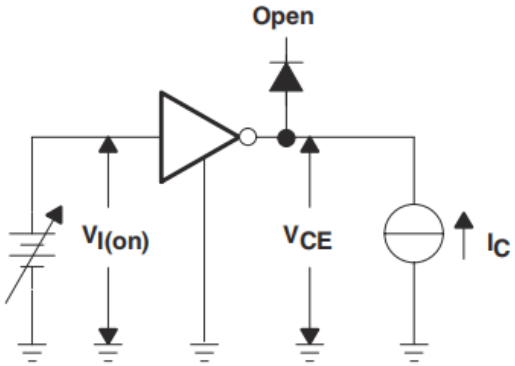
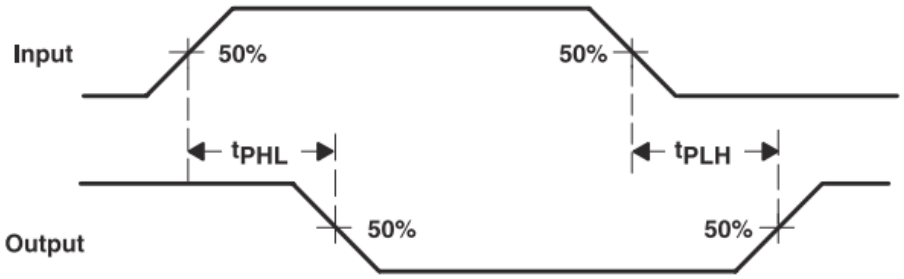
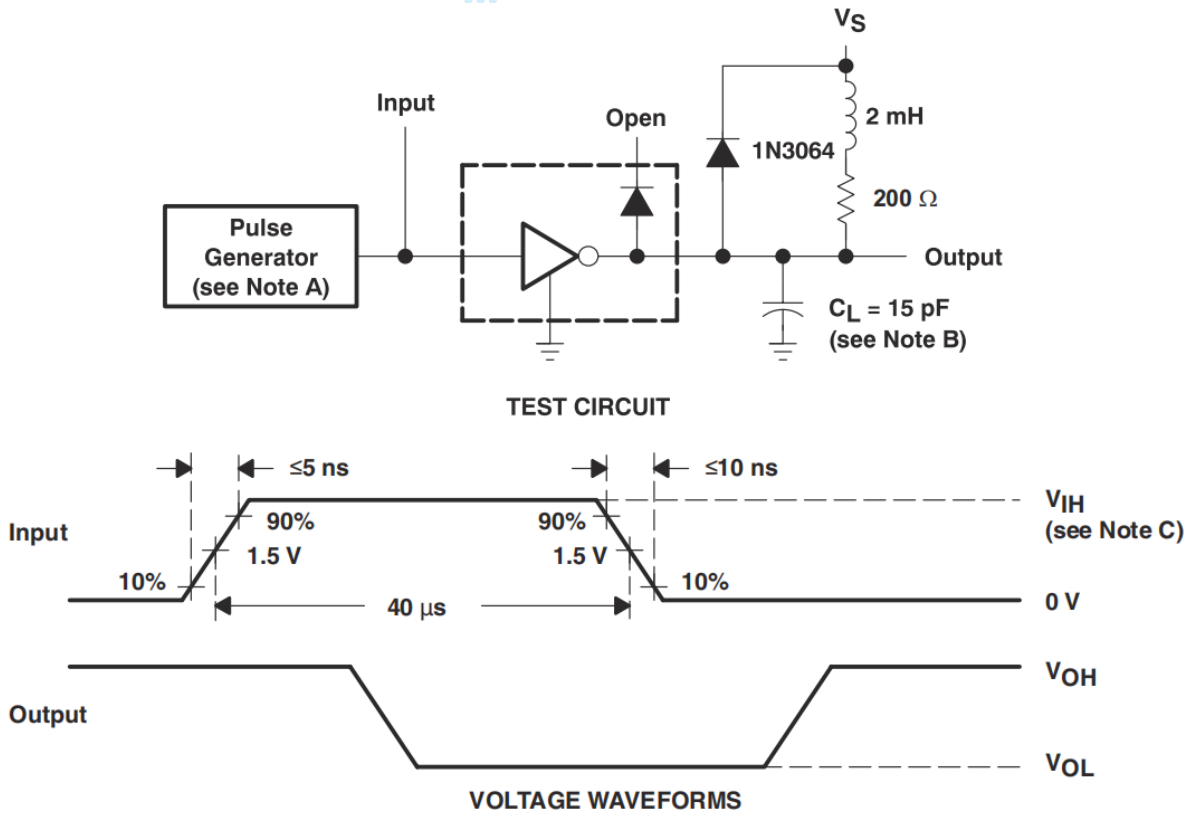



图 6-8. $V_{I(on)}$ Test Circuit




VOLTAGE WAVEFORMS

图 6-9. Propagation Delay-Time Waveforms




A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.
C. For testing the ULQ2003A, $V_{IH}$ = 3 V; for the ULQ2004A, $V_{IH}$ = 8 V.

**图 6-10. Latch-Up Test Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to integration of 7 Darlington transistors of the device that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULQ200xA-Q1 devices comprise seven high-voltage, high-current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULNQ200xA-Q1 devices have a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULQ2003xA-Q1 device offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range ( – 40°C to 105°C for ULQ200xAT or – 40°C to 125°C for ULQ2003AQ).

## 7.2 Functional Block Diagram

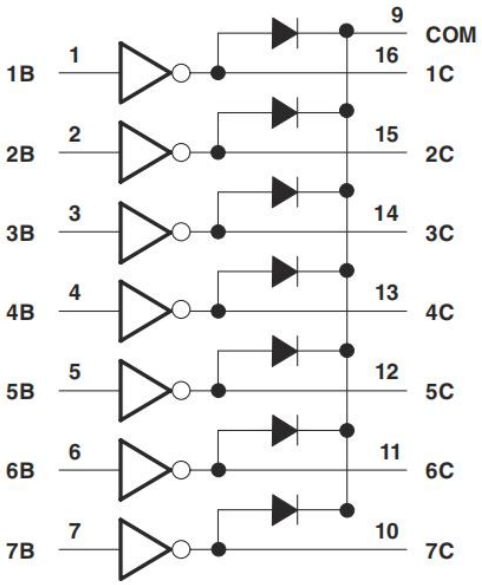
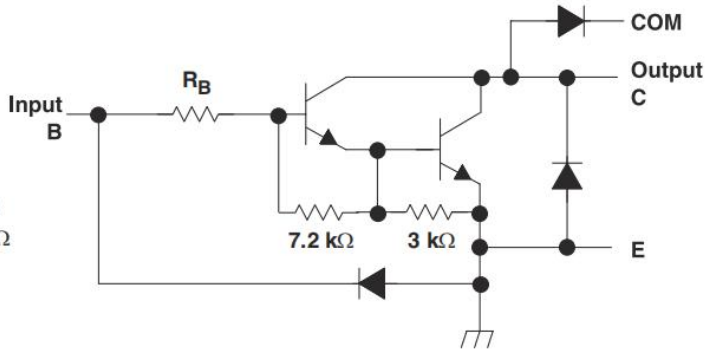



图 7-1. Logic Diagram




ULQ2003A: $R_B$ = 2.7 kΩ
ULQ2004A: $R_B$ = 10.5 kΩ

A. All resistor values shown are nominal.
B. The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

图 7-2. Schematics (Each Darlington Pair)

## 7.3 Feature Description

Each channel of the ULQ200xA-Q1 devices consist of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high-current gain ( β 2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high-output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ or 10.5-kΩ resistor connected between the input and base of the predriver Darlington NPN. The 7.2-kΩ and 3-kΩ resistors connected between the base and emitter of each respective NPN act as pulldowns and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diodes are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

## 7.4 Device Functional Modes

### *7.4.1 Inductive Load Drive*

When the COM pin is tied to the coil supply voltage, ULQ200xA-Q1 devices are able to drive inductive loads and suppress the kick-back voltage through the internal free-wheeling diodes.

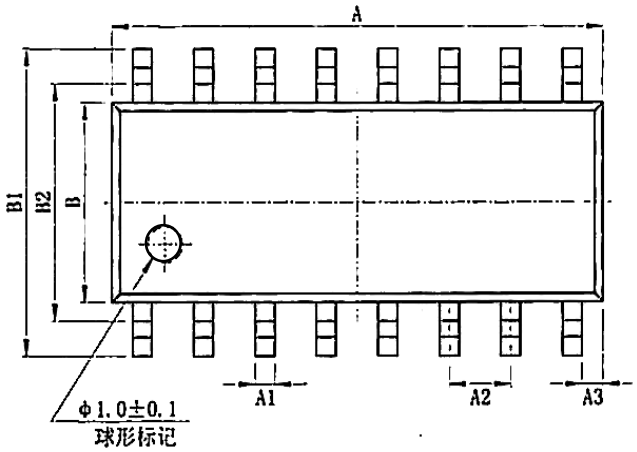
### *7.4.2 Resistive Load Drive*

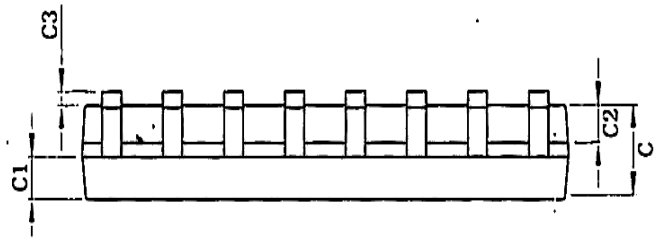
When driving a resistive load, a pullup resistor is needed in order for the ULQ200xA-Q1 devices to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

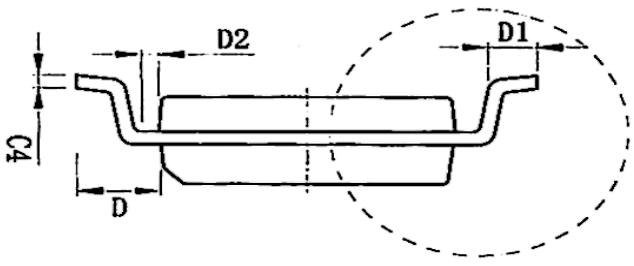
# Order information

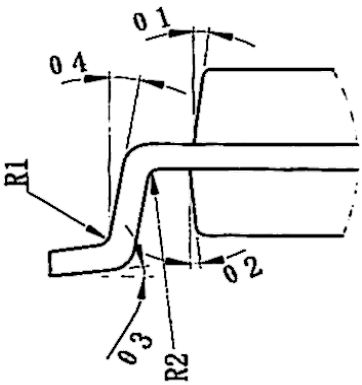
| Order Number | Package | Package Quantity | Marking On The park |
|---|---|---|---|
| ULQ2004ATDRG4Q1-TUDI | SOP16 | Tape,Reel,2500 | ULQ2004ATDRG4Q1 |

# Package SOP16




| SIZE / SYMBOL | MIN./mm | MAX./mm |
|---|---|---|
| A | 9.80 | 10.00 |
| A1 | 0.356 | 0.456 |
| A2 | 1.27TYP | |
| A3 | 0.302TYP | |
| B | 3.85 | 3.95 |
| B1 | 5.84 | 6.24 |
| B2 | 5.00 TYP | |
| C | 1.40 | 1.60 |
| C1 | 0.61 | 0.71 |
| C2 | 0.54 | 0.64 |
| C3 | 0.05 | 0.25 |
| C4 | 0.203 | 0.233 |
| D | 1.05 TYP | |
| D1 | 0.40 | 0.70 |
| D2 | 0.15 | 0.25 |
| R1 | 0.20TYP | |
| R2 | 0.20TYP | |
| 01 | 8°~12°TYP4 | |
| 02 | 8°~12°TYP4 | |
| 03 | 0°~8° | |
| 04 | 4°~12° | |

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