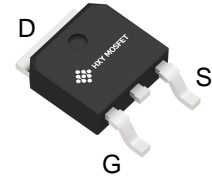




## Description

The RD3P175SNFRATL uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



**TO-252-2L  
(TO-252)**

## General Features

$V_{DS} = 100V$   $I_D = 20A$

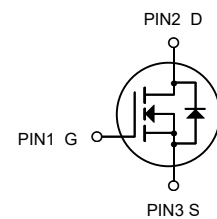
$R_{DS(ON)} < 87m\Omega$  @  $V_{GS}=10V$

## Application

Battery protection

Load switch

Uninterruptible power supply



N-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
RD3P175SNFRATL	TO-252-2L(TO-252)	HXY MOSFET	2500

## Absolute Maximum Ratings $T_c=25^\circ C$ unless otherwise noted

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V <sup>1</sup>	20	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V <sup>1</sup>	10	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	30	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	6.1	mJ
$I_{AS}$	Avalanche Current	15	A
$P_D@T_c=25^\circ C$	Total Power Dissipation <sup>4</sup>	34.7	W
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	2	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	3.6	$^\circ C/W$



**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	---	---	V
$\Delta BV_{DSS}/\Delta T$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1mA$	---	0.098	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=10A$	---	80	87	$m\Omega$
		$V_{GS}=4.5V, I_D=8A$	---	95	105	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.57	---	$mV/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=80V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=10A$	---	13	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2	---	$\Omega$
$Q_g$	Total Gate Charge (10V)	$V_{DS}=80V, V_{GS}=10V, I_D=10A$	---	26.2	---	nC
$Q_{gs}$	Gate-Source Charge		---	4.6	---	
$Q_{gd}$	Gate-Drain Charge		---	5.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=10A$	---	4.2	---	ns
$T_r$	Rise Time		---	8.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	35.6	---	
$T_f$	Fall Time		---	9.6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	1535	---	pF
$C_{oss}$	Output Capacitance		---	60	---	
$C_{rss}$	Reverse Transfer Capacitance		---	37	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	20	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	30	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=10A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	37	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	27.3	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=11A$
- 4.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications , should be limited by total power dissipation.



### Typical Characteristics

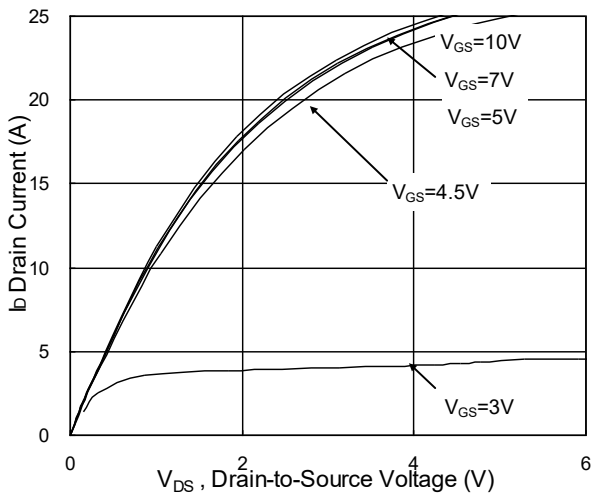


Fig.1 Typical Output Characteristics



Fig.2 On-Resistance vs. Gate-Source

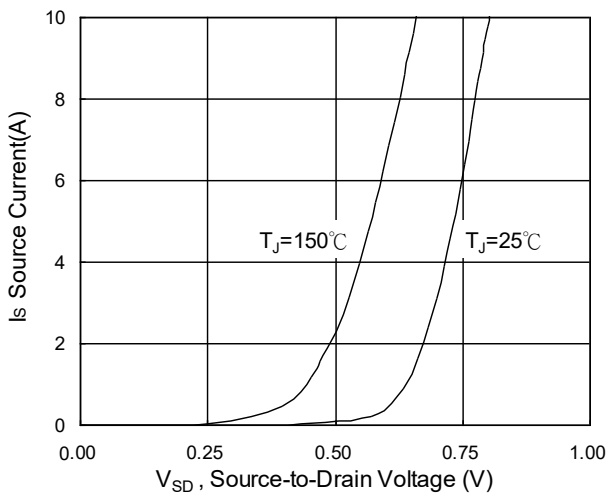


Fig.3 Forward Characteristics Of Reverse

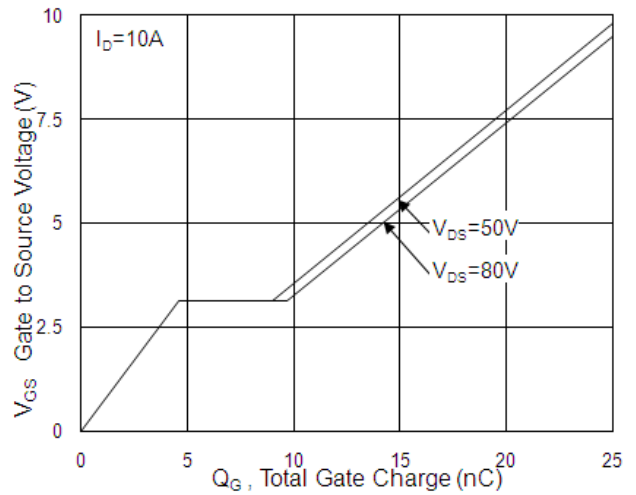


Fig.4 Gate-Charge Characteristics

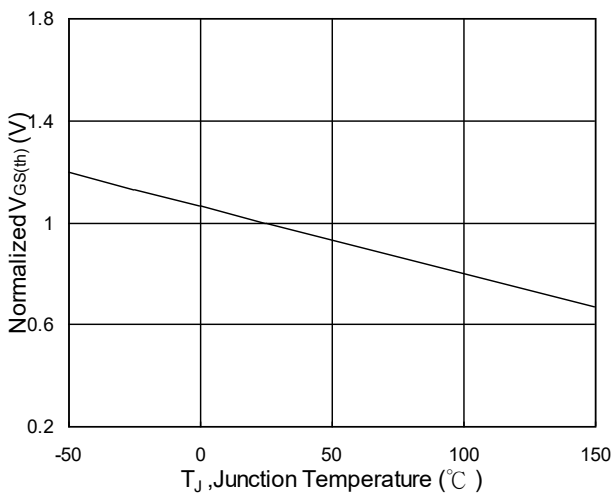


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

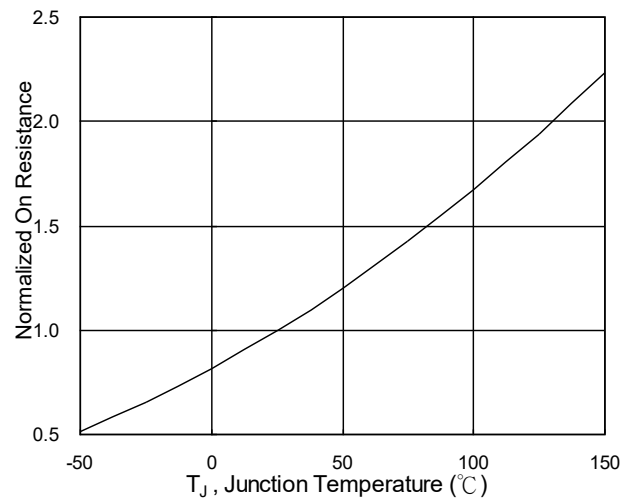
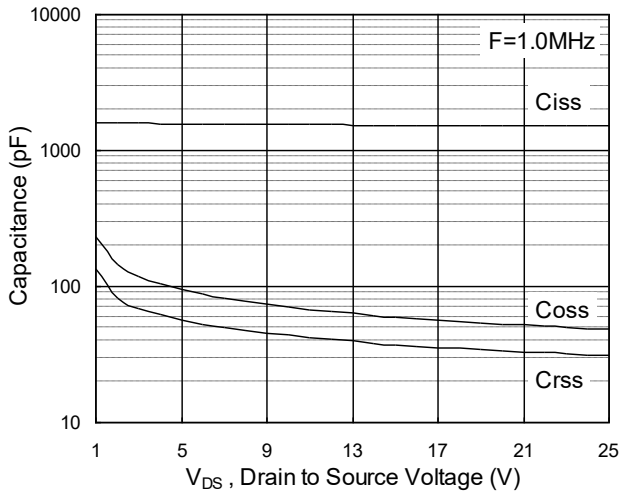
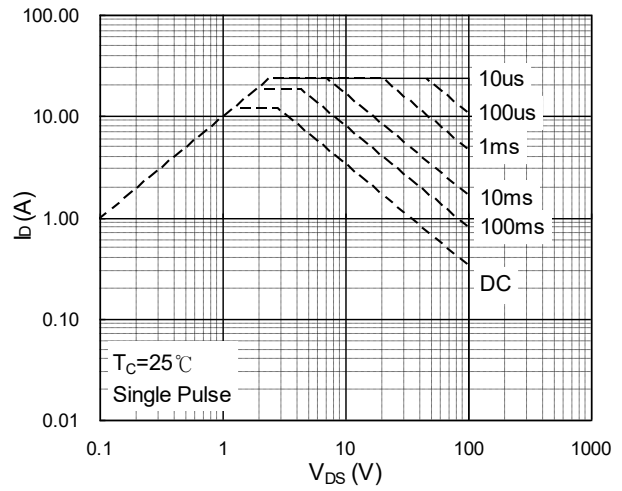


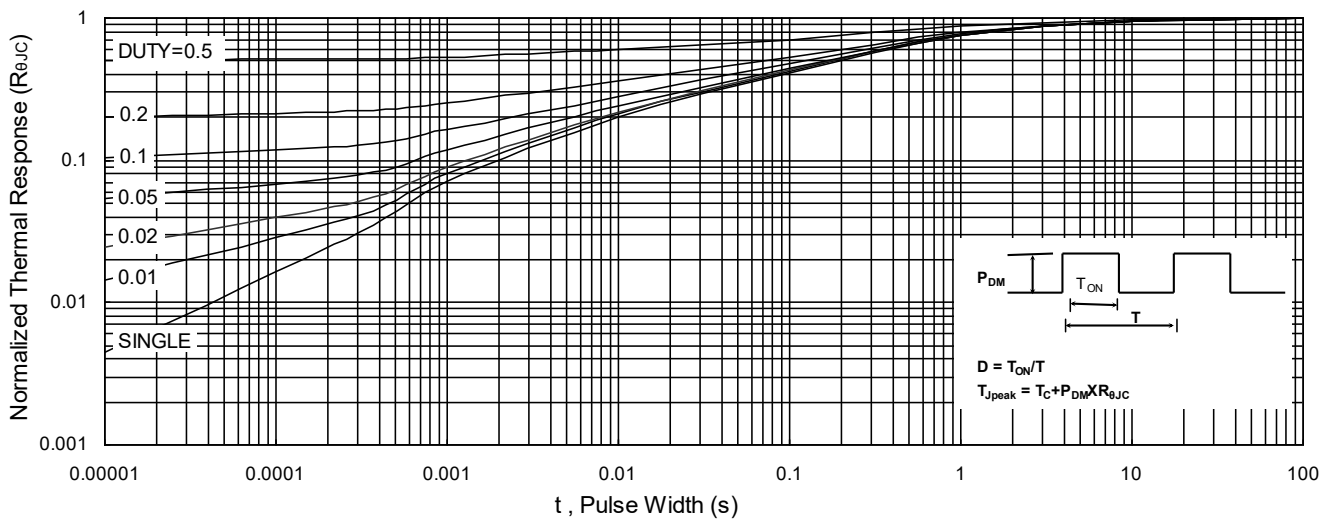
Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$



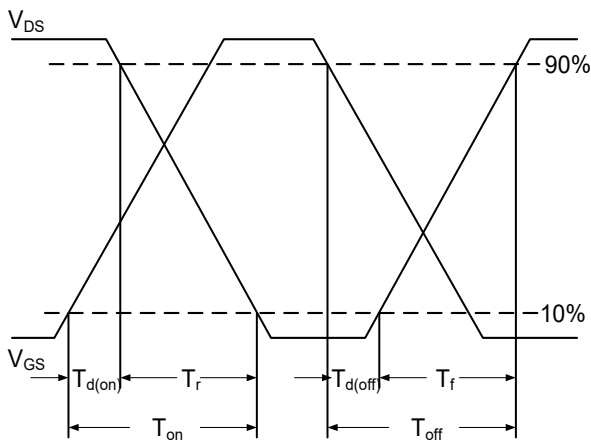
**Fig.7 Capacitance**



**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**





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