钍地半导体
Tudi Semiconductor

Product Specification

TUDI-TS912/TS912A

Rail-to-rail CMOS dual operational amplifier

网址 www.sztdbdt.com

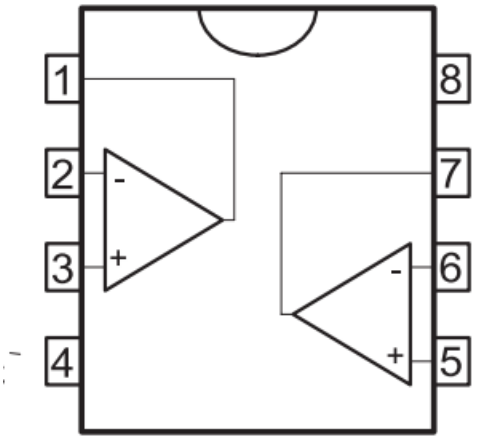
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

●Rail-to-rail input and output voltage ranges
●Single (or dual) supply operation
from 2.7 to 16 V
● Extremely low input bias current: 1 pA typ.
●Low input offset voltage: 2 mV max.
●Specified for 600 and 100 loads
● Low supply current: 200 A/amplifier (V_{CC} = 3 V)
● Latch-up immunity
● ESD tolerance: 3 kV
● Spice macromodel included in this specification
Related products
● See TS56x series for better accuracy and
smaller packages



Pin connections (top view)

Description

The TS912 device is a rail-to-rail CMOS dual operational amplifier designed to operate with a single or dual supply voltage.
The input voltage range Vicm includes the two supply rails V_{CC}^+ and V_{CC}^-.
The output reaches V_{CC}^- +30 mV, V_{CC}^+ -40 mV, with R_L = 10 kΩ and V_{CC}^- +300 mV, V_{CC}^+ -400 mV, with R_L = 600Ω .
This product offers a broad supply voltage operating range from 2.7 to 16 V and a supply current of only 200 A/amp. (V_{CC} = 3 V).
Source and sink output current capability is typically 40 mA (at V_{CC} = 3 V), fixed by an internal limitation circuit.

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	18	V
V_{id}	Differential input voltage(2)	±18	V
V_i	Input voltage(3)	-0.3 to 18	V
I_{in}	Current on inputs	±50	mA
I_o	Current on outputs	±130	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction-to-ambient(4) DIP8 SO-8	 85 125	°C/W
R_{thjc}	Thermal resistance junction to case(4) DIP8 SO-8	 41 40	°C/W
ESD	HBM: human body model(5)	3	kV
	MM: machine model(6)	200	V
	CDM: charged device model(7)	1500	V

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These values are typical.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	V_{CC-}-0.2 to V_{CC+}+0.2	V
T_{oper}	Operating free air temperature range	-40 to + 125	°C

2 Schematic diagram

Figure 1. Schematic diagram (1/2 TS912)

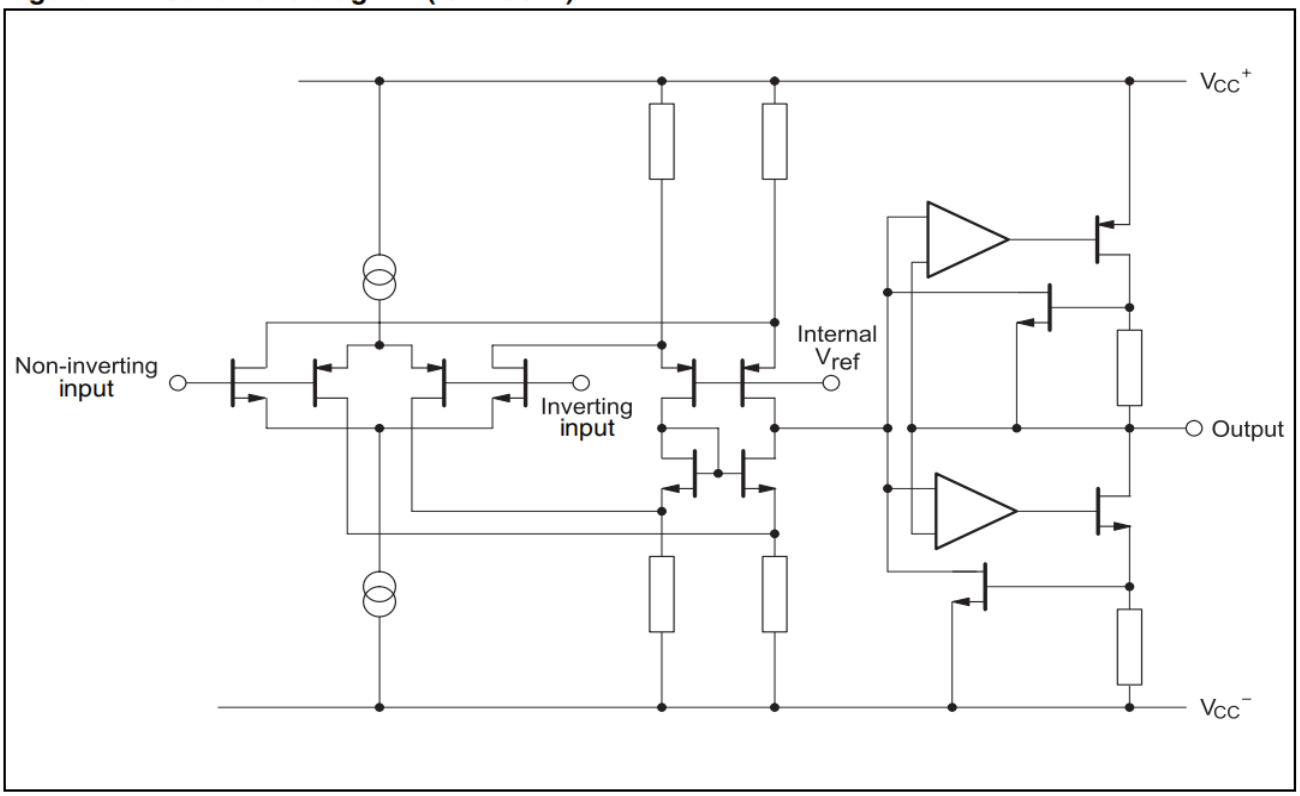


Table 3. V_{CC+} = 3 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR^+	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 1.3 V to 1.7 V)		0.4		V/µs
SR^-	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 1.3 V to 1.7 V)		0.3		V/µs
ϕm	Phase margin		30		Degrees
en	Equivalent input noise voltage (R_s = 100 Ω, f = 1 kHz)		30		nV/√Hz

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 4. V_{CC+} = 5 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
en	Equivalent input noise voltage (R_s = 100 Ω, f = 1 kHz)		30		nV/√Hz
V_{O1}/V_{O2}	Channel separation (f = 1 kHz)		120		dB
ϕm	Phase margin		30		Degrees

1. Maximum values include unavoidable inaccuracies of the industrial tests.

3 Electrical characteristics

Table 3. V_{CC+} = 3 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (V_{ic} = V_o = $V_{CC}/2$) TS912 TS912A TS912B $T_{min} \le T_{amb} \le T_{max}$ TS912 TS912A TS912B			 10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		µV/°C
I_{io}	Input offset current(1) $T_{min} \le T_{amb} \le T_{max}$		1	100 200	pA
I_{ib}	Input bias current(1) $T_{min} \le T_{amb} \le T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, A_{VCL} = 1, no load) $T_{min} \le T_{amb} \le T_{max}$		200	300 400	µA
CMR	Common mode rejection ratio V_{ic} = 0 to 3 V, V_o = 1.5 V		70		dB
SVR	Supply voltage rejection ratio (V_{CC}^+ = 2.7 to 3.3 V, V_o = $V_{CC}/2$)	50	80		dB
A_{vd}	Large signal voltage gain (R_L = 10 kΩ, V_o = 1.2 V to 1.8 V) $T_{min} \le T_{amb} \le T_{max}$	3 2	10		V/mV
V_{OH}	High level output voltage (V_{id} = 1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω	 2.95 2.9 2.3 2.8 2.1	 2.96 2.6 2		V
V_{OL}	Low level output voltage (V_{id} = -1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω		 30 300 900	 50 70 400 100 600	mV
I_o	Output short-circuit current (V_{id} = ±1 V) Source (V_o = V_{CC-}) Sink (V_o = V_{CC+})	 20 20	 40 40		mA
GBP	Gain bandwidth product (A_{VCL} = 100, R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz)		0.8		MHz

Table 4. V_{CC+} = 5 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (V_{ic} = V_o = $V_{CC}/2$) TS912 TS912A TS912B $T_{min} \le T_{amb} \le T_{max}$ TS912 TS912A TS912B			 10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		µV/°C
I_{io}	Input offset current(1) $T_{min} \le T_{amb} \le T_{max}$		1	100 200	pA
I_{ib}	Input bias current(1) $T_{min} \le T_{amb} \le T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, A_{VCL} = 1, no load) $T_{min} \le T_{amb} \le T_{max}$		230	350 450	µA
CMR	Common mode rejection ratio V_{ic} = 1.5 to 3.5 V, V_o = 2.5 V	60	85		dB
SVR	Supply voltage rejection ratio (V_{CC+} = 3 to 5 V, V_o = $V_{CC}/2$)	55	80		dB
A_{vd}	Large signal voltage gain (R_L = 10 kΩ, V_o = 1.5 V to 3.5 V) $T_{min} \le T_{amb} \le T_{max}$	10 7	40		V/mV
V_{OH}	High level output voltage (V_{id} = 1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω	 4.95 4.9 4.25 4.8 4.1	 4.95 4.55 3.7		V
V_{OL}	Low level output voltage (V_{id} = -1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω		 40 350 1400	 50 100 500 150 750	mV
I_o	Output short-circuit current (V_{id} = ±1 V) Source (V_o = V_{CC-}) Sink (V_o = V_{CC+})	 45 45	 65 65		mA
GBP	Gain bandwidth product (A_{VCL} = 100, R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz)		1		MHz
SR^+	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 1 V to 4 V)		0.8		V/µs
SR^-	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 1 V to 4 V)		0.6		V/µs

Table 5. V_{CC+} = 10 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (V_{ic} = V_o = $V_{CC}/2$) TS912 TS912A TS912B $T_{min} \le T_{amb} \le T_{max}$ TS912 TS912A TS912B			 10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		µV/°C
I_{io}	Input offset current(1) $T_{min} \le T_{amb} \le T_{max}$		1	100 200	pA
I_{ib}	Input bias current(1) $T_{min} \le T_{amb} \le T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, A_{VCL} = 1, no load) $T_{min} \le T_{amb} \le T_{max}$		400	600 700	µA
CMR	Common mode rejection ratio V_{ic} = 3 to 7 V, V_o = 5 V V_{ic} = 0 to 10 V, V_o = 5 V	 60 50	 90 75		dB
SVR	Supply voltage rejection ratio (V_{CC+} = 5 to 10 V, V_o = $V_{CC}/2$)	60	90		dB
A_{vd}	Large signal voltage gain (R_L = 10 kΩ, V_o = 2.5 V to 7.5 V) $T_{min} \le T_{amb} \le T_{max}$	15 10	50		V/mV
V_{OH}	High level output voltage (V_{id} = 1V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω	 9.95 9.85 9 9.8 8.8	 9.95 9.35 7.8		V
V_{OL}	Low level output voltage (V_{id} = -1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω		 50 650 2300	 50 150 800 150 900	mV
I_o	Output short-circuit current (V_{id} = ±1 V) Source (V_o = V_{CC-}) Sink (V_o = V_{CC+})	 45 50	 65 75		mA
GBP	Gain bandwidth product (A_{VCL} = 100, R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz)		1.4		MHz

Table 5. V_{CC+} = 10 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified) (continued)

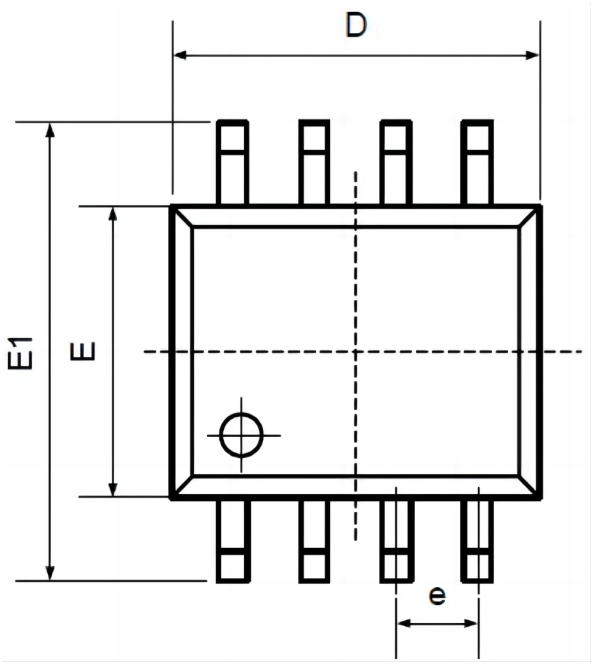
Symbol	Parameter	Min.	Typ.	Max.	Unit
SR^+	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 2.5 V to 7.5 V)		1.3		V/µs
SR^-	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 2.5 V to 7.5 V)		0.8		V/µs
ϕm	Phase margin		40		Degrees
en	Equivalent input noise voltage (R_s = 100 Ω, f = 1 kHz)		30		nV/√Hz
THD	Total harmonic distortion (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_o = 4.75 V to 5.25 V, f = 1 kHz)		0.02		%
C_{in}	Input capacitance		1.5		pF

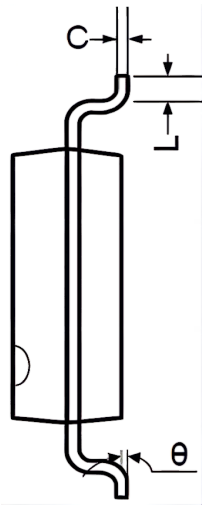
1. Maximum values include unavoidable inaccuracies of the industrial tests.

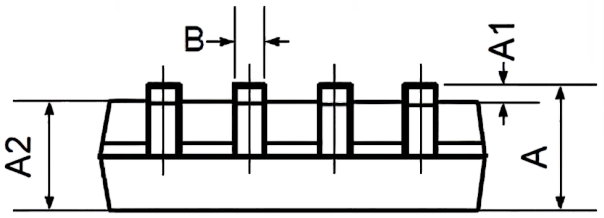
Order information

Order Number	Package	Package Quantity	Marking On The park
TS912AIDT-TUDI	SOP8	Tape,Reel,2500	TS912AIDT
TS912AIN-TUDI	DIP8	Tube,50,A box of 2000	TS912AIN
TS912IDT-TUDI	SOP8	Tape,Reel,2500	TS912IDT
TS912IN-TUDI	DIP8	Tube,50,A box of 2000	TS912IN

Package SOP8

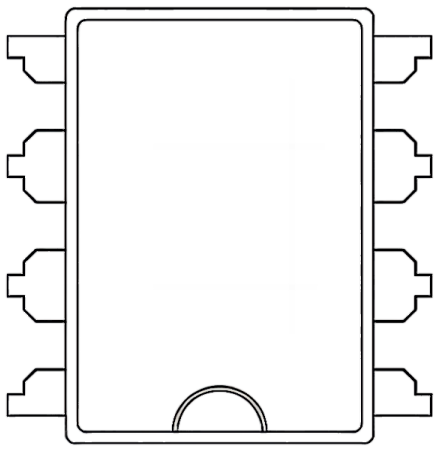


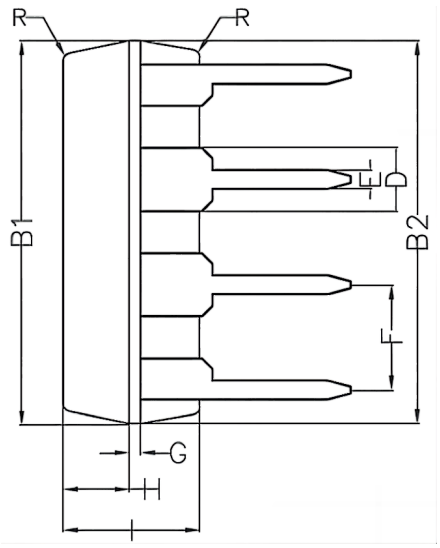


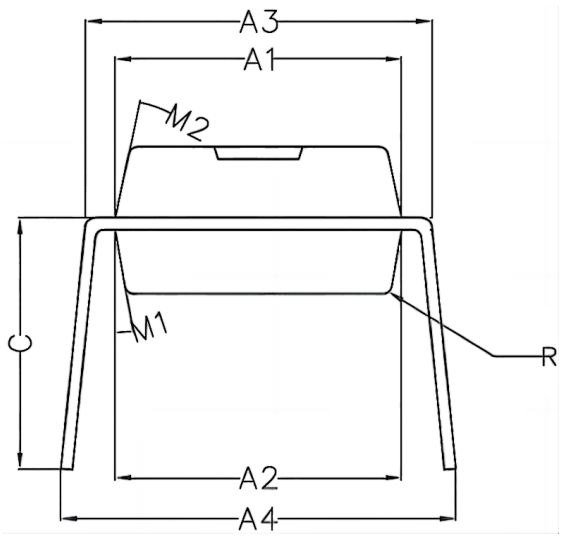


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Important statement:

●TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.

●Any semi-guide product is subject to failure or malfunction under specified conditions. It is the buyer's responsibility to comply with safety standards when using TUDI Semiconductor products for system design and whole machine manufacturing.And take the appropriate safety measures to avoid the potential in the risk of loss of personal injury or loss of property situation!

●TUDI Semiconductor products have not been licensed for life support, military, and aerospace applications,and therefore TUDI Semiconductor is not responsible for any consequences arising from the use of this product in these areas.

●If any or all TUDI Semiconductor products (including technical data, services) described or contained in this document are subject to any applicable local export control laws and regulations, they may not be exported without an export license from the relevant authorities in accordance with such laws.

●The specifications of any and all TUDI Semiconductor products described or contained in this document specify the performance, characteristics, and functionality of said products in their standalone state, but do not guarantee the performance, characteristics, and functionality of said products installed in Customer's products or equipment. In order to verify symptoms and conditions that cannot be evaluated in a standalone device, the Customer should ultimately evaluate and test the device installed in the Customer's product device.

●TUDI Semiconductor documentation is only allowed to be copied without any alteration of the content and with the relevant authorization.TUDI Semiconductor assumes no responsibility or liability for altered documents.

●TUDI Semiconductor is committed to becoming the preferred semiconductor brand for customers, and TUDI Semiconductor will strive to provide customers with better performance and better quallity products.