



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD234 /SN65HVD235

3.3-V CAN Bus Transceivers

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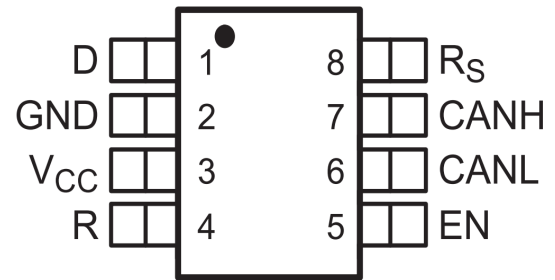


Features

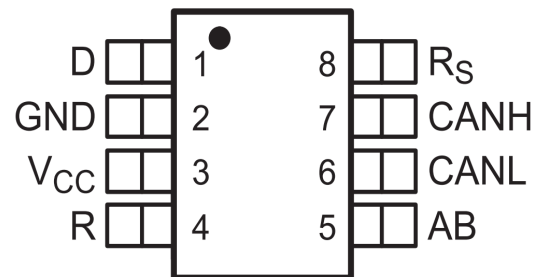
- Single 3.3-V Supply Voltage
- Bus Pins Fault Protection Exceeds ± 36 V
- Bus Pins ESD Protection Exceeds ± 16 kV HBM
- Compatible With ISO 11898-2
- GIFT/ICT Compliant
- Data Rates up to 1 Mbps
- Extended – 7 V to 12 V Common Mode Range
- High-Input Impedance Allows for 120 Nodes
- LVTTTL I/Os are 5-V Tolerant
- Adjustable Driver Transition Times for Improved Emissions Performance
- Unpowered Node Does Not Disturb the Bus
- Low Current Standby Mode, 200- μ A (Typical)
- SN65HVD233: Loopback Mode
- SN65HVD234: Ultra Low Current Sleep Mode
 - 50-nA Typical Current Consumption
- SN65HVD235: Autobaud Loopback Mode
- Thermal Shutdown Protection
- Power up and Down With Glitch-Free Bus Inputs and Outputs
 - High-Input Impedance With Low V_{CC}
 - Monolithic Output During Power Cycling

Applications

- Industrial Automation, Control, Sensors, and Drive Systems
- Motor and Robotic Control
- Building and Climate Control (HVAC)
- Backplane Communication and Control
- CAN Bus Standards such as CANopen, DeviceNet, CAN Kingdom, NMEA 2000, SAE J1939



SN65HVD234D (Marked as VP234)
(TOP VIEW)



SN65HVD235D (Marked as VP235)
(TOP VIEW)



Description

The SN65HVD233, SN65HVD234, and SN65HVD235 are used in applications employing the controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, each provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed for operation in especially harsh environments, the devices feature cross-wire protection, overvoltage protection up to ± 36 V, loss of ground protection, overtemperature (thermal shutdown) protection, and common-mode transient protection of ± 100 V. These devices operate over a wide -7 V to 12 V common-mode range. These transceivers are the interface between the host CAN controller on the microprocessor and the differential CAN bus used in industrial, building automation/transportation, and automotive applications.

Modes: The RS pin (pin 8) of the SN65HVD233, SN65HVD234, and SN65HVD235 provides three modes of operation: high-speed, slope control, and low-power standby mode. The high-speed mode of operation is selected by connecting pin 8 directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor between the RS pin and ground. The slope will be proportional to the pin's output current. With a resistor value of 10 k the device driver will have a slew rate of ~ 15 V/ μ s and with a value of 100 k the device will have ~ 2.0 V/ μ s slew rate. For more information about slope control, refer to Feature Description.

The SN65HVD233, SN65HVD234, and SN65HVD235 enter a low-current standby (listen only) mode during which the driver is switched off and the receiver remains active if a high logic level is applied to the RS pin. If the local protocol controller needs to transmit a message to the bus it will have to return the device to either high-speed mode or slope control mode via the RS pin.

Loopback (SN65HVD233): A logic high on the loopback (LBK) pin (pin 5) of the SN65HVD233 places the bus output and bus input in a high-impedance state. Internally, the D to R path of the device remains active and available for driver to receiver loopback that can be used for self-diagnostic node functions without disturbing the bus. For more information on the loopback mode, refer to Feature Description.

Ultra Low-Current Sleep (SN65HVD234): The SN65HVD234 enters an ultra low-current sleep mode in which both the driver and receiver circuits are deactivated if a low logic level is applied to EN pin (pin 5). The device remains in this sleep mode until the circuit is reactivated by applying a high logic level to pin 5.

Autobaud Loopback (SN65HVD235): The AB pin (pin 5) of the SN65HVD235 implements a bus listen-only loopback feature which allows the local node controller to synchronize its baud rate with that of the CAN bus. In autobaud mode, the bus output of the driver is placed in a high-impedance state while the bus input of the receiver remains active. There is an internal D pin to R pin loopback to assist the controller in baud rate detection, or the autobaud function. For more information on the autobaud mode, refer to Feature Description.



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
GND	2	GND	Ground connection
V _{CC}	3	Supply	Transceiver 3.3-V supply voltage
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
LBK	5	I	SN65HVD233: Loopback mode input pin
EN		I	SN65HVD234: Enable input pin. Logic high for enabling a normal mode (high speed or slope control) mode. Logic low for sleep mode.
AB		I	SN65HVD235: Autobaud loopback mode input pin
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
R _S	8	I	Mode select pin: strong pulldown to GND = high speed mode, strong pullup to V _{CC} = low power mode, 10-k Ω to 100-k Ω pulldown to GND = slope control mode

8 Specifications

8.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range unless otherwise noted

	MIN	MAX	UNIT
V _{CC} Supply voltage	-0.3	7	V
Voltage at any bus terminal (CANH or CANL)	-36	36	V
Voltage input, transient pulse, CANH and CANL, through 100 Ω (see Figure 18)	-100	100	V
V _I Input voltage, (D, R _S , EN, LBK, AB)	-0.5	7	V
V _O Output voltage	-0.5	7	V
I _O Receiver output current	-10	10	mA
Continuous total power dissipation	See Power Dissipation Ratings		
T _J Operating junction temperature		150	°C
T _{stg} Storage temperature		125	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground pin.



8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	CANH, CANL and GND	±16000	V
		All pins	3000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
	Voltage at any bus terminal (separately or common mode)		-7	12	
V_{IH}	High-level input voltage	D, EN, AB, LBK	2	5.5	
V_{IL}	Low-level input voltage	D, EN, AB, LBK	0	0.8	
V_{ID}	Differential input voltage between CANH and CANL		-6	6	
	Resistance from R_S to ground		0	100	k Ω
$V_{I(RS)}$	Input Voltage at R_S for standby		0.75 V_{CC}	5.5	V
I_{OH}	High-level output current	Driver	-50		mA
		Receiver	-10		
I_{OL}	Low-level output current	Driver		50	mA
		Receiver		10	
T_J	Operating junction temperature			150	°C
T_A	Operating free-air temperature ⁽¹⁾		-40	125	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

8.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	Low-K ⁽²⁾ board, no air flow	185	°C/W
		High-K ⁽³⁾ board, no air flow	101	
$R_{\theta JB}$	Junction-to-board thermal resistance	High-K ⁽³⁾ board, no air flow	82.8	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance		26.5	°C/W
$P_{(AVG)}$	Average power dissipation	$R_L = 60 \Omega$, R_S at 0 V, input to D a 1-MHz 50% duty cycle square wave V_{CC} at 3.3 V, $T_A = 25^\circ\text{C}$	36.4	mW
$T_{(SD)}$	Thermal shutdown junction temperature		170	°C

(1) See [SZZA003](#) for an explanation of this parameter.

(2) JESD51-3 low effective thermal conductivity test board for leaded surface mount packages.

(3) JESD51-7 high effective thermal conductivity test board for leaded surface mount packages.

8.5 Power Dissipation Ratings

PACKAGE	CIRCUIT BOARD	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	Low-K	596.6 mW	5.7 mW/°C	255.7 mW	28.4 mW
D	High-K	1076.9 mW	10.3 mW/°C	461.5 mW	51.3 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



8.6 Electrical Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	D at 0 V, R_S at 0 V, See Figure 12 and Figure 13	2.45		V_{CC}	V
		CANL		0.5		1.25	
V_O	Bus output voltage (Recessive)	CANH	D at 3 V, R_S at 0 V, See Figure 12 and Figure 13		2.3		V
		CANL			2.3		
$V_{OD(D)}$	Differential output voltage (Dominant)		D at 0 V, R_S at 0 V, See Figure 12 and Figure 13	1.5	2	3	V
			D at 0 V, R_S at 0 V, See Figure 13 and Figure 14	1.2	2	3	
V_{OD}	Differential output voltage (Recessive)		D at 3 V, R_S at 0 V, See Figure 12 and Figure 13	-120		12	mV
			D at 3 V, R_S at 0 V, No Load	-0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 21		1		V
I_{IH}	High-level input current	D, EN, LBK, AB	D = 2 V or EN = 2 V or LBK = 2 V or AB = 2 V	-30		30	μ A
I_{IL}	Low-level input current	D, EN, LBK, AB	D = 0.8 V or EN = 0.8 V or LBK = 0.8 V or AB = 0.8 V	-30		30	μ A
I_{OS}	Short-circuit output current		$V_{CANH} = -7$ V, CANL Open, See Figure 26	-250			mA
			$V_{CANH} = 12$ V, CANL Open, See Figure 26			1	
			$V_{CANL} = -7$ V, CANH Open, See Figure 26	-1			
			$V_{CANL} = 12$ V, CANH Open, See Figure 26			250	
C_O	Output capacitance		See receiver input capacitance				
$I_{IRS(s)}$	R_S input current for standby		R_S at 0.75 V_{CC}	-10			μ A
I_{CC}	Supply current	Sleep	EN at 0 V, D at V_{CC} , R_S at 0 V or V_{CC}		0.05	2	μ A
		Standby	R_S at V_{CC} , D at V_{CC} , AB at 0 V, LBK at 0 V, EN at V_{CC}		200	600	
		Dominant	D at 0 V, No Load, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}			6	mA
		Recessive	D at V_{CC} , No Load, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}			6	

(1) All typical values are at 25°C and with a 3.3-V supply.



8.7 Electrical Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	AB at 0 V, LBK at 0 V, EN at V_{CC} , See Table 1		750	900	mV
V_{IT-}	Negative-going input threshold voltage		500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			100		
V_{OH}	High-level output voltage	$I_O = -4$ mA, See Figure 17	2.4			V
V_{OL}	Low-level output voltage	$I_O = 4$ mA, See Figure 17			0.4	
I_I	Bus input current	CANH or CANL at 12 V	150		500	μ A
		CANH or CANL at 12 V, V_{CC} at 0 V	200		600	
		CANH or CANL at -7 V	-610		-150	
		CANH or CANL at -7 V, V_{CC} at 0 V	-450		-130	
C_I	Input capacitance (CANH or CANL)	Pin-to-ground, $V_I = 0.4 \sin(4E6\pi t) + 0.5$ V, D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}		40		pF
C_{ID}	Differential input capacitance	Pin-to-pin, $V_I = 0.4 \sin(4E6\pi t) + 0.5$ V, D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}		20		
R_{ID}	Differential input resistance	D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}	40		100	k Ω
R_{IN}	Input resistance (CANH or CANL) to ground		20		50	
I_{CC}	Supply current	Sleep	EN at 0 V, D at V_{CC} , R_S at 0 V or V_{CC}	0.05	2	μ A
		Standby	R_S at V_{CC} , D at V_{CC} , AB at 0 V, LBK at 0 V, EN at V_{CC}	200	600	
		Dominant	D at 0 V, No Load, R_S at 0 V, LBK at 0 V, AB at 0 V, EN at V_{CC}		6	mA
		Recessive	D at V_{CC} , No Load, R_S at 0 V, LBK at 0 V, AB at 0 V, EN at V_{CC}		6	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.8 Switching Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_S at 0 V, See Figure 15		35	85	ns
		R_S with 10 k Ω to ground, See Figure 15		70	125	
		R_S with 100 k Ω to ground, See Figure 15		500	870	
t_{PHL}	Propagation delay time, high-to-low-level output	R_S at 0 V, See Figure 15		70	120	ns
		R_S with 10 k Ω to ground, See Figure 15		130	180	
		R_S with 100 k Ω to ground, See Figure 15		870	1200	
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)	R_S at 0 V, See Figure 15		35		ns
		R_S with 10 k Ω to ground, See Figure 15		60		
		R_S with 100 k Ω to ground, See Figure 15		370		
t_r	Differential output signal rise time	R_S at 0 V, See Figure 15	20		70	ns
t_f	Differential output signal fall time		20		70	
t_r	Differential output signal rise time	R_S with 10 k Ω to ground, See Figure 15	30		135	ns
t_f	Differential output signal fall time		30		135	
t_r	Differential output signal rise time	R_S with 100 k Ω to ground, See Figure 15	350		1400	ns
t_f	Differential output signal fall time		350		1400	
$t_{en(s)}$	Enable time from standby to dominant	See Figure 19 and Figure 20		0.6	1.5	μ s
$t_{en(z)}$	Enable time from sleep to dominant			1	5	

(1) All typical values are at 25°C and with a 3.3-V supply.



8.9 Switching Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 17		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)			7		
t_r	Output signal rise time			2	5	
t_f	Output signal fall time			2	5	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.10 Switching Characteristics: Device

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	HVD233	See Figure 23		7.5	12	ns
$t_{(AB1)}$	Loopback delay, driver input to receiver output	HVD235	See Figure 24		10	20	ns
$t_{(AB2)}$	Loopback delay, bus input to receiver output		See Figure 25		35	60	ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant		R_S at 0 V, See Figure 22		70	135	ns
			R_S with 10 k Ω to ground, See Figure 22		105	190	
			R_S with 100 k Ω to ground, See Figure 22		535	1000	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive		R_S at 0 V, See Figure 22		70	135	ns
			R_S with 10 k Ω to ground, See Figure 22		105	190	
			R_S with 100 k Ω to ground, See Figure 22		535	1000	

(1) All typical values are at 25°C and with a 3.3-V supply.

9 Parameter Measurement Information

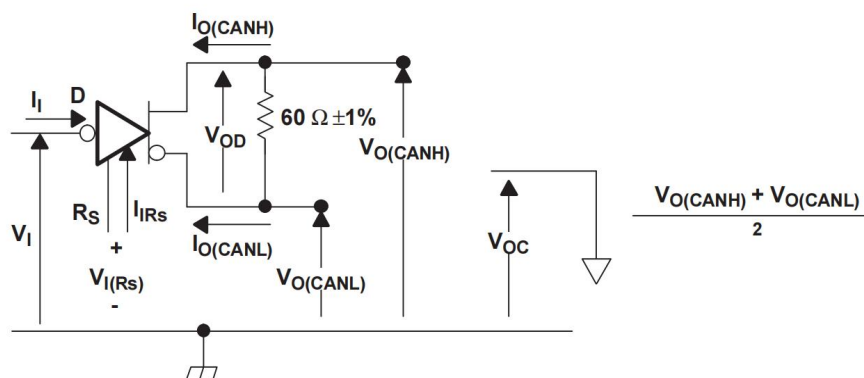


Figure 12. Driver Voltage, Current, and Test Definition

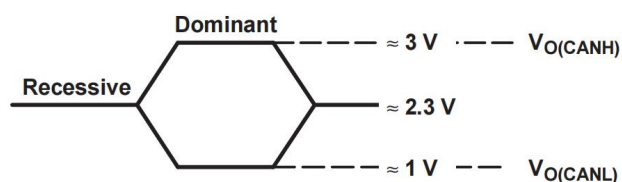


Figure 13. Bus Logic State Voltage Definitions

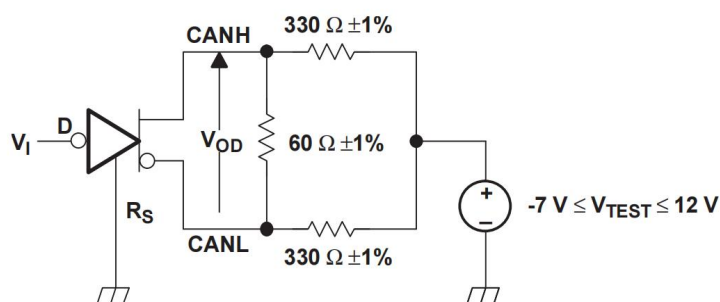
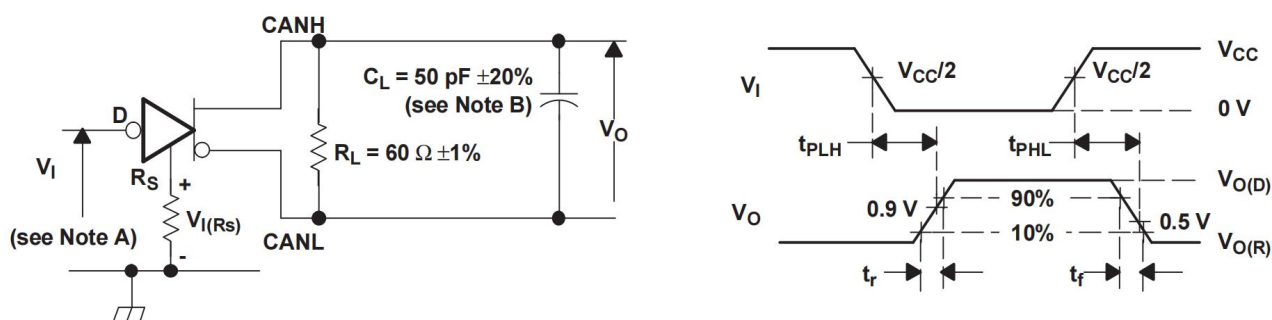


Figure 14. Driver V_{OD}



- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
- B. C_L includes fixture and instrumentation capacitance.

Figure 15. Driver Test Circuit and Voltage Waveforms



Parameter Measurement Information (continued)

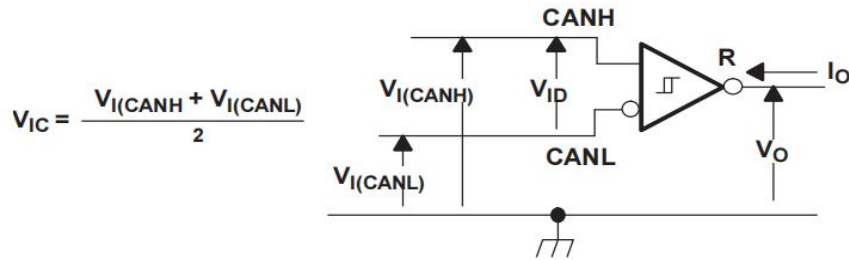
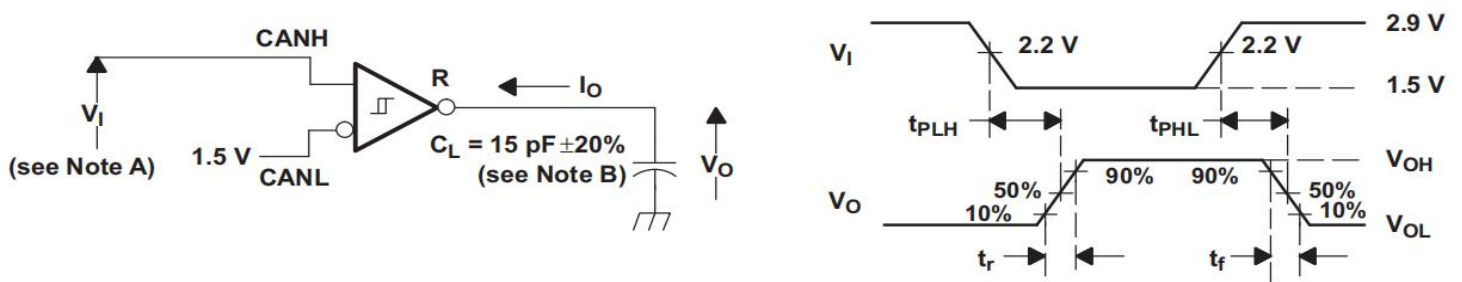


Figure 16. Receiver Voltage and Current Definitions

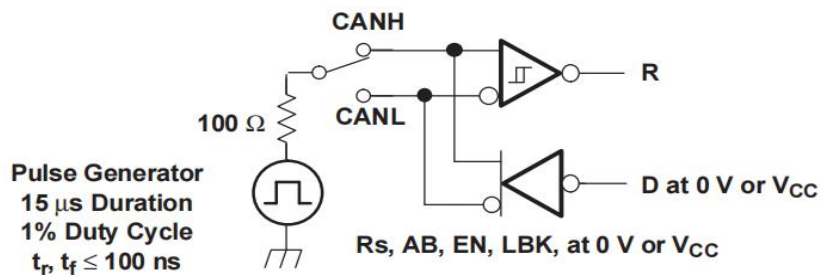


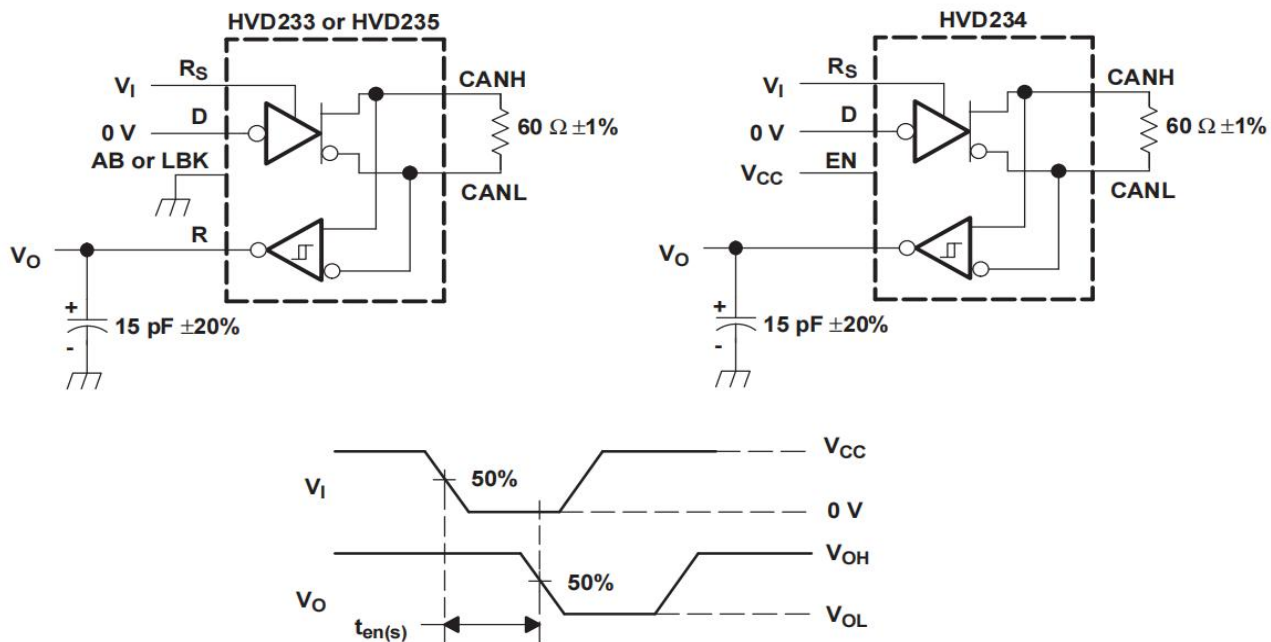
- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes fixture and instrumentation capacitance.

Figure 17. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

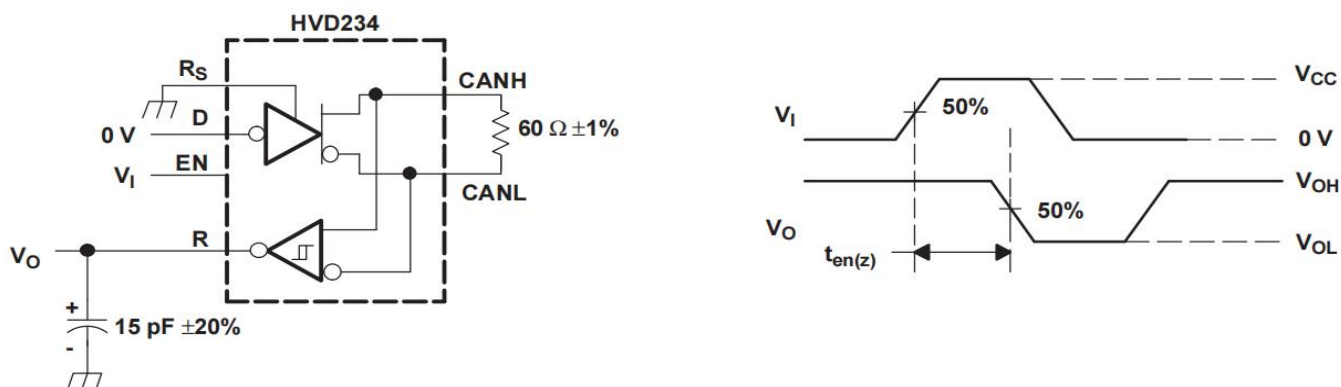
INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	R		$ V_{ID} $
-6.1 V	-7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
-1 V	-7 V	L		6 V
12 V	6 V	L		6 V
-6.5 V	-7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
-7 V	-1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X





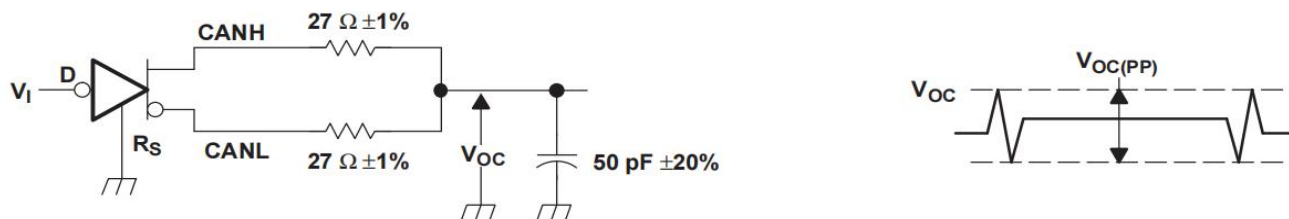
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 19. $T_{en(s)}$ Test Circuit and Voltage Waveforms



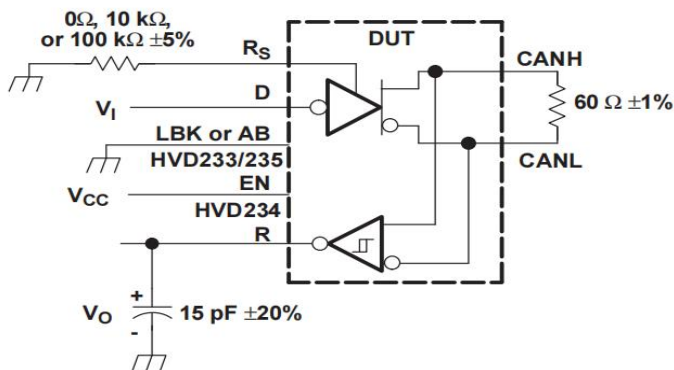
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 50 kHz, 50% duty cycle.

Figure 20. $T_{en(z)}$ Test Circuit and Voltage Waveforms



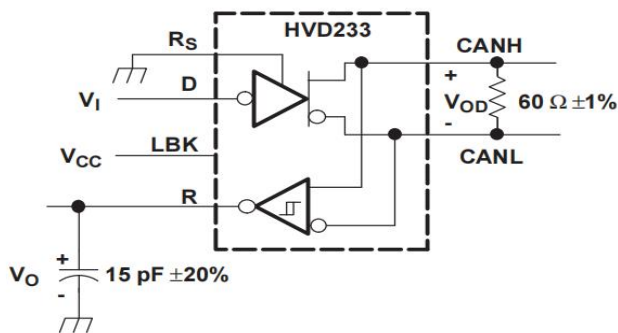
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 21. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms



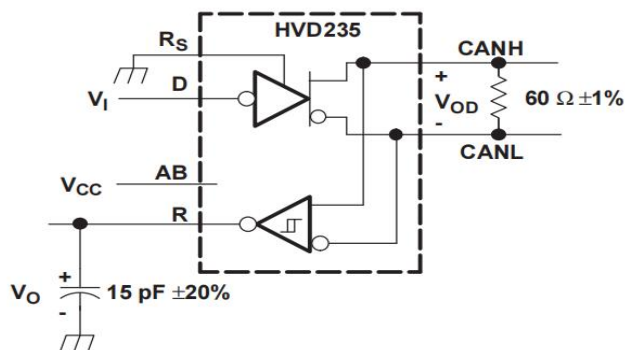
NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
 t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 22. $T_{(loop)}$ Test Circuit and Voltage Waveforms



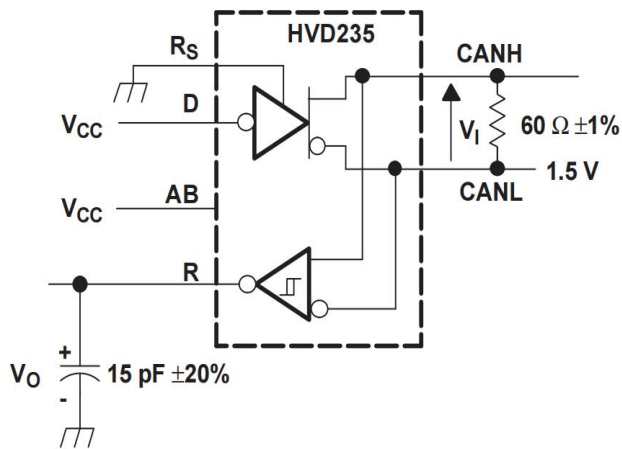
NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
 t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 23. $T_{(LBK)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
 t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 24. $T_{(AB1)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
 t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 25. $T_{(AB2)}$ Test Circuit and Voltage Waveforms

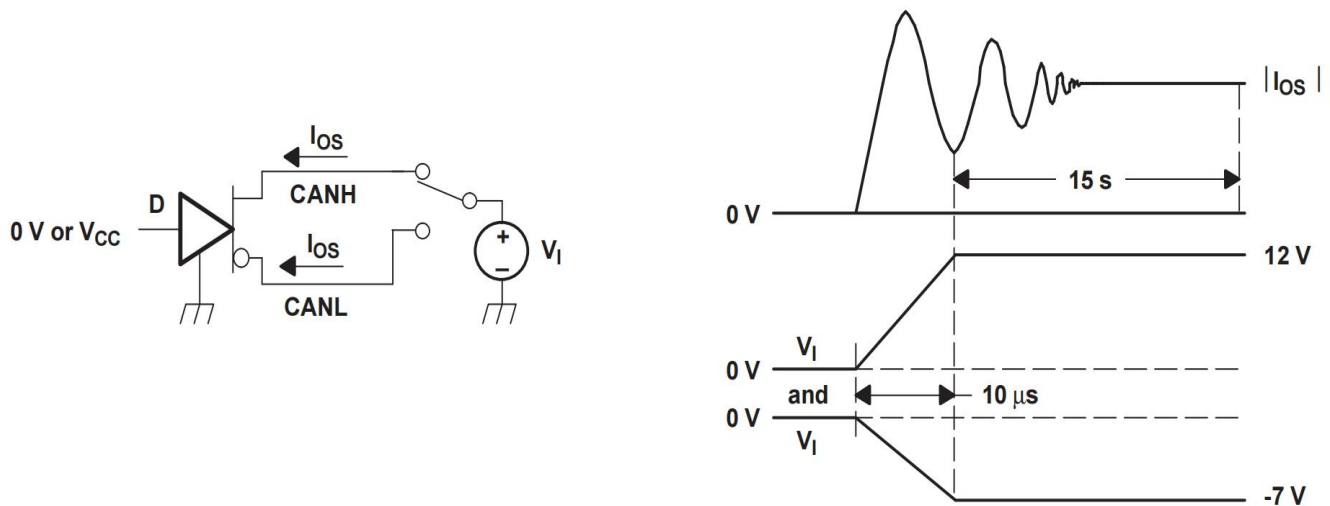
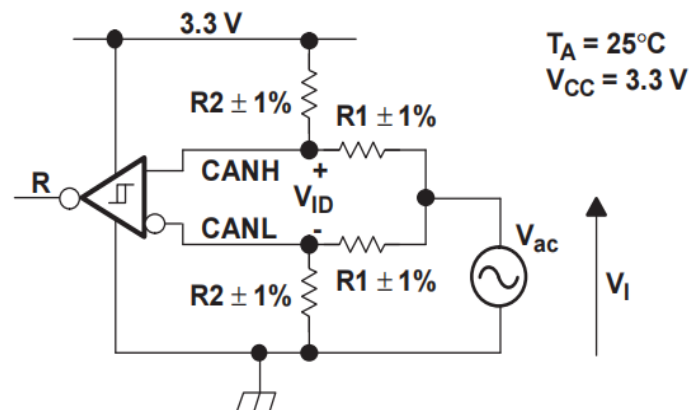


Figure 26. I_{OS} Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω



NOTE: All input pulses are supplied by a generator with $f \leq 1.5$ MHz.

Figure 27. Common-Mode Voltage Rejection

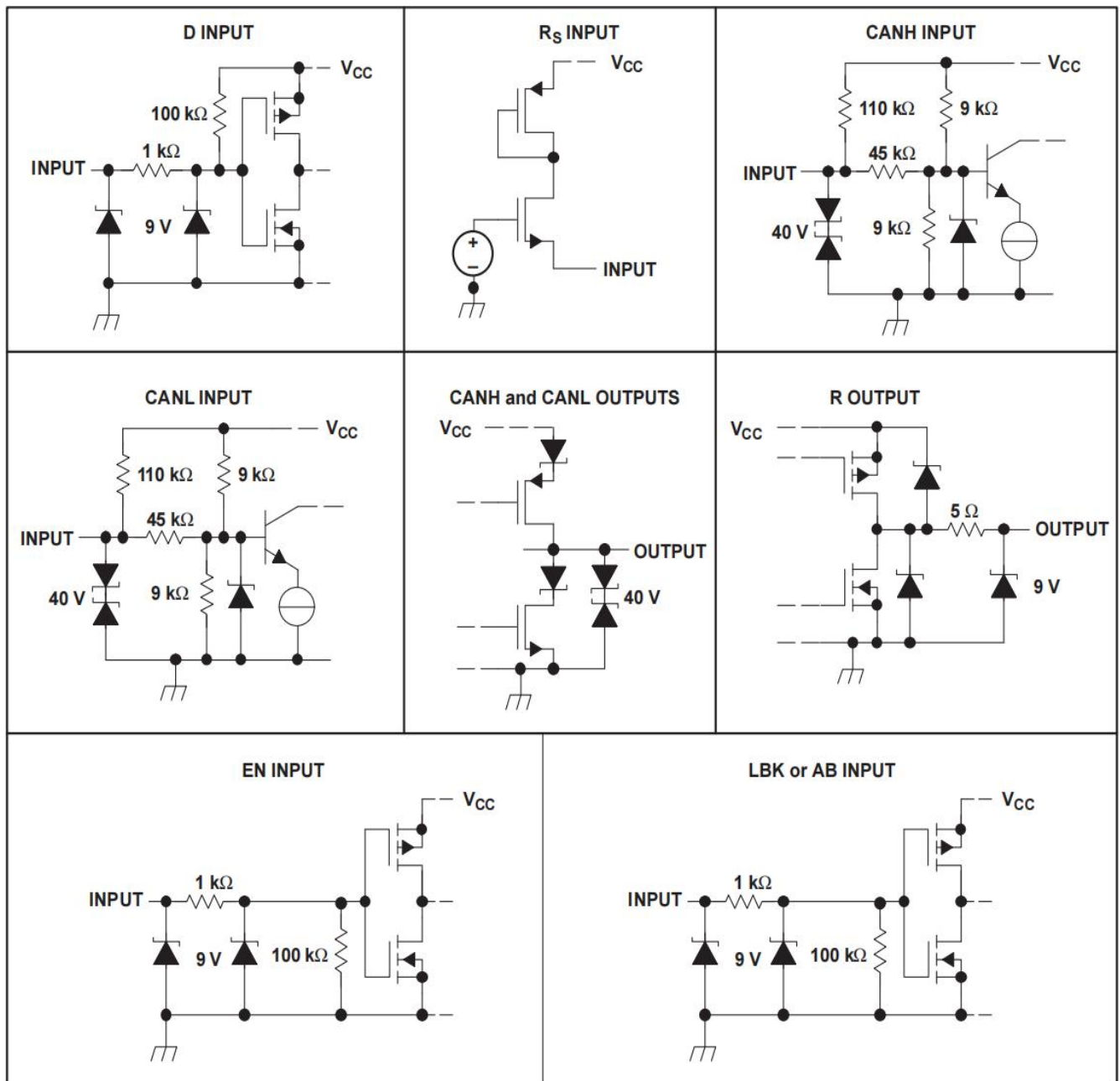


Figure 28. Equivalent Input and Output Schematic Diagrams



10 Detailed Description

10.1 Overview

This family of CAN transceivers is compatible with the ISO11898-2 High-Speed CAN (controller area network) physical layer standard. They are designed to interface between the differential bus lines in CAN and the CAN protocol controller at data rates up to 1 Mbps.

10.2 Functional Block Diagrams

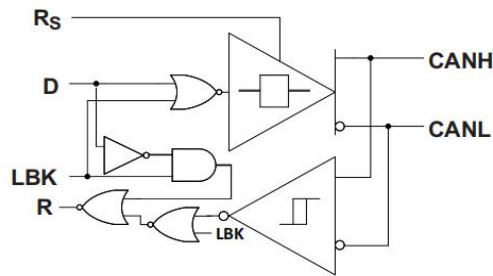


Figure 29. SN65HVD33 Functional Block Diagram

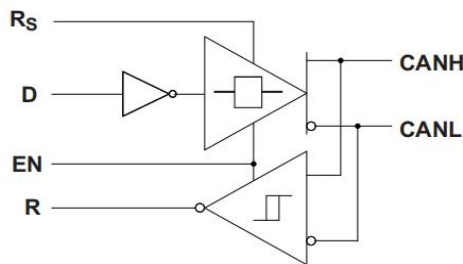


Figure 30. SN65HVD34 Functional Block Diagram

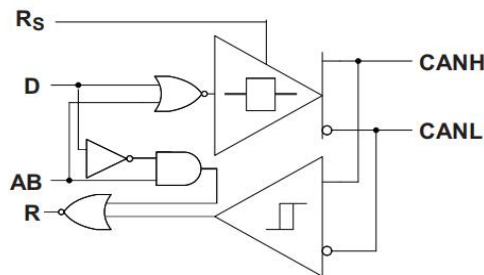


Figure 31. SN65HVD35 Functional Block Diagram

10.3 Feature Description

10.3.1 Diagnostic Loopback (SN65HVD233)

The diagnostic loopback or internal loopback function of the SN65HVD233 is enabled with a high-level input on pin 5, LBK. This mode disables the driver output while keeping the bus pins biased to the recessive state. This mode also redirects the D data input (transmit data) through logic to the received data output pin), thus creating an internal loopback of the transmit to receive data path. This mimics the loopback that occurs normally with a CAN transceiver because the receiver loops back the driven output to the R (receive data) pin. This mode allows the host protocol controller to input and read back a bit sequence or CAN messages to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in [Figure 36](#).



Feature Description (continued)

If the LBK pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.3.2 Autobaud Loopback (SN65HVD235)

The autobaud loopback mode of the SN65HVD235 is enabled by placing a high level input on pin 5, AB. In autobaud mode, the driver output is disabled, thus blocking the D pin to bus path and the bus transmit function of the transceiver. The bus pins remain biased to recessive. The receiver to R pin path or the bus receive function of the device remains operational, allowing bus activity to be monitored. In addition, the autobaud mode adds an internal logic loopback path from the D pin to R pin so the local node may transmit to itself in sync with bus traffic while not disturbing messages on the bus. Thus if the local node's CAN controller generates an error frame, it is not transmitted to the bus, but is detected only by the local CAN controller. This is especially helpful to determine if the local node is set to the same baud rate as the network, and if not adjust it to the network baud rate (autobaud detection).

Autobaud detection is best suited to applications that have a known selection of baud rates. For example, a popular industrial application has optional settings of 125 kbps, 250 kbps, or 500 kbps. Once the SN65HVD235 is placed into autobaud loopback mode the application software could assume the first baud rate of 125 kbps. It then waits for a message to be transmitted by another node on the bus. If the wrong baud rate has been selected, an error message is generated by the local CAN controller because the sample times will not be at the correct time. However, because the bus-transmit function of the device has been disabled, no other nodes receive the error frame generated by this node's local CAN controller.

The application would then make use of the status register indications of the local CAN controller for message received and error warning status to determine if the set baud rate is correct or not. The warning status indicates that the CAN controller error counters have been incremented. A message received status indicates that a good message has been received. If an error is generated, the application would then set the CAN controller with the next possibly valid baud rate, and wait to receive another message. This pattern is repeated until an error free message has been received, thus the correct baud rate has been selected. At this point the application would place the SN65HVD235 in a normal transmitting mode by setting pin 5 to a low-level, thus enabling bus-transmit and bus-receive functions to normal operating states for the transceiver.

If the AB pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.3.3 Slope Control

The rise and fall slope of the SN65HVD233, SN65HVD234, and SN65HVD235 driver output can be adjusted by connecting a resistor from the Rs (pin 8) to ground (GND), or to a low-level input voltage as shown in [Figure 32](#).

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 k Ω to achieve a ~ 15 V/ μ s slew rate, and up to 100 k Ω to achieve a ~ 2.0 V/ μ s slew rate. A typical slew rate versus pulldown resistance graph is shown in [Figure 33](#). Typical driver output waveforms with slope control are displayed in [Figure 39](#).

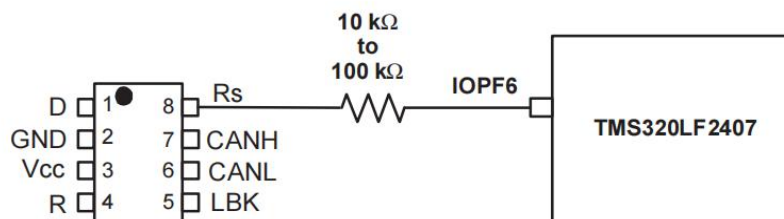


Figure 32. Slope Control/Standby Connection to a DSP



Table 2. Driver (SN65HVD233 or SN65HVD235)

INPUTS			OUTPUTS		
D	LBK/AB	R_s	CANH	CANL	BUS STATE
X	X	$> 0.75 V_{CC}$	Z	Z	Recessive
L	L or open	$\leq 0.33 V_{CC}$	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	$\leq 0.33 V_{CC}$	Z	Z	Recessive

Table 4. Receiver (SN65HVD235)⁽¹⁾

INPUTS				OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	AB	D	R
Dominant	$V_{ID} \geq 0.9 V$	L or open	X	L
Recessive	$V_{ID} \leq 0.5 V$ or open	L or open	H or open	H
?	$0.5 V < V_{ID} < 0.9 V$	L or open	H or open	?
Dominant	$V_{ID} \geq 0.9 V$	H	X	L
Recessive	$V_{ID} \leq 0.5 V$ or open	H	H	H
Recessive	$V_{ID} \leq 0.5 V$ or open	H	L	L
?	$0.5 V < V_{ID} < 0.9 V$	H	L	L

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

Table 5. Driver (SN65HVD234)

INPUTS			OUTPUTS		
D	EN	R_s	CANH	CANL	BUS STATE
L	H	$\leq 0.33 V_{CC}$	H	L	Dominant
H	X	$\leq 0.33 V_{CC}$	Z	Z	Recessive
Open	X	X	Z	Z	Recessive
X	X	$> 0.75 V_{CC}$	Z	Z	Recessive
X	L or open	X	Z	Z	Recessive

Table 6. Receiver (SN65HVD234)⁽¹⁾

INPUTS			OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	EN	R
Dominant	$V_{ID} \geq 0.9 V$	H	L
Recessive	$V_{ID} \leq 0.5 V$ or open	H	H
?	$0.5 V < V_{ID} < 0.9 V$	H	?
X	X	L or open	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate



11.1 Application Information

The CAN bus has two states during powered operation of the device; *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to $V_{CC} / 2$ via the high-resistance internal resistors R_{IN} and R_{ID} of the receiver, corresponding to a logic high on the D and R pins. See [Figure 34](#) and [Figure 35](#).

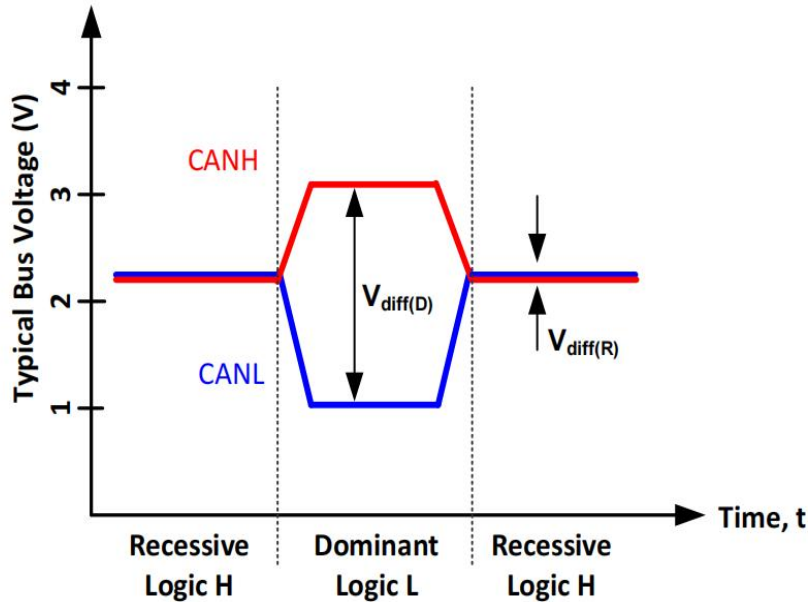


Figure 34. Bus States (Physical Bit Representation)

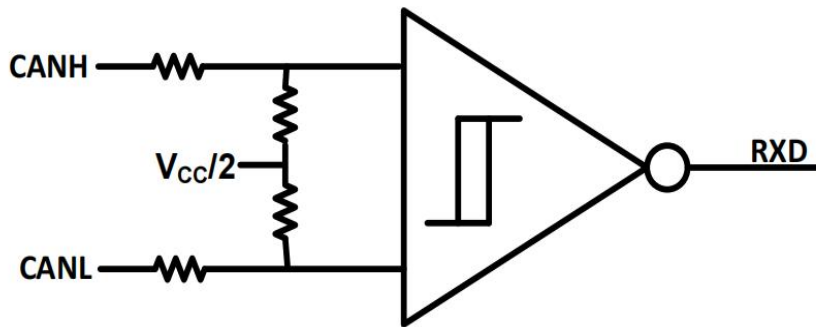


Figure 35. Simplified Recessive Common Mode Bias and Receiver

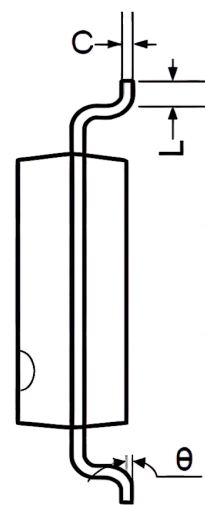
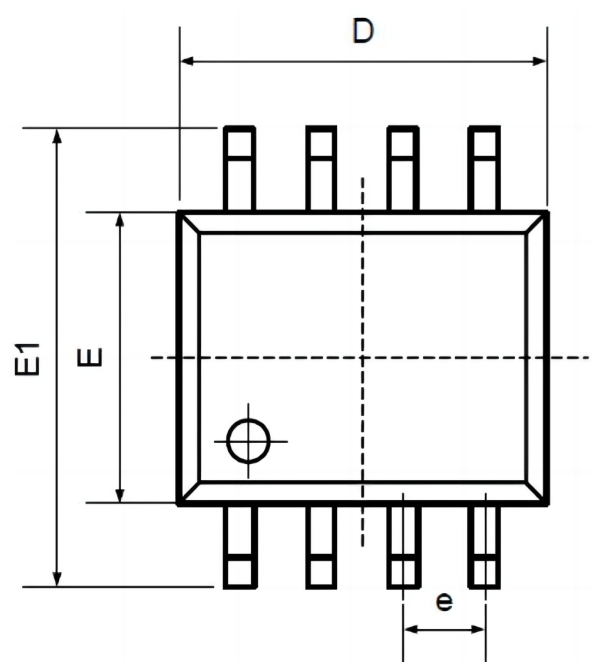
These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120- Ω characteristic impedance twisted-pair cable with termination on both ends of the bus.



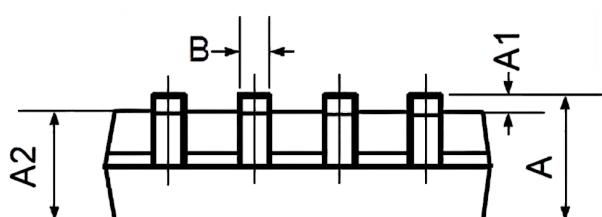
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD234DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD234DR
SN65HVD235DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD235DR

Package SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°





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