8V Fast Startup With F0 Detect And Tracking LRA Haptic Driver

Features

- 1MHz I2C Bus
- 4-KByte Memory
- 8k/12k/24k/48k input wave sampling rate
- F0 detect and tracking
- Advance autobrake engine integrated
- Playback mode:
  - Real time playback(Up to 4KByte FIFO)
  - Auto dynamic sine playback
  - Memory playback
  - 3 Trigger playback
  - One wire playback
  - Cont playback
  - I2S/TDM playback
- Resistance-Based LRA Diagnostics
- Drive signal monitor for LRA protect
- Drive Compensation Over Battery Discharge
- Fast Start Up Time ＜1ms
- Charge pump output voltage up to 8V
- Po=2W@Vbat=4.2V THD 1%
- Support automatically switch to standby mode
- Standby current：3.3μA @Vbat=4.2V
- Shutdown current：0.1μA
- Supply voltage range 2.7 to 5.5V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage, Battery Protection
- AW86727AFCR and AW86728ACSR include immersion IP license for mobile phones and wearables

Applications

- Mobile phones
- Tablets
- Wearable Devices

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General Description

AW8672X is a high voltage H-bridge, single chip LRA haptic driver, with F0 detecting and tracking based on BEMF, with a charge pump up to 8V drive voltage inside, supporting real time playback, auto dynamic sine playback, memory playback, cont playback, one wire playback, I2S/TDM playback and hardware pin trigged playback. A typical startup time of 1ms makes the AW8672X an ideal haptic driver for fast responses.

AW8672X integrates a 4KByte SRAM for user-defined waveforms to achieve a variety of vibration experiences, supporting 4 sampling rate (8k/12k/24k/48k) of waveforms loaded in SRAM, supporting output waveform sampling rate up-sampling to 48k.

AW8672X integrates an autobrake engine to suppress the aftershocks to zero for different drive waveforms(short or long) on different LRA motors.

AW8672X supports LRA fault diagnostic based on resistance measurement and protections of short-circuit, over-temperature and under-voltage.

AW8672X integrates a high-efficiency charge pump as the H-Bridge driver supply rail. The output voltage, maximum current limit and maximum charge pump current are configurable.

AW8672X features configurable automatically switch to standby mode after haptic waveform playback finished. This can less quiescent power consumption. The RSTN pin provides further power saving by fully shut down the whole device. Dedicated interrupt output pin can detect real time FIFO status and the error status of the chip.

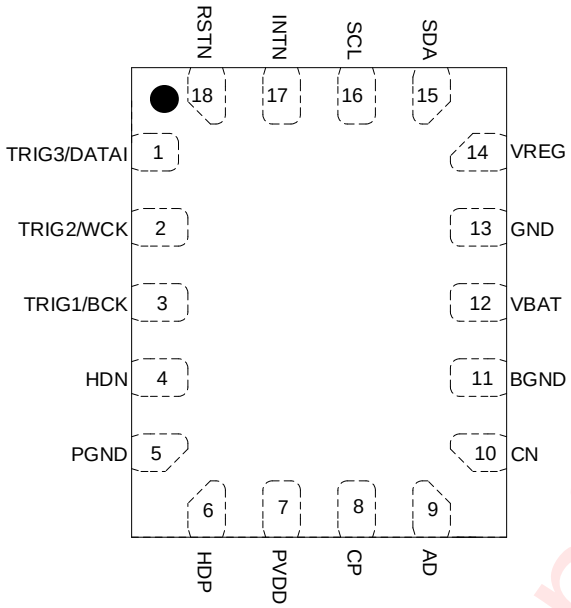
AW8672X features general settings are communicated via an I2C-bus interface and its I2C address is configurable.

Device Information

Device Name	Package	Body Size
AW86727FCR AW86727AFCR	FCQFN	2.5mm X 2mm X 0.55mm-18L
AW86728CSR AW86728ACSR	WLCSP	2.213mm X 1.733mm X0.566mm-20B

Pin Configuration And Top Mark(NOTE 1)

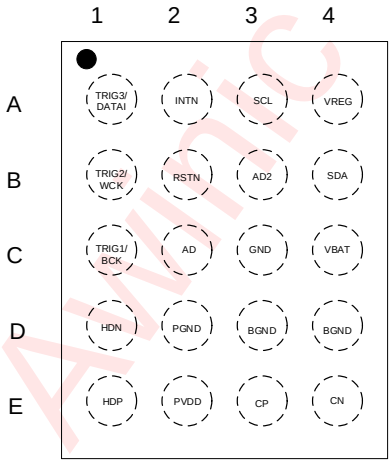
AW86727FCR
(Top View)



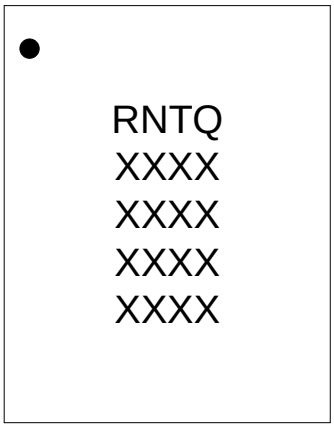
AW86727FCR Marking
(Top View)

KE43-AW86727FCR
XXXX-Production Tracing Code

AW86728CSR
(Top View)



AW86728CSR Marking
(Top View)



RNTQ-AW86728CSR
XXXX/XXXX/XXXX/XXXX
-Production Tracing Code

Figure 1 Pin Configuration and Top Mark

NOTE1：AW86727AFCR's pin configuration and top mark is same as AW86727FCR's
AW86728ACSR's pin configuration and top mark is same as AW86728CSR's

Pin Definition

Pin number		NAME	I/O	DESCRIPTION
AW86727	AW86728			
1	A1	TRIG3/DATAI	I	Hardware trigger 3 or DATAI in I2S mode.
2	B1	TRIG2/WCK	I	Hardware trigger 2 or WCK in I2S mode.
3	C1	TRIG1/BCK	I/O	Hardware trigger 1 or BCK in I2S mode.
4	D1	HDN	O	Negative haptic driver differential output.
5	D2	PGND	Ground	H-bridge driver GND.
6	E1	HDP	O	Positive haptic driver differential output.
7	E2	PVDD	Power	High voltage driver power rail output.
8	E3	CP	O	Capacitance of charge pump.
9	C2	AD	I	I2C bus address selection.
10	E4	CN	O	Capacitance of charge pump.
11	D3/D4	BGND	Ground	Charge pump GND.
12	C4	VBAT	Power	Chip power supply.
13	C3	GND	Ground	Supply ground.
14	A4	VREG	Power	Digital power supply output.
15	B4	SDA	IO	I2C bus data input/output, open drain.
16	A3	SCL	I	I2C bus clock input.
17	A2	INTN	O	Interrupt open drain output, low active.
18	B2	RSTN	I	Active low hardware reset. High: standby/active mode Low: power-down mode
/	B3	AD2	I	I2C bus address selection.

Functional Block Diagram

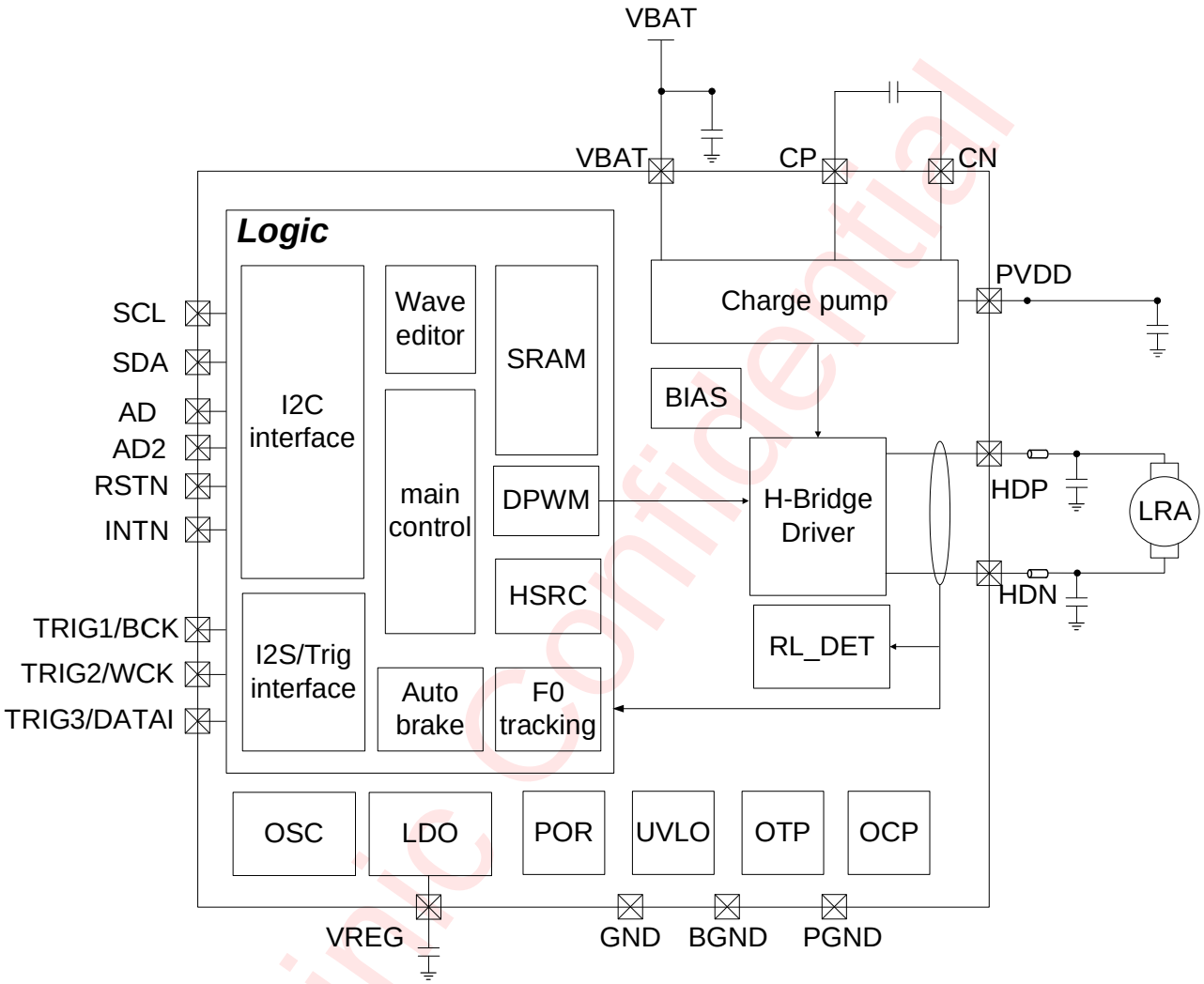


Figure 2 FUNCTIONAL BLOCK DIAGRAM

Typical Application Circuits

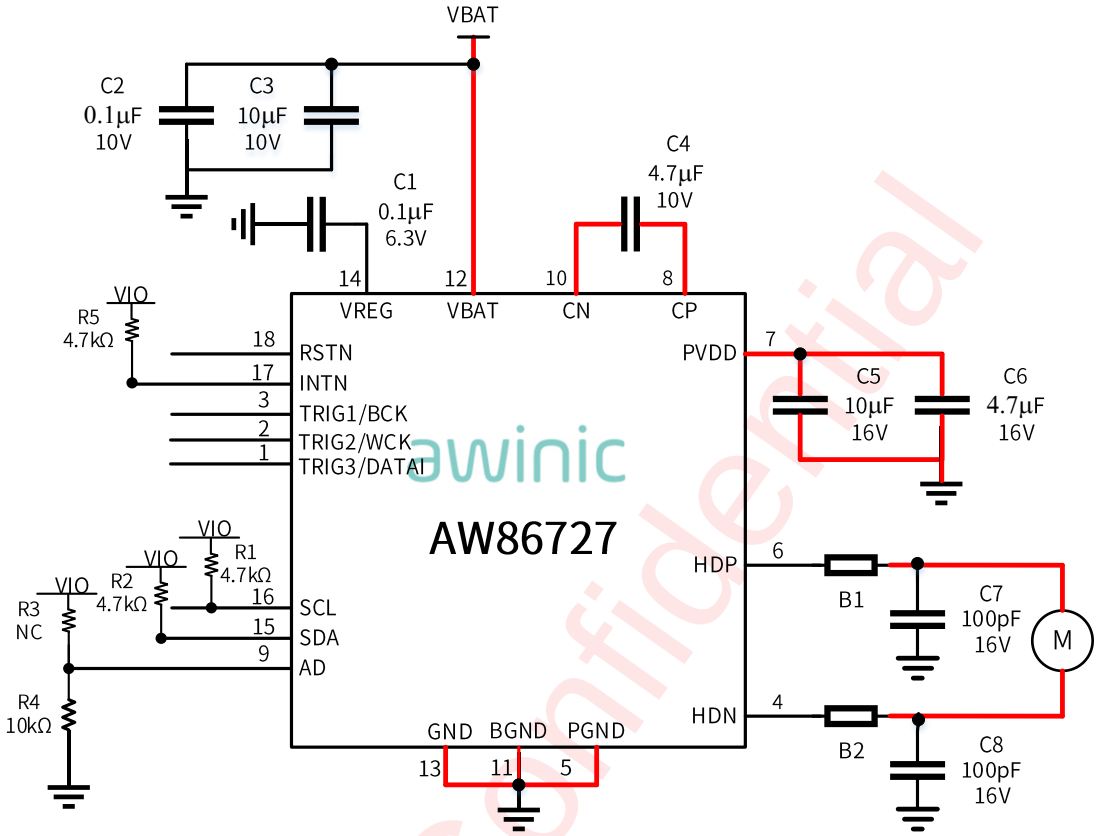


Figure 3 Typical Application Circuit of AW86727

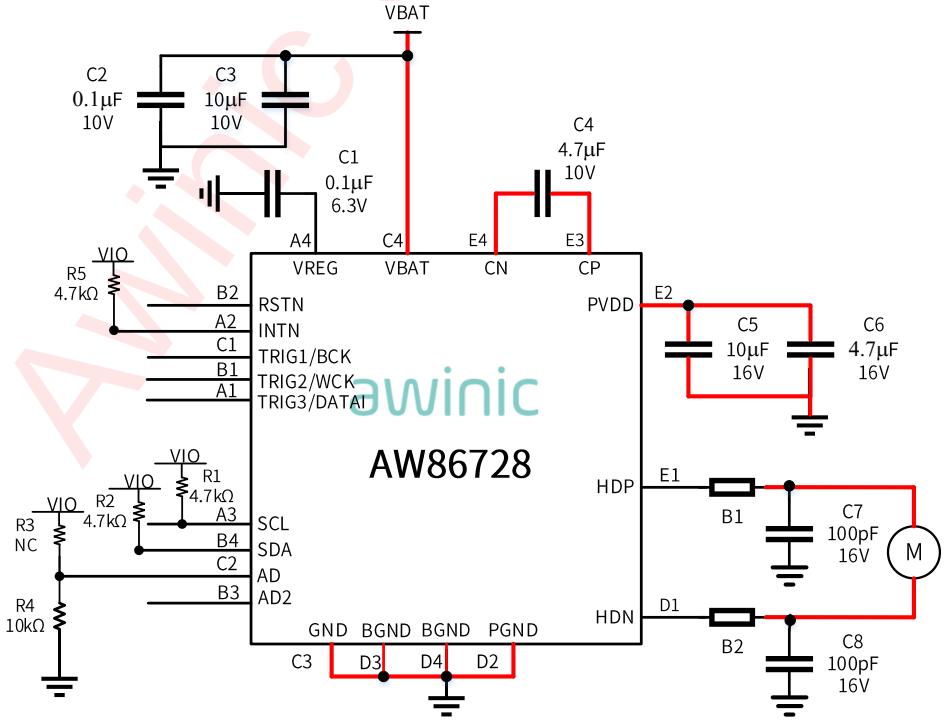


Figure 4 Typical Application Circuit of AW86728

Notice for Typical Application Circuits:

1: Please place C1，C2，C3，C4，C5，C6 as close to the chip as possible, and C5 and C6 close to the PVDD pin and the capacitors should be placed in the same layer with the AW8672X chip.

2: In order to prevent EMI problems, it is recommended to reserve bead B1/B2 (default 0Ω) and capacitor C7/C8 (default NC) at the output pin HDP/HDN, the value of C7/C8 can not exceed 100pF.

3: For the sake of driving capability, the connection lines of VBAT, CN, CP, PVDD, HDP, HDN, GND, BGND and PGND should be short and wide as possible.

4: VBAT, CN and CP traces according to 2A power line alignment rules; PVDD, HDP, HDN, BGND and PGND traces according to 1.5A power line alignment rules.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environment Information	Delivery Form
AW86727FCR	-40°C ~ 85°C	FCQFN 2.5mmX2mm-18L	KE43	MSL1	ROHS+HF	6000 units/ Tape and Reel
AW86727AFCR	-40°C ~ 85°C	FCQFN 2.5mmX2mm-18L	KE43	MSL1	ROHS+HF	6000 units/ Tape and Reel
AW86728CSR	-40°C ~ 85°C	WLCSP 1.733mmX2.213mm-20B	RNTQ	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW86728ACSR	-40°C ~ 85°C	WLCSP 1.733mmX2.213mm-20B	RNTQ	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE 2)

Parameter	Range
Battery Supply Voltage VBAT	-0.3V to 6.0V
Digital power supply VREG	-0.3V to 1.8V
Charge pump output voltage PVDD	-0.3V to 9.5V
CP,CN	-0.3V to PVDD+0.3V
HDP, HDN	-0.3V to PVDD+0.3V
TRIG2/TRIG3/SDA/SCL/AD/AD2	-0.3V to 6V
TRIG1/ INTN	-0.3V to VBAT+0.3V
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	150°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature(Soldering 10 Seconds)	260°C
ESD Rating (NOTE 3 4)	
HBM(Human Body Model)	±2KV
CDM(Charge Device Model)	±1.5KV
Latch-up	
Test Condition: JEDEC EIA/JESD78E	+IT: 200mA -IT: -200mA

NOTE 2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE 3：The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2017.

NOTE 4：Charge Device Model test method: ANSI/ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VBAT	Input voltage	2.7	4.2	5.5	V
C1	VREG capacitance	0.1	0.1	0.47	μF
C2	Input capacitance	0.1	0.1	10	μF
C3	Input capacitance	10	10	47	μF
C4	CP capacitance	4.7	4.7	10	μF
C5	Charge Pump output capacitance	4.7	10	10	μF
C6	Charge Pump output capacitance	4.7	4.7	10	μF
R1/R2/R5	Pull up resistor	1	4.7	10	kΩ

Thermal Information

PARAMETERS	AW86727	AW86728	UNIT
Junction-to-ambient thermal resistance θ_{JA}	72	66	°C/W
Junction-to-board characterization parameter Ψ_{JB}	12	15	°C/W
Junction-to-top-center characterization parameter Ψ_{JT}	3	2	°C/W

Electrical Characteristics

Characteristics

Test condition: TA=25°C，VBAT=4.2V，PVDD=8V，RL=8Ω+100μH(unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{BAT}	Battery supply voltage	In VBAT Pin	2.7		5.5	V
VREG	Voltage at VREG pin			1.5		V
V_{IL}	Logic input low level	RSTN/TRIG1/TRIG2/TRIG3/ AD/AD2/SCL/SDA			0.35	V
V_{IH}	Logic input high level	RSTN/TRIG1/TRIG2/TRIG3/ AD/AD2/SCL/SDA	0.8			V
V_{OL}	Logic output low level	INTN/SDA I_{OUT}=10mA			0.4	V
V_{OS}	Output offset voltage	I^2C signal input 0	-30	0	30	mV
I_{SD}	Shutdown current	RSTN =0V		0.1	1	μA
I_{STBY}	Standby current	AD=AD2= 0V TRIG1=TRIG2=TRIG3=0V RSTN=SCL=SDA=1.8V		3.3		μA
I_Q	Quiescent current	Bypass		3		mA
UVP	Under-voltage protection voltage	UVLO_ADJ=00		2.4		V
		UVLO_ADJ=01		2.5		
		UVLO_ADJ=10		2.6		
		UVLO_ADJ=11		2.7		
	Under-voltage protection hysteresis voltage		50	100	150	mV
T_{SD}	Over temperature protection threshold			150		°C
T_{SDR}	Over temperature protection recovery threshold			130		°C
T_{on1}	Time from shutdown to standby				4	ms
T_{on2}	Time from standby to active	From trigger to output signal			1	ms
Charge pump						
F_{CP}	Operating Frequency			1.6		MHz
T_{ST}	Soft-start time	No load, COUT=14.7μF		0.6		ms
HDRIVER						

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
RDSON	Drain-Source on-state resistance	Include H and L NMOS		500		mΩ
R_{OCP}	Load impedance threshold for over current protection	PVDD=8V		3.2		Ω
F_{PWM}	PWM output frequency	PD_HWM=0		96		kHz
		PD_HWM=1		48		kHz
$F_{CALI\_ACC\_LRA}$	LRA Consistency Calibration accuracy		F0-2	F0	F0+2	Hz
V_{PEAK}	Output voltage	RL=16Ω+100μH PVDD set 8V		7.6		V
	Output voltage	RL=8Ω+100μH PVDD set 8V		7.3		V

I2C Interface Timing

Parameter			fast mode			fast mode plus			UNIT
No.	Symbol	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.26			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			0.26			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			10			ns

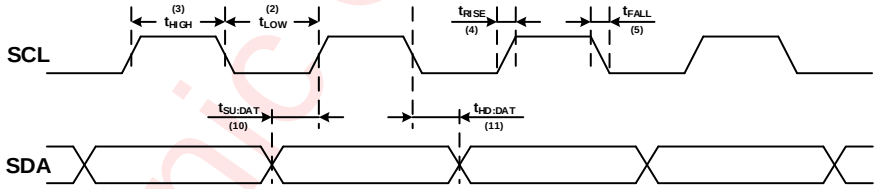


Figure 5 SCL and SDA timing relationships in the data transmission process

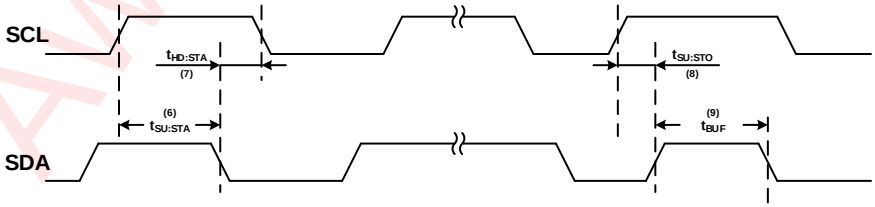


Figure 6 The timing relationship between START and STOP state

Digital Audio Interface Timing

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WCK	8		96	kHz
f_{bck}	Bit clock frequency, on pin BCK	32*fs		12.288M (NOTE4)	Hz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns

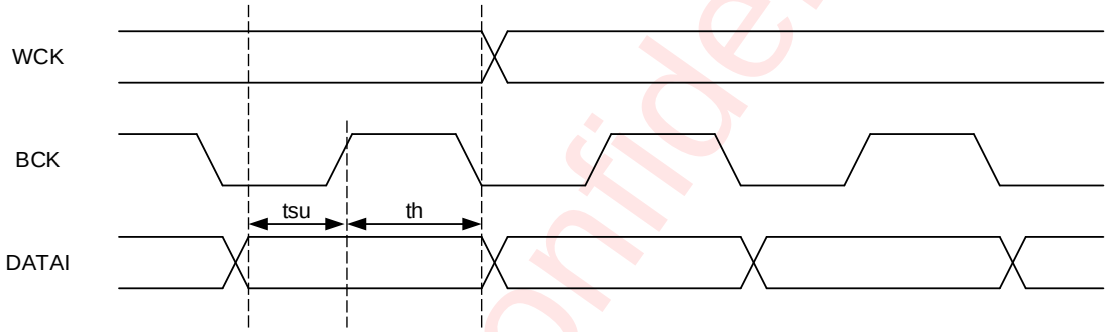


Figure 7 Digital Audio Interface Timing

NOTE4: *The digital audio interface supports up to 6/ 8 slots (32-bit) at a 8/12/16/24/48 kHz sample rate, and 1/2/4 slots (32-bit) at a 8/12/16/24/48/96 kHz sample rate.*

Measurement Setup

AW8672X features switching digital output, as shown in Figure 8. Need to connect a low pass filter to HDP/HDN output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

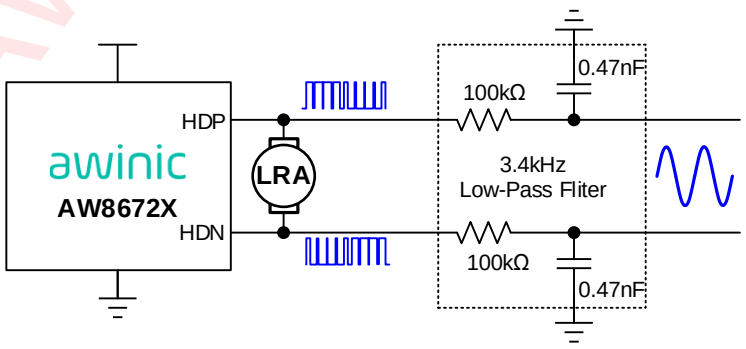


Figure 8 AW8672X test setup

Typical Characteristics:

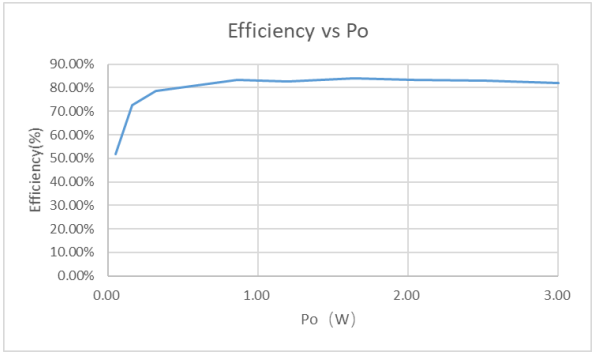


Figure 9 VBAT=4.2V@8ohm+100uH Efficiency vs Po

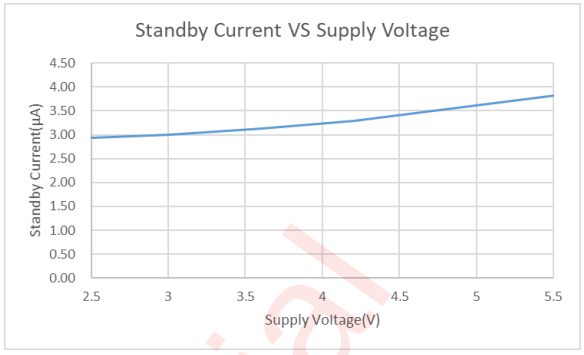


Figure 12 Standby current VS supply voltage

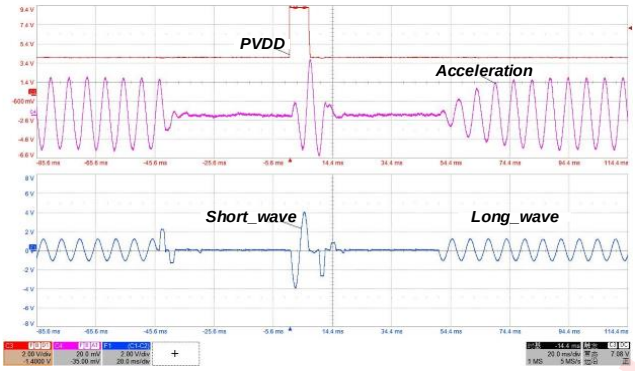


Figure 10 Long Vibration with Short Vibration inside

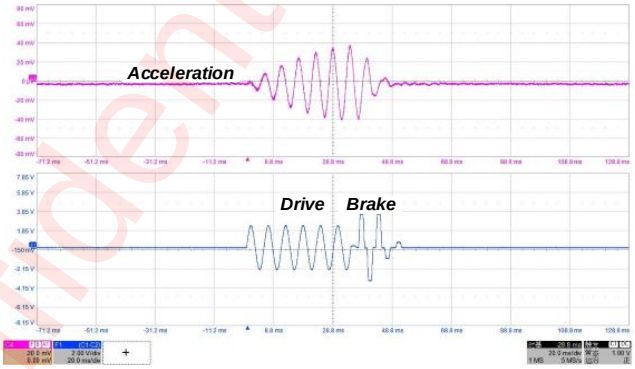


Figure 13 LRA with Automatic Braking

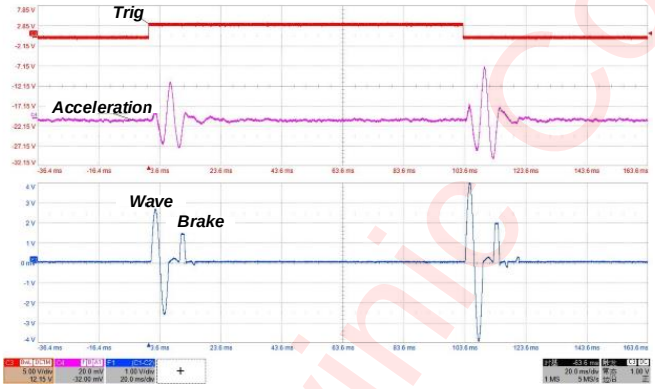


Figure 11 Trig Application

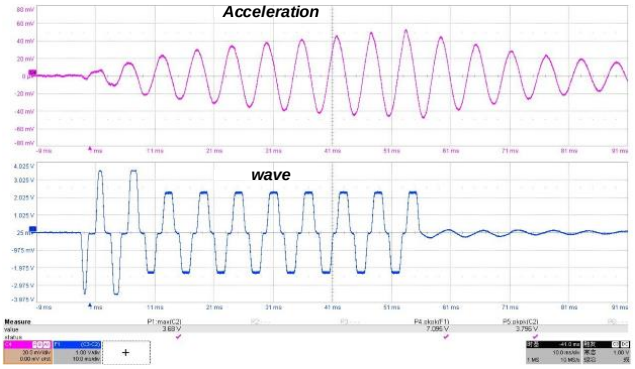


Figure 14 Automatic Resonance Tracking

Detailed Functional Description

Power On Reset

The device provides a power-on reset feature that is controlled by VREG OK. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers. When the VBAT power on, the VREG voltage raises and produce the OK indication, the reset is over.

Operation Mode

The device supports 3 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	VBAT = 0V or RSTN = 0V	Power supply is not ready or RSTN is tie to low. Whole chip shutdown including I²C interface.
Standby	VBAT > 2.7V and RSTN = HIGH and no wave is going	Power supply is ready and RSTN is tie to high. Most parts of the device are power down for low power consumption except I²C interface and LDO.
Active	Playing a waveform	Most parts of the device are working

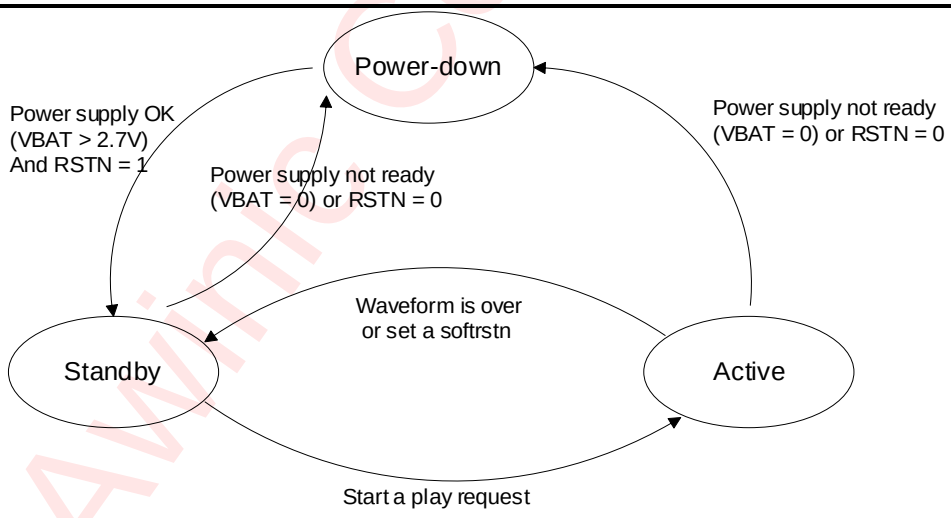


Figure 15 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when the supply voltage is not ready or RSTN pin is set to low.
In this mode, all circuits inside this device will be shut down. I²C interface isn't accessible in this mode, and all of the internal configurable registers and Memory are cleared.
The device will jump out of the power-down mode automatically when the supply voltages are OK and RSTN pin is set to high.

Standby Mode

The device switches standby mode when the power supply voltages are OK and RSTN pin set to high. In this mode I²C interface is accessible, other modules except LDO module are still powered down. Also in this mode, customer can initialize waveform library in SRAM. Device will be switched to this mode after haptic waveform playback finished.

Active Mode

The device is fully operational in this mode. Charge pump and H-bridge driver circuits will start to work. Users can send a playback request to make device in this mode.

Power On And Power Down Sequence

This device power on and power down sequence is illustrated in the following figure:

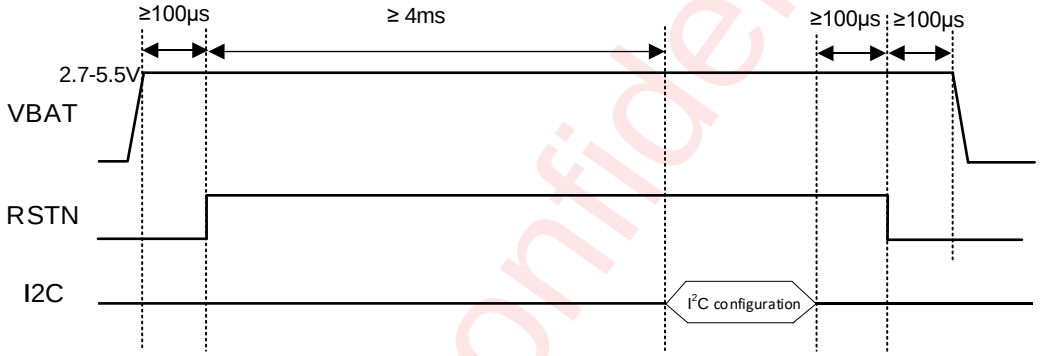


Figure 16 Power On and Power Down Sequence

Playback Sequence

Make sure the device is not in POWER-DOWN MODE before sending a playback request, then the playback sequence is illustrated in the following figure:

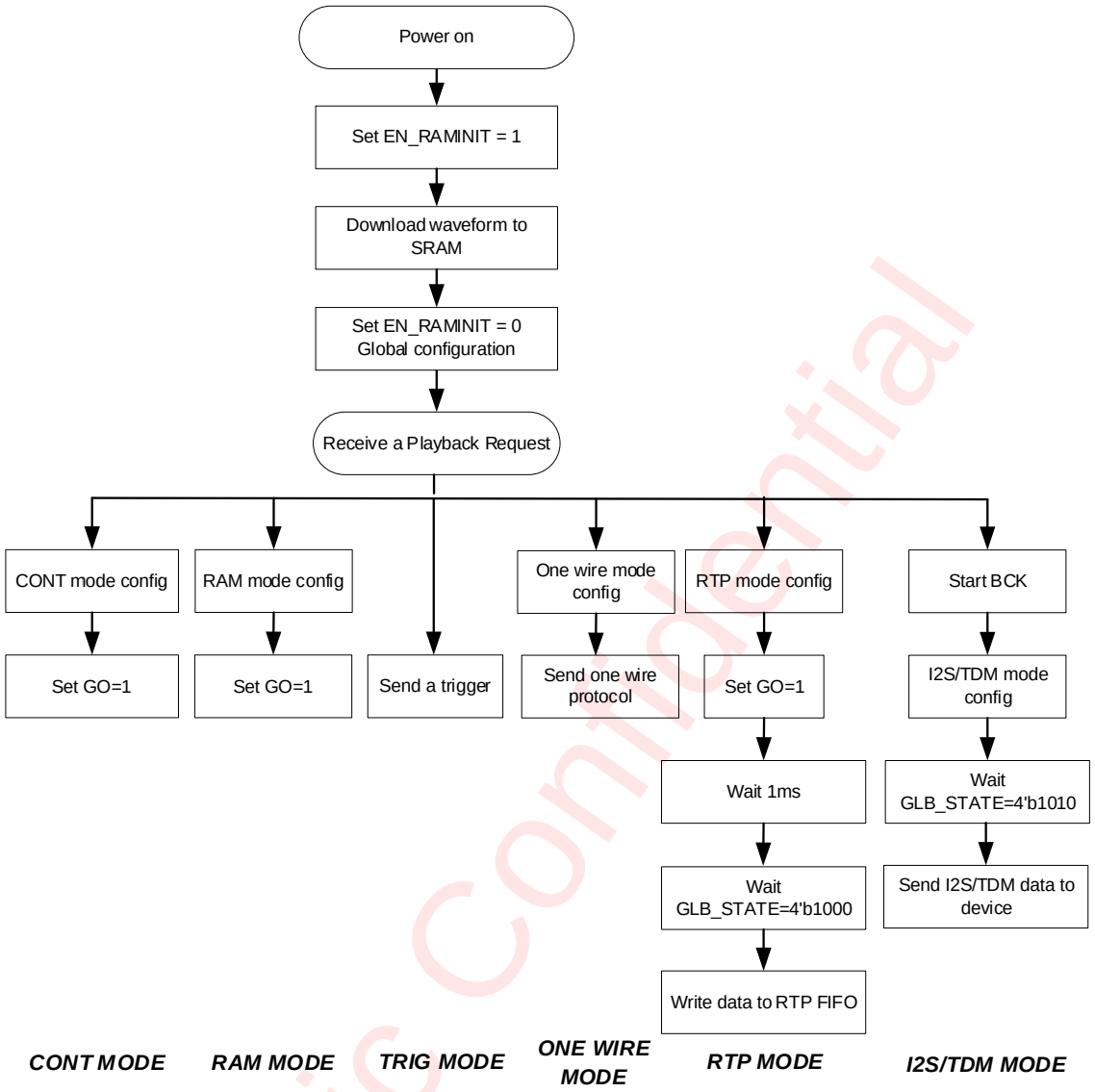


Figure 17 Power on and playback sequence

Software Reset

Writing 0xAA to register SOFTRST(0x00) via I²C interface will reset the device internal circuits except SRAM, including configuration registers.

Battery Voltage Detect

Software can send command to detect the battery voltage.

Detect steps:

- Set EN_RAMINIT to 1 in register 0x45;
- Set DET_SEQ0 to 0 in register 0x4e;
- Set DET_GO to 1 in register 0x4d;
- Wait 3ms;
- Set DET_GO to 0 in register 0x4d;

- Set EN_RAMINIT to 0 in register 0x45;
- Read AVG_DATA_H in register 0x4f and AVG_DATA_L in register 0x50. Code= AVG_DATA_H*256+ AVG_DATA_L.

The code is a 10bit unsigned number.

$$VBAT = \frac{6.1 \times code}{1023}(V)$$

Constant Vibration Strength

The device features power-supply feedback. If the supply voltage discharge over time, the vibration strength remains the same as long as enough supply voltage is available to sustain the required output voltage. It is especially useful for ringtone application. Power-supply feedback works in all playback mode.

Use steps:

- Set VBAT_REF in register 0x4d;
- Set VBAT_MODE to 1 in register 0x4c;
- Initiates a playback request.

LRA Consistency Calibration

Different motor batches, assembly conditions and other factors can result in f0 deviation of LRA. When the drive waveform does not match the LRA monomer, the vibration may be inconsistent and the braking effect becomes worse, especially for short vibration waveforms. So it's necessary to perform consistency calibration of LRA. Firstly the power-on f0 detection can be launched to get the f0 of LRA. Secondly the waveform frequency stored in SRAM and the f0 of LRA are used to calculate the code for calibration. The f0 accuracy after LRA consistency calibration is ±2Hz.

LRA Resistance Detect

Software can send command to detect the LRA's resistance.

Detect steps:

- Set EN_RAMINIT to 1 in register 0x45;
- Read D2S_GAIN register and save the result as d2s_gain_pre;
- Set DET_SEQ0 to 3 and set D2S_GAIN with an appropriate value in register 0x4e;
- Set DET_GO to 1 in register 0x4d;
- Wait 3ms;
- Set DET_GO to 0 in register 0x4d;
- Set EN_RAMINIT to 0 in register 0x45;
- Restore the value of D2S_GAIN register to d2s_gain_pre;
- Read AVG_DATA_H in register 0x4f and AVG_DATA_L in register 0x50. Code= AVG_DATA_H*256+ AVG_DATA_L.

Based on this code host can diagnosis used LRA's status. The code is a 10bit unsigned number.

$$RL = \frac{610 \times code}{1023 \times \mathrm{D2S\_GAIN}}(\Omega)$$

The values of the D2S_GAIN that can be configured for different sizes of RL are listed below. The higher the

RL, the smaller the configurable D2S_GAIN.

Table 2 D2S_GAIN Selection

RL(Ω)	D2S_GAIN
2~25	20
20~60	10

Flexible Haptic Data Playback

The device offers multiple ways to playback haptic effects data. The PLAY_MODE bits select RAM mode, RTP mode, CONT mode. Additional flexibility is provided by the three hardware TRIG pins, which can override PLAY_MODE bit to playback haptic effects data as configuration.

The device contains 8kB of integrated SRAM to store customer haptic waveforms' data. The whole SRAM is separated to RAM waveform library and RTP FIFO region by base address. And RAM waveform library is including waveform library version, waveform header and waveform data.

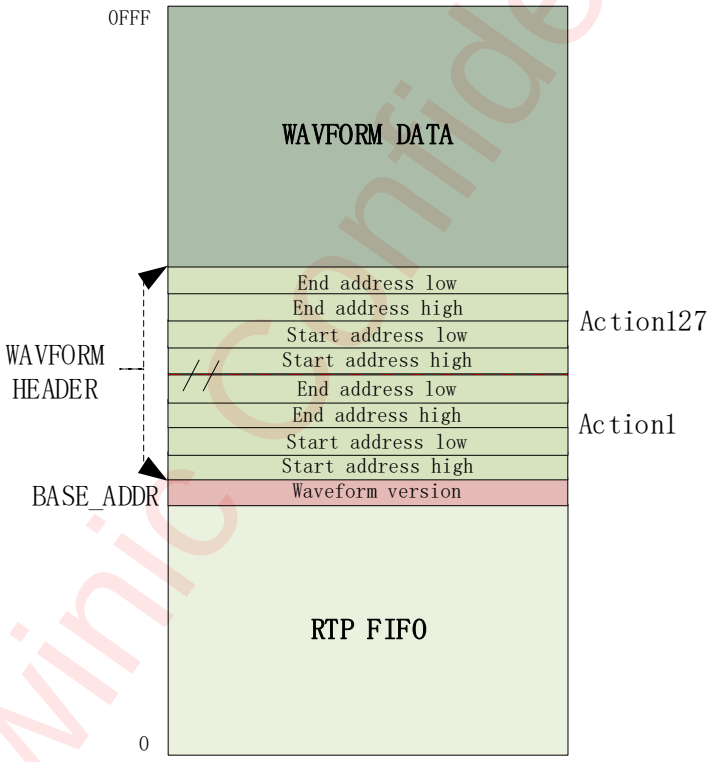


Figure 18 Data structure in SRAM

RAM mode and TRIG mode playback the waveforms in SRAM waveform library and RTP mode playback the waveform data written in RTP FIFO, CONT mode playback non-filtered or filtered square wave with rated drive voltage.

SRAM Structure

A SRAM waveform library consists of a waveform version byte, a waveform header section, and the waveform data content. The waveform header defines the data boundaries for each waveform ID in the data field, and the waveform data contains a signed data format (2's complement) to specify the magnitude of the drive.

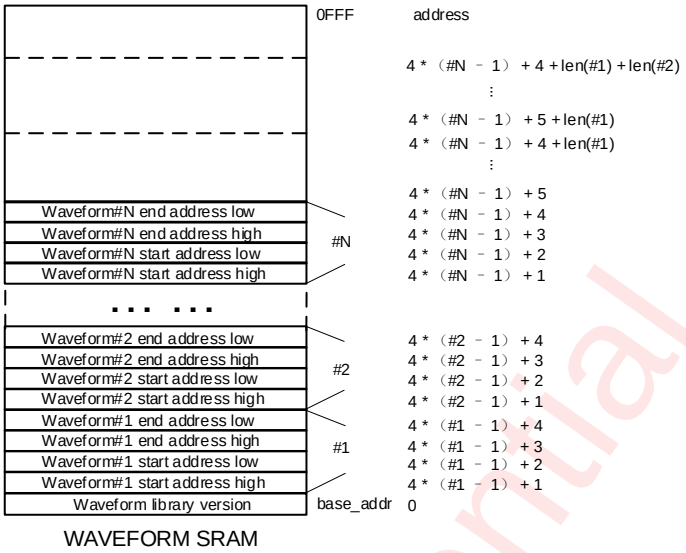


Figure 19 Waveform library data structure

Waveform version:

One byte located on SRAM base address, setting to different value to identify different version of RAM waveform library.

Waveform header:

The waveform header block consist of N-boundary definition blocks of 4 bytes each. N is the number of waveforms stored in the SRAM (N cannot exceed 127). Each of the boundary definition blocks contain the start address (2 bytes) and end address (2 bytes). So the total length of waveform header block are N*4 bytes.

The start address contains the location in the memory where the waveform data associated with this waveform begins.

The end address contains the location in the memory where the waveform data associated with this waveform ends.

The waveform ID is determined after base address is defined. Four bytes begins with the address next to base address are the first waveform ID's header, and next four bytes are the second waveform ID's header, and so on.

Waveform data:

The waveform data contains a signed data format (2's complement) to specify the magnitude of the drive. The begin address and end address is specified in waveform ID's header.

Waveform library initialization steps:

- Before waveform library initialization, make sure the chip is in STANDBY mode;
- Prepare waveform library data including: waveform library version, waveform header fields for waveform in library and waveform data of each waveform;
- Set register EN_RAMINIT=1 in register 0x45, open clock to enable SRAM initial;
- Delay 1ms;
- Set base address (register 0x2D, 0x2E);
- Set Ram address (register 0x40, 0x41);
- Write waveform library data into register 0x42 continually until all the waveform library data written;

- Set register EN_RAMINIT=0, close clock to disable SRAM initial.

Ram Mode

To playback haptic data with RAM mode, the waveform ID must first be configured into the waveform playback queue and then the waveform can be played by writing GO bit register.

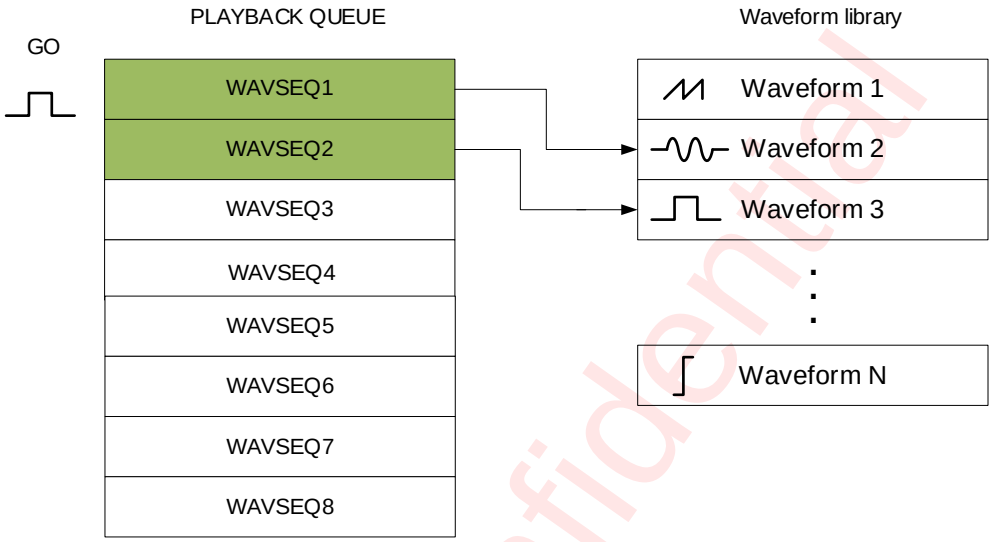


Figure 20 RAM mode playback

The waveform playback queue defines waveform IDs in waveform library for playback. Eight WAVSEQx registers queue up to eight library waveforms for sequential playback. A waveform ID is an integer value referring to the index of a waveform in the waveform library. Playback begins at WAVSEQ1 when the user triggers the waveform playback queue. When playback of that waveform ends, the waveform queue plays the next waveform ID held in WAVSEQ2 (if non-zero). The waveform queue continues in this way until the queue reaches an ID value of zero or until all eight IDs are played whichever comes first.

The waveform ID is a 7-bit number. The MSB of each ID register can be used to implement a delay between queue waveforms. When the SEQxWAIT is high, bits 6-0 indicate the length of the wait time. The wait time for that step then becomes WAVSEQ[6:0] × wait_time unit. Wait_time unit can be configuration of WAITSLOT register(in 0x16 register).

The device allows for looping of individual waveforms by using the SEQxLOOP registers. When used, the state machine will loop the particular waveform the number of times specified in the associated SEQxLOOP register before moving to the next waveform. The device allows for looping of the entire playback sequence by using the MAIN_LOOP register. The waveform-looping feature is useful for long, custom haptic playbacks, such as a haptic ringtone.

Playback steps:

- Waveform library must be initialized before playback;
- Set PLAY_MODE bits to 0 in register 0x08;
- Set playback queue registers (0x0A ~ 0x11) as desired;
- Set playback loop registers (0x12~ 0x16) as desired;
- Set GO bit to 1 in register 0x09 to trigger waveform playback;
- Device will be switched to STANDBY mode after haptic waveform playback finished.

Rtp Mode

The real-time playback mode is a simple, single 8-bit register interface that holds an amplitude value. When real-time playback is enabled, beginning to enters a register value to RTP_DATA over the I²C will trigger the playback, the value is played until the data sending finished or removes the device from RTP mode. The maximum FIFO space is 4Kbyte. During writing data to the RTP_DATA register, the I2C speed cannot be too low, see the table below for details.

Table 3 Minimum I2C speed

WAVDAT_MODE(0x46)	Sample rate of waveform	I2C speed
2'b11	8K	⩾150KHz
2'b10	12K	⩾250KHz
2'b00	24K	⩾400KHz
2'b01	48K	1MHz

After FF_AEM or FF_AFM register is set to 0, HOST can obtain the RTP FIFO almost empty or almost full status through interrupt signal(pin INTN) or read FF_AES or FF_AFS register. RTP FIFO almost empty and almost full threshold can be configured through FIFO_AE and FIFO_AF registers.

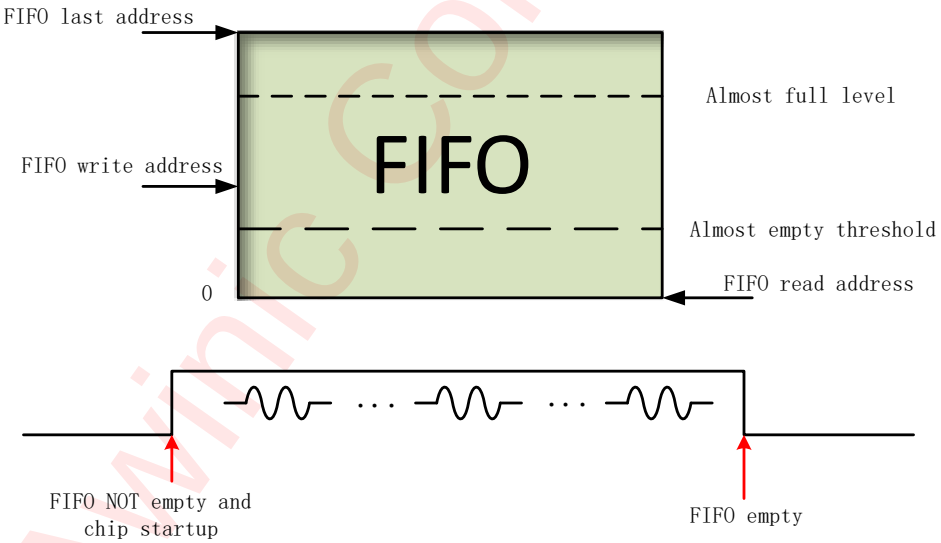


Figure 21 RTP mode playback

Playback steps:

- Prepare RTP data before playback;
- Set PLAY_MODE bit to 1 in register 0x08;
- Set GO bit to 1 in register 0x09 to trigger waveform playback;
- Delay 1ms.
- Check GLB_STATE=4'b1000，if HOST don't send data to FIFO, chip will wait for RTP data coming in this state forever;

- Write RTP data continually to register 0x32 to playback RTP waveform;
- HOST need monitor the almost full and almost empty status for RTP FIFO;
- Device will be switched to STANDBY mode after wave data in RTP FIFO is played empty.

Dual motor real-time playback mode

Dual motor real-time playback mode can control the simultaneous playback of two motors, so as to realize the tactile synergy of two motors. When this mode is enabled, beginning to enter register values to RTP_DATA register will trigger the playback until the data sending finished or removes the device from RTP mode.

During writing data to the RTP_DATA register in this mode, the I2C speed cannot be too low because of the maximum FIFO space is 4Kbyte. The table 4 is shown below for details.

Table 4 Minimum I2C speed

WAVDAT_MODE(0x46)	Sample rate of waveform	I2C speed
2'b11	8K	⩾250KHz
2'b10	12K	⩾500KHz
2'b00	24K	⩾1MHZ

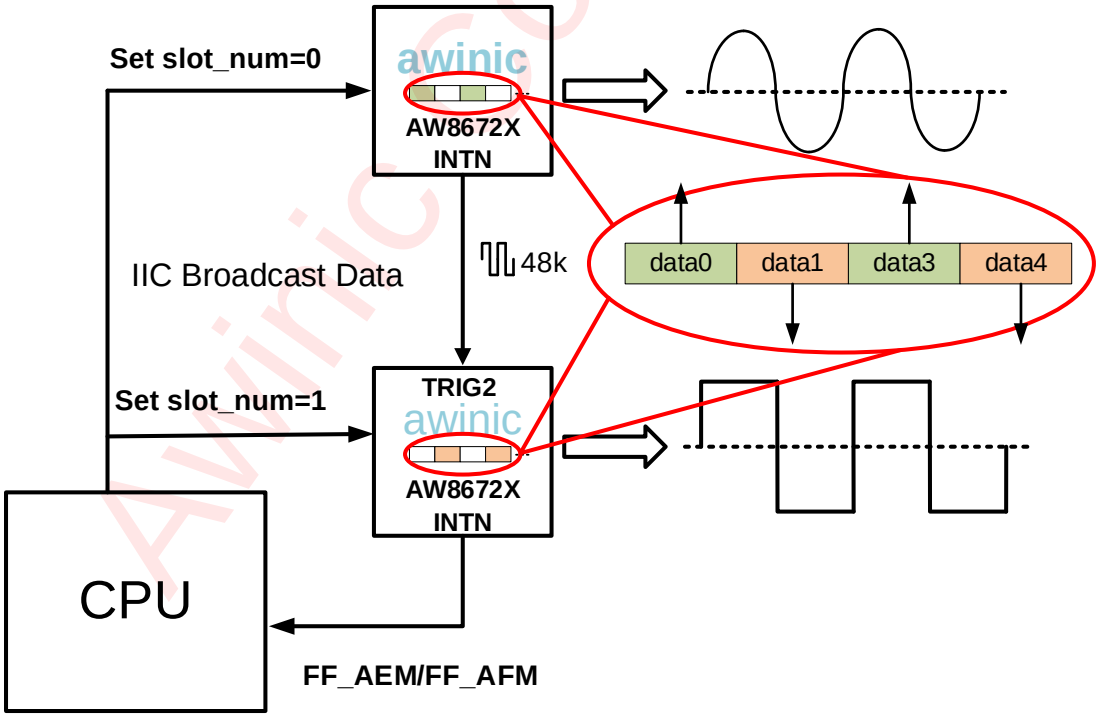


Figure 22 Dual motor real-time playback

Playback steps:

Left motor (0x5A) configuration:

- Set SLOT_CHSEL bit to 0 in register 0x45;

- Set EN_BRO_ADDR bit to 1 in register 0x47;
- Set BROADCAST_ADDR in register 0x47 such as 0x5c;
- Set EN_INTN_CLKOUT bit to 1 in register 0x44;

Right motor (0x5B) configuration:

- Set SLOT_CHSEL bit to 1 in register 0x45;
- Set EN_DLL bit to 1 in register 0x46;
- Set EN_BRO_ADDR bit to 1 in register 0x47;
- Set BROADCAST_ADDR in register 0x47 such as 0x5c;
- Set WCK_PIN bit to 1 in register 0x44;

Change to broadcast address(0x5C) :

- Set EN_TWORTP bit to 1 in register 0x2D;
- The other steps is same to rtp mode.

Auto Dynamic Sine Mode

Auto dynamic sine mode can generate full amplitude half period sine wave through 5 bytes and 10 bytes for a whole period. For the whole period sine wave, the first 5 bytes is same as the last five bytes. The 5 bytes are sinh,sinl,cosh,cosl,rtp_gain. Compared with rtp mode, Auto dynamic sine mode consumes less I2C resource to generate the same sine wave. The calculation formula of relevant parameters is as follow. The wav_frequency range from 60Hz to 300Hz. The sampling rate can be set to 48k or 96k by register 0x2D. All the result need round down.

Sinh=65536*sin(2*pi*wav_frequency/sampling rate)/256

sinl=65536*sin(2*pi*wav_frequency/sampling rate)%256

cosh=65536*cos(2*pi*wav_frequency/sampling rate)/256

cosl=65536*cos(2*pi*wav_frequency/sampling rate)%256

rtp_gain represent gain of the sine wave, it is better to set the rtp_gain<0x80,otherwise the waveform will be clipped.

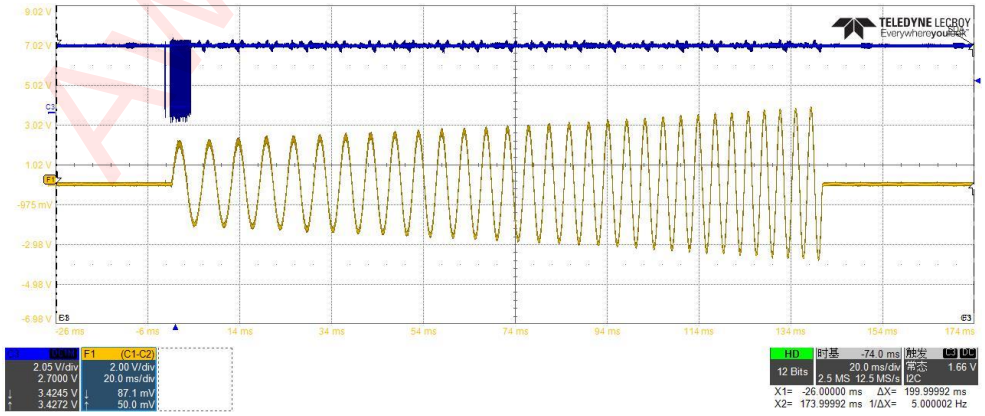


Figure 23 Auto Dynamic Sine mode playback

Playback steps:

- Set AUTO_DYNAMIC_SIN bit to 1 to enable auto dynamic sine mode;
- Prepare auto dynamic sine data before playback;
- The other steps is same with rtp mode.

Trig Mode

The device have three dedicated hardware pins for quickly trigger haptic data playback. Each pin can be configured pos-edge/neg-edge/both-edge/level trigger.

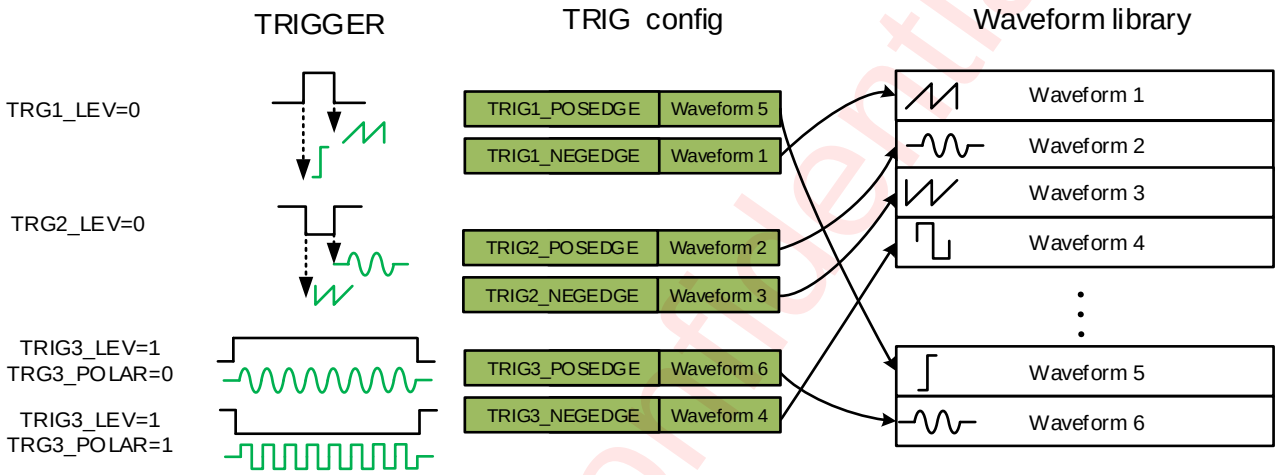


Figure 24 TRIG mode playback

Edge mode or level mode is accessible by configing register TRGx_LEV. When the edge mode is needed, user should set TRGx_LEV =0. In edge mode, register TRGxSEQ_P and TRGx_POS respestively represent the waveform and enable signal of positive edge, where register TRGxSEQ_N and TRGx_NEG respestively represent the waveform and enable signal of negative edge.

When a level mode is needed, user should set TRGx_LEV =1, and positive level and negative level can be supported by setting register TRGX_POLAR=0 and setting TRGX_POLAR=1.

Table 5 TRIG MODE CONFIG

I2C reg				Trigger	Waveform
TRGx_LVL	TRGx_POLAR	TRGx_POS	TRGx_NEG		
0	X	0	0	-	none
	X	1	0	↑	TRGxSEQ_P
	X	0	1	↓	TRGxSEQ_N
	X	1	1	↑ / ↓	TRGxSEQ_P/ TRGxSEQ_N
1	0	X	X	High level	TRGxSEQ_P
	1	X	X	Low level	TRGxSEQ_N

Playback steps:

- Waveform library must be initialized before playback;
- Set trigger playback registers (0x33 ~ 0x3A ,0x43) as desired;
- Send trigger pulse (≥1μs) or trigger level (≥1ms) on TRIG pins to playback waveform;

- Device will be switched to STANDBY mode after haptic waveform playback finished.

One wire Mode

The function of one wire mode mainly transfer two information : sequence number and gain of waveform，TRIG1 is the interface pin.

Playback steps:

- Waveform library must be initialized before playback;
- Set TRG_ONEWIRE to 1 in register 0x3A to enable one wire mode;
- Determine sequence number and gain of waveform which you want to playback;
- Combine sequence number and gain data into a 15 bit transformation data（low 8 bit is gain, high 7 bit is sequence number），the data is sent from the lowest bit;
- Chip will automatically enter standby mode after playing. The interval time between two sending protocol data should be greater than “3ms+time length of waveform”.

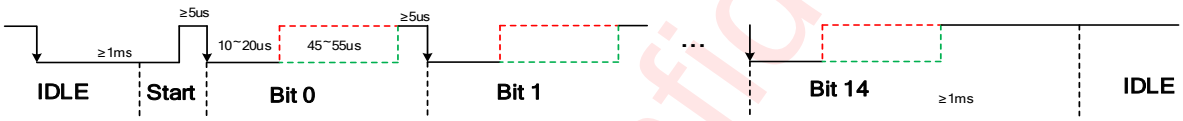


Figure 25 One wire mode playback

Cont Mode

The CONT mode mainly performs two functions: F0 detection and real-time resonance-frequency tracking. F0 detection can be launched by setting EN_F0_DET=1. When set TRACK_EN=1, real-time resonance-frequency tracking will be launched by tracking the BEMF of actuator constantly. It provides stronger and more consistent vibrations and lower power consumption. If the resonant frequency shifts for any reason, the function tracks the frequency from cycle to cycle. When TRACK_EN is set to 0, the width of waveform of cont mode is determined by DRV_WIDTH in register 0x1A.

When the EDGE_FRE register is set to 4’b1xxx, the CONT mode outputs a filtered square wave. The edge of filtered square wave is composed of SIN or COS wave whose frequency can be configured by EDGE_FRE register. When SIN_MODE register is set to 1, filtered square wave is composed of COS wave.

Playback steps:

- Set PLAY_MODE = 2 in register 0x08 to enable CONT mode;
- (optional)Set EN_F0_DET = 1 and BRK_EN =1;
- Set cont mode by configuring registers(0x18~0x22);
- Set GO bit to 1 in register 0x09 to trigger waveform playback;
- Delay 1ms;
- If enable F0 detection, read until GLB_STATE=0. then get F0 information from registers(0x25~0x28);
- Device will be switched to STANDBY mode after haptic waveform playback finished.

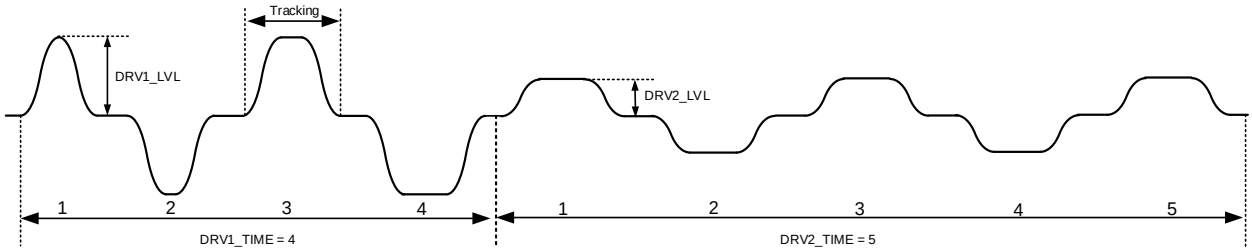


Figure 26 Cont mode playback

Smart loop

Smart loop is an unique function for small size LRA. It can turn the close loop into open loop automatically.

To enable smart loop function, there are some points to note:

- Set F_PRE (0x19) as the nominal F0,
- Enable smart_loop function(0x18);

I2S/TDM Mode

Device support I2S/TDM interface to playback wave data from I2S/TDM master. I2S/TDM mode can be used to playback waveform following the music which is playing.

Playback steps:

- Start BCK from I2S master;
- Set I2S/TDM playback registers (0x52 ~ 0x53) as desired;
- (optional)Set EN_DLL=1;
- Set I2S_EN =1;
- Wait GLB_STATE=4'b1010;
- Send I2S/TDM data to device.

Auto Brake Engine

An auto-brake engine is integrated into this device. Users can adjust the brake strength by setting D2S_GAIN in register 0x4e. The greater D2S_GAIN, the greater brake strength and the worse loop stability. Auto-brake engine is disabled when setting BRK_EN=0 or BRK_TIME=0.

To enable Auto-brake engine, there are some points to note:

- TRGx_BRK in register 0x39, 0x3A;
- Auto-brake engine will not work when BRK_EN=0 in register 0x08；
- Auto-brake engine will not work when EN_F0_DET in register 0x18 is set to 1;
- Auto-brake engine will not work when BRK_TIME in register 0x21 is set to 0;

- Device will be switched to STANDBY mode after haptic waveform playback finished.

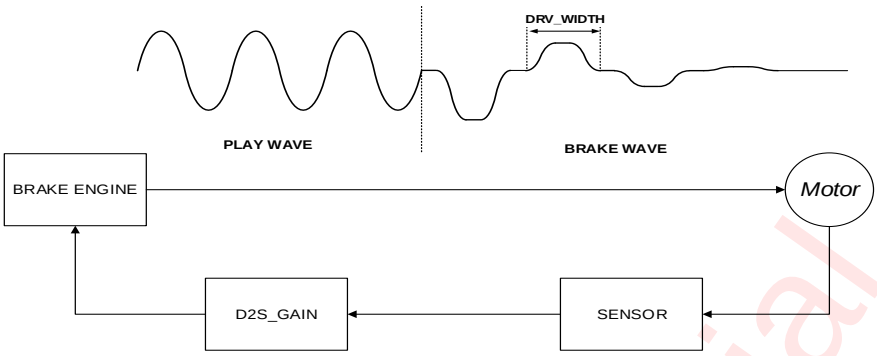


Figure 27 Brake loop

DC-DC Converter

The device integrated peak current mode synchronous PWM Charge pump as H-bridge power stage supply, significantly increase the output voltage dynamic range. Reduces the size of external components and saves PCB space by using about 1.6 MHz switching frequency. Charge pump output voltage can be set through the I^2C register 0x06;

The device synchronous Charge pump with soft-start function to prevent overshoot current at powering-on; integrated the output protection circuit and self-recovery function.

Protection Mechanisms

Over Voltage Protection (OVP)

The charge pump circuit has integrated the over voltage protection control loop. When the output voltage PVDD is above the threshold, the charge pump circuits will stop working, until the voltage of PVDD going down and under the normal fixed working voltage.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 160°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

Over Current (Short) Protection (OCP)

The short circuit protection function is triggered when HDP/HDN is short to PVDD/GND or HDP is short to HDN, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

Vbat Under Voltage Lock Out Protection (UVLO)

The device has a battery monitor that monitors the VBAT level to ensure that is above threshold 2.7V, In the event of a VBAT drop, the device immediately power down the Charge Pump and H-bridge driver and latches the UVLO flag.

Drive Data Error Protection (DDEP)

When haptic data sent to drive LRA is error such as: a DC data or almost DC data, it will cause the LRA heat to brake. The device configurable immediately power down the Charge pump and H-bridge driver and latched the DDEP flag.

Battery protection

In order to reduce the power consumption, the chip will reduce the gain automatically When battery's voltage is low and enable the VBAT_PRO function.

To enable VBAT_PRO, there are some points to note:

- Auto_CP function must be disable when use battery protection;
- There is a contradiction between constant vibration strength mode and battery protection mode.
- When detect the voltage is below the protection threshold ,the chip will reduce gain at soon. When detect the battery voltage is higher than protection threshold for a period time, the chip will recovery at the crossing point;
- There is four level of battery protection, normal output->pro1->pro2->pro3->off.
- Set related register (0x4C) to configure battery protection mode.

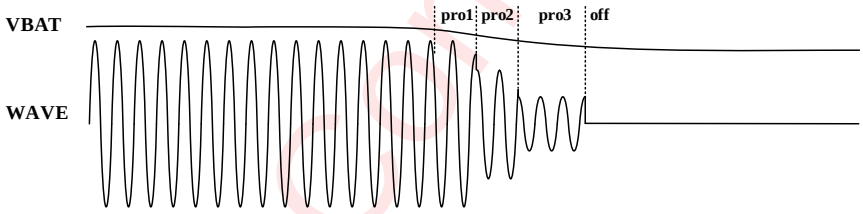


Figure 28 Battery protection process

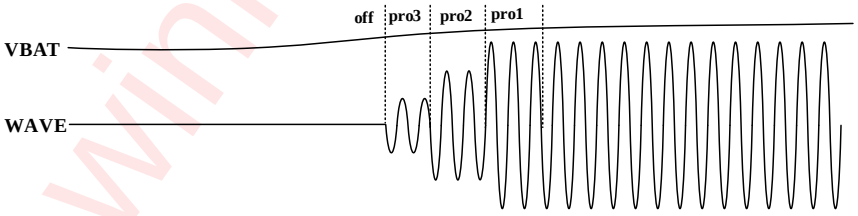


Figure 29 Battery protection release process

Digital Audio Interface

Wave data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface via 3 dedicated pins:

- BCK
- WCK(8K/12K/16K/24K/48K/96K is supported)
- DATAI

I²S and 1/2/4/6/8-slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 24, or 32 bits by configurable registers.

Two modes of I²S are supported, including standard I²S mode and Left-Justified mode, which can be configured via I2SCFG1.I2S_MODE.The data width is programmable via I2SCFG2.BCK_MODE.

The bit clock BCK is used to sample the data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. The frequency of BCK can be calculated according to the following equation:

BCK frequency = ***SampleRate*** * ***SlotLength*** * ***SlotNumber***

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface.

For I2S mode the audio source can be from left channel, right channel .For TDM mode, the audio source can be from slot1, slot2, slot3, slot4, slot5, slot6,slot7 or slot8, which is controlled by I2SCFG1.

Table 6 Supported I2S interface parameters

Interface format(MSB first)	Data width	WCK frequency
Standard I²S/ Left-Justified	16b/24b/32b	8K/12K/16K /24K/ 48K/96K
TDM 1/2/4 slots	16b/24b/32b	8K/12K /16K /24K/ 48K/96K
TDM 6/8 slots	16b/24b/32b	8K/12K/16K /24K/ 48K

Standard I²S Mode

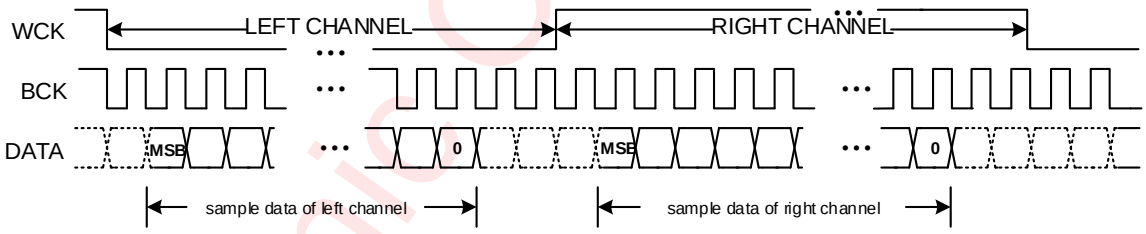


Figure 30 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

Left-Justified Mode

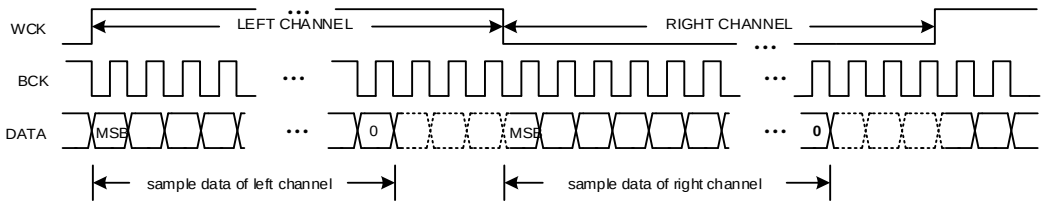


Figure 31 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

TDM MODE

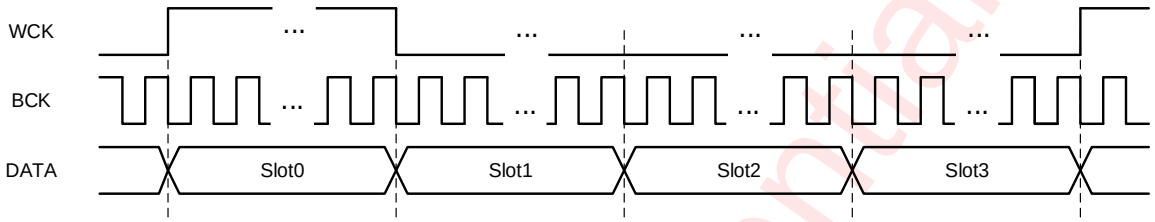


Figure 32 TDM Timing

- The difference between TDM and I²S is the supported slot-number. 1/2/4/6/8-slot is supported in TDM mode, while 2-slot is supported in I²S mode.
- The MSB of the slot 1 is valid on the first rising or second edge of the bit clock after the rising edge of the WCK which can be configured via I2SCFG1.I2S_MODE.

I2C Interface

This device supports the I²C serial bus and data transmission protocol in fast mode at 400kHz and fast mode plus at 1000kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pin SDA and I pin SCL. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.2V~3.3V) of this I²C interface.

Device Address

The I²C device address (7-bit) can be set using the AD pin according to the following table:

Table 7 AW86727FCR Address Selection

AD	I²C address (7-bit)
0	0x5A
1	0x5B

Table 8 AW86728CSR Address Selection

AD	AD2	I²C address (7-bit)
0	0	0x5A
1	0	0x5B
0	1	0x58
1	1	0x59

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

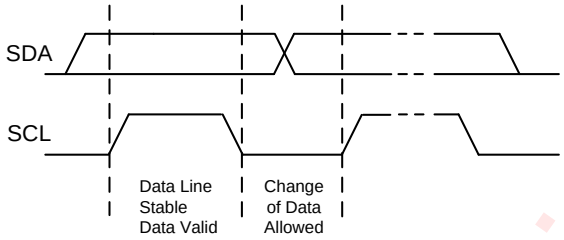


Figure 33 Data Validation Diagram

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

START state: The SCL maintain a high level, SDA from high to low level

STOP state: The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 34.

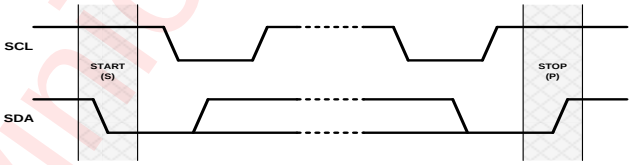


Figure 34 START and STOP state generation process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 35. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 36. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

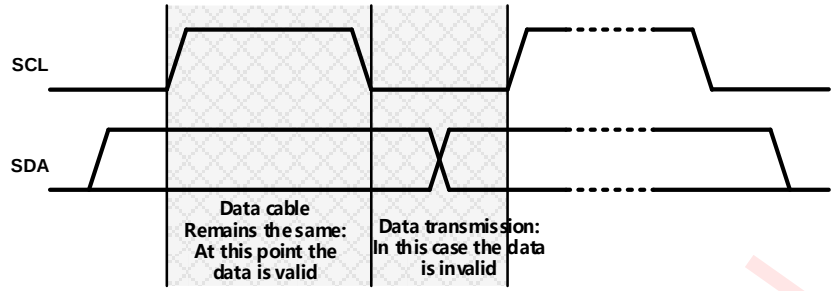


Figure 35 The data transfer rules on the I²C bus

The whole process of actual data transmission is shown in Figure 36. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

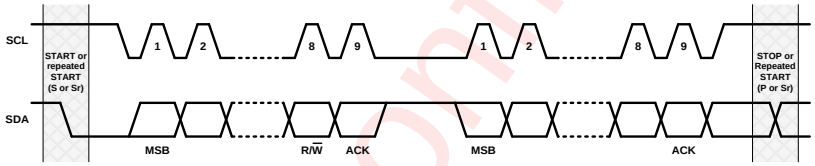


Figure 36 Data transmission on the I²C bus

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in Figure 37:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit register address to which the first data byte will written；

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the device.

The master device generates the STOP state to end the data transmission.

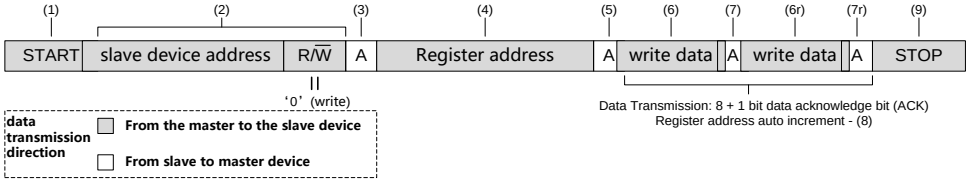


Figure 37 Writing process (data transmission direction remains the same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW8672X as the slave device, the transmission process carried out by following steps listed in Figure 38:
Master device asserts a start condition;

Master device transmits the 7 bits address of the device, and followed by a "read / write" flag ($R/\overline{W}$ = 0);
The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
The master device transmits the register address to make sure where the first data byte will read;
The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again;
The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
Master transmits 8 bits of data to register which needs to be read;
The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;
The device automatically increment register address once after sent each acknowledge bit (ACK),
The master device generates the STOP state to end the data transmission.

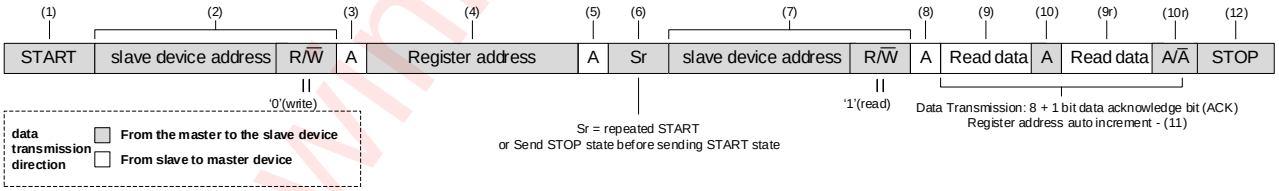


Figure 38 Reading process (data transmission direction remains the same)

Register Configuration

Register List

ADDR	NAME	*R/W*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	RSTCFG	***RW***	SOFTRST								0x80/0x81
0x01	SYSST	***RO***			UVLS	FF_AES	FF_AFS	OCDS	OTS	DONES	0x10
0x02	SYSINT	***RC***			UVLI	FF_AEI	FF_AFI	OCDI	OTI	DONEI	0x10

0x03	SYSINTM	RW			UVLM	FF_AEM	FF_AFM	OCDM	OTM	DONEM	0x7F
0x06	PLAYCFG1	RW								EN_CP_2X	0Xd0
0x07	PLAYCFG2	RW	GAIN								0x80
0x08	PLAYCFG3	RW				AUTO_CP	STOP_MODE	BRK_EN	PLAY_MODE		0x14
0x09	PLAYCFG4	RW							STOP	GO	0x00
0x0A	WAVCFG1	RW	SEQ1WAIT	WAVSEQ1							0x01
0x0B	WAVCFG2	RW	SEQ2WAIT	WAVSEQ2							0x00
0x0C	WAVCFG3	RW	SEQ3WAIT	WAVSEQ3							0x00
0x0D	WAVCFG4	RW	SEQ4WAIT	WAVSEQ4							0x00
0x0E	WAVCFG5	RW	SEQ5WAIT	WAVSEQ5							0x00
0x0F	WAVCFG6	RW	SEQ6WAIT	WAVSEQ6							0x00
0x10	WAVCFG7	RW	SEQ7WAIT	WAVSEQ7							0x00
0x11	WAVCFG8	RW	SEQ8WAIT	WAVSEQ8							0x00
0x12	WAVCFG9	RW	SEQ1LOOP				SEQ2LOOP				0x00
0x13	WAVCFG10	RW	SEQ3LOOP				SEQ4LOOP				0x00
0x14	WAVCFG11	RW	SEQ5LOOP				SEQ6LOOP				0x00
0x15	WAVCFG12	RW	SEQ7LOOP				SEQ8LOOP				0x00
0x16	WAVCFG13	RW			WAITSLOT		MAINLOOP				0x00
0x18	CONTCFG1	RW	SMART_LOOP	BRK_CP_MD	EN_F0_DET	SIN_MODE	EDGE_FRE				0x1E
0x19	CONTCFG2	RW	F_PRE								0x8D
0x1A	CONTCFG3	RW	DRV_WIDTH								0x6A
0x1C	CONTCFG5	RW	CP_BRK_GAIN				BRK_GAIN				0x58
0x1D	CONTCFG6	RW	TRACK_EN	DRV1_LVL							0xFF
0x1E	CONTCFG7	RW		DRV2_LVL							0x50
0x1F	CONTCFG8	RW	DRV1_TIME								0x04
0x20	CONTCFG9	RW	DRV2_TIME								0x06
0x21	CONTCFG10	RW	BRK_TIME								0x08
0x22	CONTCFG11	RW				TRACK_MARGIN					0x0C
0x25	CONTRD14	RO	F_LRA_F0_H								0x00
0x26	CONTRD15	RO	F_LRA_F0_L								0x00
0x27	CONTRD16	RO	CONT_F0_H								0x00
0x28	CONTRD17	RO	CONT_F0_L								0x00
0x2D	RTPCFG1	RW		EN_TWORTP	AUTO_SIN_96K	AUTO_DYNAMIC_SIN	BASE_ADDR_H				0x08
0x2E	RTPCFG2	RW	BASE_ADDR_L								0x00
0x2F	RTPCFG3	RW	FIFO_AEH				FIFO_AFH				0x26
0x30	RTPCFG4	RW	FIFO_AEL								0x00
0x31	RTPCFG5	RW	FIFO_AFL								0x00
0x32	RTPDATA	RW	RTP_DATA								0x00
0x33	TRGCFG1	RW	TRG1_POS	TRG1SEQ_P							0x01
0x34	TRGCFG2	RW	TRG2_POS	TRG2SEQ_P							0x01
0x35	TRGCFG3	RW	TRG3_POS	TRG3SEQ_P							0x01
0x36	TRGCFG4	RW	TRG1_NEG	TRG1SEQ_N							0x01
0x37	TRGCFG5	RW	TRG2_NEG	TRG2SEQ_N							0x01
0x38	TRGCFG6	RW	TRG3_NEG	TRG3SEQ_N							0x01
0x39	TRGCFG7	RW	TRG1_POLAR	TRG1_LEV	TRG1_BRK	TRG1_CP	TRG2_POLAR	TRG2_LEV	TRG2_BRK	TRG2_CP	0x33
0x3A	TRGCFG8	RW	TRG3_POLAR	TRG3_LEV	TRG3_BRK	TRG3_CP	TRG_ONEWIRE	TRG1_STOP	TRG2_STOP	TRG3_STOP	0x30
0x3C	GLBCFG2	RW	START_DLY								0x08
0x3E	GLBCFG4	RW	GO_PRIO		TRG3_PRIO		TRG2_PRIO		TRG1_PRIO		0x1B
0x3F	GLBRD5	RO	STATE MODULE				GLB_STATE				0x00
0x40	RAMADDRH	RW				RAMADDRH					0x00
0x41	RAMADDRL	RW	RAMADDRL								0x00
0x42	RAMDATA	RW	RAMDATA								0x00
0x43	TRGCFG9	RW	TRG_GAIN								0x80
0x44	SYSCTRL1	RW	EN_INTN_OUT	WCK_PIN							0x28
0x45	SYSCTRL2	RW		WAKE	STANDBY			EN_RAMINIT	EN_FIR		0x0A
0x46	SYSCTRL3	RW		WAVDAT_MODE					EN_DLL	GAIN_BYPASS	0x88
0x47	SYSCTRL4	RW	EN_BRO_ADDR	BROADCAST_ADDR							0x00
0x48	PWMCFG1	RW	PRC_EN	PRCTIME							0xA0

0x49	PWMCFG2	RW				PD_HWM				0x28
0x4A	PWMCFG3	RW	PR_EN	PRLVL						0xBF
0x4B	PWMCFG4	RW	PRTIME							0x32
0x4C	VBAT_CTRL	RW	VBAT_PRO	VBAT_MODE		DELTA_VBAT	REL_VBAT	ABS_VBAT		0x00
0x4D	DETCFG1	RW		VBAT_REF			ADC_FS	DET_GO		0x24
0x4E	DETCFG2	RW		DET_SEQ0			D2S_GAIN			0x04
0x4F	DET_RD1	RO					ADC_DATA_H	AVG_DATA_H		0x00
0x50	DET_RD2	RO	AVG_DATA_L							0x00
0x51	DET_RD3	RO	ADC_DATA_L							0x00
0x52	I2SCFG1	RW	I2S_EN	SLOT_NUM			I2S_MODE	RX_SLOTVLD		0x00
0x53	I2SCFG2	RW	CKERR_MASK		WSINV	BCKINV	I2S_INT		BCK_MODE	0x08
0x56	SYSCTRL6	RW							UVLO_ADJ	0x03
0x57	IDH	RO	CHIPID_H							0x72
0x58	IDL	RO	CHIPID_L							0x70/0x80
0x59	TRIMCFG5	RW		TRIM_LRA						0x00

Register Detailed Description

Note: Reserved register should not be written

RSTCFG: (Address 00h)

Bit	Symbol	R/W	Description	Default
7:0	SOFTRST	RW	All configuration registers will be reset to default value after 0xaa is written	0x80/0x81

SYSST: (Address 01h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	UVLS	RO	VDD voltage is currently under UV voltage 0: no 1: yes	0
4	FF_AES	RO	RTP FIFO is currently almost empty 0: no 1: yes	1
3	FF_AFS	RO	RTP FIFO is currently almost full 0: no 1: yes	0
2	OCDS	RO	Over current is happening 0: no 1: yes	0
1	OTS	RO	Over Temperature status is happening 0: no 1: yes	0
0	DONES	RO	The playing is over and chip is going to standby 0: no 1: yes	0

SYSINT: (Address 02h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RC	Not used	0
5	UVLI	RC	UVLS=1 has happened at least once since the last read 0: no 1: yes	0
4	FF_AEI	RC	FF_AES=1 has happened at least once since the last read 0: no 1: yes	1
3	FF_AFI	RC	FF_AFS=1 has happened at least once since the last read 0: no 1: yes	0

2	OCDI	RC	OCDS=1 has happened at least once since the last read 0: no 1: yes	0
1	OTI	RC	OTS=1 has happened at least once since the last read 0: no 1: yes	0
0	DONEI	RC	DONES=1 has happened at least once since the last read 0: no 1: yes	0

SYSINTM: (Address 03h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	1
5	UVLM	RW	Interrupt(INTN pin low) mask for UVLI: 0: open 1: mask	1
4	FF_AEM	RW	Interrupt(INTN pin low) mask for FF_AEMI: 0: open 1: mask	1
3	FF_AFM	RW	Interrupt(INTN pin low) mask for FF_AFMI: 0: open 1: mask	1
2	OCDM	RW	Interrupt(INTN pin low) mask for OCDI: 0: open 1: mask	1
1	OTM	RW	Interrupt(INTN pin low) mask for OTI: 0: open 1: mask	1
0	DONEM	RW	Interrupt(INTN pin low) mask for DONEI: 0: open 1: mask	1

PLAYCFG1: (Address 06h)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RW	Not used	0x68
0	EN_CP_2X	RW	Charge Pump mode 0: Bypass mode 1: 2X mode	0

PLAYCFG2: (Address 07h)

Bit	Symbol	R/W	Description	Default
7:0	GAIN	RW	gain setting for waveform data for RAM/RTP/I2S, GAIN=code/128	0x80

PLAYCFG3: (Address 08h)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	0
4	AUTO_CP	RW	1: disable CP when data is 0 in RTP ,I2S and RAM mode	1
3	STOP_MODE	RW	0: stop when current wave is over 1: stop right now	0
2	BRK_EN	RW	When set 1, enable auto brake after RTP/RAM/CONT/I2S playback mode is stopped	1
1:0	PLAY_MODE	RW	Waveform play mode for GO trig b00: RAM mode b01: RTP mode b10: CONT mode b11: no play	0

PLAYCFG4: (Address 09h)

Bit	Symbol	R/W	Description	Default

7:2	Reserved	RW	Not used	0
1	STOP	RW	When set 1, stop the current playback mode	0
0	GO	RW	RAM/RTP/CONT mode playback trig bit when set to 1, chip will playback one of the play mode.	0

WAVCFG1: (Address 0Ah)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	SEQ1WAIT	RW	When set to 1 , WAVSEQ1 means wait time, else means wave sequence number	0
6:0	WAVSEQ1	RW	Wait time (code*WAITSLOT) or wave sequence number	1

WAVCFG2: (Address 0Bh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	SEQ2WAIT	RW	When set to 1 , WAVSEQ2 means wait time, else means wave sequence number	0
6:0	WAVSEQ2	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG3: (Address 0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	SEQ3WAIT	RW	When set to 1 , WAVSEQ3 means wait time, else means wave sequence number	0
6:0	WAVSEQ3	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG4: (Address 0Dh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	SEQ4WAIT	RW	When set to 1 , WAVSEQ4 means wait time, else means wave sequence number	0
6:0	WAVSEQ4	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG5: (Address 0Eh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	SEQ5WAIT	RW	when set to 1 , WAVSEQ5 means wait time, else means wave sequence number	0
6:0	WAVSEQ5	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG6: (Address 0Fh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	SEQ6WAIT	RW	When set to 1 , WAVSEQ6 means wait time, else means wave sequence number	0
6:0	WAVSEQ6	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG7: (Address 10h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	SEQ7WAIT	RW	when set to 1 , WAVSEQ7 means wait time, else means wave sequence number	0
6:0	WAVSEQ7	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG8: (Address 11h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	SEQ8WAIT	RW	When set to 1 , WAVSEQ8 means wait time, else means wave sequence number	0
6:0	WAVSEQ8	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG9: (Address 12h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:4	SEQ1LOOP	RW	Control the loop number of the first sequence b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or SEQ1LOOP ≠0xF	0
3:0	SEQ2LOOP	RW	Control the loop number of the second sequence b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or SEQ2LOOP ≠0xF	0

WAVCFG10: (Address 13h)

Bit	Symbol	R/W	Description	Default
7:4	SEQ3LOOP	RW	Control the loop number of the third sequence b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or SEQ3LOOP ≠0xF	0
3:0	SEQ4LOOP	RW	Control the loop number of the fourth sequence b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or SEQ4LOOP ≠0xF	0

WAVCFG11: (Address 14h)

Bit	Symbol	R/W	Description	Default
7:4	SEQ5LOOP	RW	Control the loop number of the fifth sequence b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or SEQ5LOOP ≠0xF	0
3:0	SEQ6LOOP	RW	Control the loop number of the sixth sequence b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or SEQ6LOOP ≠0xF	0

WAVCFG12: (Address 15h)

Bit	Symbol	R/W	Description	Default
7:4	SEQ7LOOP	RW	Control the loop number of the seventh sequence b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or SEQ7LOOP ≠0xF	0
3:0	SEQ8LOOP	RW	Control the loop number of the eighth sequence b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or SEQ8LOOP ≠0xF	0

WAVCFG13: (Address 16h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5:4	WAITSLOT	RW	Unit of wait time b00: (1/WAVDAT_MODE) s b01: (8/WAVDAT_MODE) s b10: (64/WAVDAT_MODE) s b11: (512/WAVDAT_MODE) s	0
3:0	MAINLOOP	RW	Control the main loop number b0000~b1110: play (code+1) time b1111: playback infinitely until STOP set to 1 or MAINLOOP ≠0xF	0

CONTCFG1: (Address 18h)

Bit	Symbol	R/W	Description	Default
7	SMART_LOOP	RW	Enable open loop mode and not to detect zero crossing: 0: disable 1: enable	0
6	BRK_CP_MD	RW	When set 1, CP_mode in brake is the same with current playback mode, otherwise the CP_mode in brake is 0	0

5	EN_F0_DET	RW	F0 detection mode enable 1: enable 0: disable	0
4	SIN_MODE	RW	Edge mode for filtered square wave of CONT mode: 1: cos 0: sine	1
3:0	EDGE_FRE	RW	Define the edge frequency b1000 : 200Hz b1001 : 210Hz b1010 : 260Hz b1011 : 280Hz b1100 : 300Hz b1101 : 600Hz b1110 : 700Hz b1111 : 800Hz b0000-b0111: play non-filtered square wave in CONT mode	14

CONTCFG2: (Address 19h)

Bit	Symbol	R/W	Description	Default
7:0	F_PRE	RW	Set the value of F0, F0=(24K/code)Hz	0x8D

CONTCFG3: (Address 1Ah)

Bit	Symbol	R/W	Description	Default
7:0	DRV_WIDTH	RW	Half cycle drive time of brake and it is also the half cycle drive time of drive when TRACK_EN=0, this value must be smaller than half cycle time of F0. Time = code/48000 (s)	0x6A

CONTCFG5: (Address 1Ch)

Bit	Symbol	R/W	Description	Default
7:4	CP_BRK_GAIN	RW	Gain factor of brake when CP_MODE is 1	5
3:0	BRK_GAIN	RW	Gain factor of brake when CP_MODE is 0	8

CONTCFG6: (Address 1Dh)

Bit	Symbol	R/W	Description	Default
7	TRACK_EN	RW	Track switch 1: enable 0: disable	1
6:0	DRV1_LVL	RW	Level for the first cont drive. When VBAT_MODE=1: no load output voltage=VBAT_REF*DRV1_LVL/128; if (VBAT_REF*DRV1_LVL)/VBAT > 128, no load output voltage=PVDD; When VBAT_MODE=0/CP_MODE=1: no load output voltage=PVDD*DRV1_LVL/128	0x7F

CONTCFG7: (Address 1Eh)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:0	DRV2_LVL	RW	Level for the second cont drive When VBAT_MODE=1: no load output voltage=VBAT_REF*DRV2_LVL/128; if (VBAT_REF*DRV2_LVL)/VBAT > 128, no load output voltage=PVDD; When VBAT_MODE=0/CP_MODE=1: no load output voltage=PVDD*DRV2_LVL/128	0x50

CONTCFG8: (Address 1Fh)

Bit	Symbol	R/W	Description	Default
7:0	DRV1_TIME	RW	Number of half cycle for the first cont drive	4

CONTCFG9: (Address 20h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	DRV2_TIME	RW	Number of half cycle for the second cont drive	6

CONTCFG10: (Address 21h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	BRK_TIME	RW	The num of half cycle of brake mode	8

CONTCFG11: (Address 22h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	Reserved	RW	Not used	0
4:0	TRACK_MARGIN	RW	Margin value of tracking, the smaller margin, the higher tracking accuracy and the lower loop stability. Time = code/480000 (s)	12

CONTRD14: (Address 25h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	F_LRA_F0_H	RO	High 8 bit of the measure value for the f0 of LRA in the f0 detection mode F0=(384000/(F_LRA_F0_H*256+F_LRA_F0_L))Hz	0

CONTRD15: (Address 26h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	F_LRA_F0_L	RO	Low 8 bit of the measure value for the f0 of LRA in the f0 detection mode F0=(384000/(F_LRA_F0_H*256+F_LRA_F0_L))Hz	0

CONTRD16: (Address 27h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CONT_F0_H	RO	The measure value for the f0 of LRA in the continuous detection mode (high eight bits) F0=(384000/(CONT_F0_H*256+CONT_F0_L))Hz	0

CONTRD17: (Address 28h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CONT_F0_L	RO	The measure value for the f0 of LRA in the continuous detection mode (low eight bits) F0=(384000/(CONT_F0_H*256+CONT_F0_L))Hz	0

RTPCFG1: (Address 2Dh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0
6	EN_TWORTP	RW	Enable double channel for RTP playbcak mode: 0: single RTP 1: double RTP	0
5	AUTO_SIN_96K	RW	Set sampling rate of rtp auto sin function: 0: 48K 1: 96K	0
4	AUTO_DYNAMIC_SIN	RW	Five data generate a half-period sin waveform with amplitude of 127. The order of the 5 data is as follws: sinh [7:0],sinl[7:0],cosh[7:0],cosl[7:0],rtp_gain[7:0] [sinh,sinl]= 65536*sin(2*pi*wav_frequence/sampling rate) [cosh,cosl]=65536*cos(2*pi*wav_frequence/sampling rate) rtp_gain control sin wave gain, gain = rtp_gain/128 0: disable 1: enable	0
3:0	BASE_ADDR_H	RW	High five bits of start address of wave SRAM BASE_ADDR = BASE_ADDR_H * 256 + BASE_ADDR_L	0x08

RTPCFG2: (Address 2Eh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:0	BASE_ADDR_L	RW	Low eight bits of start address of wave SRAM BASE_ADDR = BASE_ADDR_H * 256 + BASE_ADDR_L	0

RTPCFG3: (Address 2Fh)

Bit	Symbol	R/W	Description	Default
7:4	FIFO_AEH	RW	High four bits of RTP FIFO almost empty threshold FIFO_AE = FIFO_AEH * 256 + FIFO_AEL	0x02
3:0	FIFO_AFH	RW	High four bits of RTP FIFO almost full threshold FIFO_AF = FIFO_AFH * 256 + FIFO_AFL	0x06

RTPCFG4: (Address 30h)

Bit	Symbol	R/W	Description	Default
7:0	FIFO_AEL	RW	Low eight bits of RTP FIFO almost empty threshold FIFO_AE = FIFO_AEH * 256 + FIFO_AEL	0x00

RTPCFG5: (Address 31h)

Bit	Symbol	R/W	Description	Default
7:0	FIFO_AFL	RW	Low eight bits of RTP FIFO almost full threshold FIFO_AF = FIFO_AFH * 256 + FIFO_AFL	0x00

RTPDATA: (Address 32h)

Bit	Symbol	R/W	Description	Default
7:0	RTP_DATA	RW	RTP mode , data write entry, when data written into this register, the data will be written into RTP FIFO	0

TRGCFG1: (Address 33h)

Bit	Symbol	R/W	Description	Default
7	TRG1_POS	RW	TRG1 rising edge enable/disable control 1: enable 0: disable	0
6:0	TRG1SEQ_P	RW	TRG1 pos-edge trigged wave sequence number	1

TRGCFG2: (Address 34h)

Bit	Symbol	R/W	Description	Default
7	TRG2_POS	RW	TRG2 rising edge enable/disable control 1: enable 0: disable	0
6:0	TRG2SEQ_P	RW	TRG2 pos-edge trigged wave sequence number	1

TRGCFG3: (Address 35h)

Bit	Symbol	R/W	Description	Default
7	TRG3_POS	RW	TRG3 rising edge enable/disable control 1: enable 0: disable	0
6:0	TRG3SEQ_P	RW	TRG3 pos-edge trigged wave sequence number	1

TRGCFG4: (Address 36h)

Bit	Symbol	R/W	Description	Default
7	TRG1_NEG	RW	TRG1 falling edge enable/disable control 1: enable 0: disable	0
6:0	TRG1SEQ_N	RW	TRG1 neg-edge trigged wave sequence number	1

TRGCFG5: (Address 37h)

Bit	Symbol	R/W	Description	Default

7	TRG2_NEG	RW	TRG2 falling edge enable/disable control 1: enable 0: disable	0
6:0	TRG2SEQ_N	RW	TRG2 neg-edge trigged wave sequence number	1

TRGCFG6: (Address 38h)

Bit	Symbol	R/W	Description	Default
7	TRG3_NEG	RW	TRG3 falling edge enable/disable control 1: enable 0: disable	0
6:0	TRG3SEQ_N	RW	TRG3 neg-edge trigged wave sequence number	1

TRGCFG7: (Address 39h)

Bit	Symbol	R/W	Description	Default
7	TRG1_POLAR	RW	TRIG1 pin active polarity, when host supply positive level, this bit set to 0, else set to 1	0
6	TRG1_LEV	RW	TRG1 mode control 1: level 0: edge	0
5	TRG1_BRK	RW	Auto brake setting for TRG1 0: disable 1: enable	1
4	TRG1_F	RW	Enable CP mode in TRG1 playback mode. 0: disable 1: enable	1
3	TRG2_POLAR	RW	Configuration of level mode for TRIG2 0: High active 1: low active	0
2	TRG2_LEV	RW	TRG2 mode control 0: disable 1: enable	0
1	TRG2_BRK	RW	Auto brake setting for TRG2. 0: disable 1: enable	1
0	TRG2_CP	RW	Enable CP mode in TRG2 playback mode. 0: disable 1: enable	1

TRGCFG8: (Address 3Ah)

Bit	Symbol	R/W	Description	Default
7	TRG3_POLAR	RW	Configuration of level mode for TRIG3 0: High active 1: low active	0
6	TRG3_LEV	RW	TRG3 mode control 1: level 0: edge	0
5	TRG3_BRK	RW	Auto brake setting for TRG3 0: disable 1: enable	1
4	TRG3_CP	RW	Enable CP mode in TRG1 playback mode. 0: disable 1: enable	1
3	TRG_ONEWIRE	RW	When set 1,enable one wire mode	0
2	TRG1_STOP	RW	Stop mode for TRIG1 0: stop when current wave is over 1: stop right now	0
1	TRG2_STOP	RW	Stop mode for TRIG2 0: stop when current wave is over 1: stop right now	0
0	TRG3_STOP	RW	Stop mode for TRIG3 0: stop when current wave is over 1: stop right now	0

GLBCFG2: (Address 3Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	START_DLY	RW	Startup delay time, unit time is (1/48k)s	0x08

GLBCFG4: (Address 3Eh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	GO_PRIO	RW	Priority value of GO TRIG High priority can interrupt the playback of low priority, and low priority cannot interrupt the playback of high priority. When the priority settings are consistent, the default priority will be implemented	0
5:4	TRG3_PRIO	RW	Priority value of TRIG3 pin High priority can interrupt the playback of low priority, and low priority cannot interrupt the playback of high priority. When the priority settings are consistent, the default priority will be implemented	1
3:2	TRG2_PRIO	RW	Priority value of TRIG2 pin High priority can interrupt the playback of low priority, and low priority cannot interrupt the playback of high priority. When the priority settings are consistent, the default priority will be implemented	2
1:0	TRG1_PRIO	RW	Priority value of TRIG1 pin High priority can interrupt the playback of low priority, and low priority cannot interrupt the playback of high priority. When the priority settings are consistent, the default priority will be implemented	3

GLBRD5: (Address 3Fh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	MODULE_STATE	RO	sub module state machine state	0
3:0	GLB_STATE	RO	The state of glb state b0000: STANDBY b0110: CONT b0111: RAM b1000: RTP b1001: TRIG b1010: I2S/TDM b1011: BRAKE	0

RAMADDRH: (Address 40h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	Reserved	RW	Not used	0
4:0	RAMADDRH	RW	SRAM address high five bits	0

RAMADDRL: (Address 41h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	RAMADDRL	RW	SRAM address low eight bits	0

RAMDATA: (Address 42h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	RAMDATA	RW	SRAM data entry	0

TRGCFG9: (Address 43h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	TRG_GAIN	RW	Gain setting for waveform data of TRIG playback mode, GAIN=code/128	0x80

SYSCTRL1: (Address 44h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	EN_INTN_OUT	RW	enable clk_48k output from INTN PIN 0：enable	0

			1: not enable	
6	WCK_PIN	RW	Enable external clock(48K to TRIG2) synchronized RTP playback feature, 0: disable 1: enable	0
5:0	Reserved	RW	Not used	0x28

SYSCTRL2: (Address 45h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6	WAKE	RW	Chip enable control 0: chip at normal mode 1: set chip into active mode	0
5	STANDBY	RW	Chip disable control 0: chip at normal mode 1: set chip into standby mode	0
4:3	Reserved	RW	Not used	1
2	EN_RAMINIT	RW	Enable clock: 1: open the digital module clock 0: close the digital module clock	0
1	EN_FIR	RW	Set enable of FIR filter	1
0	Reserved	RW	Not used	0

SYSCTRL3: (Address 46h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	1
6:5	WAVDAT_MODE	RW	Waveform data up sample rate selection: b00: 24KHz b01: 48kHz b10: 12KHz b11: 8KHz	0
4:2	Reserved	RW	Not used	1
1	EN_DLL	RW	DLL function which making the internal OSC clock automatically follow the external clock RCK 0: disable 1: enable	0
0	GAIN_BYPASS	RW	Whether the GAIN register works during playback: 0: shield 1: bypass	0

SYSCTRL4: (Address 47h)

Bit	Symbol	R/W	Description	Default
7	EN_BRO_ADDR	RW	Enable broadcast address control 0: I2C communication through hardware device address 1: I2C communication through hardware device address or BROADCAST_ADDR	0
6:0	BROADCAST_ADDR	RW	Software device address configuration	0x00

PWMCFG1: (Address 48h)

Bit	Symbol	R/W	Description	Default
7	PRC_EN	RW	When HDP/HDN keeps high maintains (PRCTIME/3k)s, HDP/HDN is pulled down protectively 0: disable 1: enable	1
6:0	PRCTIME	RW	Set protection time of output signal protection mode of pwm, unit time is (1/3k) s	0x20

PWMCFG2: (Address 49h)

Bit	Symbol	R/W	Description	Default

7:5	reserved	RW	Not used	1
4	PD_HWM	RW	shutdown half wave modulate 0: half wave mode 1: full wave mode	0
3:0	reserved	RW	Not used	8

PWMCFG3: (Address 4Ah)

Bit	Symbol	R/W	Description	Default
7	PR_EN	RW	Set enable of input signal protection mode of pwm: 0: disable 1: When output voltage >= PRLVL/128*PVDD maintains (PRTIME/3k)s, HDP/HDN is pulled down protectively	1
6:0	PRLVL	RW	Set protection voltage of input signal protection mode of pwm	0x3F

PWMCFG4: (Address 4Bh)

Bit	Symbol	R/W	Description	Default
7:0	PRTIME	RW	Set protection time of input signal protection mode of pwm, unit time is (1/3k) s	0x32

VBATCTRL: (Address 4Ch)

Bit	Symbol	R/W	Description	Default
7	VBAT_PRO	RW	Enable/Disable power supply safeguard: 0: disable 1: enable	0
6	VBAT_MODE	RW	VBAT adjust mode: 0: software adjust mode 1: hardware adjust mode	0
5	reserved	RW	Not used	0
4	DELTA_VBAT	RW	Delta voltage of protection voltage grade: 0: 0.1V 1: 0.2V	0
3:2	REL_VBAT	RW	b00: 10ms b01: 25ms b10: 50ms b11: 100ms	0
1:0	ABS_VBAT	RW	b00: 3.2V b01: 3.3V b10: 3.4V b11: 3.5V	0

DETCFG1: (Address 4Dh)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:4	VBAT_REF	RW	Reference voltage for VBAT hardware adjust mode: b000: 3.3V b001: 3.6V b010: 4.0V b011: 4.2V b100: 4.5V b101: 4.8V b110: 5.0V b111: 5.5V When VBAT_MODE=1: no load output voltage=VBAT_REF*WAVE_DATA/128; if (VBAT_REF* WAVE_DATA)/VBAT > 128, no load output voltage=PVDD; When VBAT_MODE=0/CP_MODE=1: no load output voltage=PVDD*WAVE_DATA /128.	2
3:2	ADC_FS	RW	ADC clock sampling rate: b00: 192KHz(ADC_CLK=6.144MHz) b01: 96KHz(ADC_CLK=3.072MHz) b10: 48KHz(ADC_CLK=1.536MHz) b11: 24KHz(ADC_CLK=768KHz)	1

1:0	DET_GO	RW	ADC sampling mode control: b01: det others: not det	0

DETCFG2: (Address 4Eh)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:3	DET_SEQ0	RW	Sequence0 detect type control: b0000: VBAT b0001: PVDD b0011: RL b0100: OS Others: for test	0
2:0	D2S_GAIN	RW	Set D2S gain: b000: 1 b001: 2 b010: 4 b011: 8 b100: 10 b101: 16 b110: 20 b111: 40	4

DET_RD1: (Address 4Fh)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0
3:2	ADC_DATA_H	RO	The measured value of one time adc data(high two bits)	0
1:0	AVG_DATA_H	RO	The measured value of 16 times adc average data(high two bits)	0

DET_RD2: (Address 50h)

Bit	Symbol	R/W	Description	Default
7:0	AVG_DATA_L	RO	The measured value of 16 times adc average data(low eight bits)	0

DET_RD3: (Address 51h)

Bit	Symbol	R/W	Description	Default
7:0	ADC_DATA_L	RO	The measured value of 16 times adc average data(low eight bits)	0

I2SCFG1: (Address 52h)

Bit	Symbol	R/W	Description	Default
7	I2S_EN	RW	0: shutdown i2s playback 1: enable i2s playback	0
6:4	SLOT_NUM	RW	I2S TDM mode control(support max to 8 slots): b000: I2S mode b001: TDM1s b010: TDM2s b011: TDM4s b100: TDM6s Others: TDM8s	0
3	I2S_MODE	RW	Mode choose: 0: Philip standard I2S/TDM 1: MSB justified	0
2:0	RX_SLOTVLD	RW	Channel choose, TDM channel slot selection(1~8), only one slot channel valid	0

I2SCFG2: (Address 53h)

Bit	Symbol	R/W	Description	Default
7	CKERR_MASK	RW	0: clock detection 1: 8K/12K/24K has no clock detection	0

6	Reserved	RW	Not used	0
5	WSINV	RW	I2S Left/Right channel switch 0: No switch 1: Left/Right switch	0
4	BCKINV	RW	I2S bit clock invert control 0: not invert 1: inverted	0
3	I2S_INT	RW	0: I2S mode can not be interrupted 1: I2S mode can be interupted	1
2	Reserved	RW	Not used	0
1:0	BCK_MODE	RW	BCK bits of signal WCK channel b00: 16bit b01: 24bit b10: 32bit b11: 32bit	0

UVLOCFG: (Address 56h)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1:0	UVLO_ADJ	RW	UVLO voltage setup: Enter Exit b00: 2.4V 2.5V b01: 2.5V 2.6V b10: 2.6V 2.7V b11: 2.7V 2.8V	3

IDH: (Address 57h)

Bit	Symbol	R/W	Description	Default
7:0	CHIPID_H	RO	High 8 bit of CHIP_ID	0x72

IDL: (Address 58h)

Bit	Symbol	R/W	Description	Default
7:0	CHIPID_L	RO	Low 8 bit of CHIP_ID AW86727:70 AW86728:80	0x70/0x80

TRIMCFG: (Address 59h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:0	TRIM_LRA	RW	Change the frequency of output waveform, and one LSB is 0.24% 0111111: 63xLSB 0111110: 62xLSB …… 0000001: 1xLSB 0000000: 0xLSB 1111111: -1xLSB …… 1000001: -63xLSB 1000000: -64xLSB	0

Application Information

Capacitors Selection

Charge Pump Capacitor Selection

Charge pump output capacitor is usually within the range 0.1μF~47μF. It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically $BaTiO_3$), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

A) temperature stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive; X5R capacitance change within ± 15% in temperature range of -55°C to 85°C, X7R capacitance change within ±15% in temperature range of -55°C~125°C. The Charge pump output capacitance of AW8672X recommends X5R ceramic capacitors.

B) Voltage Stability

Class II type capacitor has poor voltage stability Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take for TDK C series X5R for example, its pressure voltage value is 16V or 25V; the package size is 0805, 1206 or 0603, the capacitance value is 10μF. The capacitor's voltage stability of different types of capacitor is as shown below:

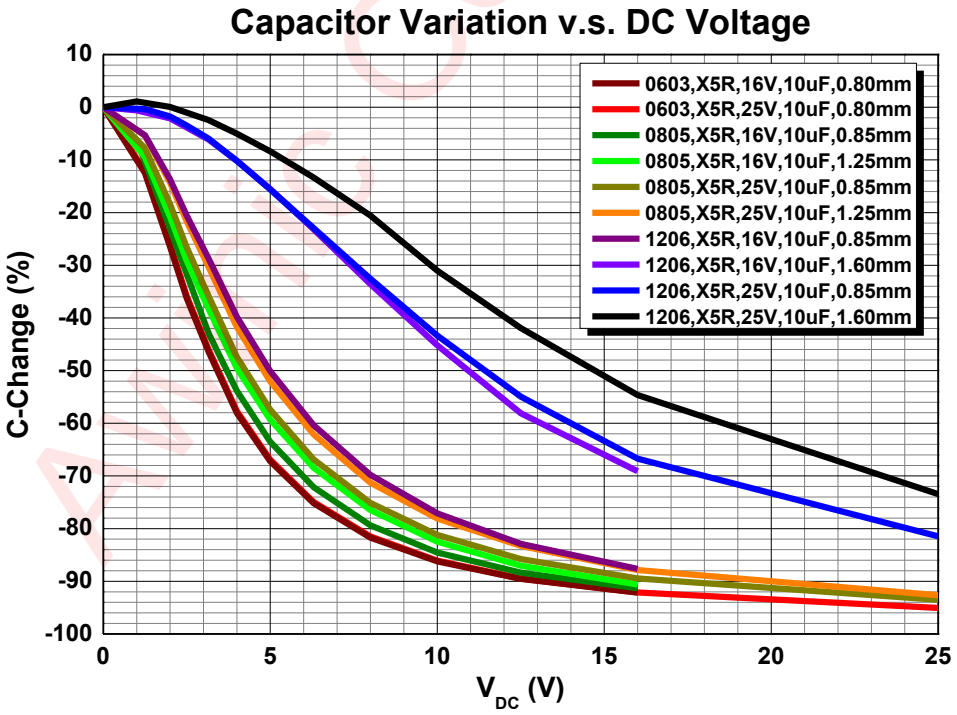


Figure 39 Different types of capacitive voltage stability

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. The higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of

smaller package size (0603) capacitor change affected by the pressure value is very small.
In AW8672X typical applications, it is necessary to ensure the output value of the charge pump capacitor ≥ 2μF when PVDD=8V.

Supply Decoupling Capacitor（C_S）

The device is a high voltage driver that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

Output beads, capacitors

The device output is a square wave signal, which causing switch current at the output capacitor, increasing static power consumption, and therefore output capacitor should not be too large, 0.1nF ceramic capacitors is recommended.

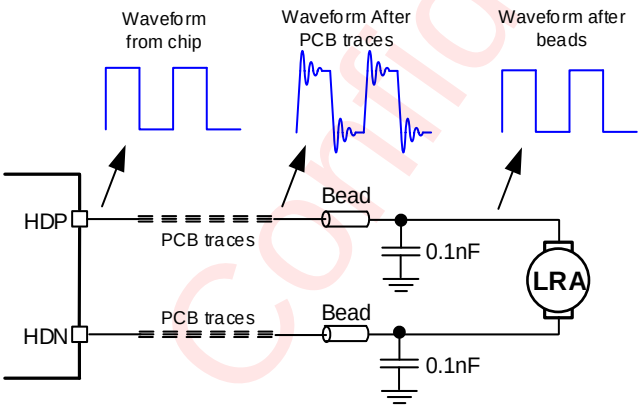


Figure 40 Ferrite Chip Bead and capacitor

The device output is a square wave signal. The voltage across the capacitor will be much larger than the PVDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 16V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 16V.

PCB Layout Consideration

Layout Considerations

This device is a high voltage driver chip. To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

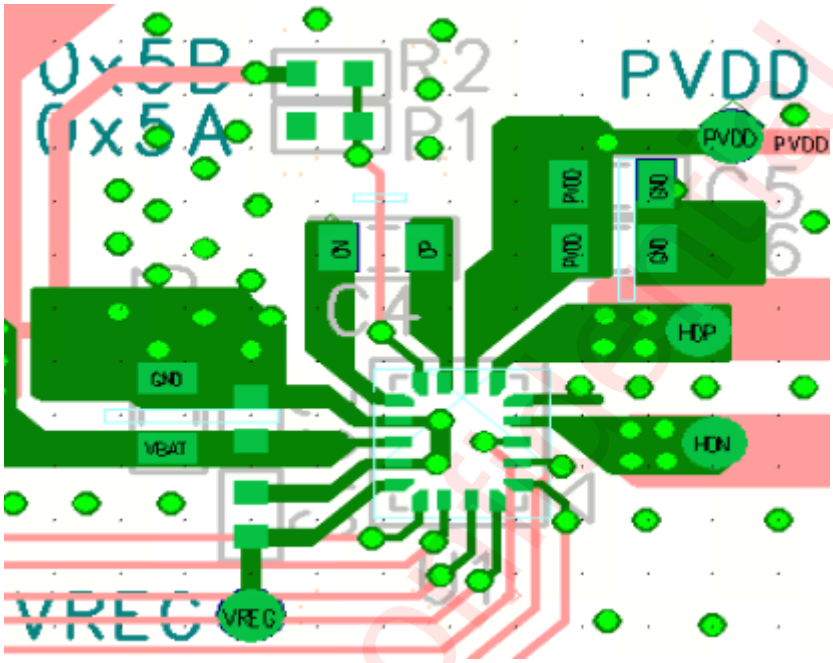


Figure 41 AW86727 Board Layout

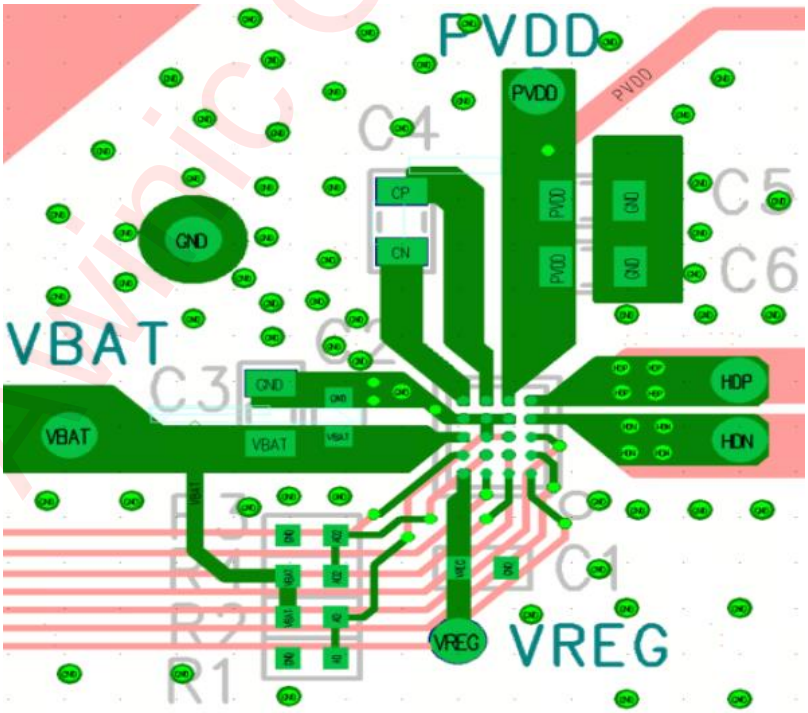


Figure 42 AW86728 Board Layout

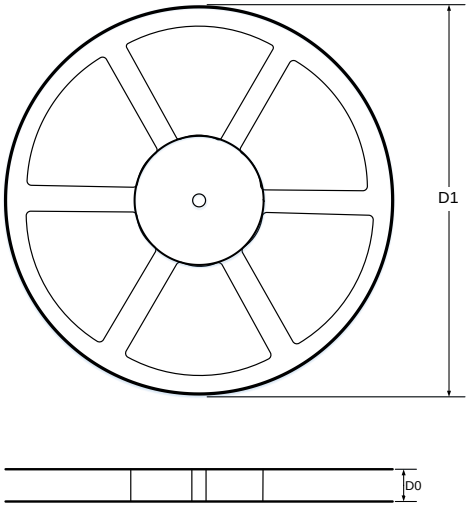
Here are some guidelines:

1. All of the external components should be placed as close as possible to IC in top layer PCB.
2. SCL and SDA should be shield by ground.
3. C2 and C3 should be placed close to VBAT pin of IC.
4. C5 and C6 are within 1.5mm to pin PVDD , and the overcurrent capability of the PVDD traces must be meet $\frac{PVDD}{R_L+R_{DSON}}$, and the GND side of the PVDD capacitor should be directly connected to surface layer ground or punched to the main ground of the PCB. In addition, create solid GND plane near and around the IC, connect BGND, PGND and GND together, and the overcurrent capability of the via should be designed according to the PVDD overcurrent capability.
5. Routing overcurrent capability of HDP/HDN output to the load should meet $\frac{PVDD}{R_L+R_{DSON}}$. HDP and HDN should be shield by ground and far away from the interference source especially the FLY capacitor of the high-power charging IC, otherwise it will cause the abnormal F0 detection.

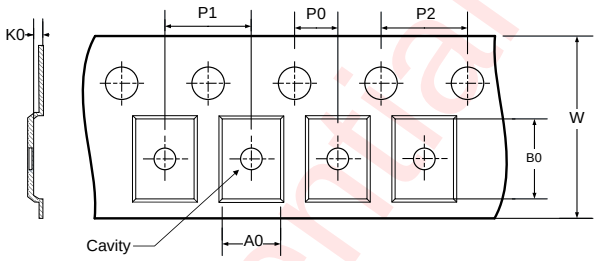
Tape And Reel Information

AW86727FCR:

REEL DIMENSIONS

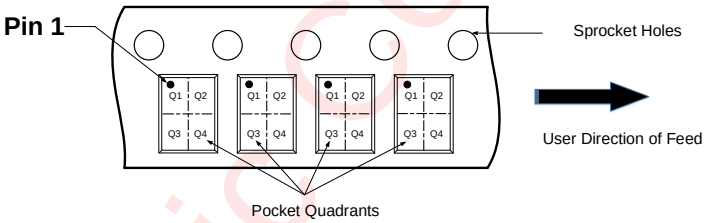


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

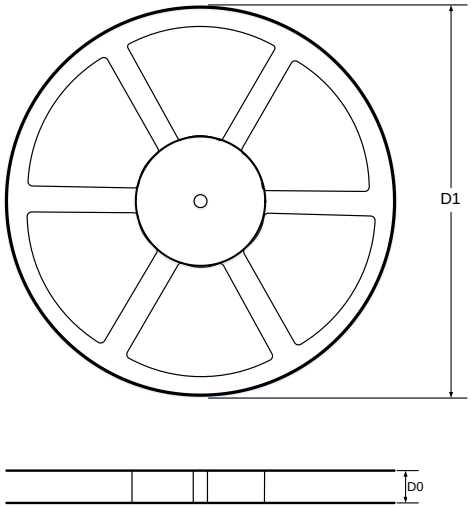
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	2.2	2.67	0.83	2	8	4	12	Q1

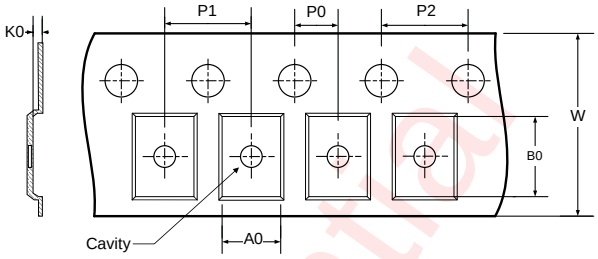
All dimensions are nominal

AW86728CSR:

REEL DIMENSIONS

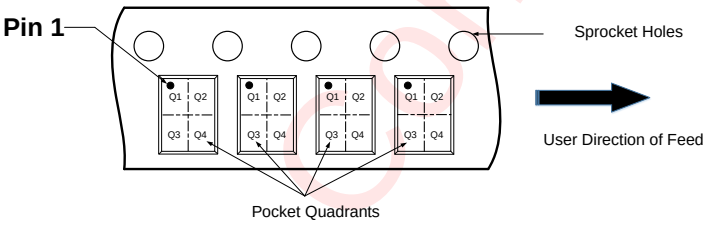


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

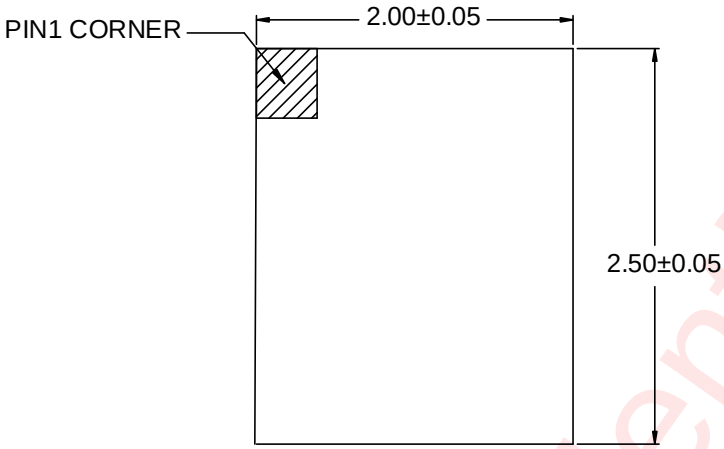
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	8.6	1.86	2.36	0.72	2	4	4	8	Q1

All dimensions are nominal

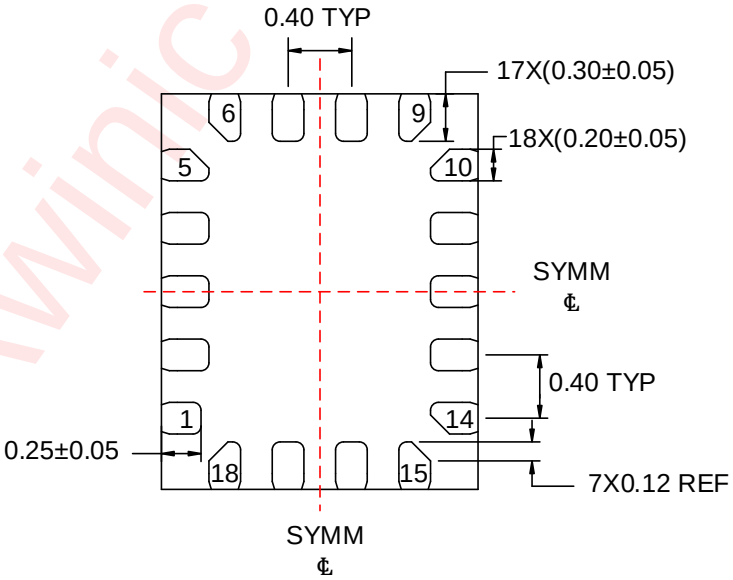
Package Description

AW86727FCR:



Top View

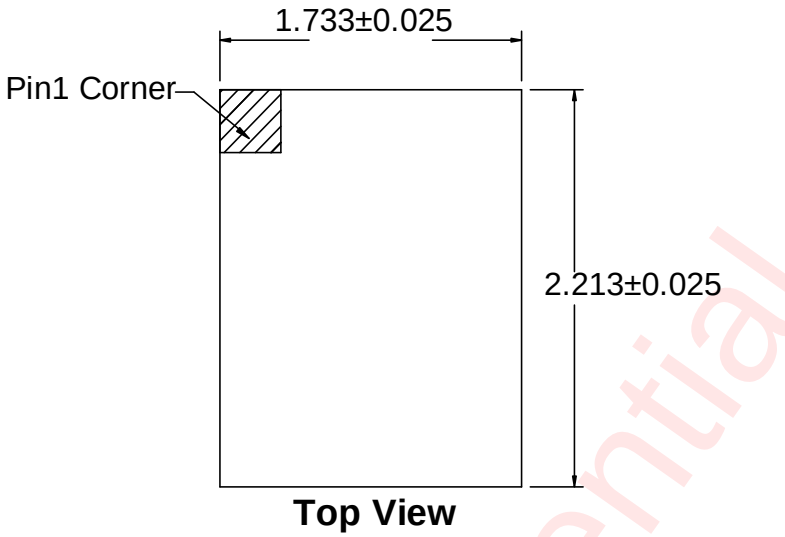
Side View



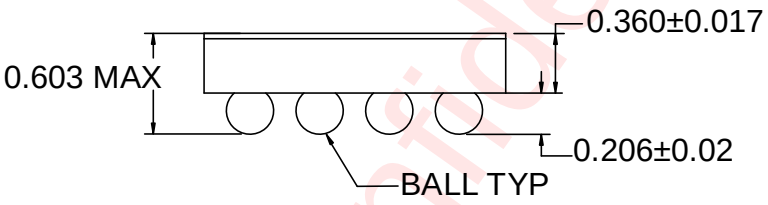
Bottom View

Unit:mm

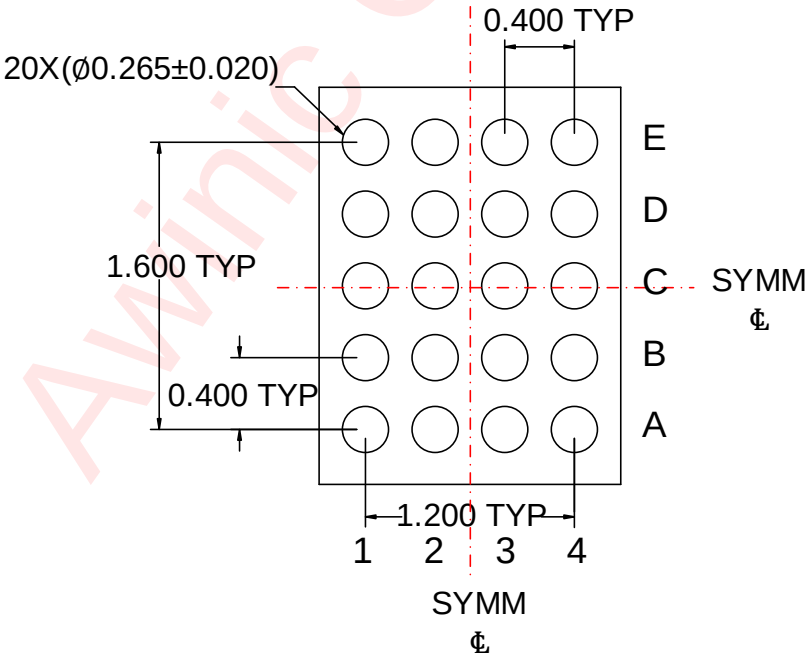
AW86728CSR:



Top View



Side View

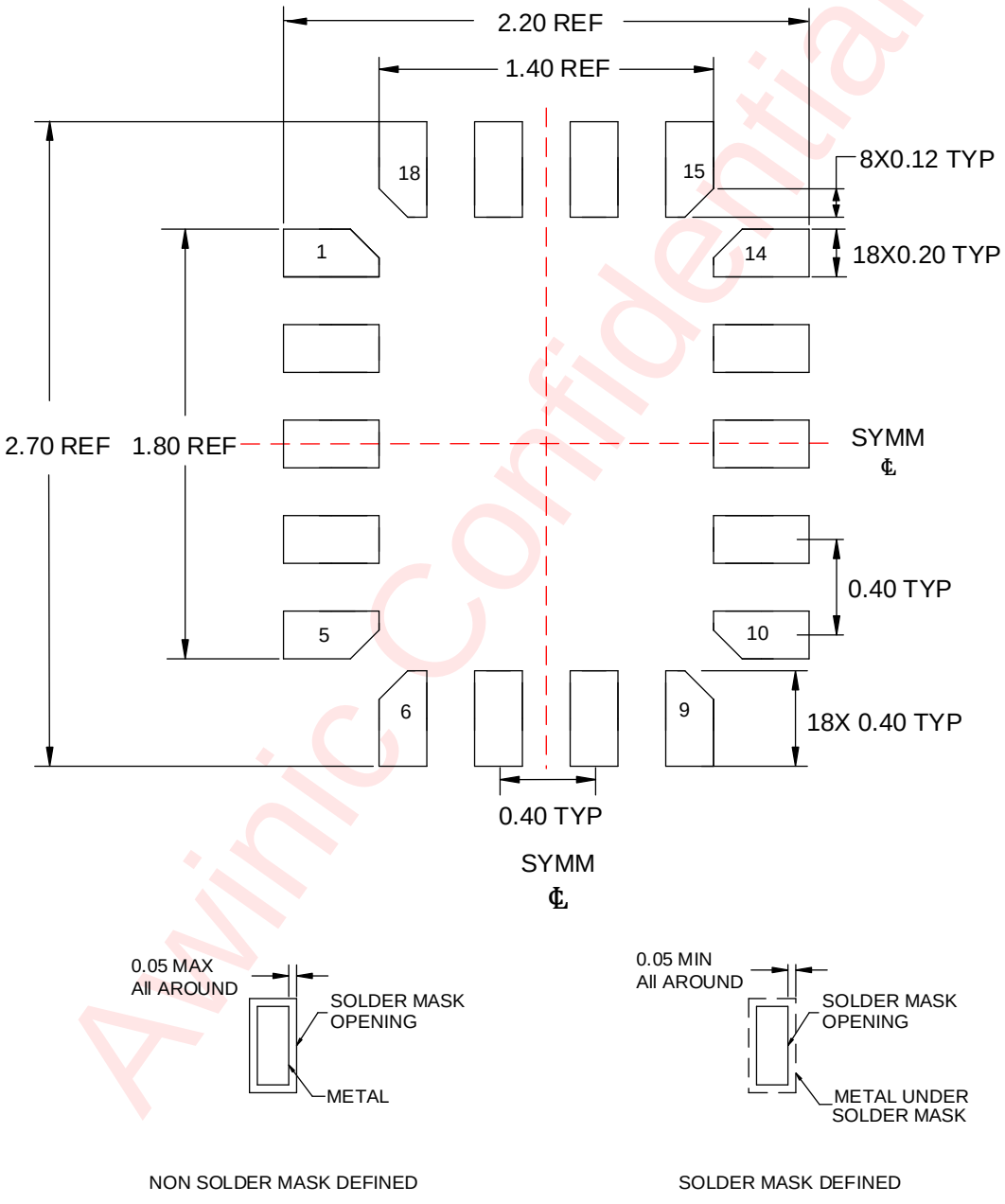


Bottom View

Unit：mm

Land Pattern Data

AW86727FCR:



Unit:mm

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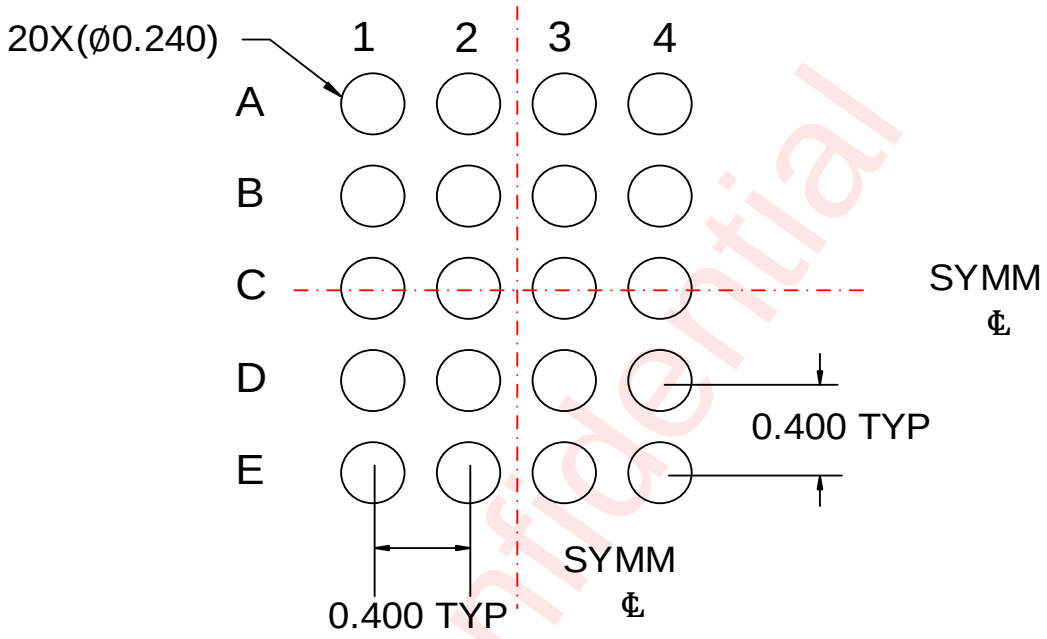
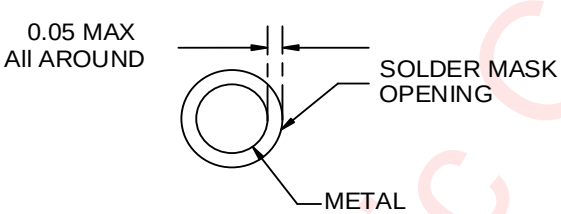
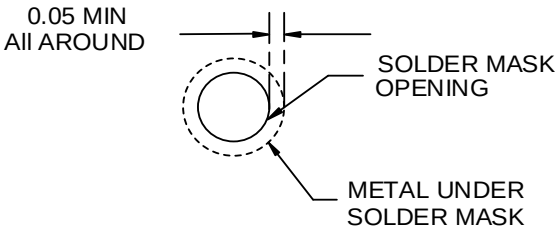




NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	October 2023	Initial Version
V1.1	October 2023	Modify Register List Modify Register Detailed Description
V1.2	January 2024	Add part number including immersion IP license
V1.3	November 2024	Delete duplicate parts of the typical application circuit

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