钍地半导体
Tudi Semiconductor

Product Specification

TUDI-TRS202E

具有 ±15kV IEC ESD 保护功能的 5V 双路 RS-232 线路驱动器和接收器

网址 www.sztdbdt.com

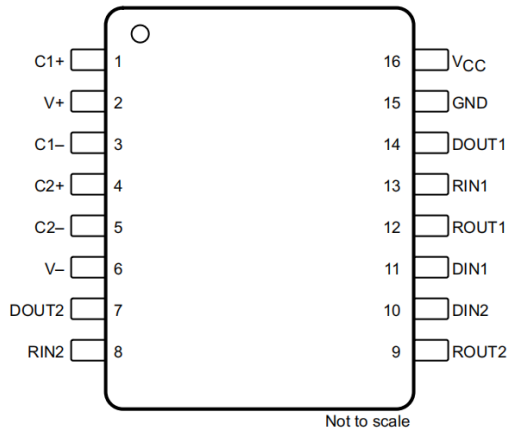
用芯智造 · 卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

特性

●用于 RS-232 总线引脚的
IEC61000-4-2（4 级）ESD 保护：
– ±8kV 接触放电
– ±15kV 气隙放电
– ±15kV 人体放电模型
●符合或超出 TIA/EIA-232-F 和
ITU v.28 标准的要求
● 由 5V V_{CC} 电源供电
● 速率高达 120kbit/s
● 外部电容器：4 个 0.1μF 或 4 个 1μF
●闩锁性能超过 100mA，
符合 JESD 78 II 级规范



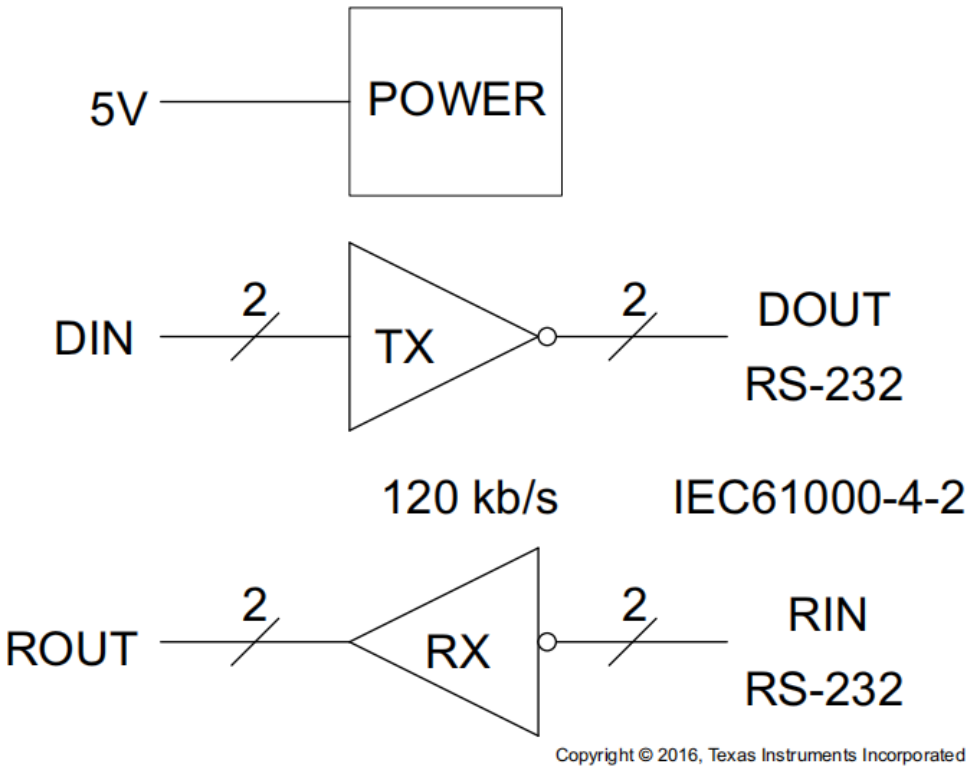
D, DW, N or PW Package, 16-Pin SOIC or TSSOP
(Top View)

应用

●电池供电型系统
● 笔记本电脑
●便携式计算机
● 机顶盒
●手持设备

说明

TRS202E 由两个线路驱动器、两个线路接收器和一个 双路电荷泵电路组成。TRS202E 具有 IEC61000-4-2（4 级）ESD 引脚对引脚（串行端口连接引脚，包括 GND）保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。 电荷泵和四个小型外部电容器支持由单个 5V 电源供电。该器件以高达 120kbit/s 的数据信号传输速率和最高 30V/μs 的驱动器输出压摆率运行。



逻辑图（正逻辑）

表 **4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	V+	O	Positive charge pump output for storage capacitor only
3	C1 –	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2 –	—	Negative lead of C2 capacitor
6	V –	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	V_{CC}	—	Supply voltage, connect to external 5-V power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		-0.3	6	V
Positive charge pump voltage, V+(2)		V_{CC} - 0.3	14	V
Negative charge pump voltage, V-		-14	0.3	V
Input voltage, V_I	Drivers	-0.3	V+ + 0.3	V
	Receivers		±30	
Output voltage, V_O	Drivers	V- - 0.3	V+ + 0.3	V
	Receivers	-0.3	V_{CC} + 0.3	
Short-circuit duration, D_{OUT}		Continuous		
Operating virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 7, 8, 13, 14, 15	±15000	V
			All other pins	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	
		IEC 61000-4-2 contact discharge	Pins 7, 8, 13, 14, 15	±8000	
		IEC 61000-4-2 air-gap discharge	Pins 7, 8, 13, 14, 15	±15000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

see 图 7-1 (1)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage (D_{IN})		2			V
V_{IL}	Driver low-level input voltage (D_{IN})				0.8	V
V_I	Driver input voltage (D_{IN})		0		5.5	V
	Receiver input voltage		-30		30	
T_A	Operating free-air temperature	TRS202EC	0		70	°C
		TRS202EI	-40		85	

(1) Test conditions are C1 to C4 = 0.1µF at V_{CC} = 5V ±0.5V.

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	DW (SOIC) 16 PINS	N (PDIP) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	77.1	44.1	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	39.9	30.8	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	41.8	24.2	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	12.9	15.2	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	41.3	24	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see 图 7-1)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 5V		8	15	mA

(1) Test conditions are C1 to C4 = 0.1μF at V_{CC} = 5V + 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.

5.6 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 7-1)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	D_{OUT} at R_L = 3kΩ to GND, D_{IN} = GND	5	9		V
V_{OL}	Low-level output voltage	D_{OUT} at R_L = 3kΩ to GND, D_{IN} = V_{CC}	− 5	− 9		V
I_{IH}	High-level input current	V_I = V_{CC}		15	200	μA
I_{IL}	Low-level input current	V_I at 0V		− 15	− 200	μA
I_{OS} (3)	Short-circuit output current	V_{CC} = 5.5V and V_O = 0V		±10	±60	mA
r_o	Output resistance	V_{CC}, V+, V − = 0V, and V_O = ±2V	300			Ω

(1) Test conditions are C1 to C4 = 0.1μF at V_{CC} = 5V + 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output must be shorted at a time.

5.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see 图 7-1)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = − 1mA	3.5	V_{CC} − 0.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5V and T_A = 25°C		1.7	2.4	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 5V and T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis (V_{IT+} − V_{IT-})		0.2	0.5	1	V
r_i	Input resistance	V_I = ±3V to ±25V	3	5	7	kΩ

(1) Test conditions are C1 to C4 = 0.1μF at V_{CC} = 5V + 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.

5.8 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see 图 7-1)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 50 to 1000pF, one D_{OUT} switching, and R_L = 3kΩ to 7kΩ (see 图 6-1)	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	C_L = 2500pF, all drivers loaded, and R_L = 3kΩ (see 图 6-1)		2		µs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	C_L = 2500pF, all drivers loaded, and R_L = 3kΩ (see 图 6-1)		2		µs
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 to 2500pF and R_L = 3kΩ to 7kΩ (see 图 6-2)		300		ns
SR(tr)	Slew rate, transition region	C_L = 50 to 1000pF, V_{CC} = 5V, and R_L = 3kΩ to 7kΩ (see 图 6-1)	3	6	30	V/µs

(1) Test conditions are C1 to C4 = 0.1µF at V_{CC} = 5V + 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.9 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see 图 6-3)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150pF		0.5	10	µs
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150pF		0.5	10	µs
$t_{sk(p)}$	Pulse skew(3)			300		ns

(1) Test conditions are C1 to C4 = 0.1µF at V_{CC} = 5V + 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.4.3 Truth Tables

表 6-1 and 表 6-2 list the function for each driver and receiver (respectively).

表 6-1. Function Table for Each Driver

INPUT DIN(1)	OUTPUT DOUT
L	H
H	L

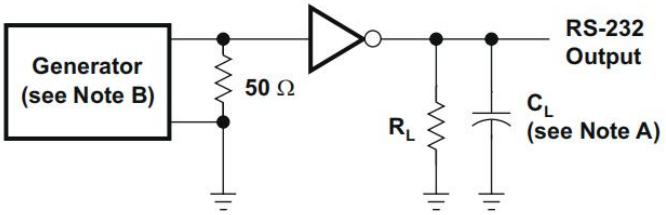
(1) H = high level, L = low level

表 6-2. Function Table for Each Receiver

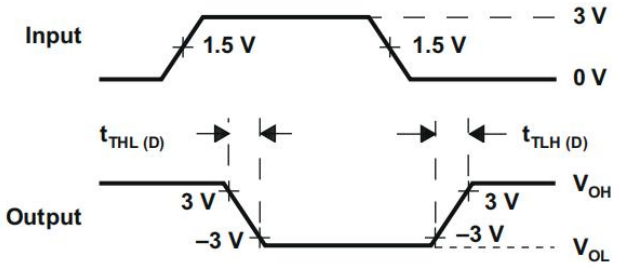
INPUT RIN(1)	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

Parameter Measurement Information



TEST CIRCUIT

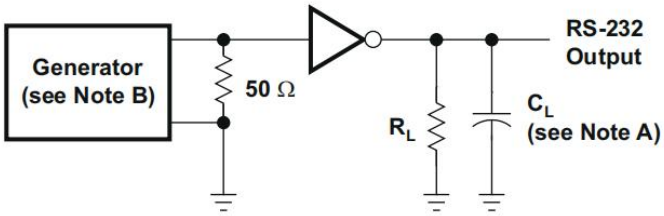


VOLTAGE WAVEFORMS

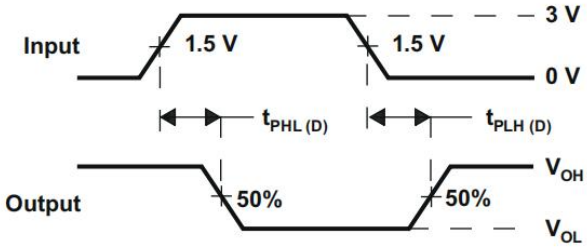
$$SR(t_f) = \frac{6\ V}{t_{THL(D)} \text{ or } t_{TLH(D)}}$$

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

图 6-1. Driver Slew Rate



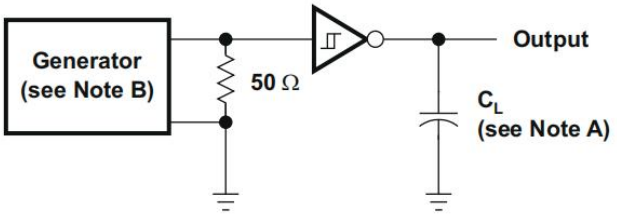
TEST CIRCUIT



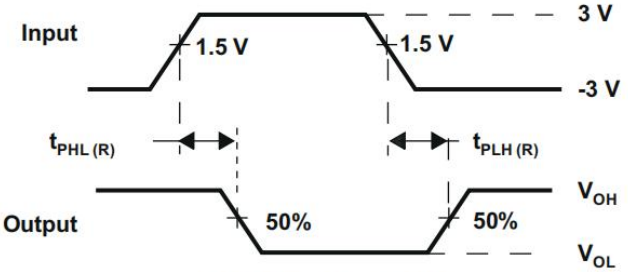
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

图 6-2. Driver Pulse Skew



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

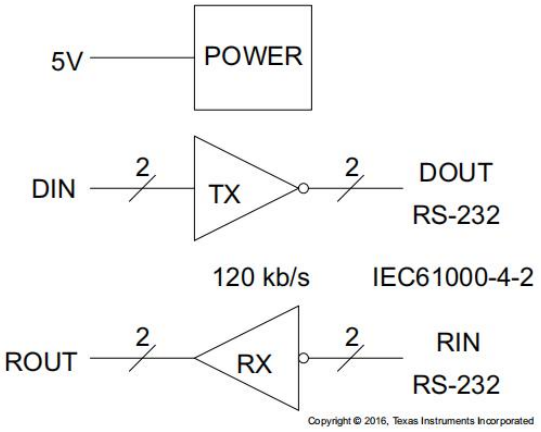
图 6-3. Receiver Propagation Delay Times

6 Detailed Description

6.1 Overview

The TRS202E device is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5V supply. All RS-232 pins have 15kV HBM and IEC61000-4-2 Air-Gap discharge protection. RS-232 pins also have 8-kV IEC61000-4-2 contact discharge protection. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to ±30V inputs and decode inputs as low as ±3V. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power

The power block increases and inverts the 5V supply for the RS-232 driver using a charge pump that requires four 0.1μF or 1μF external capacitors.

6.3.2 RS-232 Driver

Two drivers interface standard logic levels to RS-232 levels. The driver inputs do not have internal pullup resistors. Do not float the driver inputs.

6.3.3 RS-232 Receiver

Two Schmitt trigger receivers interface RS-232 levels to standard logic levels. Each receiver has an internal 5-kΩ load to ground. An open input results in a high output on R_{OUT}.

6.4 Device Functional Modes

6.4.1 V_{CC} Powered by 5V

The device is in normal operation when powered by 5V.

6.4.2 V_{CC} Unpowered

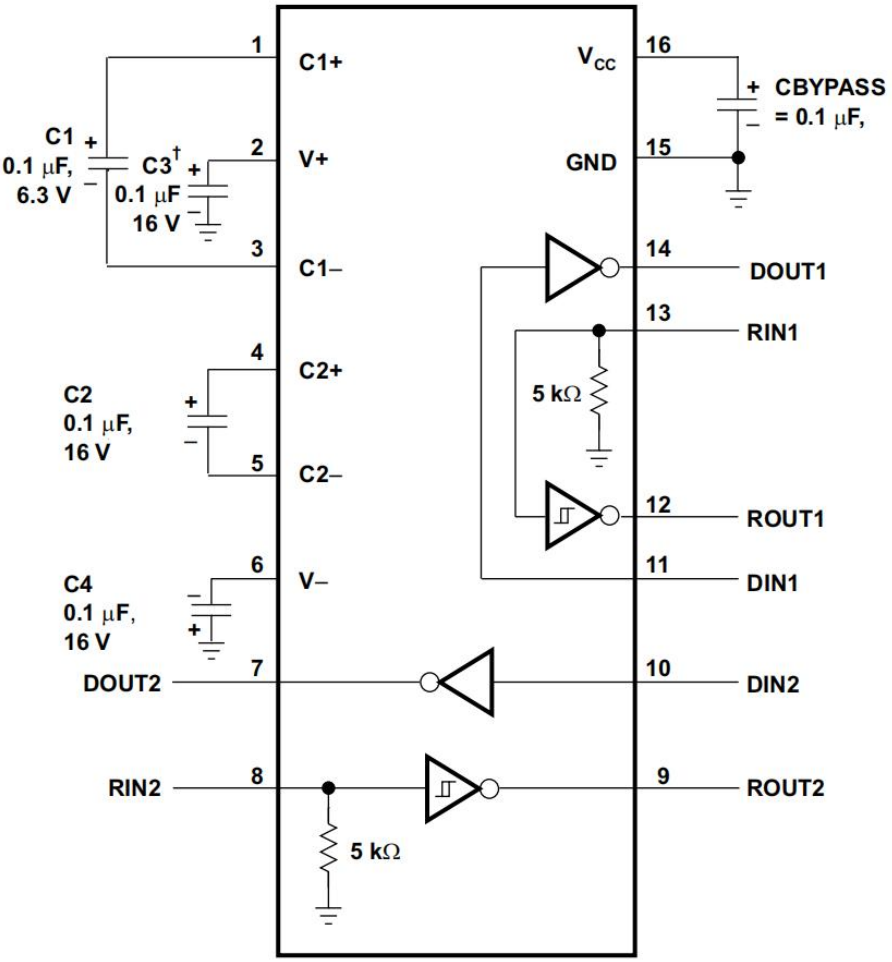
When TRS202E is unpowered, it can be safely connected to an active remote RS-232 device.

7.1 Application Information

For proper operation, add capacitors as shown in 图 7-1. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

7.2 Typical Application

Two driver and two receiver channels are supported for full duplex transmission with hardware flow control. The two 5kΩ-resistors are internal to the TRS202E.



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

图 7-1. Typical Operating Circuit and Capacitor Values

7.2.1 Design Requirements

- V_{CC} minimum is 4.5V and maximum is 5.5V.
- Maximum recommended bit rate is 120kbps.

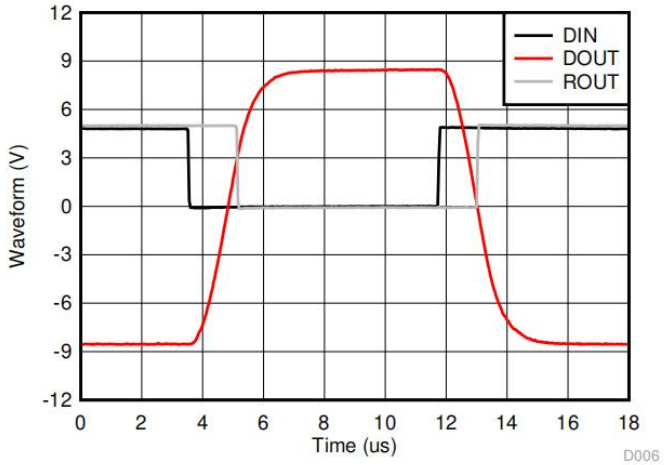
7.2.2 Detailed Design Procedure

7.2.2.1 Capacitor Selection

The capacitor type used for C1 through C4 is not critical for proper operation. The TRS202E requires 0.1μF capacitors. 1-μF capacitors are also acceptable. TI recommends ceramic dielectrics. When using the minimum recommended capacitor values, ensure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V－.

Bypass V_{CC} to ground with at least 0.1μF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

7.2.3 Application Curves



120 kbit/s, 1-nF load

图 **7-2. Driver and Receiver Loopback Signal**

7.3 Power Supply Recommendations

The V_{CC} voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} must be between 4.5V and 5.5V.

7.4 Layout

7.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from TRS202E ground pin and circuit boards ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

7.4.2 Layout Example

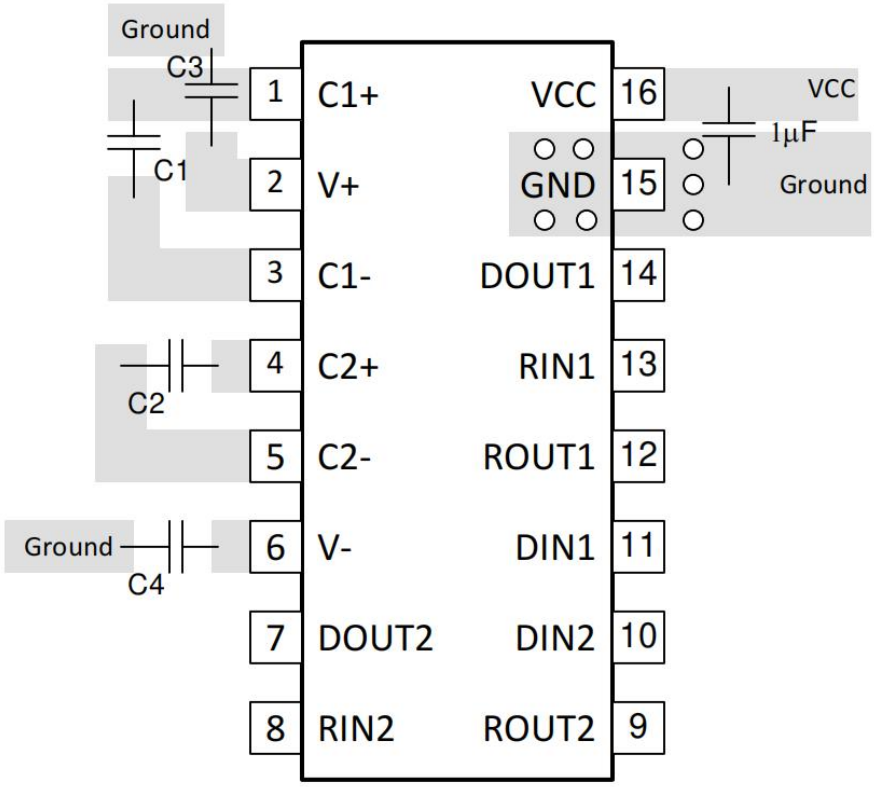
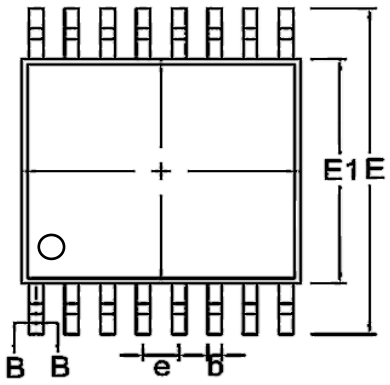


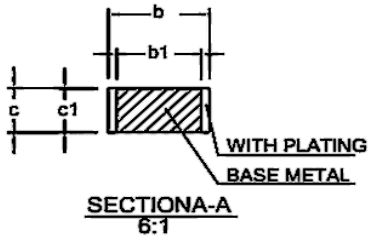
图 **7-3. TRS202E Layout**

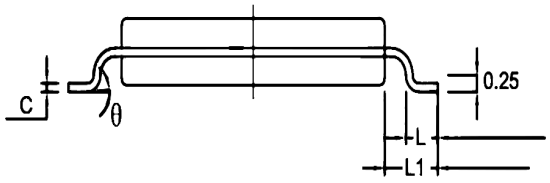
Order information

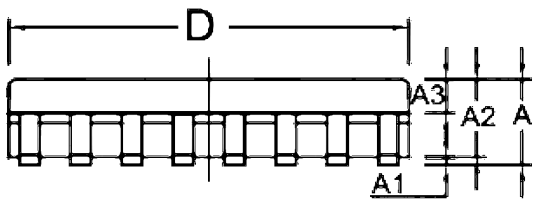
Order Number	Package	Package Quantity	Marking On The park
TRS202ECPWR-TUDI	TSSOP16	Tape,Reel,2500	TRS202ECPWR
TRS202EIPWR-TUDI	TSSOP16	Tape,Reel,2500	TRS202EIPWR

Package TSSOP16









SIZE / SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	--	--	1.20
A1	0.05		0.15
A2	0.90	1.00	1.05
b	0.20	--	0.30
b1	0.19	0.22	0.25
C	0.110	0.127	0.145
cl	0.12	0.13	0.14
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
	0°	--	8°

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