

30V 80A N-Channel MOSFET

Features

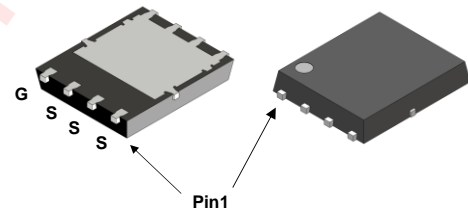
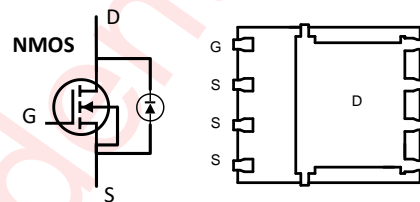
- Advanced shielded-gate technology
- Ultra-low on-resistance and gate-charge
- RoHS compliant
- 100% UIS tested
- 100% R_g tested
- DFN 5mmX6mmX1.1mm-8L Package

Applications

- Motor controllers
- DC-to-DC converters
- Battery-driven electronic products, electrical equipment and machines

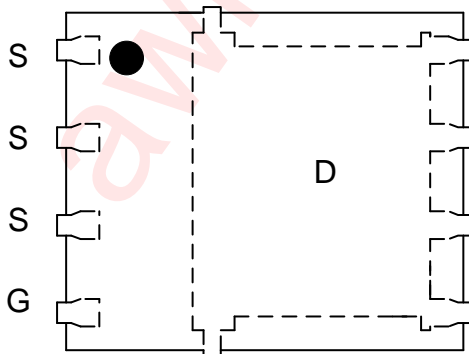
General Description

Product Summary	
V _{DS}	30V
R _{DS(ON)}	2.5mΩ (Typ.)@10V
	3.4mΩ (Typ.)@4.5V
I _D	80A

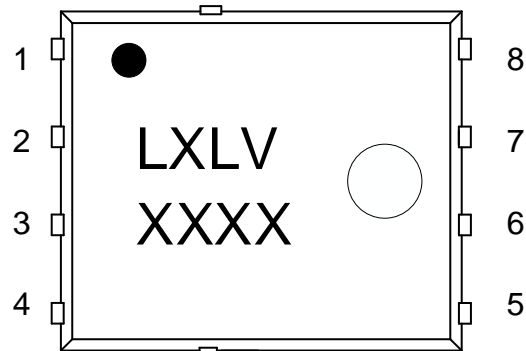


Pin Configuration And Top Mark

AW403004NDNR
(Top View)



AW403004NDNR Marking
(Top View)



LXLV-AW403004NDNR
XXXX-Production Tracing Code

Ordering Information

Part Number	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW403004NDNR	DFN 5mmX6mmX 1.1mm-8L	LXLV	MSL3	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings (NOTE 1)

T_A= 25°C unless otherwise noted

Symbol	Parameter	Maximum	Unit	
V _{DS}	Drain-Source Voltage	30	V	
V _{GS}	Gate-Source Voltage	±16	V	
I _D	Drain Current(DC) (NOTE 6)	T _C = 25°C	80	A
	Drain Current(DC) (NOTE 7)	T _C = 100°C	60	A
I _{DM}	Drain Current(Pulse) (NOTE 3)	320	A	
P _D	Power Dissipation (T _C = 25°C)	48	W	
T _J	Maximum Operating Junction Temperature	150	°C	
T _{STG}	Storage Temperature	-55 to 150	°C	
I _{AS}	Avalanche Current (NOTE 5)	42	A	
E _{AS}	Avalanche Energy (NOTE 5)	88	mJ	

Thermal Information

Symbol	Parameter	Condition	Value	Unit
R _{θJA}	Maximum Junction to Ambient (NOTE 2, 4)	Steady-State	54	°C/W
R _{θJC}	Maximum Junction-to-Case	Steady-State	2.6	°C/W

NOTE 1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE 2: Mounted on FR-4 material with 1inch², 2oz. Copper.

NOTE 3: Test condition 380μs 25°C.

NOTE 4: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE 5: L= 0.1mH, V_{GS}= 10V, R_g= 25Ω, V_{DS}= 15V.

NOTE 6: Limited by package.

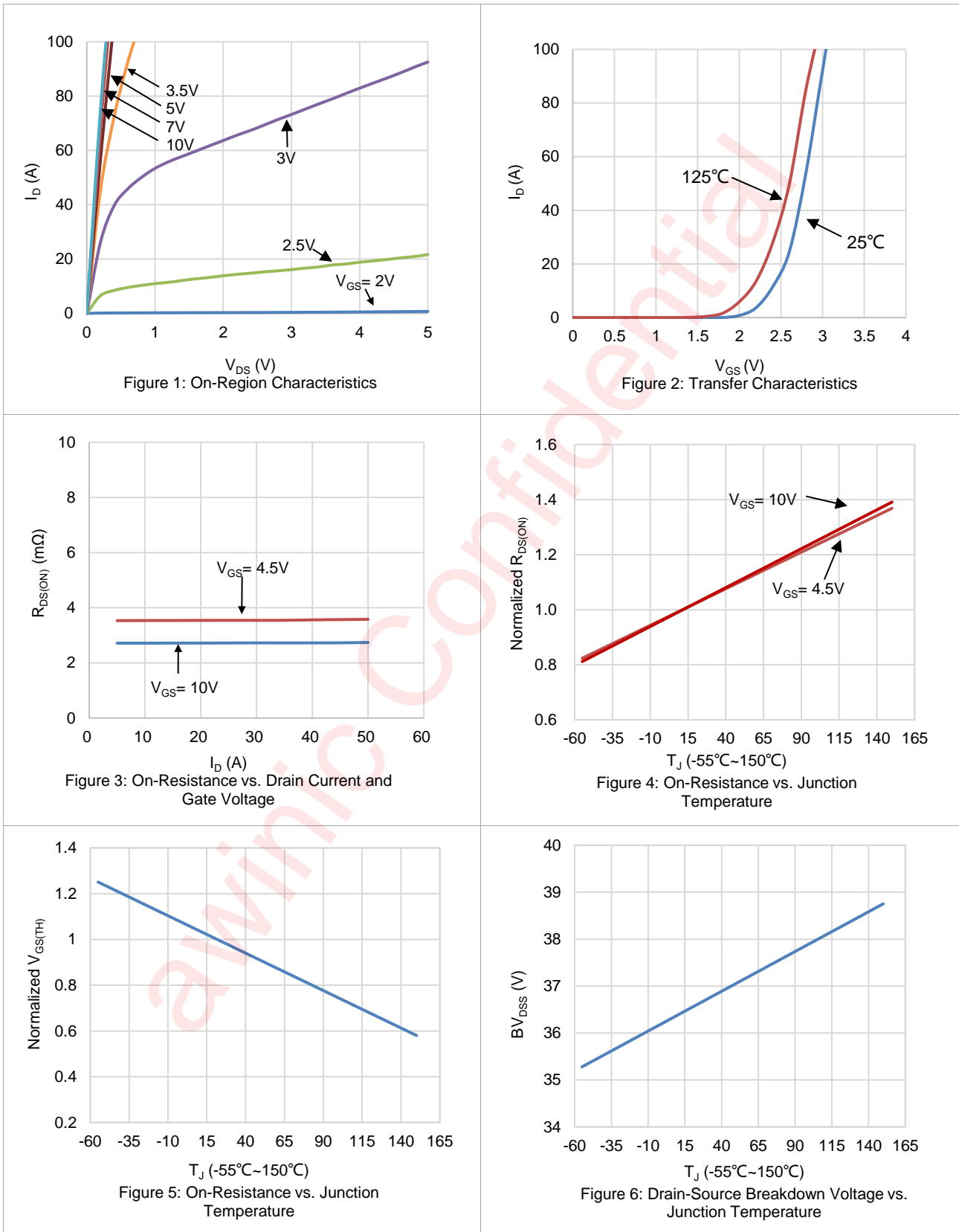
NOTE 7: Rated according to R_{θJC}.

Electrical Characteristics

$T_J = 25^\circ\text{C}$ for typical values (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate Leakage Current	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 16\text{V}$	-	-	± 100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1.0	-	2.2	V
$R_{DS(ON)}$	Static Drain to Source On-Resistance	$V_{GS} = 10\text{V}$, $I_D = 20\text{A}$	-	2.5	3.3	m Ω
		$V_{GS} = 4.5\text{V}$, $I_D = 20\text{A}$	-	3.4	4.8	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}$, $I_D = 20\text{A}$	-	90	-	S
V_{SD}	Diode Forward Voltage	$I_S = 1\text{A}$, $V_{GS} = 0\text{V}$	-	0.7	-	V
DYNAMIC PARAMETERS						
R_g	Gate Resistance	$f = 1\text{MHz}$	-	3.5	-	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 15\text{V}$, $f = 1\text{MHz}$	-	2200	-	pF
C_{oss}	Output Capacitance		-	1050	-	pF
C_{rss}	Reverse Transfer Capacitance		-	50	-	pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS} = 10\text{V}$, $V_{DS} = 15\text{V}$, $I_D = 20\text{A}$	-	30	-	nC
Q_{gs}	Gate Source Charge		-	6	-	nC
Q_{gd}	Gate Drain Charge		-	5.5	-	nC
$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 15\text{V}$, $I_D = 20\text{A}$, $R_g = 3\Omega$, $V_{GS} = 10\text{V}$	-	11	-	ns
t_r	Turn-On Rise Time		-	5.6	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	35	-	ns
t_f	Turn-Off Fall Time		-	10.5	-	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_D = 10\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$	-	24	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_D = 10\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$	-	30	-	nC

Typical Electrical and Thermal Characteristics



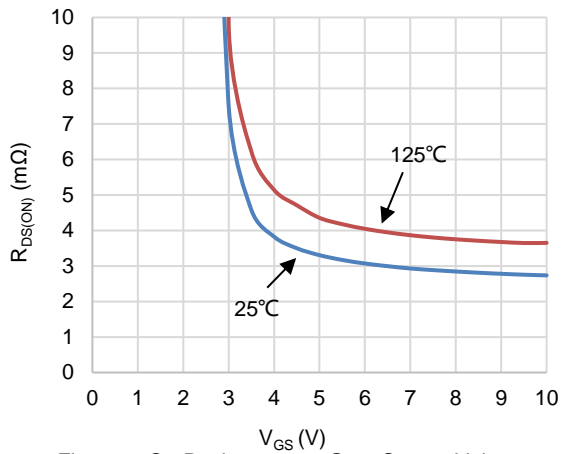


Figure 7: On-Resistance vs. Gate-Source Voltage

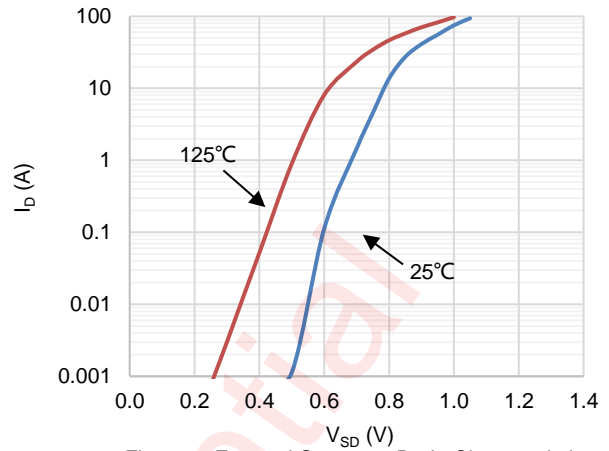


Figure 8: Forward Source to Drain Characteristics

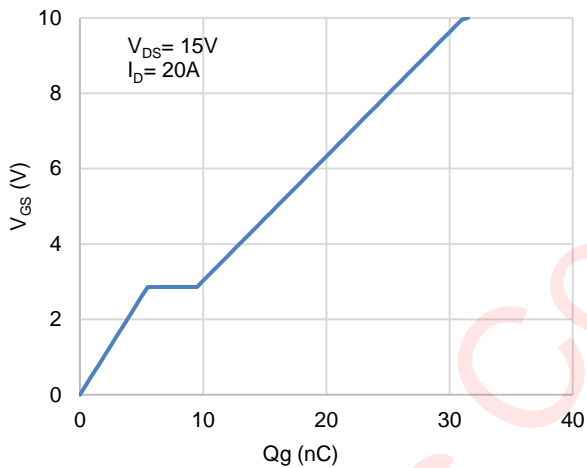


Figure 9: Gate-Charge Characteristics

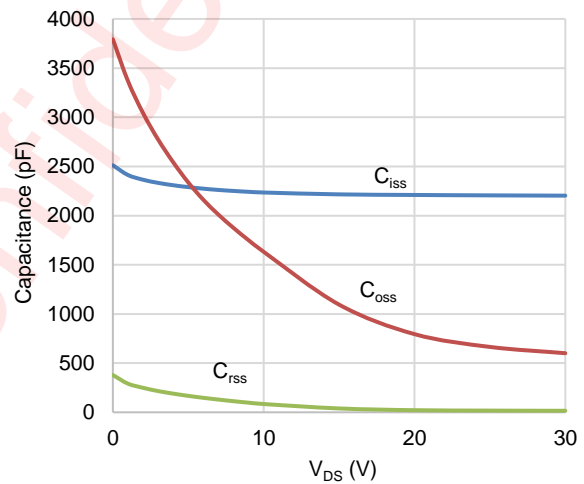


Figure 10: Capacitance Characteristics

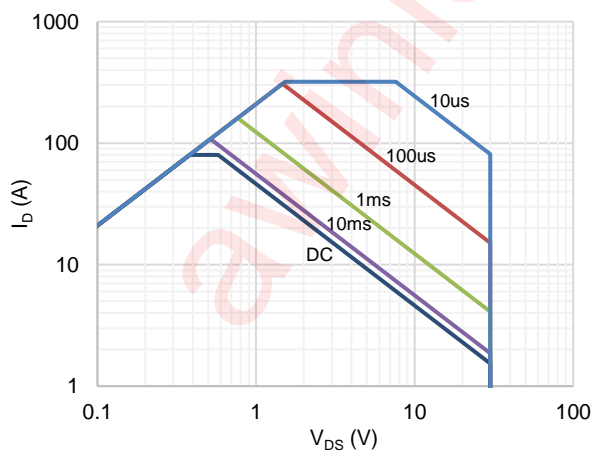


Figure 11: Maximum Forward Biased Safe Operating Area

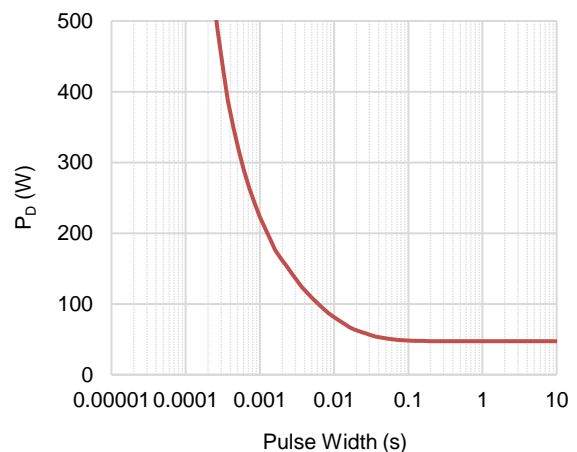
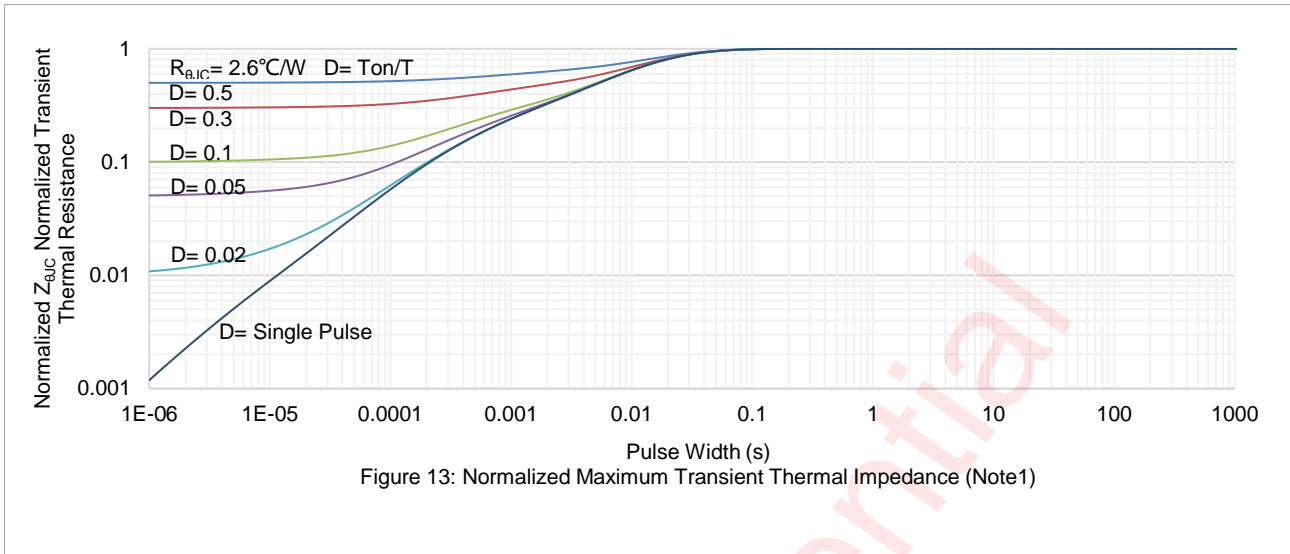
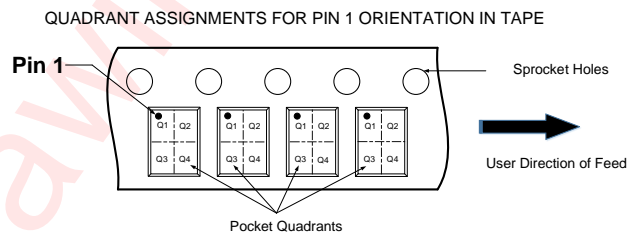
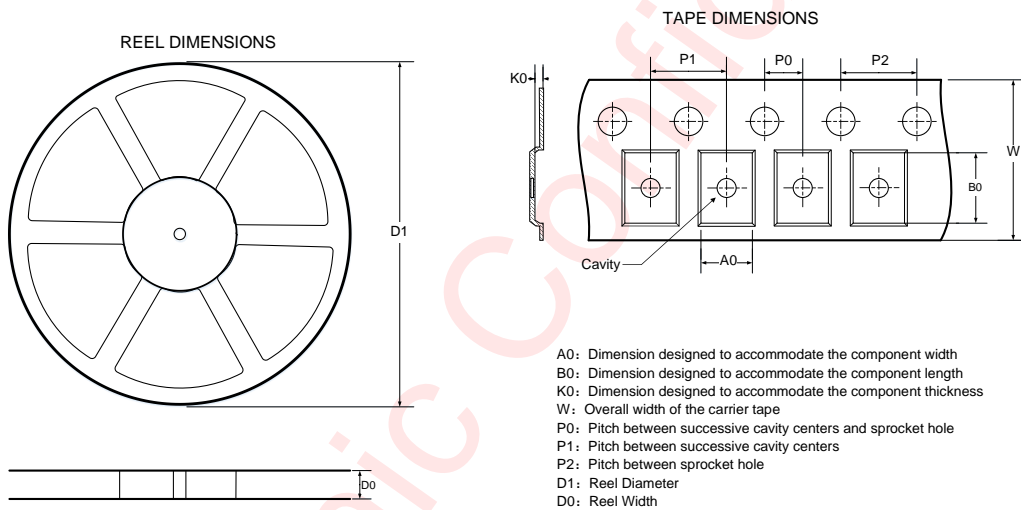


Figure 12: Single Pulse Power Rating Junction-to-Case



Tape And Reel Information

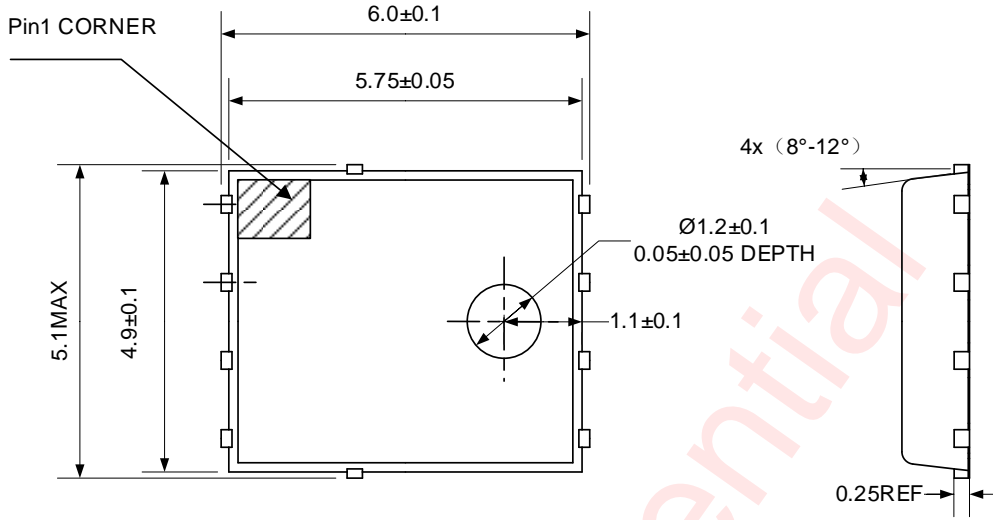


Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION									
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	6.45	5.3	1.4	2	8	4	12	Q1

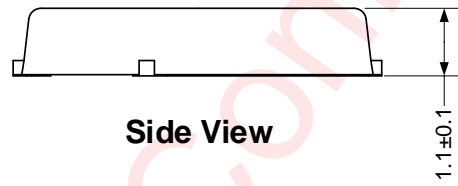
All dimensions are nominal

Package Description

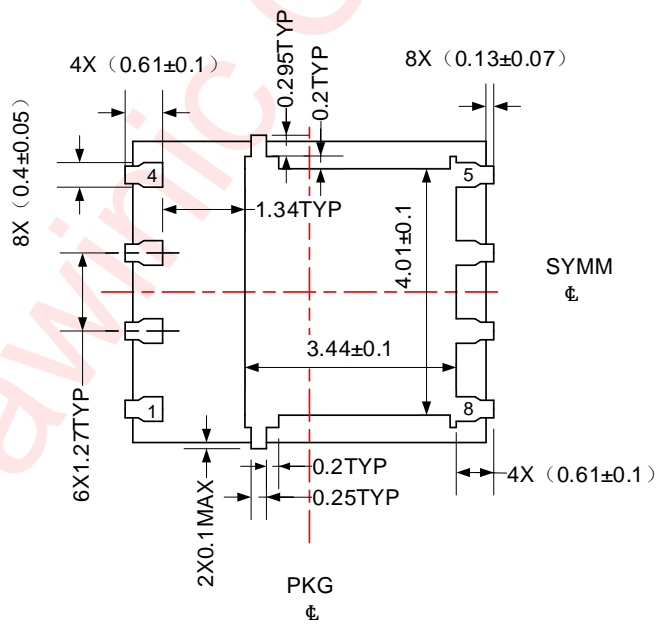


Top View

Side View



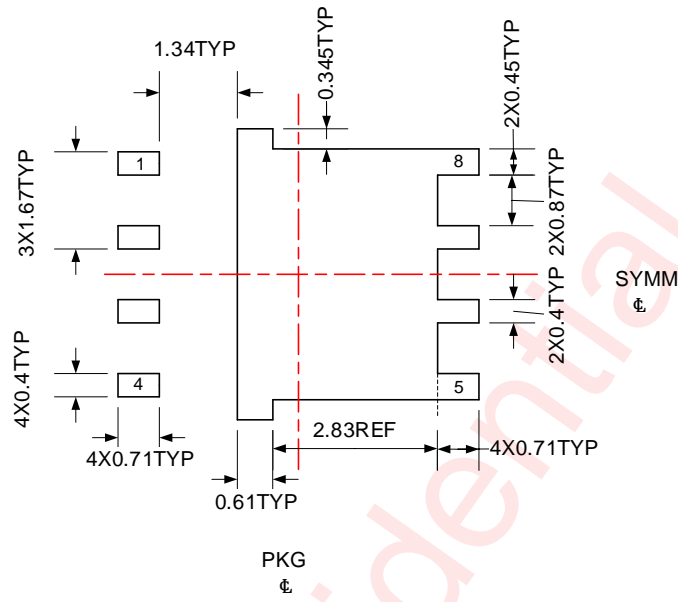
Side View



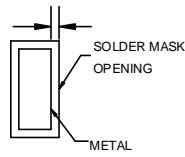
Bottom View

Unit: mm

Land Pattern Data

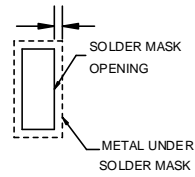


0.05 MAX
All AROUND



NON SOLDER MASK DEFINED

0.05 MIN
All AROUND



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Nov. 2022	Official released

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