# XPA5991

16-V Input, 50-A, 1mΩ $R_{DS\_ON}$, Hot-Swap Efuse

## FEATURES

- 4V to 16V Operating Input Range
- Maximum 50A Output Current
- Maximum 60A Output Current with Air Flow
- Integrated Power FET with 1mΩ $R_{DS\_ON}$
- Built-In MOSFET Driver
- ±1% Current Monitor Accuracy
- Integrated Current Sense with Sense Output
- Adjustable Over-current Limit
- Adjustable Short-circuit Current Limit
- 3.3V LDO Output
- Built-In Insertion Delay
- External adjustable Soft Start (SS)
- Output Short-circuit Protection (SCP)
- Thermal Protection (OTP)
- Efuse Health Reporting
- Fault Signal Output (GOK)
- Fault Type Indication (FLT_TYPE)
- Supports Parallel Operation for High-Current Applications
- Integrated Intelli-Fuse Temperature Sense
- Available in LGA-32 (5mmx5mm) Package

## APPLICATIONS

- Servers
- Hot Swap
- Laptops
- Disk Drives
- Networking

## DESCRIPTION

The XPA5991 is a powerfet-integrated hot-swap/Efuse device designed to protect its load circuitry from input transients. It also prevents the input from unwanted shorts and transients coming from the output. It can supply high to 50A continuous output current at room temperature, and up to 60A with air flow.

You can parallel multiple XPA5991 parts to get extreme large output current. The current balance loop could balance the inrush current at softstart.

The gate of the power device is driven by a built-in charge pump, enabling a very low RDS_ON of 1mΩ.

Full protection features include current limit (OCP), short-circuit protection (SCP), thermal shutdown (TSD), damaged MOSFET detection, over-voltage protection (OVP), and under-voltage lockout (UVLO).

XPA5991 is available in LGA-32 (5mmx5mm) package.

# FUNCTIONAL BLOCK DIAGRAM

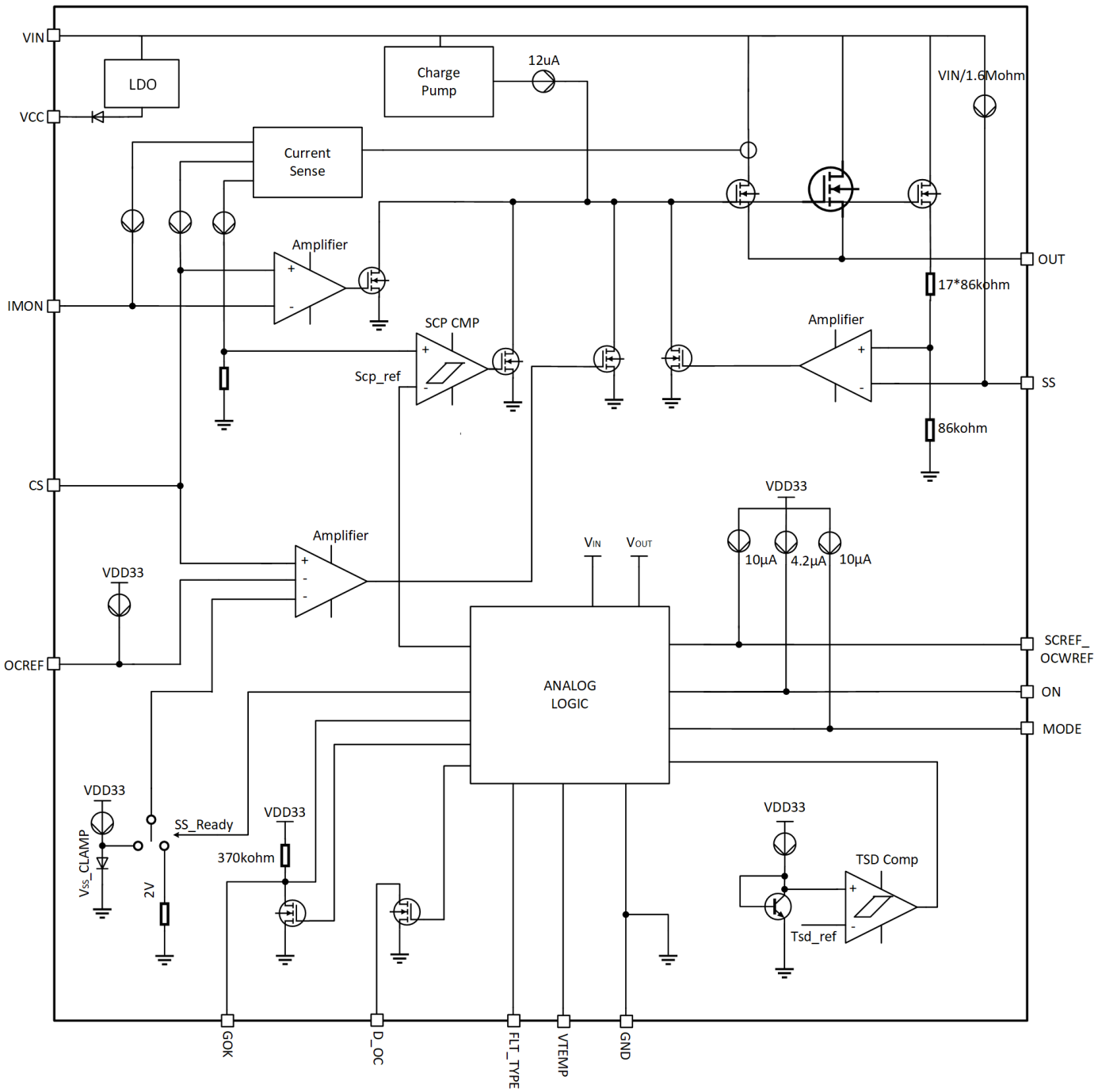



**Fig.1 Functional Block Diagram**

# REVISION HISTORY

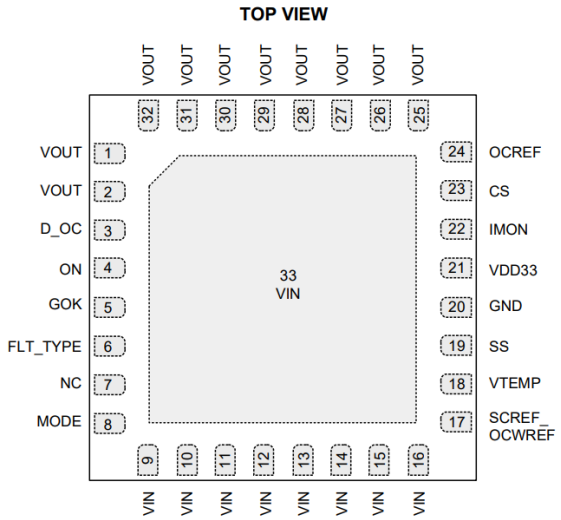
| Release | Rev | Changes | Date |
|---|---|---|---|
| Released | 1.0 | First release | 2025.01 |

# ORDERING INFORMATION

| Part Number | Output Current (A) | VOUT (V) | Top Marking | MPQ |
|---|---|---|---|---|
| XPA5991G32R | 50 | E-fuse | A5991 | 3,000 |
| | | | | |

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

# PIN CONFIGURATION AND DESCRIPTION




Pin Description

| Pin Number | Pin Name | Description |
|---|---|---|
| 1, 2, 25, 26, 27, 28, 29, 30, 31, 32 | VOUT | **Output voltage.** VOUT is the output voltage controlled by XPA5991. A Schottky diode should be placed between VOUT and GND to absorb potential negative voltage spikes. |
| 3 | D_OC | **Over-current indication digital output.** The D_OC pin is an open-drain output. D_OC is pulled low when the CS voltage (VCS) exceeds 85% of the OCREF voltage (VOCREF) in standalone mode, and VCS exceeds the OCWREF voltage (VOCWREF) in slave mode. |
| 4 | ON | **MOSFET on/off control.** Pull the ON above 1.4V to turn the power MOSFET on, and below 1.2V to turn power MOSFET off. Do not float ON pin. |
| 5 | GOK | **Intelli-Fuse fault reporting output.** The GOK pin is an open-drain output. GOK is pulled low and latches once there is a fault detected. The following faults can pull low GOK: an input over-voltage (OV) fault, an output over-current (OC) fault, a short circuit (SC) fault, an over-temperature (OT) fault, or a MOSFET health fault. |
| 6 | FLT_TYPE | **Intelli-Fuse fault type indication output.** The FLT_TYPE pin indicates a voltage level based on the fault detected. |
| 7 | NC | **Not connected.** Float the NC pin. |
| 8 | MODE | **Mode selection.** Connect different resistors between the MODE and GND pins to select the different operation modes (latch-off mode, hiccup mode or slave mode). |
| 9, 10, 11, 12, 13, 14, 15, 16, 33 | VIN | **System input power supply.** The VIN pin is connected to the drain of the MOSFET. |

| | | |
|---|---|---|
| 17 | SCREF_ OCWREF | **Multifunctional (short-circuit current limit and over-current warning reference in slave mode).** The SCREF_OCWREF pin is a multifunctional pin. Connect different resistors between SCREF_OCWREF and GND pins to select different short-circuit current limits (40A, 60A, 80A, 100A or 120A). In slave mode, SCREF_OCWREF is used as the OC warning reference. |
| 18 | VTEMP | **Junction temperature sense output.** Place a ≤1nF capacitor and a ≥10kΩ resistor in parallel on the VTEMP pin. |
| 19 | SS | **Soft-start time setting.** Connect an external capacitor between SS and GND pins to sets the soft-start time (tSS). The internal circuitry controls the output voltage (VOUT) slew rate during start-up. |
| 20 | GND | **Signal ground.** |
| 21 | VDD33 | **Internal 3.3V LDO output.** Place a ⩾1μF decoupling capacitor close to the VDD33 and GND pins. |
| 22 | IMON | **Output current monitor.** The IMON pin reports the current flowing through the power device. Connect a resistor between the IMON and GND pins to generate the IMON voltage (VIMON). Place a 2.2nF to 100nF capacitor in parallel to reduce noise and maintain a smooth voltage. |
| 23 | CS | **Current-sense output.** Connect a resistor between the CS and GND pins to generate VCS which is compared to VOCREF to determine the OC limit. The CS pin is also used to assert D_OC. The D_OC is pulled low If VCS exceeds 85% of VOCREF in standalone mode, and VCS exceeds VOCWREF in slave mode. |
| 24 | OCREF | **Current-limit reference voltage input.** Connect a 1nF to 10nF capacitor between the OCREF and GND pins to reduce noise and maintain a smooth voltage. |

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| VIN | DC | -0.3V ~ +20V |
| | 1us | +24V |
| | 25ns | +29V |
| VOUT | | -0.3V ~ +20V |
| All other pins | | -0.3V ~ +6V |
| Continuous power dissipation ($T_A$=25°C) (2) | | 8.23W |
| Junction temperature | $T_J$ | –40°C to 150°C |
| Storage temperature | $T_{stg}$ | –65°C to 155°C |
| Lead soldering temperature | $T_s$(10s) | 280°C |
| Junction-to-ambient thermal resistance | $\theta_{JA}$ | 14.58°C/W |
| Junction-to-case thermal resistance | $\theta_{JC}$ | 5.33°C/W |
| ESD | HBM | 2kV |
| ESD | CDM | 2kV |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| VIN | Input voltage | 2.7 | 16 | V |
| $T_J$ | Operating junction temperature | -40 | 125 | °C |

### Notes

(1) Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.

(2) The max allowable continuous power dissipation at any ambient temperature is defined by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$.

Excessive die temperature will cause the device to go into thermal shutdown, hence protects it from permanent damage.

(3) The device is not guaranteed to function outside of its operating conditions.

# ELECTRICAL SPECIFICATIONS

**VIN = 12V, $R_{CS}$ = 2kΩ, $R_{IMON}$ = 2kΩ, $T_A$ = 25°C, unless otherwise noted**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| Quiescent current | $I_Q$ | EN = high, no load | | 2.5 | 2.9 | mA |
| | | Fault latch off | | 2.3 | 2.7 | mA |
| | | EN = 0, $V_{IN}$ = 12V | | 2.3 | 2.7 | mA |
| | | EN = 0, $V_{IN}$ = 16V | | 2.3 | 2.7 | mA |
| **Power FET** | | | | | | |
| On resistance | $R_{DS\_ON}$ | TJ = 25°C, Iout=2A, | | 1 | 1.25 | mΩ |
| | | TJ = 125°C, Iout=2A | | TBD | TBD | |
| **VDD33 Regulator and Under-Voltage Protection (UVLO)** | | | | | | |
| VDD33 regulator output voltage | VDD33 | $I_{VDD33}$=0mA | 3.2 | 3.3 | 3.4 | V |
| | | $I_{VDD33}$=25mA | 3.17 | 3.27 | 3.37 | V |
| | | $I_{VDD33}$=40mA | 3.16 | 3.26 | 3.36 | V |
| VDD33 UVLO threshold, rising | $VDD33_{VTH\_R}$ | | 2.55 | 2.7 | 2.85 | V |
| VDD33 UVLO threshold, falling | $VDD33_{VTH\_F}$ | | 2.15 | 2.3 | 2.45 | V |
| VDD33 UVLO threshold, hysteresis | $VDD33_{HYS}$ | | | 400 | | mV |
| **Thermal Shutdown** | | | | | | |
| Shutdown temperature (4) | $T_{STD}$ | | | 145 | | °C |
| **VIN Under-Voltage Protection (UVLO) and Over-Voltage Protection (OVP)** | | | | | | |
| VIN UVLO threshold, rising | $VIN_{VTH\_R}$ | | 3.05 | 3.2 | 3.35 | V |
| VIN UVLO threshold, falling | $VIN_{VTH\_F}$ | | 2.55 | 2.7 | 2.95 | V |
| Over-voltage protection | $V_{OVP}$ | | 17 | 18.5 | 20 | V |
| OVP hysteresis | $V_{OVP\_HYS}$ | Auto-retry | | 1 | | V |
| **MOSFET On/Off Control (ON)** | | | | | | |
| Internal ON current | Ion | | 3.2 | 4.2 | 5.2 | uA |
| ON input rising threshold | $V_{ON\_Rising}$ | $V_{ON}$ is rising | 1.3 | 1.4 | 1.5 | V |
| ON input falling threshold | $V_{ON\_Falling}$ | $V_{ON}$ is falling | 1.1 | 1.2 | 1.3 | V |
| MOSFET turn-on hysteresis | $V_{ON\_HYS}$ | | | 200 | | mV |
| MOSFET turn-on insertion delay time | $t_{ON\_DELAY}$ | $V_{DD33}$ > $V_{DD33\_UVLO\_RISING}$, $V_{IN}$ > $V_{IN\_UVLO\_RISING}$ | 0.8 | 1.3 | 1.8 | ms |
| ON blanking time | $t_{ON\_BLANK}$ | $V_{ON}$ recycling | 0.7 | 1 | 1.5 | ms |
| **Current-Sense Output (CS)** | | | | | | |
| Current-sense gain | $A_{CS}$ | $I_{CS}$ / $I_{OUT}$, $I_{OUT}$ > 4A | 9.6 | 10 | 10.4 | μA/A |

| | | | | | | |
|---|---|---|---|---|---|---|
| Current-sense gain offset | | $I_{OUT}$ > 4A | -1 | | 1 | μA |
| **Current Monitor Output (IMON)** | | | | | | |
| IMON sense gain | $A_{IMON}$ | $I_{MON}$/ $I_{OUT}$, $I_{OUT}$ > 4A | 9.9 | 10 | 10.1 | μA/A |
| IMON sense offset | | $I_{OUT}$ > 4A | -0.6 | | 0.6 | μA |
| **Over-Current (OC) Limit Reference (OCREF)** | | | | | | |
| Internal OCREF current | $I_{OCREF}$ | Standalone mode | 9 | 10 | 11 | μA |
| | | Slave mode | | 0 | | μA |
| Current limit at normal operation | $I_{OC\_NOR}$ | $R_{ISET}$ = 12k | -6% | 25 | +6% | A |
| OCREF clamp voltage | $V_{OCREF\_CLAMP}$ | $V_{SS\_CLAMP}$ at $V_{OUT}$ < 80%$V_{IN}$, $T_J$ = 25°C | 570 | 635 | 699 | mV |
| | | $V_{SS\_CLAMP}$ at $V_{OUT}$ < 80%$V_{IN}$, $T_J$ = 125°C | 340 | 440 | 570 | mV |
| | | $V_{OUT}$ ≥ 80%$V_{IN}$ | 1.9 | 2 | 2.1 | V |
| OCREF operating voltage (4) | $V_{OCREF}$ | | 0.3 | | 1.8 | V |
| OCREF OC regulation timer | $t_{OC\_REG}$ | $V_{OUT}$ ≥ 90%$V_{IN}$, $V_{OCREF}$ ≥ 0.3V | | 220 | | μs |
| **Short-Circuit Current Limit Reference (SCREF)** | | | | | | |
| Internal SCREF current | $I_{SCREF}$ | Standalone mode, $T_A$ = 25°C | 9 | 10 | 11 | μA |
| | | Standalone mode, $T_A$ = -40 to 125°C | 9 | 10 | 11 | μA |
| | | Slave mode | | 0 | | μA |
| SCREF clamp voltage | $V_{SCREF}$ | $I_{LIMIT\_SC}$ = 40A | | 0 | 0.16 | V |
| | | $I_{LIMIT\_SC}$ = 60A | 0.24 | 0.3 | 0.36 | V |
| | | $I_{LIMIT\_SC}$ = 80A | 0.48 | 0.6 | 0.72 | V |
| | | $I_{LIMIT\_SC}$ = 120A | 0.96 | 1.2 | 1.44 | V |
| | | $I_{LIMIT\_SC}$ = 100A | 1.68 | | | V |
| Short-circuit current limit(4) | $I_{LIMIT\_SC}$ | $V_{SCREF}$ > 1.6V | | 100 | | A |
| Short-circuit protection response time(4) | $t_{SC}$ | | | 200 | | ns |
| Short-circuit start-up protection timer | $t_{SC\_TIMER}$ | $V_{OUT}$ < 1/8 $V_{IN}$, $I_{FET}$ is regulated by $V_{SS\_CLAMP}$ | | 2.1 | 3.2 | ms |
| **Temperature Sense (VTEMP)** | | | | | | |
| Temperature sense gain(4) | | | | 8.7 | | mV/°C |
| Temperature sense output (4) | | $T_J$ = 25°C | | 370 | | mV |
| **Thermal Shutdown (TSD)** | | | | | | |
| Thermal Shutdown rising Threshold(4) | | | | 148 | | °C |
| Thermal Shutdown falling Threshold(4) | | | | 100 | | °C |
| **Soft Start (SS)** | | | | | | |

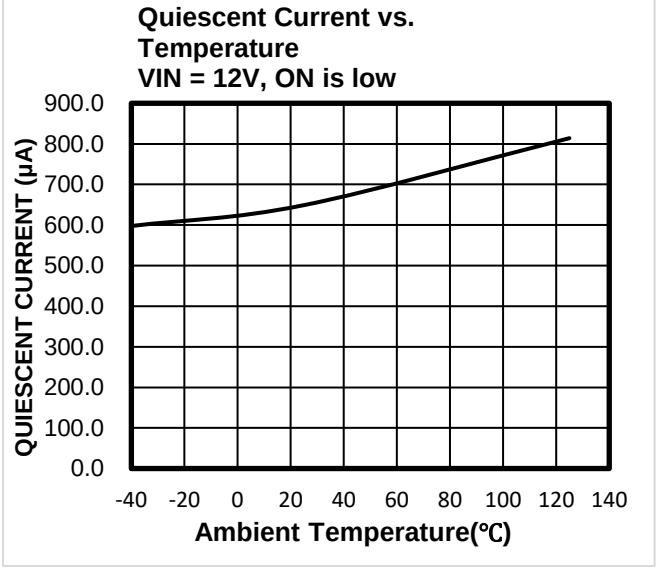
| | | | | | | |
|---|---|---|---|---|---|---|
| SS pull-up current | $I_{SS}$ | $V_{SS}$= 12V, ISS is dependent on $V_{IN}$, $R_{SS}$= 1.6MΩ | 6.5 | 7.5 | 8.5 | μA |
| SS low voltage | $V_{SS\_LOW}$ | SS is pull low internally via $R_{SS}$, $I_{SINK}$=10mA | | | 0.2 | V |
| SS leakage current | $I_{LKG\_SS}$ | $V_{ON}$= 0V, $V_{SS}$=3.3V, MOSFET is off | | | 1 | μA |
| **GOK Output and Comparator** | | | | | | |
| Output low voltage | $V_{GOK\_LOW}$ | $I_{SINK}$ =10mA | | | 0.3 | V |
| GOK leakage current (4) | $I_{LKG\_GOK}$ | $V_{GOK}$ = 3.3V | | | 1 | μA |
| GOK internal pull-up resistor | $R_{GOK}$ | | | 370 | | kΩ |
| GOK comparator falling threshold | $V_{GOK\_FALLING}$ | Fault status | 1.05 | 1.16 | 1.3 | ms |
| GOK comparator hysteresis | $V_{GOK\_HYS}$ | | | 900 | | mV |
| GOK fault delay time | | | 1 | 3 | 5 | μs |
| **D_OC Output** | | | | | | |
| Output low voltage | $V_{D\_OC\_LOW}$ | $I_{SINK}$ =10mA | | | 0.3 | V |
| D_OC leakage current | $I_{LKG\_D\_OC}$ | $V_{D\_OC}$ = 3.3V | | | 1 | μA |
| D_OC high to low threshold (OC warning) | $V_{D\_OC\_TH}$ | Standalone mode, $V_{OUT}$≥ 90%$V_{IN}$, 0.3V ≤ $V_{OCREF}$ ≤ 1.8V | 0.8 | 0.85 | 0.9 | $V_{CS}$ / $V_{OCREF}$ |
| | | Slave mode, $V_{OUT}$ ≥ 90%$V_{IN}$, 0.3V ≤ $V_{OCREF}$ ≤ 1.8V | 0.95 | 1 | 1.05 | $V_{CS}$ / $V_{OCWREF}$ |
| **MOSFET Short Detection** | | | | | | |
| MOSFET drain-to-source short entry threshold | $V_{DSTH\_ENT}$ | Measured at $V_{OUT}$ during start-up | 85 | 90 | 95 | % of VIN |
| MOSFET drain-to-source short recovery threshold | $V_{DSTH\_EXT}$ | Measured at $V_{OUT}$ during start-up | 65 | 70 | 75 | % of VIN |
| MOSFET Gate-to-source short protection delay time | $T_{GS\_ST}$ | $V_{SS}$ > $V_{DD33}$-0.7V | 200 | 250 | 300 | ms |
| **Fault Type Indication Output (FLT_TYPE) (6 Indication Types)** | | | | | | |
| short-circuit FLT_TYPE voltage (4) | $V_{FLT\_TYPE\_SC}$ | SCP | | 1.5 | | V |
| OC fault FLT_TYPE voltage | $V_{FLT\_TYPE\_OC}$ | OCP during SS or normal operation | 1.16 | 1.2 | 1.24 | V |
| OT/OV fault FLT_TYPE voltage | $V_{FLT\_TYPE\_OT/OV}$ | VIN OVP and OTP | 0.865 | 0.9 | 0.935 | V |
| MOSFET DS/GS short fault FLT_TYPE voltage | $V_{FLT\_TYPE\_DS/GS}$ | MOSFET DS/GS short | 0.57 | 0.6 | 0.63 | V |
| GOK fault FLT_TYPE voltage | $V_{FLT\_TYPE\_GOK}$ | GOK fault | 0.275 | 0.3 | 0.325 | V |
| FLT_TYPE voltage for other conditions | $V_{FLT\_TYPE\_OTHER}$ | | 0.08 | 0.1 | 0.12 | V |
| **Mode Selection (MODE)** | | | | | | |

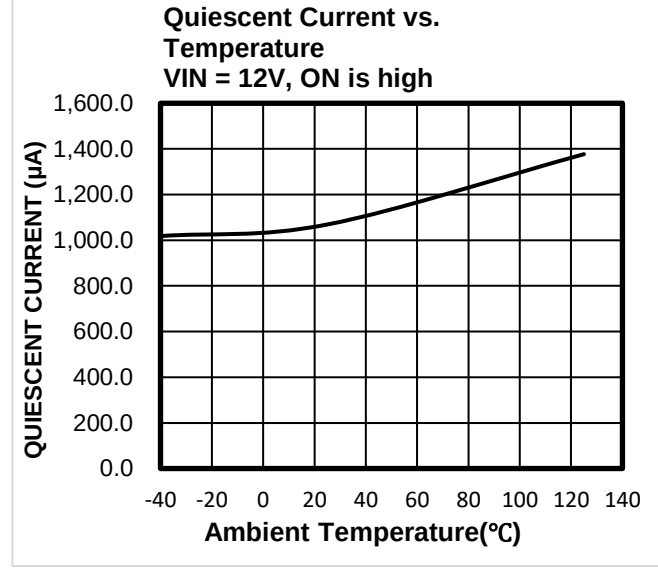
| | | | | | | |
|---|---|---|---|---|---|---|
| MODE current | $I_{MODE}$ | | 9 | 10 | 11 | μA |
| Hiccup mode with 250ms auto-retry delay | $V_{MODE1}$ | $R_{MODE}$ = 30kΩ，$t_{RETRY}$ = 250ms | 0.24 | 0.3 | 0.36 | V |
| Hiccup mode with 500ms auto-retry delay | $V_{MODE2}$ | $R_{MODE}$ = 0kΩ，$t_{RETRY}$ = 500ms | | 0 | 0.16 | V |
| Hiccup mode with 1s auto-retry delay | $V_{MODE3}$ | $R_{MODE}$ = 60kΩ，$t_{RETRY}$ = 1s | 0.48 | 0.6 | 0.72 | V |
| slave mode | $V_{MODE4}$ | $R_{MODE}$ = 120kΩ | 0.96 | 1.2 | 1.44 | V |
| latch-off mode | $V_{MODE5}$ | MODE is pulled up to VDD33 | 1.68 | | | V |

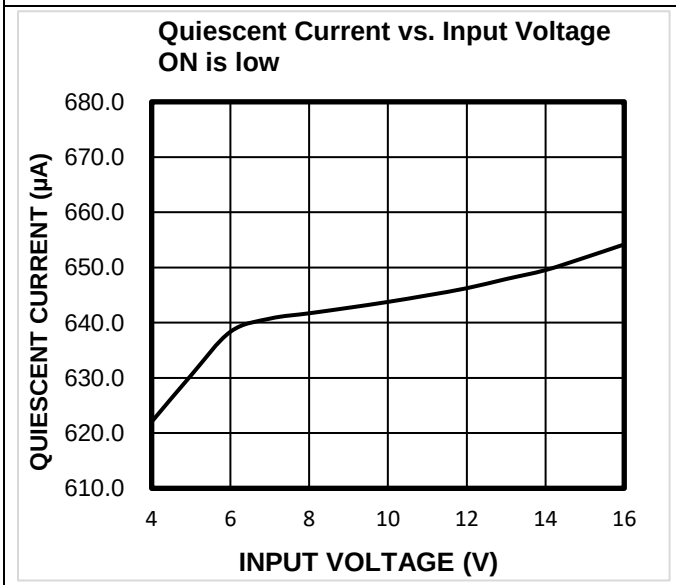
Notes:
(4) Guaranteed by design.

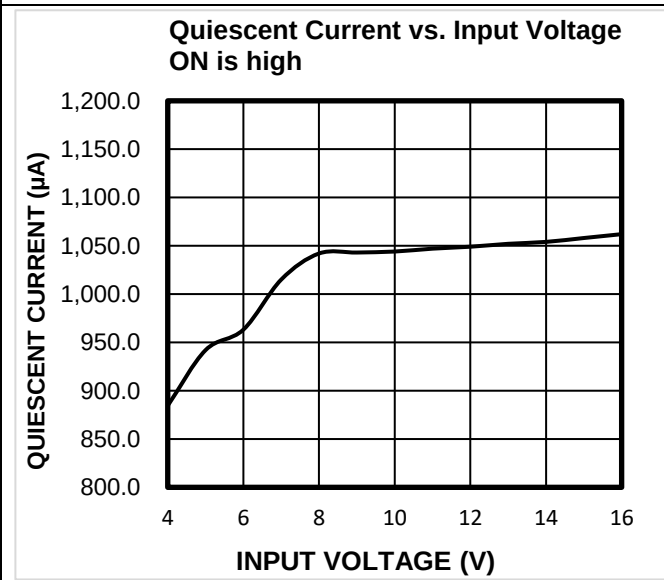
## TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

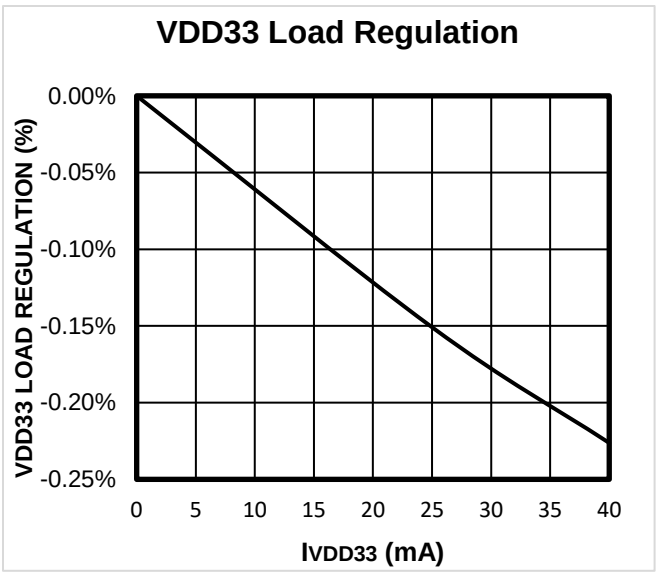
**$V_{IN}$ = 12V, $R_{CS}$ = $R_{IMON}$=2kΩ , TA= 25°C, unless otherwise noted.**

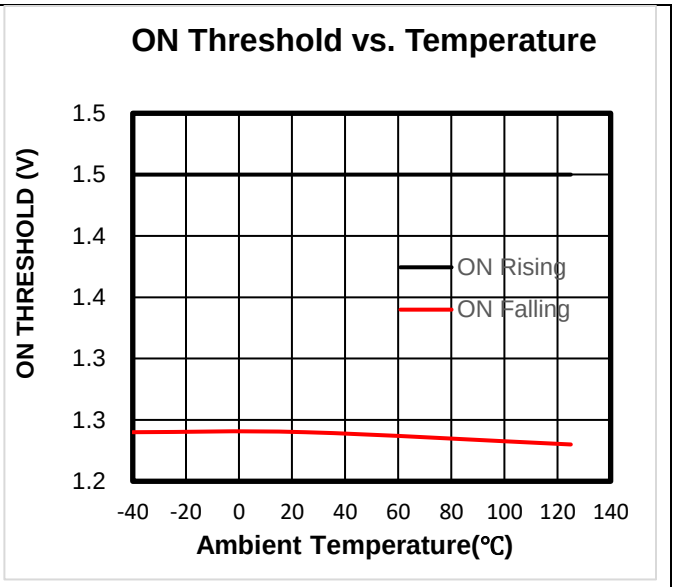


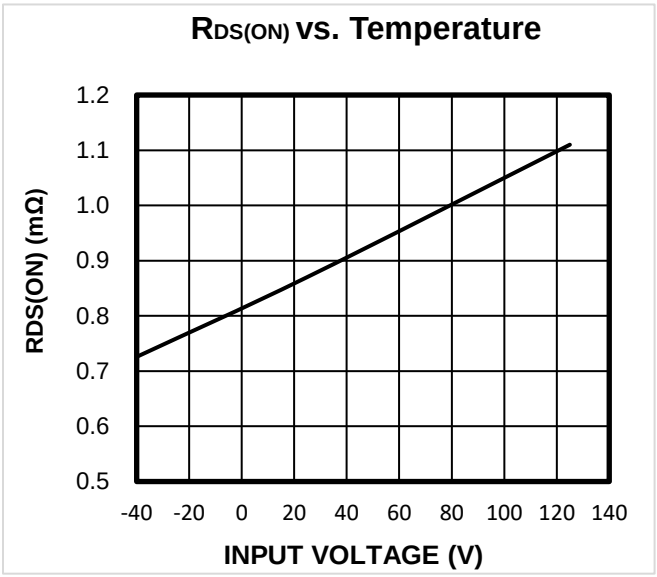



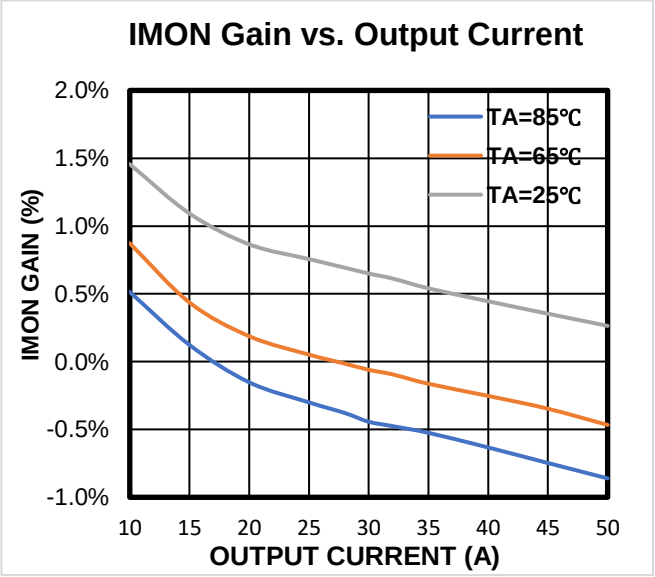



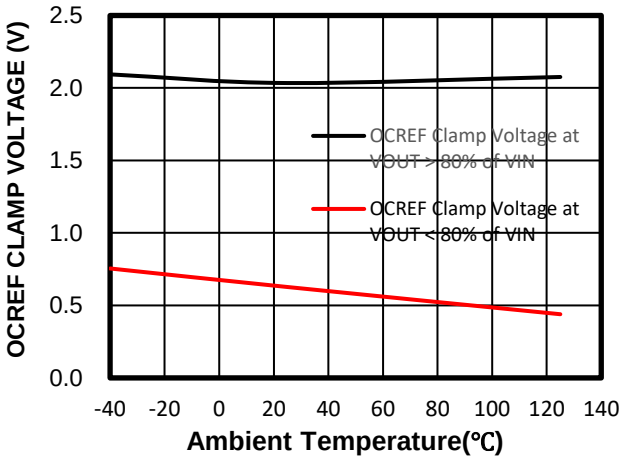

VDD33 Load Regulation
VDD33 LOAD REGULATION (%)
0.00%
-0.05%
-0.10%
-0.15%
-0.20%
-0.25%
0
5
10
15
20
25
30
35
40
IVDD33 (mA)


ON Threshold vs. Temperature
ON THRESHOLD (V)
1.5
1.5
1.4
1.4
1.3
1.3
1.2
ON Rising
ON Falling
-40
-20
0
20
40
60
80
100
120
140
Ambient Temperature(℃)

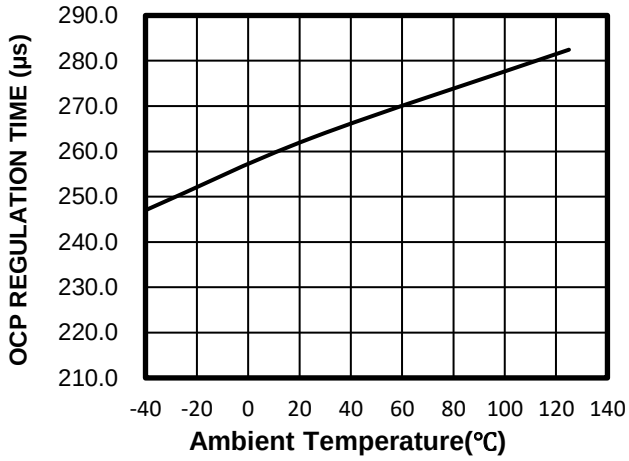

RDS(ON) vs. Temperature
RDS(ON) (mΩ)
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
-40
-20
0
20
40
60
80
100
120
140
INPUT VOLTAGE (V)


IMON Gain vs. Output Current
IMON GAIN (%)
2.0%
1.5%
1.0%
0.5%
0.0%
-0.5%
-1.0%
TA=85℃
TA=65℃
TA=25℃
10
15
20
25
30
35
40
45
50
OUTPUT CURRENT (A)

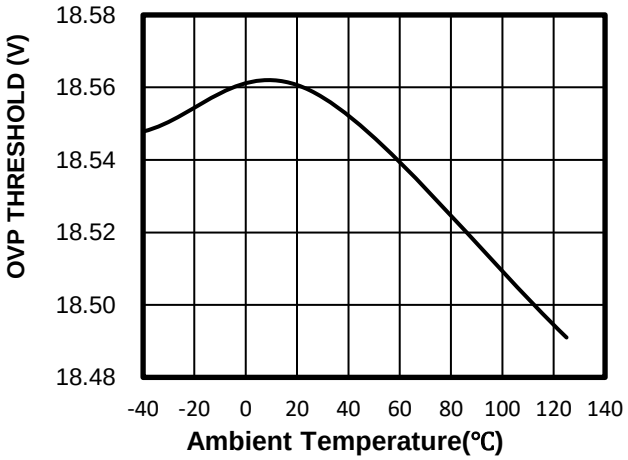
**OCREF Clamp Voltage vs. Temperature**



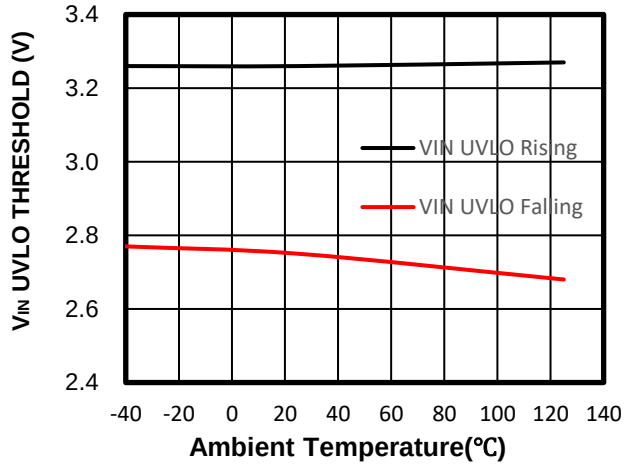

**OCP Reguation Time vs. Temperature**




**OVP Threshold vs. Temperature**




**$V_{IN}$ UVLO Threshold vs. Temperature**



# FUNCTIONAL DESCRIPTION

The XPA5991 is a monolithic Intelli-Fuse device with 1mΩ $R_{DS(ON)}$ internal power MOSFET, compatible with multi-fuse hot-swap applications. The XPA5991 can operate alone or can be controlled via a hot-swap controller for multi-fuse operation. It can drive up to 50A of continuous output current ($I_{OUT}$) per device at room temperature, and up to 60A of continuous $I_{OUT}$ with air flow.

The device limits the backplane voltage drop by limiting the inrush current to the load while a circuit card is inserted into a live backplane power source. It also provides an integrated current mirror to monitor $I_{OUT}$ and the integrated on-die temperature sense. This eliminates the need for an external current-sense power resistor, power MOSFET, and temperature-sense device.

The XPA5991 monitors the current and temperature to feedback information to the processor or controller. It limits the internal MOSFET current ($I_{FET}$) by controlling the gate voltage ($V_{GATE}$) via the current limit ($I_{LIMIT}$) reference input and soft-start ramp

### MOSFET On/Off Control (ON)

The ON pin controls the power MOSFET to turn on and off while system input power supply exists. Pull ON above 1.4V to turn on the MOSFET and below 1.2V to turn it off. There is a fixed $t_{ON\_DELAY}$ (1.3ms) that starts when ON is pulled above 1.4V and the MOSFET remains off within the $t_{ON\_DELAY}$. If there is no fault, ON pin above 1.4V can turn on the MOSFET after 1.3ms. Figure 2 shows the MOSFET on/off control when GOK is pulled up to VDD33.

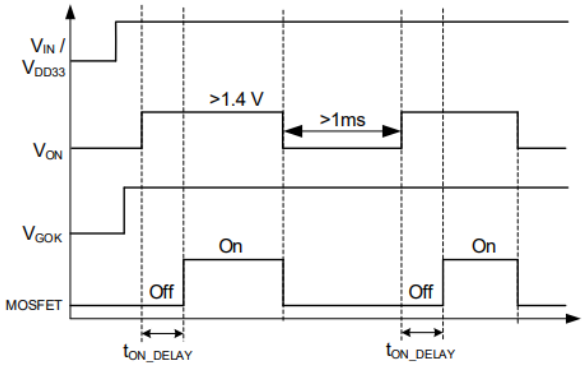



**Fig.2 MOSFET On/Off Control**

If any fault detected, the GOK is pulled low and MOSFET is turned off. Regardless of whether the fault is removed, pull low ON can clear the fault states and allow GOK being pulled high. There is blanking time $t_{ON\_BLANK}$ (1ms) starts when ON is pulled low and ON above 1.4V is valid until the blanking time is finished. If the fault is removed when ON is low, pull ON above 1.4V after the 1ms can turn on the MOSFET once $t_{ON\_DELAY}$ is finished. Figure 3 shows the MOSFET on/off control if a fault occurs.

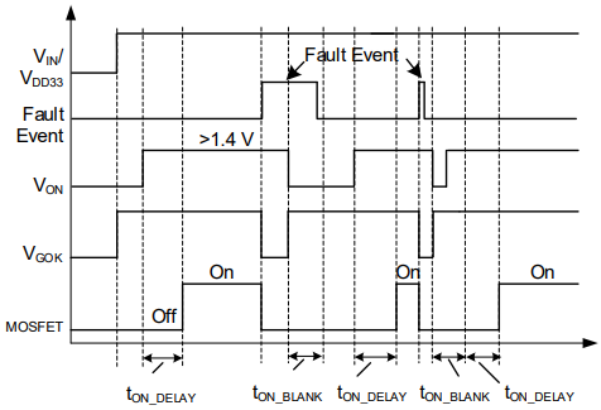



**Fig.3 MOSFET On/Off Control if a Fault Occurs**

In standalone mode, a capacitor connected between ON and GND pins ($C_{ON}$) can be charged by the internal pull-up constant current source (4.2μA) for automatic start-up. If the XPA5991 is paired with an Intelli-Fuse master or a controller, then ON is controlled via the master or controller.

### Soft start (SS)

When ON is pulled high and tON_DELAY ends, a constant-current source proportional to the input voltage charges up the capacitor connected to the SS pin, which determines the soft- start time. The output voltage rises at a similar slew rate to the SS voltage. The SS capacitor value can be calculated with Equation (1):

$$C_{SS}\ (nF) = 18 \times \frac{t_{SS}\ (ms)}{R_{SS}} \quad (1)$$

Where $t_{SS}$ is the soft-start time, and $R_{SS}$ is 1.6MΩ.

For example, a 100nF capacitor gives a soft-start time of 8.9ms. If the load capacitance is extremely large, the current required to maintain the preset soft-start time exceed the current limit ($I_{LIMIT}$). In this case, the rise time is controlled by the load capacitor and the current limit. A 12μA current source pulls up the gate of the power MOSFET, and the gate charge current controls the output voltage rise time, and in this case, $t_{SS}$ is minimum soft start time, which is about 1.5ms.

When multiple XPA5991s are operating in parallel, their SS pins should be connected together, so all of devices can be controlled the soft-start slew rate during soft start.

### Start-Up Sequence

$V_{GATE}$ should be pulled low during $V_{IN}$ plug-in with high dv/dt when $V_{IN}$ rises immediately in hot-swap applications. The XPA5991 has two operation modes: standalone mode and slave mode.

### Standalone Mode

In standalone mode, ON can be pulled high via the internal current source (4.2μA) charges $C_{ON}$ once the VDD33 voltage ($V_{DD33}$) exceeds its UVLO rising threshold or pulled up to VDD33 externally. The OCREF determines the over current limit ($I_{LIMIT\_OC}$) level via the $V_{OCREF}$ generated by the OCREF current (10μA) through the OCREF resistor ($R_{OCREF}$). The SCREF determines the short-circuit current limit ($I_{LIMIT\_SC}$) level via the $V_{SCREF}$ generated by the SCREF current (10μA) through the SCREF resistor ($R_{SCREF}$).

The gate of power MOSFET is charged by the internal charge pump (12μA) after ON above 1.4V and $t_{ON\_DELAY}$ finished. Once the gate-to-source voltage ($V_{GS}$) exceeds its threshold ($V_{GS\_TH}$), the MOSFET turns on and $V_{OUT}$ starts rise. During start-up, the actual current-limit reference is clamped internally at $V_{SS\_CLAMP}$ (about 635mV with

a negative temperature coefficient) if $V_{OCREF}$ exceeds the $V_{SS\_CLAMP}$, while the current-limit reference is determined by $V_{OCREF}$ if the external $V_{OCREF}$ is below $V_{OCREF\_CLAMP}$ ($V_{OCREF\_CLAMP}$ equals $V_{SS\_CLAMP}$ when $V_{OUT}$ is below 80% of $V_{IN}$). Figure 4 indicates the start-up in standalone mode.

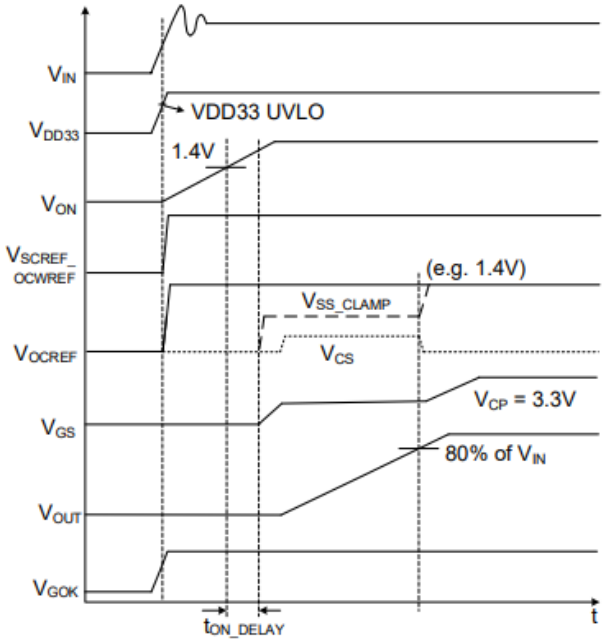



**Fig.4 start-up in standalone mode**

### Slave Mode

XPA5991 is configured to operate in slave mode when it is controlled by a hot-swap master or controller. In slave mode, $V_{OCREF}$, $V_{SCREF}$ and the OCWREF voltage ($V_{OCWREF}$) are configured via the controller.

The gate of power MOSFET is charged by internal charge pump once $V_{ON}$ is pulled high and $t_{ON\_DELAY}$ finished. The MOSFET is on when $V_{GS}$ exceeds $V_{GS\_TH}$ and $V_{OUT}$ rises, which is shown in Figure 5.

If $I_{LOAD}$ is high during soft start, the CS voltage ($V_{CS}$) is clamped at $V_{SS\_CLAMP}$. The XPA5991 can also be turned on or off via the VIN pin when ON signal from the hot-swap controller keeps high.

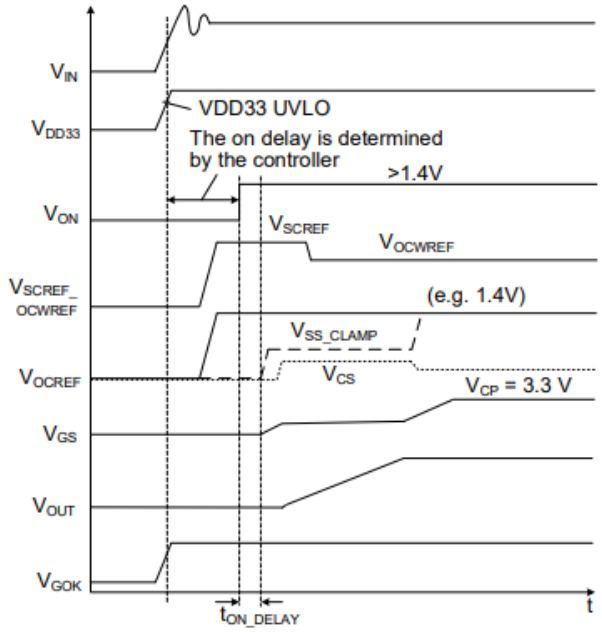



**Fig.5 start-up in slave mode**

### Current-sense Output (CS)

The CS pin can provide a current which is proportional to the current flowing through the power transistor ($I_{OUT}$). The voltage $V_{CS}$ is produced by current-sense resistor ($R_{SS}$) that can be used as OC limiting, OC warning, and devices operate in parallel with start-up current balancing. When the MOSFET is on fully, the current-sense gain is about 10μA/A. The current of CS pin ($I_{CS}$) can be calculated with Equation (2):

$$I_{CS} = I_{OUT} \times 10\mu A/A \quad (2)$$

Then $V_{CS}$ can be calculated with Equation (3):

$$V_{CS} = I_{CS} \times R_{CS} \quad (3)$$

Once $V_{CS}$ exceeds the OCREF $I_{LIMIT}$ threshold, the internal circuity regulates gate of power transistor to maintain a constant $I_{FET}$.

The insertion delay timer starts once the device is enabled. Upon the end of the insertion delay time, an internal 24μA current source starts charging up the power FET's $V_{GS}$, and it takes around 1ms for $V_{GS}$ to reach its threshold. The output voltage then rises following the slew rate controlled by SS.

### Current Monitor Output (IMON)

The XPA5991 provides a high-precise power MOSFET current monitor output ($I_{IMON}$) whose gain is 10μA/A. A resistor ($R_{IMON}$), between the IMON pin and ground, generate the IMON voltage ($V_{IMON}$), the voltage range is 0V to 1.8V to keep the IMON current ($I_{IMON}$) linearly proportional to $I_{FET}$. The IMON current IMON can be calculated with Equation (4):

$$I_{IMON} = I_{OUT} \times 10\mu A/A \quad (4)$$

Then VIMON can be calculated with Equation (5):

$$V_{IMON} = I_{IMON} \times R_{IMON} \quad (5)$$

The IMON pin can accurately monitor the $I_{OUT}$ by the master or controller. Place a 2.2nF to 100nF capacitor between the IMON pin and ground to reduce the noise and keep a smooth indicator voltage.

**Current Balance for Parallel Operation**

In higher-current applications, Multiple XPA5991s can operate in parallel. Connect the IMON pins of all devices, so the current balance loop balances the start-up current for each active channel.

The sensed current from each active IMON pin can be summed together, and then divided by the different active channels. The resulting average $I_{LOAD}$ provides a measure of the total $I_{LOAD}$. By comparing the sensed CS current ($I_{CS}$) in each device, then internal circuity can regulate appropriate gate voltage ($V_{GATE}$), so each intelli-Fuse can achieve current balance during start-up. The equivalent average RIMON (RIMON_AVG) can be calculated with Equation (6):

$$R_{IMON\_AVG} = R_{CS} / N \quad (6)$$

Where N is the number of devices.

It is essential for start-up current balancing to improve thermal performance during parallel operation. Good current sharing reduces power loss by dissipating it across the devices and across a larger area.

**Over-Current Limit Reference (OCREF)**

The $I_{LIMIT\_OC}$ is determined by $V_{OCREF}$ and the external $R_{CS}$. There is an internal amplifier regulating $V_{GATE}$ via comparing $V_{CS}$ to $V_{OCREF}$, which prevents the current through the power MOSFET from exceeding $I_{LIMIT}$ set. The internal OCREF current $I_{OCREF}$ flows through the $R_{OCREF}$ to generate $V_{OCREF}$ and it can be calculated as equation (7):

$$V_{OCREF} = I_{OCREF} \times R_{OCREF} \quad (7)$$

Where $I_{OCREF}$ is 10μA.

For protecting XPA5991 from overheating, there is an internal clamp voltage ($V_{OCREF\_CLAMP}$), which is related to $V_{IN}$ and $V_{OUT}$, to set the actual current-limit reference during start-up. Figure 6 illustrates the OCREF clamp voltage.

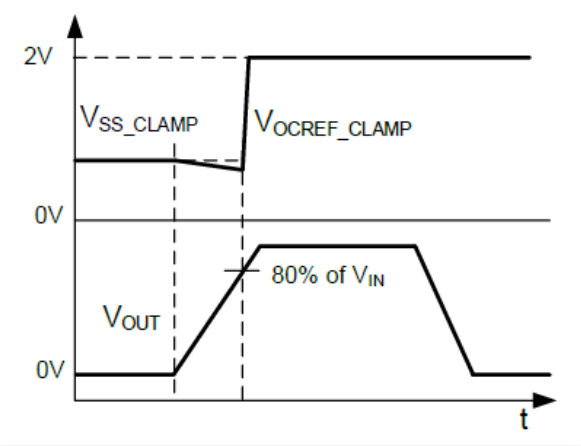



**Fig.6 OCREF Clamp Voltage**

$V_{OCREF\_CLAMP}$ is equal to $V_{SS\_CLAMP}$ when $V_{OUT}$ is below 80% of $V_{IN}$ while it is 2V if $V_{OUT}$ exceeds 80% of $V_{IN}$. The current-limit reference voltage is determined by $V_{OCREF}$ if $V_{OCREF}$ is below $V_{OCREF\_CLAMP}$, and it is determined by $V_{OCREF\_CLAMP}$ when $V_{OCREF}$ exceeds $V_{OCREF\_CLAMP}$.

The expected $I_{LIMIT\_OC}$ is a function of $V_{OCREF}$, $R_{CS}$ and the current sense gain ($g_{CS}$), and it can be calculated as Equation (8):

$$I_{LIMIT} = \frac{V_{OCREF}}{g_{CS} \times R_{CS}} \quad (8)$$

$I_{LIMIT\_OC}$ can exceed the maximum load current ($I_{LOAD\_MAX}$) during normal operation to allow for tolerances in the current-sense value.

**Over-Current Protection (OCP) during Start-Up**

$V_{GATE}$ is regulated to maintain the current through power MOSFET ($I_{FET}$) constant once $V_{CS}$ exceeds $V_{OCREF}$ during soft start. If $V_{CS}$ exceeds $V_{SS\_CLAMP}$ when $V_{OUT}$ is below 1/8 of $V_{IN}$, $I_{FET}$ is regulated for 2.1ms, then the MOSFET latches off and GOK is pulled low (depicted in figure 7).

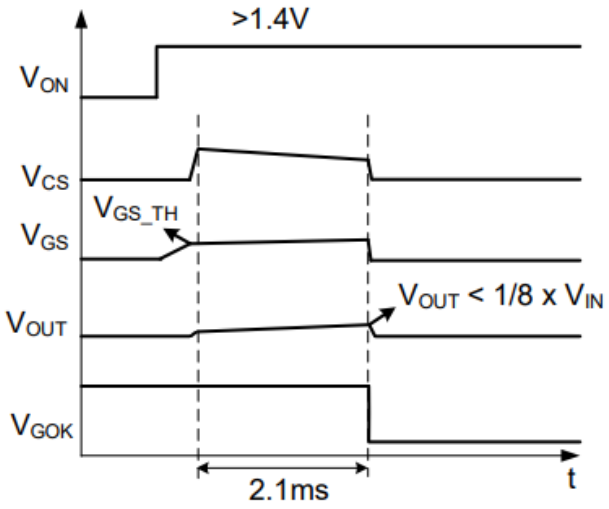



**Fig.7 Failed Start-Up with Output Hard Short**

**OCP during Normal Operation**

When $V_{OUT}$ exceeds 80% of $V_{IN}$, then $V_{OCREF\_CLAMP}$ is pulled to 2V and $V_{GATE}$ is close to the internal charge pump voltage ($V_{CP}$). Once soft start is complete, the XPA5991 works in normal operation.

In normal operation, $V_{GATE}$ is regulated to keep $I_{FET}$ constant once $V_{CS}$ exceeds $V_{OCREF}$. The response

time is about 22μs and $I_{FET}$ may have a small overshoot during this response time.

Once $I_{FET}$ exceeds $I_{LIMIT\_OC}$, an internal OCP fault timer (220us) starts. The power MOSFET resumes normal operation, and the fault timer stops with clearing the count If $I_{FET}$ drops below $I_{LIMIT\_OC}$ within 220us, while it latches off and GOK is pulled low when $I_{FET}$ exceeds $I_{LIMIT\_OC}$ for 220μs.

When an OC fault detected, the GOK and SS pins are pulled low, and FLT_TYPE pin outputs 1.2V to indicate the OC fault.

In latch-off mode, cycle the power on VIN, VDD33, or ON to reset FLT_TYPE to 0.1V. This initiates a soft start, and then MOSFET turns on.

In hiccup mode, the device attempts to initiate a new soft start automatically, and GOK is pulled high after a retry delay time ($t_{RETRY}$). FLT_TYPE continues to indicate an OC fault during $t_{RETRY}$ and is reset to 0.1V after $t_{RETRY}$.

**Short-Circuit Current Limit (SCREF)**

If $I_{LOAD}$ increases rapidly because of short circuit, the current exceeds $I_{LIMIT\_OC}$ significantly before the hot-swap control loop can respond. In this case, the $I_{FET}$ reaches the short-circuit current limit (ILIMIT_SC) and a fast turn-off circuit in the Intelli-Fuse can turn the MOSFET off. The total short-circuit response time is about 200ns. GOK is pulled low when $I_{FET}$ exceeds $I_{LIMIT\_SC}$.

Once the ON voltage ($V_{ON}$) exceeds its rising threshold during the $t_{ON\_DELAY}$, the XPA5991 samples the SCREF voltage ($V_{SCREF}$) to determine $I_{LIMIT\_SC}$ (showed in Figure 8).

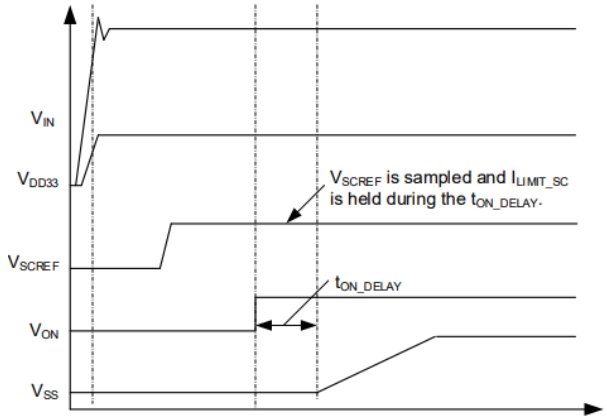



**Fig.8 SCREF Voltage Sampling to Determine the Short-Circuit Current Limit**

$I_{LIMIT\_SC}$ is held once $t_{ON\_DELAY}$ is finished. Modifying $V_{SCREF}$ after $t_{ON\_DELAY}$ does not change $I_{LIMIT\_SC}$. Cycle the power on VIN, VDD33, or ON to enter another $t_{ON\_DELAY}$ and set a new $I_{LIMIT\_SC}$.

The XPA5991 provides five types of short-circuit current levels that can be selected via the SCREF pin. Table 1 shows the selectable short-circuit current limits for different SCREF voltages in standalone mode.

**Table 1: Short-Circuit Current Limit Selection for Different VSCREF in Standalone Mode**

| $V_{SCREF}$ (V) | $R_{SCREF}$ | $I_{LIMIT\_SC}$ (A) |
|---|---|---|
| <0.16 | Pulled to GND | 40 |
| 0.24 to 0.36 | 30kΩ | 60 |
| 0.48 to 0.72 | 60kΩ | 80 |
| 0.96 to 1.44 | 120kΩ | 120 |
| >1.68 | 200kΩ | 100 |

In latch-off mode, cycle the power on VIN, VDD33, or ON to reset FLT_TYPE to 0.1V and GOK is pulled high. This initiates a soft start, and then MOSET turns on.

In hiccup mode, the device attempts to retry automatically, and GOK is pulled high after $t_{RETRY}$. FLT_TYPE continues to indicate an SC fault during $t_{RETRY}$. After $t_{RETRY}$, FLT_TYPE is reset to 0.1V.

**Temperature-Sense Output (VTEMP)**

The VTEMP pin reports the junction temperature ($T_J$) while there is no thermal gradient on the IC. After $V_{DD33}$ exceeds its UVLO rising threshold, the VTEMP voltage ($V_{TEMP}$) is 8.7mV/℃, and has a 152.5mV offset, which is also proportional to $T_J$. VTEMP can be calculated with Equation (9):

$$V_{TEMP} = T_J \times 8.7mV + 152.5mV \quad (9)$$

For example, if $T_J$ is 100°C, then $V_{TEMP}$ is 1.022V. Vtemp can indicate the temperature accurately low to 10°C.

When multiple Intelli-Fuses operate in parallel, the VTEMP pins of each device can be connected to the controller's temperature monitor pin. VTEMP pin connects a ⩽1nF capacitor and a ⩾10kΩ resistor in parallel. The temperature sense function during multi-fuse parallel operation shows in the Figure 9.

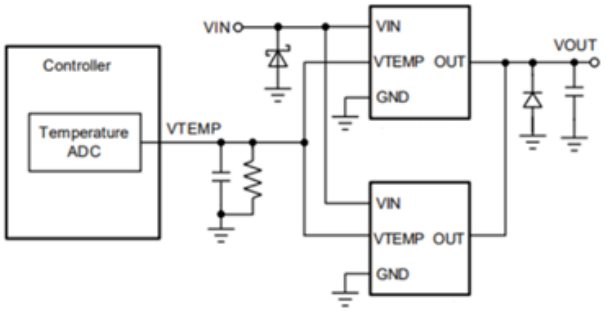



**Fig.9 Temperature Sense during Multi-Fuse Parallel Operation**

**Mode Selection (MODE)**

The XPA5991 provides both latch-off mode and hiccup mode for the following protections: input over-voltage protection (OVP), output over-current protection (OCP), short-circuit protection (SCP), over-temperature protection (OTP) and MOSFET GS short protection. Connect a resistor with different resistance to the MODE pin can selects either latch-off mode or hiccup mode with $t_{RETRY}$. MODE also determines whether the XPA5991 operates in slave mode.

In slave mode, the part operates with the following conditions:

- $V_{OCREF}$ and $V_{SCREF}$ are determined by the controller. The internal $I_{OCREF}$ (10μA) and $I_{SCREF}$ (10μA) are disabled.
- $V_{OCREF\_CLAMP}$ remains active. $V_{SS\_CLAMP}$ controls the soft-start current-limit threshold.
- $V_{ON}$ is determined by the controller and the internal current (4.2μA) charging ON is disabled.
- D_OC is pulled low when $V_{CS}$ exceeds $V_{OCWREF}$, and remains high if $V_{CS}$ exceeds 85% of $V_{OCREF}$.
- Latch-off mode and hiccup mode with $t_{RETRY}$ are selected by the controller.

The device detects the voltage of MODE pin to select mode when $V_{DD33}$ or $V_{IN}$ exceed their UVLO rising threshold. After selecting the mode, it is held until the power on VDD33 or VIN is cycled again.

Table 2 shows the mode selection and $t_{RETRY}$ with corresponding resistor values.

**Table 2: Mode Selection**

| $R_{MODE}$ | Protection Mode | Retry Delay Time |
|---|---|---|
| Pulled to GND | Hiccup mode | 500ms |
| 30kΩ | Hiccup mode | 250ms |
| 60kΩ | Hiccup mode | 1s |
| 120kΩ | Slave mode | |
| Pulled to VDD33 or floating | Latch-off mode | |

### GOK Reporting

The GOK pin is an open-drain with an internal weak pull-up, active-low signal that reports Intelli-Fuse faults. GOK is pulled low when a fault occurs, Pull GOK up to the VDD33 via a 10kΩ to 100kΩ resistor. During start-up, the GOK voltage ($V_{GOK}$) rises according to VDD33.

The MOSFET also can be controlled by a comparator on GOK pin in internal circuity. If $V_{GOK}$ falls below 1.16V, the device can detect this as a fault, then the MOSFET turns off.

### Fault Type Indication (FLT_TYPE)

It indicates that the fault type for XPA5991 via a Voltage on the FLT_TYPE pin. Table 3 shows each fault condition of different FLT_TYPE voltage.

**Table 3: Fault Type Indication**

| Fault Types | Short circuit | OC fault during normal operation or during SS | OT fault or $V_{IN}$ OV fault | GS/DS short | GOK fault | Other statues |
|---|---|---|---|---|---|---|
| Fault Type Voltage | 1.5V | 1.2V | 0.9V | 0.6V | 0.3V | 0V |

Do not short FLT_TYPE to ground. $V_{FLT\_TYPE}$ indicates the related to value only while the fault is present and the MOSFET is off. For example, when device occurs Over-Current fault, the $V_{FLT\_TYPE}$ can output 1.2V after the fault timer (220μs) finishes, and the MOSFET turns off.

A higher $V_{FLT\_TYPE}$ indicates a more serious fault has occurred in the device. When multiple faults occur at the same time, then FLT_TYPE outputs the highest voltage for the most serious fault. For example, if a SC fault and an OV fault occur simultaneously, then $V_{FLT\_TYPE}$ is 1.5V to indicates the SC fault, which is more serious fault.

In multi-fuse operation, the FLY_TYPE pin of each device should be connected together to indicate the highest-priority fault in the entire system.

### D_OC Reporting

The D_OC pin is an open-drain, active-low output that reports OC warnings while $V_{OUT}$ exceeds 90% of $V_{IN}$. In standalone mode, D_OC is pulled low when $V_{CS}$ exceeds 85% of $V_{OCREF}$ while it is pulled high If $V_{CS}$ drops below

85% of $V_{OCREF}$. In slave mode, this threshold is determined by $V_{OCWREF}$. Pull D_OC up to VDD33 via a 10kΩ to 100kΩ resistor.

**Other Fault Protections**

**Over-Temperature Protection (OTP)/Thermal Shutdown**

The XPA5991 senses the junction temperature ($T_J$) of power MOSFET internally. The device shuts down when $T_J$ exceeds the thermal shutdown threshold (about 145°C), which cause GOK and SS pins to be pulled low and FLT_TYPE output 0.9V to indicate the over-temperature (OT) fault (if there are no other higher-priority faults).

In latch-off mode, cycle the power on VIN, VDD33, or ON to reset FLT_TYPE to 0.1V. This initiates a soft start, and then MOSFET turns on.

In hiccup mode, the device attempts to restart automatically when $T_J$ is below 100°C, and GOK is pulled high after $t_{RETRY}$. FLT_TYPE keeps indicating an OT fault during $t_{RETRY}$ and reset to 0.1V after $t_{RETRY}$.

**VIN Over-Voltage Protection (OVP)**

The XPA5991 monitors $V_{IN}$ to detect whether there is the over-voltage (OV) fault. The device shuts down when $V_{IN}$ exceeds 18.5V, which cause GOK and SS pins to be pulled low and FLT_TYPE output 0.9V to indicate the OV fault (if there are no other higher-priority faults).

In latch-off mode, cycle the power on VIN, VDD33, or ON to reset FLT_TYPE to 0.1V. This initiates a soft start, and then MOSFET turns on.

In hiccup mode, the device attempts to restart automatically when $V_{in}$ is below 17.5V, and GOK is pulled high after $t_{RETRY}$. FLT_TYPE keeps indicating an OV fault during $t_{RETRY}$ and reset to 0.1V after $t_{RETRY}$.

**Damaged intelli-fuse MOSFET Detection**

The XPA5991 can detect a shorted pass MOSFET during start-up. Once $V_{DD33}$ exceeds its UVLO rising threshold and $V_{ON}$ exceeds its rising threshold (1.4V), the intelli-fuse treat $V_{OUT}$ that exceeds 90% of $V_{IN}$ during the $t_{ON\_DELAY}$ as a short, which is called a drain-to-source (DS) short. In this case, GOK is pulled low, and the $V_{FLT\_TYPE}$ is 0.9V to indicates the DS short. The DS short is non-latch fault in all operation mode. Once the device detects that $V_{OUT}$ is below 70% of $V_{IN}$, then DS short is removed and GOK is pulled high, at this case, FLT_TYPE is reset to 0.1V, after that, the XPA5991 initiates a soft start and resumes normal operation.

**Power MOSFET is Not Fully On**

When the device starts up and VOUT starts to ramp up, the following conditions are met, which means the power MOSFET is not fully on:

- $V_{SS}$ exceeds $V_{DD33}$ - 0.7V.
- $V_{GS}$ is below $V_{CP}$ - 0.7V.
- No OC faults have occurred.
- No SC faults have occurred.

The XPA5991 stops operating and the device turns off after 250ms. The GOK and SS pins are pilled low, and FLT_TYPE pin outputs 0.6V to indicate a GS short has occurred (illustrated in figure 10).

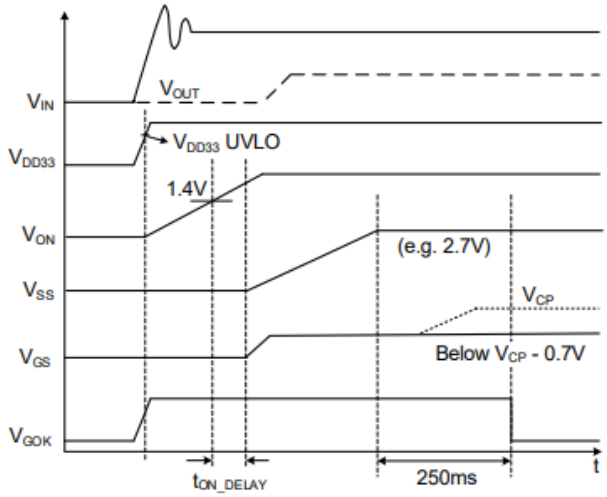



**Fig.10 Power MOSFET is Not Fully On in Latch-Off Mode**

In latch-off mode, cycle the power on VIN, VDD33, or ON to reset $V_{FLT\_TYPE}$ to 0.1V. This initiates a soft start, and then MOSFET turns on.

In hiccup mode, the device attempts to retry automatically, and GOK is pulled high after $t_{RETRY}$ ends. FLT_TYPE continues to indicate a GS short fault during $t_{RETRY}$. $V_{FLT\_TYPE}$ reset to 0.1V after $t_{RETRY}$.

**GOK Fault**

The XPA5991 monitors the voltage of GOK ($V_{GOK}$) to control the power MOSFET. When $V_{GOK}$ drops below 1.16V, which seems like a fault, the MOSFET is turned off after a fixed delay (10μ) and FLT_TYPE outputs 0.3V to indicate a GOK fault.

GOK fault is a non-latch fault. Once $V_{GOK}$ rises and exceeds 2.06V, the device initiates a soft start and resumes normal operation with FLT_TYPE being reset to 0.1V.

There is an internal pull-up resistor (370kΩ) connected with GOK to avoid falsely triggering a GOK fault when no external pull-up resistor connected in standalone mode.

**Under-Voltage Lockout (UVLO) Protection**

There are two UVLO protections in XPA5991: VDD33 UVLO with a 2.7V rising threshold, and VIN UVLO with a 3.2V rising threshold. The device starts up when both $V_{IN}$ and $V_{DD33}$ exceed their UVLO rising threshold respectively, and it shuts down when one of the two UVLO protections is detected. The two UVLO protections are both non-latch protection.

**Input and Output Transient Protection**

Parasitic inductance in the input circuitry can cause the hot-swap system to experience positive transients on the input during a hot plug or during rapid shutdown with a high current. To reduce input transients, a transient voltage suppressor (TVS) diode may be required on the input to limit transient voltages below the absolute maximum ratings.

Inductance in the output circuitry can cause the output to experience negative transients during rapid turn-off with a high current. If a transient causes the output to drop further, then the MOSFET may not turn off properly. An output voltage clamp diode is required on the output to limit negative transients. Select a Schottky diode with a low forward voltage.

**Parallel Operation**

To support higher currents, the XPA5991 is able to work in parallel operation (maximum 20-phase parallel operation). The following connections and conditions are required to support multi-phase parallel operation:

- Connect the VIN pins to the same input bus.
- Connect the VOUT pins to the same output bus.
- Connect the ON pins together for start-up sequence and power MOSFET control.
- Connect the SS pins together for soft-start sequence control.
- Connect the GOK pins together for system fault control.
- Connect the same current-sense resistors ($R_{CS}$) to each phase separately.
- Connect the IMON pins together, and design the total system's IMON resistance to equal $R_{CS}$/ N (where N is the number of phases) for soft-start current-balance control.
- Connect the OCREF pins together.
- Select the same mode for all phases.
- Connect the VTEMP pins together to report the highest $T_J$ of all the phases.
- Connect the FLT_TYPE pins together to indicate the highest-priority fault.

# TYPICAL APPLICATION

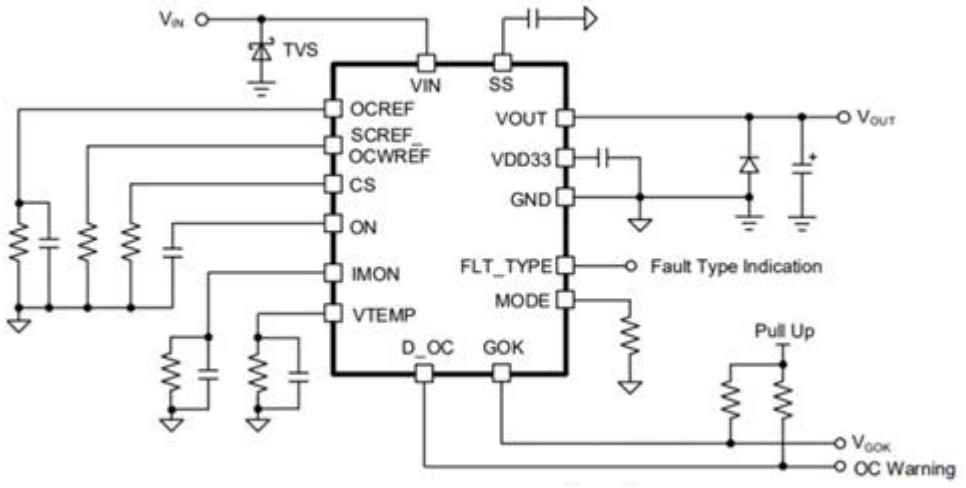



**Fig. 11 Typical Application Diagram of XPA5991**

### Selecting the Current-Limit Resistor ($R_{CS}$)

The $I_{LIMIT\_OC}$ of XPA5991 is supposed to exceed the normal $I_{LOAD\_MAX}$, which allows for tolerances in the current-sense value. $I_{LIMIT\_OC}$ can be calculated as Equation (10):

$$I_{LIMIT} = \frac{V_{OCREF}}{R_{CS}} \times 10^5 \quad (10)$$

According to the equation (10), if $R_{CS}$ is 3kΩ and $V_{OCREF}$ is 1.2V, then $I_{LIMIT\_OC}$ is 40A. If $R_{CS}$ is 3kΩ and $V_{OCREF}$ is 0.3V, then $I_{LIMIT\_OC}$ is 10A.

### Current-Limit Reference Voltage (OCREF)

The OCREF pin sets the current-limit reference via the hot-swap controller in slave mode or via a resistor connected to ground in standalone mode. For both two modes, place a 1nF to 10nF capacitor between the OCREF and GND pins to reduce noise and maintain a smooth indicator voltage.

During normal operation, $V_{OCREF}$ can be set between 0.3V and 1.8V to configure $I_{LIMIT}$ either low or high while $R_{CS}$ is fixed.

### Current Monitor Setting (IMON)

The XPA5991 provides a high-precise power MOSFET current monitor output (IMON) whose gain is 10μA/A. A resistor ($R_{IMON}$), between the IMON pin and ground, generate the IMON voltage ($V_{IMON}$) to set the IOUT gain.

If in s single-fuse application, $R_{IMON}$ should be $\geqslant$ $R_{CS}$. If in a multi-fuse parallel application, each device can connect the IMON pins together to achieve the start-up current balance.

The equivalent average IMON resistance ($R_{IMON\_AVG}$) can be calculated with Equation (6). Figure 12 shows the IMON and CS connections of multiple XPA5991s in a multi-fuse parallel application.

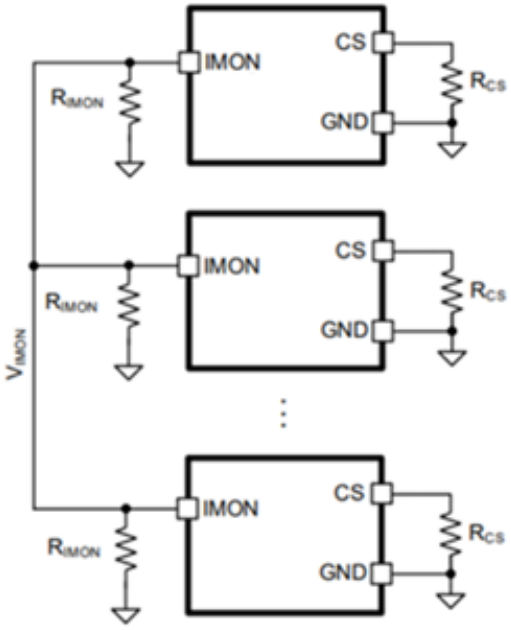



**Fig.12 IMON and CS Connections in Multi-Fuse Parallel Application**

Where $R_{IMON} = R_{CS}$, $R_{IMON\_AVE} = R_{CS}/N$, and N is the number of phases.

**Maximum Output Current**

The XPA5991 can drive up to 50A of continuous $I_{OUT}$ per device at room temperature, and up to 60A $I_{OUT}$ with air flow.

# PCB LAYOUT

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended for improved thermal performance. For the best results, refer to Figure 13 and follow the guidelines below:

1) Place a 1μF capacitor as close to VDD33 as possible.
2) Place a small input capacitor (e.g. 100nF) close to VIN and GND to minimize transients on the input.
3) Place the IC close to the VIN to minimize trace inductance.
4) Route the high-current path and the return path between the input and the load close to each other in parallel to minimize loop inductance.
5) Place an analog signal ground (AGND) plane locally in the IC.
6) Connect the AGND plane to PGND planes at a single point.
7) Place multiple vias on the board to improve better thermal performance
   - 7.1 Place ⩾9 vias on the bottom of the VIN pad.
   - 7.2 Place ⩾12 vias close to the VIN pads at the edge of the IC.
   - 7.3 Place ⩾9 vias close to VOUT pads.

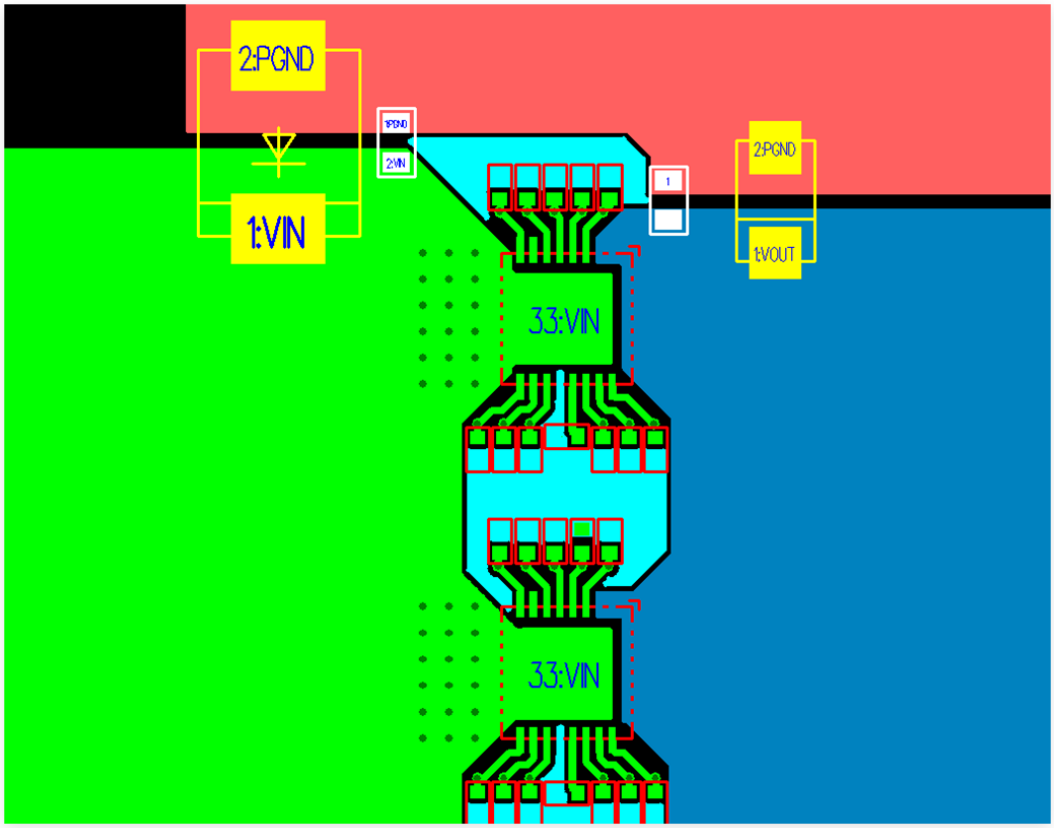
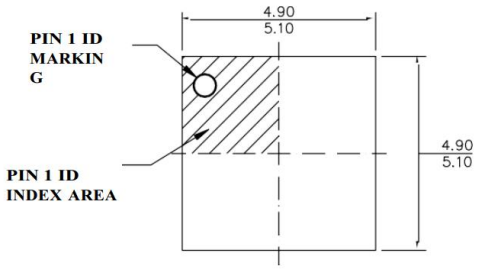


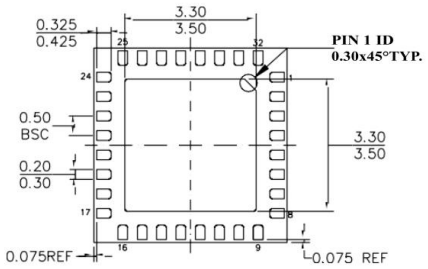

**Figure 13: Recommended PCB Layout**

# PHYSICAL DIMENSIONS

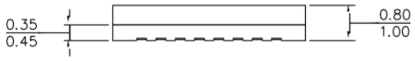
**LGA-32 (5mmx5mm)**



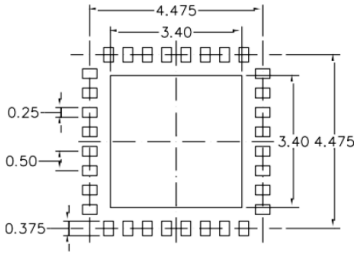

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

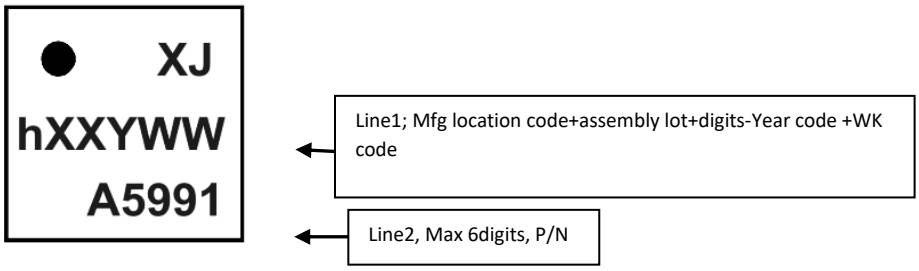
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

TOP MARKINGS

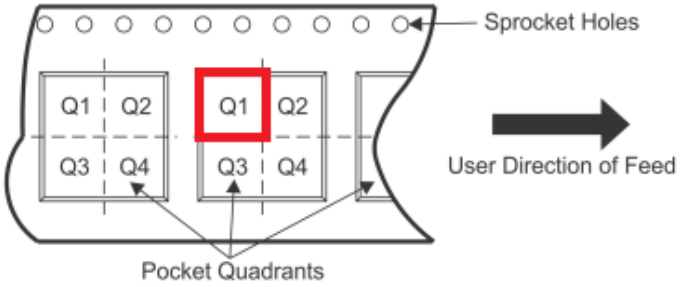
## Package Marking & PQ information

## XPA5991G32R Marking

Format:




Pin 1 located in Q1 direction in T&R




Remark :

Font: Arial

Letter height of 160um, wide of 120um

Letter pitch of 50um

Line space of 50um

LOGO Line 1 right

Logo of XJ should be required and placed on assigned Logo position as upside illustration.

Pin 1 Line 1 left

Pin 1 should be designed at left of line 1 for recognition.

Traceability Code: Line 2 and Line 3

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code

a) 1st digit: Assembly location code
b) 2nd & 3rd digit: Assembly lot number
XX means serial number for traceability, either of the 2 characters can be replaced by "0-9, A-Z, a-z"

c) 4th digit: Year code.

Year Code 2020-2051

| Year | Code | Year | Code | Year | Code | Year | Code |
|---|---|---|---|---|---|---|---|
| 2020 | 0 | 2028 | D | 2036 | N | 2044 | Y |
| 2021 | 1 | 2029 | E | 2037 | P | 2045 | Z |
| 2022 | 2 | 2030 | F | 2038 | R | 2046 | b |
| 2023 | 3 | 2031 | H | 2039 | S | 2047 | c |
| 2024 | 4 | 2032 | I | 2040 | T | 2048 | d |
| 2025 | 5 | 2033 | J | 2041 | U | 2049 | h |
| 2026 | 7 | 2034 | K | 2042 | V | 2050 | i |
| 2027 | C | 2035 | L | 2043 | X | 2051 | j |

d)5th & 6th digit: Week code, 01 means the 1st Work Week based on XinJi's calendar.

WK01 means the 1st Work Week based on XinJi's calendar.

2.Product Number Code: Line 3

| Product Name | P/N Code | Remark |
|---|---|---|
| XPA5991G32R | A5991 | |

3. Packing: 3K/Reel