

3.6A DC Motor Driver with Integrated Current Sensing and Regulation

Features

- Drives a DC Motor or Other Loads
- $R_{dson\ HS + LS}$: 560m Ω
- 3.6-A Maximum Drive Current
- VM: 4.5V to 33V Operating Voltage Range
- PWM Control Interface
- Low-Power Sleep Mode
- Integrated IPROPI current sensing for stall detection and current regulation
- Over-Current Protection (OCP)
- Thermal Shutdown (TSD)
- Under-Voltage Protection(UVLO)

Applications

- Printers
- Electrical appliances
- Industrial equipment
- Fitness equipment
- ATM (Automated Teller Machines)

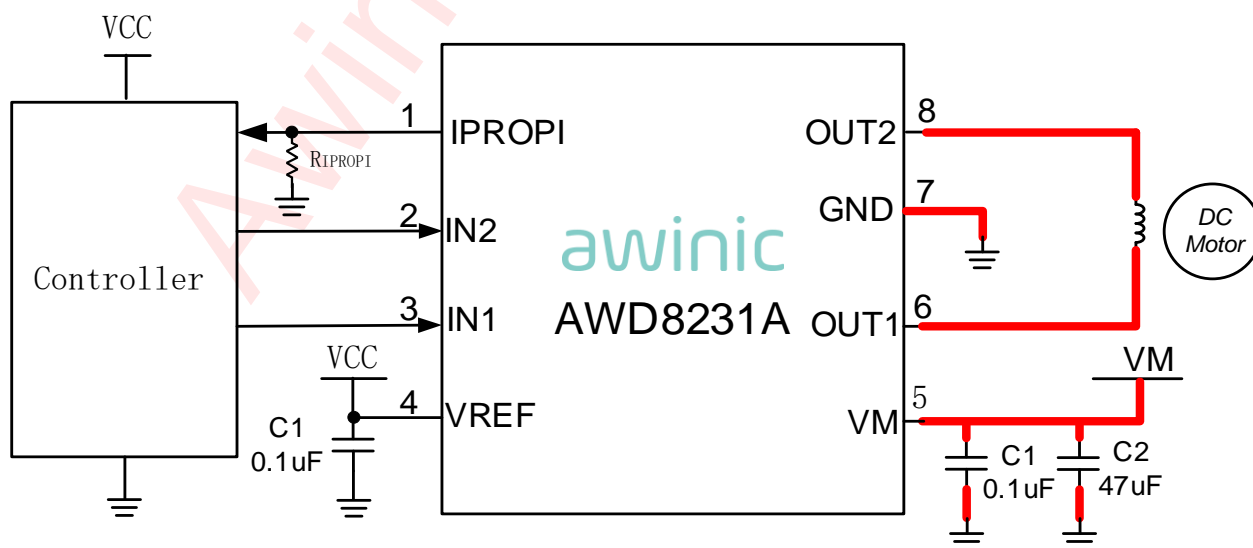
General Description

The AWD8231A device is an integrated motor driver, which is equipped with an N-channel H-bridge, a charge pump, current-sensing feedback, current regulation and protection circuits. The charge pump boosts efficiency by supporting N-channel MOSFET half bridges and 100% duty cycle driving.

The internal current mirror architecture on the IPROPI pin realizes the functions of current sensing and regulation, which eliminates the necessity of using large power shunt resistors, thus saving the board area and reducing the system cost. The IPROPI current-sensing output enables the microcontroller to detect motor stall or changes in load conditions. The external voltage reference pin VREF can determine the threshold of current regulation during startup and stall events without the intervention of the microcontroller.

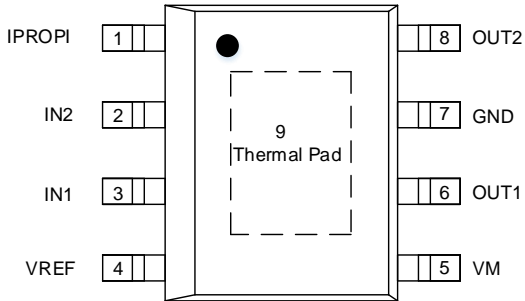
The low-power sleep mode achieves ultra-low quiescent current consumption by shutting down most of the internal circuits. Its internal protection features include power undervoltage lockout, output overcurrent and device overheating protection.

Typical Application Circuit

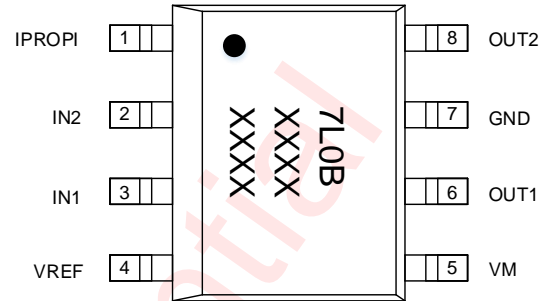


Pin Configuration And Top Mark

AWD8231ASPR
(Top View)

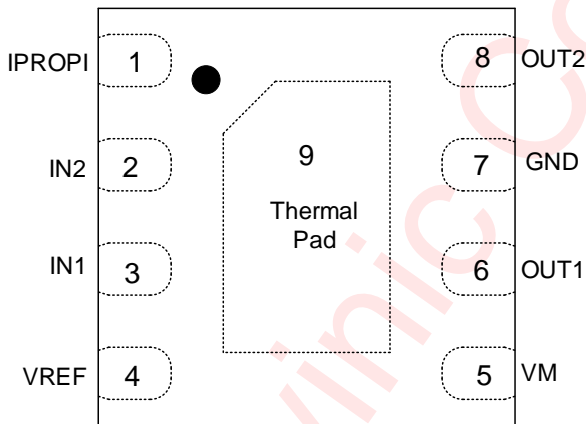


AWD8231ASPR Marking
(Top View)

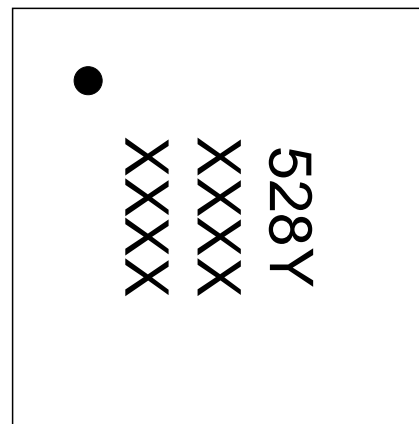


7L0B - AWD8231ASPR
XXXX/XXXX - Production Tracing Code

AWD8231ADNR
(Top View)



AWD8231ADNR Marking
(Top View)

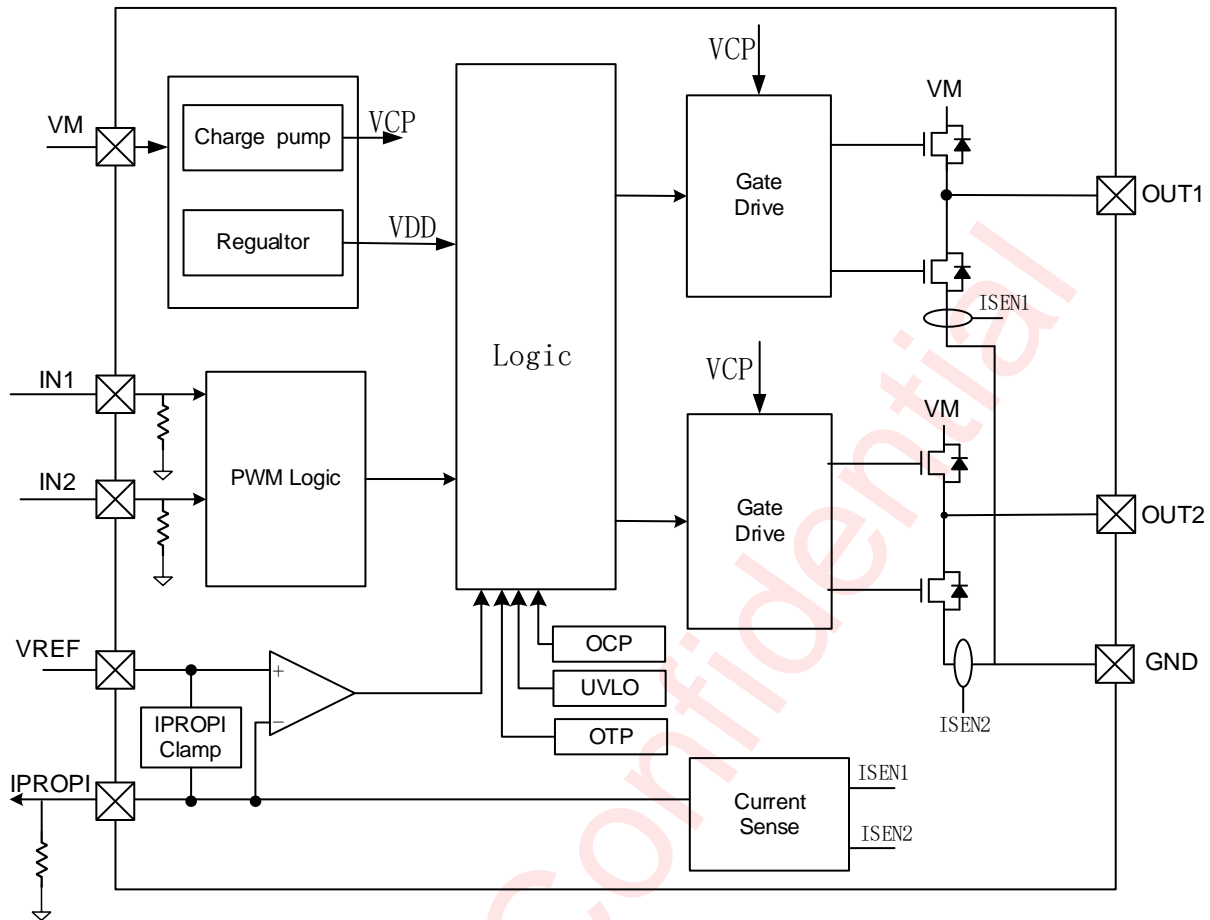


528Y - AWD8231ADNR
XXXXX/XXXXX - Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
1	IPROPI	Analog current output proportional to load current.
2	IN2	Logic inputs Controls the H-bridge output. Has internal pulldowns.
3	IN1	Logic inputs Controls the H-bridge output. Has internal pulldowns.
4	VREF	Analog input for current regulation. Apply a voltage between 0.3 to 5 V.
5	VM	4.5V to 33V power supply. Connect a 0.1- μ F bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
6	OUT1	H-bridge output Connect directly to the motor or other inductive load.
7	GND	Device power ground. Connect to system ground.
8	OUT2	H-bridge output Connect directly to the motor or other inductive load.
9	Thermal PAD	Connect to the board ground. For good thermal dissipation, use large ground planes on multiple layers and connect those planes with multiple nearby vias

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWD8231ASPR	-40°C~125°C	WBESOP-8L	7L0B	MSL3	ROHS+HF	3000 units/ Tape and Reel
AWD8231ADNR	-40°C~125°C	WBDFN 2mmX2mm- 8L(0.75)	528Y	MSL1	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
Motor power-supply voltage (VM)	-0.3V to 35V
Control pin voltage (IN1, IN2)	-0.3V to 6V
Reference input pin voltage (VREF)	-0.3V to 6V
OUT pin voltage (OUT1, OUT2)	-0.7V to VM+0.7V
Current Sensing and Regulation input pin voltage (IPROPI)	-0.3V to 5.75V
Output current	Internally Limited
Maximum operating junction temperature T _{JMAX}	160°C
Storage temperature TSTG	-65°C to 150°C
ESD(Including CDM HBM MM) ^(NOTE 2)	
HBM(Human Body Model)	±2000V
CDM(Charge Device Model)	±1500V
Latch-Up	
Test Condition: JESD78F	IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS -002-2022(CDM), ESDA/JEDEC JS-001-2023(HBM).

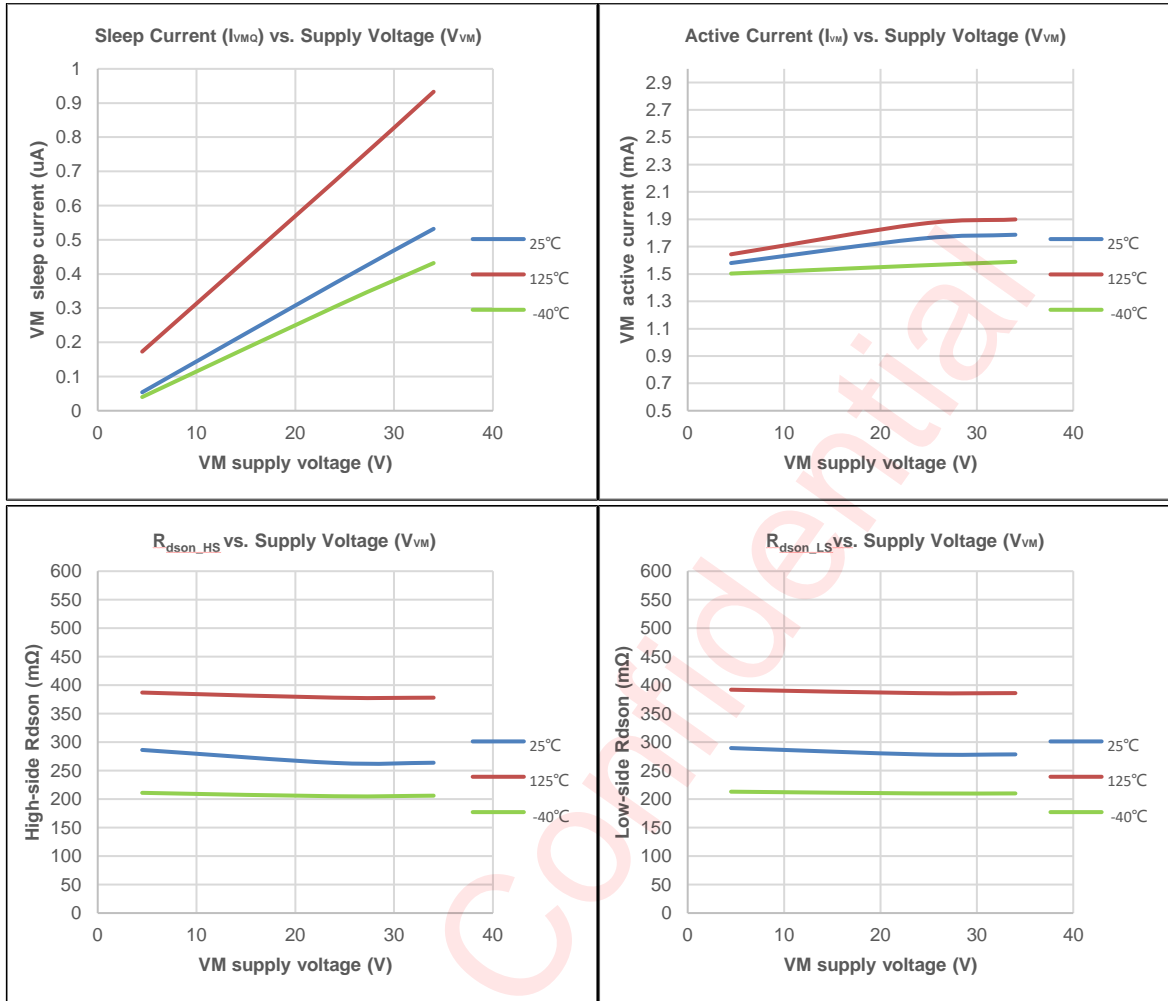
Electrical Characteristics

V_{VM}=24V, T_A=25°C for typical values (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
POWER SUPPLY(VM)						
V _{VM}	Power supply voltage	VM	4.5	33	V	
I _{VMQ}	VM sleep mode current	V _{VM} =24V, IN1=IN2=0, T _J =25°C		1	μA	
I _{VM}	VM active mode current	V _{VM} =24V, IN1=IN2=1	2	3	mA	
t _{WAKE}	Turn on time	Control signal to active mode		250	μs	
t _{SLEEP}	Turn off time	Control signal to sleep mode	0.8	1.5	ms	
LOGIC-LEVEL INPUTS (INx)						
V _{IH}	Input logic low voltage		1.5		V	
V _{IL}	Input logic high voltage			0.5	V	
V _{HYS}	Input hysteresis		200		mV	
I _{IL}	Input logic low current	V _{IN} =0V	-1	1	μA	
I _{IH}	Input logic high current	V _{IN} =3.3V		33	80	μA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
R _{PD}	Input pulldown resistors	To GND		100		kΩ
DRIVER OUTPUTS(OUTx)						
R _{dson_HS}	High-side MOSFET on resistance	V _{VM} =24V, I _{OUT} =1A		275		mΩ
R _{dson_LS}	Low-side MOSFET on resistance	V _{VM} =24V, I _{OUT} =1A		285		mΩ
V _{SD}	Body diode forward voltage	I _{OUT} =1A		0.8		V
t _{RISE}	Output rise time	V _{VM} =24V, OUTx rising from 10% to 90%		240		ns
t _{FALL}	Output fall time	V _{VM} =24V, OUTx rising from 90% to 10%		220		ns
t _{PD}	Input to output propagation delay	INx to OUTx		0.7	1	us
t _{DEAD}	Output dead time			360		ns
INTEGRATED CURRENT SENSE AND REGULATION (IPROPI, VREF)						
A _{IPROPI}	Current mirror scaling factor			1500		μA/A
A _{ERR} (Note1)	Current mirror total error	I _{OUT} =1A, V _{VM} >6.5V, V _{IPROPI} ≤3.0V	-5		5	%
t _{OFF}	Current regulation off time			25		μs
t _{BLK}	Current regulation blanking time			1.4		μs
t _{DELAY}	Current sense delay time			1.1		μs
t _{DEG}	Current regulation deglitch time			0.7		μs
PROTECTION CIRCUITS						
V _{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising	4.0	4.3	4.45	V
		Supply falling	3.9	4.2	4.35	V
V _{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		100		mV
t _{UVLO}	Supply undervoltage deglitch time			10		μs
I _{OC}	Overcurrent protection trip point		3.7			A
t _{OC}	Overcurrent protection deglitch time			1.5		μs
t _{RETRY}	Overcurrent protection retry time			3		ms
T _{TSD} (Note1)	Thermal shutdown temperature		150	175		°C
T _{HYS}	Thermal shutdown hysteresis			40		°C
Note1: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.						

Typical Characteristics



Detailed Functional Description

The AWD8231A is an 8-pin device for driving brushed DC motors from a 4.5V to 33V supply. Logic inputs control the H-bridge with four N-channel MOSFETs. Single power input VM powers the device and motor. The integrated charge pump enhances high-side FETs. Motor speed is PWM-controlled (0 – 200 kHz). Sleep mode activates when inputs are low. AWD8231A integrates current sensing via low-side MOSFET mirrors, outputting proportional current on IPROPI. This current can be converted to voltage using an external resistor. Integrated current regulation limits output current, configured via VREF.

Protection features include undervoltage lockout, overcurrent protection, and overtemperature shutdown.

Bridge Control

The AWD8231A is controlled using a PWM input interface. Each output is controlled by a corresponding input pin. **Table 1** shows the logic for the AWD8231A device.

Table 1 AWD8231A Device Logic

IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	0	Z	Z	Coast , sleep entered after 1.5ms
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake, low-side slow decay

The input pins can be powered before VM is applied. The H-bridge driver is controlled using a PWM interface (IN1 and IN2), and PWM input can adjust the motor speed by changing the duty cycle and frequency. The H-bridge current paths can be controlled by setting IN1 and IN2. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current.

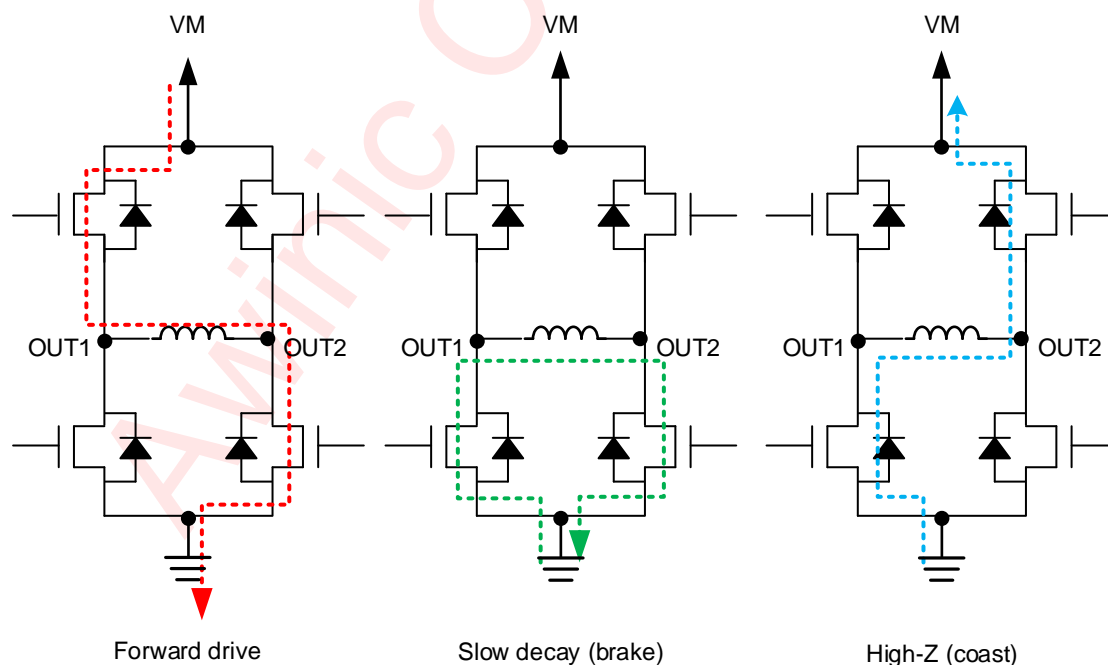


Figure 1 H-Bridge Forward drive Paths

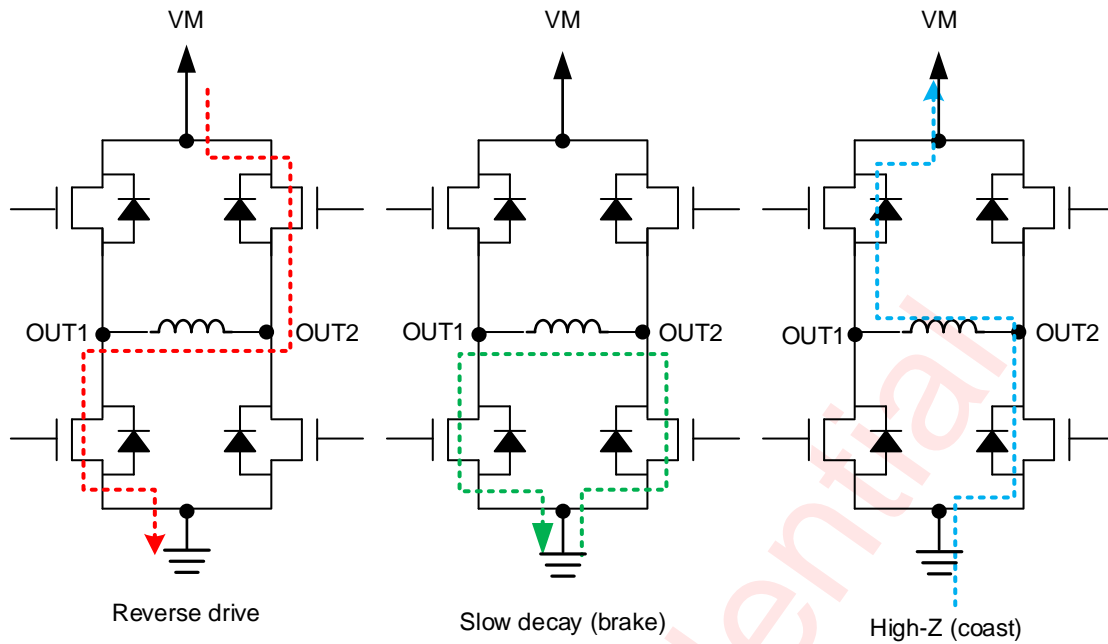


Figure 2 H-Bridge Reverse drive Paths

When transitioning an output from driving high to low, or vice versa, a dead time (t_{DEAD}) is automatically introduced to prevent shoot-through current. During this interval, the output enters a high-impedance (High-Z) state. If the output pin is measured during t_{DEAD} , its voltage level depends on the direction of the current flow. When current flows out of the pin, the voltage will be one diode drop below ground. Conversely, when current flows into the pin, the voltage will be one diode drop above VM. This diode represents the body diode of either the high-side or low-side FET.

The propagation delay (t_{PD}) is defined as the time between an input transition and the corresponding output change. This includes the input deglitch time and additional delays due to internal logic processing. The input deglitch filter helps to ensure that transient noise on the input pins does not erroneously affect the output states. Additional timing considerations include the rise (t_{RISE}) and fall (t_{FALL}) times of the output, which account for the turn-on and turn-off characteristics of the FETs.

Figure 3 below illustrates the timing relationship between the inputs and outputs of the motor driver.

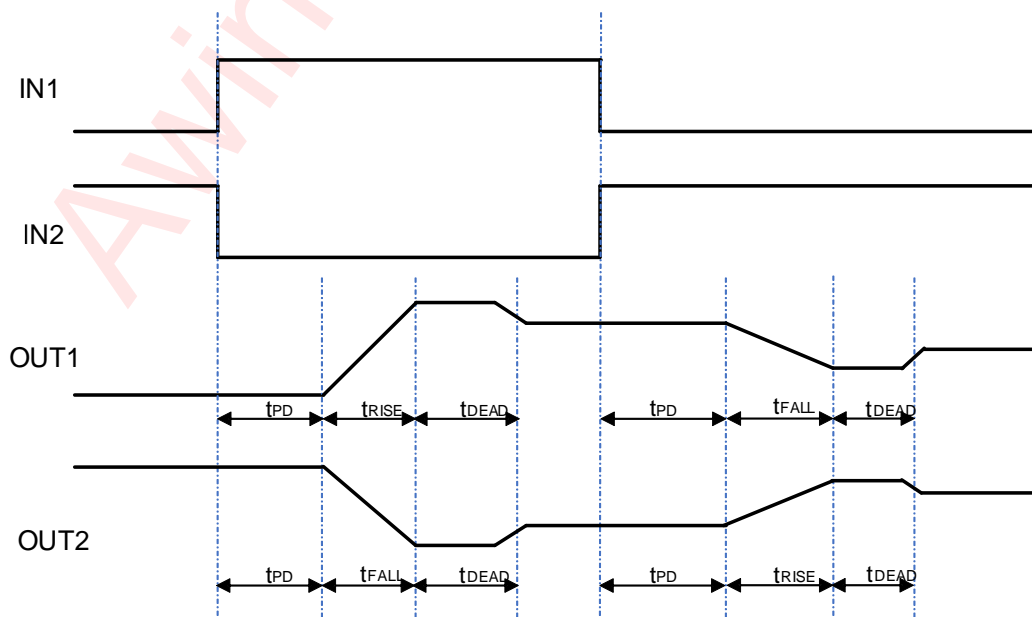


Figure 3 H-Bridge Timing Diagram

Current Sense and Regulation (IPROPI)

The AWD8231A device incorporates advanced current sensing, regulation, and feedback capabilities through its innovative IPROPI feature. This allows the device to monitor output current without requiring an external sense resistor or additional circuitry, significantly reducing system size, cost, and complexity. Additionally, in scenarios such as motor stalls or high torque events, the device can effectively limit the output current while providing precise feedback to the controller regarding load current via a current-proportional output. As illustrated in **Figure 4**, the IPROPI timings are detailed in the Electrical Characteristics table, offering a comprehensive overview of the device's performance and functionality. This design ensures reliable operation and optimal performance for a wide range of applications.

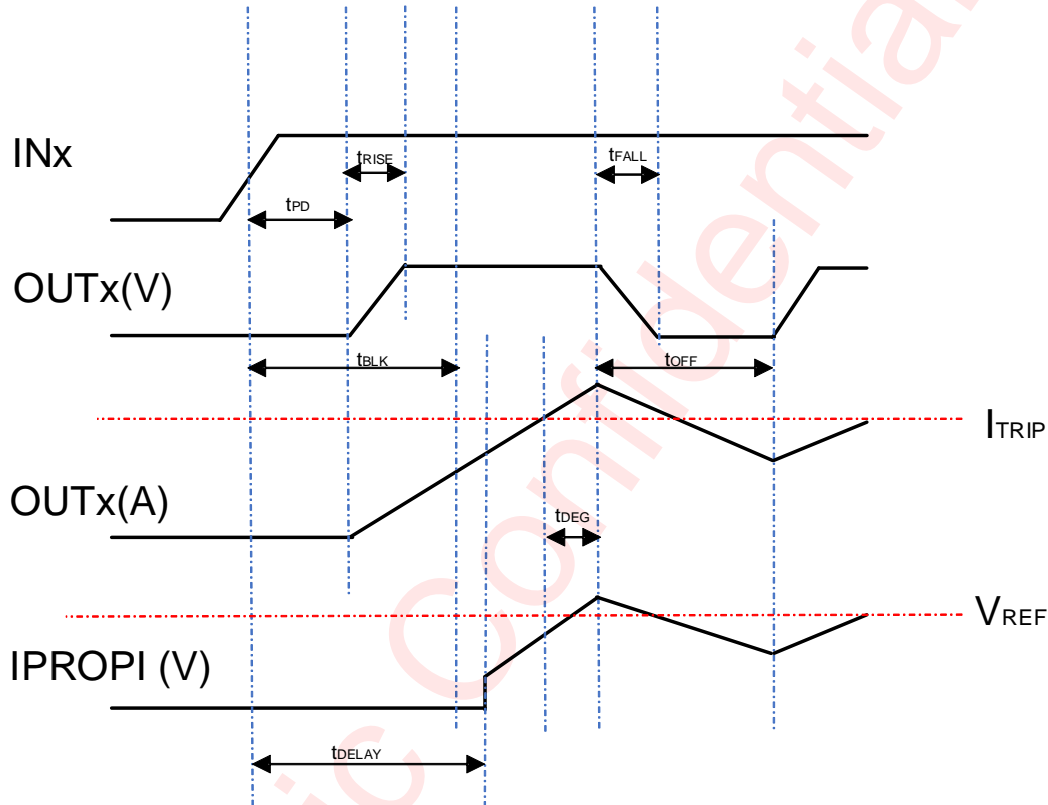


Figure 4 IPROPI Timing Diagram

Current Sensing

The IPROPI pin provides an analog output current that is proportional to the current flowing through the low-side power MOSFETs in the H-bridge, scaled by the A_{IPROPI} factor. The output current of IPROPI can be determined using **Equation 1**. In this equation, I_{LSx} is valid only when the current flows from drain to source in the low-side MOSFET. If the current flows in the reverse direction (source to drain) or through the body diode, the value of I_{LSx} for that channel becomes zero. For example, during the braking phase in slow-decay mode, the current out of the IPROPI pin is proportional only to the current in one of the low-side MOSFETs.

$$I_{PROPI} (\mu A) = (I_{LS1} + I_{LS2}) (A) \times A_{IPROPI} (\mu A/A) \quad (1)$$

In the Electrical Characteristics table, the parameter A_{ERR} represents the error associated with the A_{IPROPI} gain. This includes both the offset error added to the output current and the gain error.

The motor current is measured using an internal current mirror architecture on the low-side FETs, eliminating the need for an external power sense resistor as illustrated in Typical Application Circuit. This design allows continuous monitoring of the motor winding current during both drive and brake low-side slow-decay periods,

which is particularly useful in typical bidirectional brushed DC motor applications. In coast mode, the current freewheels and cannot be directly sensed because it flows from source to drain. However, the current can still be sampled by briefly reactivating the driver in either drive or slow-decay modes, measuring the current, and then switching back to coast mode.

The IPROPI pin is designed to interface with an external resistor (R_{IPROPI}) connected to ground, which generates a proportional voltage (V_{IPROPI}) corresponding to the analog current output (I_{IPROPI}). This configuration enables the load current to be accurately measured as the voltage drop across R_{IPROPI} using a standard analog-to-digital converter (ADC). The value of R_{IPROPI} can be selected based on the expected load current in the application, ensuring optimal utilization of the full range of the controller's ADC. Furthermore, the AWD8231A incorporates an internal IPROPI voltage clamp circuit that limits V_{IPROPI} relative to the VREF pin voltage (V_{VREF}), safeguarding the external ADC against potential overcurrent or unexpected high current events. The relationship between the IPROPI voltage and the output current is defined by **Equation 2**:

$$V_{IPROPI} (V) = I_{IPROPI} (A) \times R_{IPROPI} (\Omega) \quad (2)$$

The bandwidth of the IPROPI output is constrained by the sense delay time (t_{DELAY}) of the internal current sensing circuit. This parameter represents the delay from the issuance of a low-side MOSFET enable command (via the INx pins) until the IPROPI output becomes valid.

In applications where the device alternates between drive and slow-decay (brake) modes following an H-bridge PWM pattern, the low-side MOSFET responsible for current sensing remains continuously active. In this scenario, the sense delay time does not affect the IPROPI output. However, if the INx pins receive a command that disables the low-side MOSFETs, the IPROPI output will immediately disable in response to the input logic signal. It should be noted that even though the low-side MOSFETs may continue conducting current during their turn-off period, as determined by the device's slew rate (t_{RISE} specified in the Electrical Characteristics table), the IPROPI output will not reflect the current in the low-side MOSFETs during this transition.

Current Regulation

The AWD8231A device incorporates a current regulation feature utilizing a fixed off-time current chopping method. This enables the device to automatically constrain the output current during motor stall conditions, high torque demands, or other instances of excessive load current, all without requiring intervention from the external controller as illustrated in **Figure 5**.

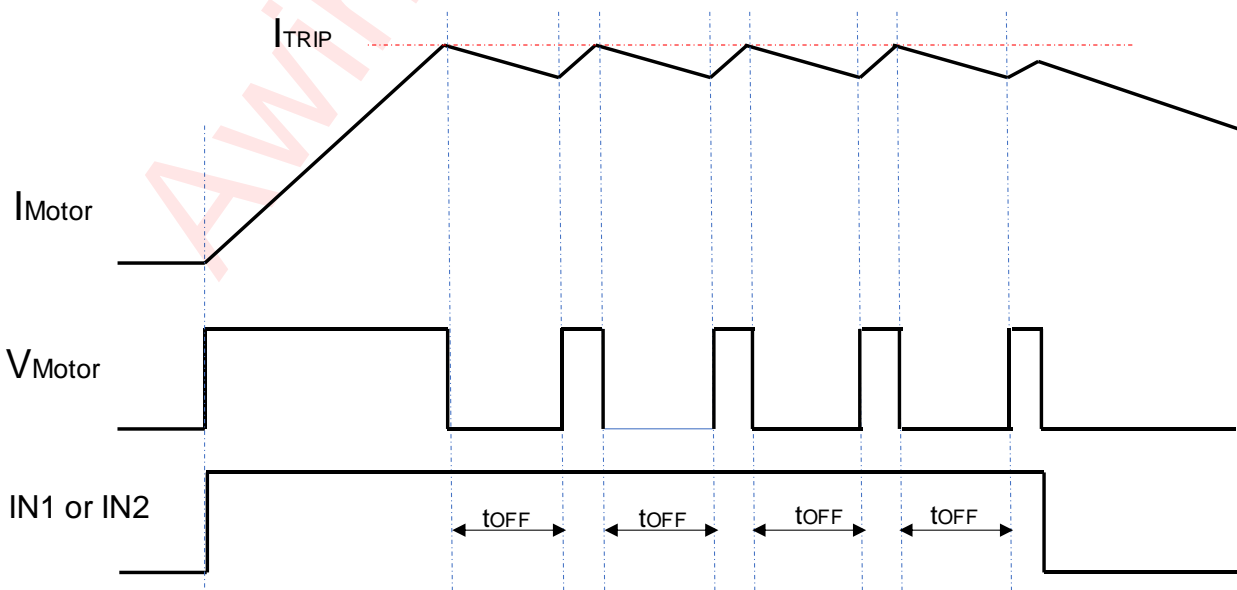


Figure 5 Off-Time Current-Regulation

The AWD8231A device employs an advanced current regulation mechanism that establishes the current chopping threshold (I_{TRIP}) through a combination of the reference voltage (V_{VREF}) and the output resistor (R_{IPROPI}). This is achieved by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} using an internal comparator. The relationship between these parameters can be expressed as follows:

$$I_{TRIP} (A) \times A_{IPROPI} (\mu A/A) = V_{VREF} (V) / R_{IPROPI} (\Omega) \quad (3)$$

For instance, if V_{VREF} is set to 3.3 V, R_{IPROPI} is configured at 1000 Ω , and A_{IPROPI} is defined as 1500 $\mu A/A$, the resulting I_{TRIP} will approximate 2.2 A.

The fixed off-time current chopping scheme facilitates up to 100% duty cycle current regulation. Upon expiration of the t_{OFF} period, the H-bridge automatically reactivates without requiring a new control input edge on the INx pins to reset the outputs. If the motor current surpasses the I_{TRIP} threshold, the outputs transition into a current chopping mode characterized by a fixed off time (t_{OFF}). During this interval, the H-bridge enters a brake/low-side slow decay state (both low-side MOSFETs ON) for the duration of t_{OFF} following an I_{OUT} exceeding I_{TRIP} . Subsequent to t_{OFF} , the outputs resume operation in accordance with the control inputs provided I_{OUT} remains below I_{TRIP} . Conversely, if I_{OUT} continues to exceed I_{TRIP} , the H-bridge initiates another phase of brake/low-side slow decay lasting t_{OFF} . Should the state of the INx control pins alter during the t_{OFF} period, any remaining t_{OFF} time is disregarded, and the outputs conform to the updated inputs.

To enhance operational stability, the I_{TRIP} comparator incorporates both a blanking time (t_{BLK}) and a deglitch time (t_{DEG}). The internal blanking time effectively mitigates the influence of voltage and current transients during output switching on the current regulation process. Such transients may arise from capacitors within the motor or along the motor terminal connections. The internal deglitch time ensures transient conditions do not prematurely activate the current regulation. In scenarios where transient conditions persist longer than the deglitch time, positioning a 10nF capacitor on the IPROPI pin near the device assists in filtering transients on the IPROPI output, thereby preventing premature triggering of current regulation. The capacitor value can be adjusted as necessary; however, excessively large capacitor values may impair the response time of the current regulation circuitry.

Internal current regulation and current feedback functionalities can be disabled by connecting IPROPI to GND and setting the VREF pin voltage above GND. If current feedback is desired while current regulation is unnecessary, configure V_{VREF} and R_{IPROPI} such that V_{IPROPI} never attains the V_{VREF} threshold. For optimal performance of the current regulation circuit, ensure V_{VREF} resides within the range of VREF pin voltages specified in the Recommended Operating Conditions table.

Device Functional Modes

The AWD8231A has three functional modes, as shown in Table 2.

Table 2 AWD8231A Functional Modes

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	N1 or IN2 =1	Operating	Operating
Sleep Mode	N1 = IN2 =0	Disabled	Disabled
Fault Mode	Trigger Protection	Disabled	Protection Circuit Operation

Active Mode

Once the supply voltage on the VM pin exceeds the undervoltage threshold (V_{UVLO}), and the INx pins are not in the state where $IN1 = 0$ and $IN2 = 0$, after the wake-up time (t_{WAKE}) has passed, the device transitions into active mode. In this mode, the H-bridge, charge pump, and internal logic circuits are fully operational, allowing the device to accept input signals.

Sleep Mode

If the IN1 and IN2 pins are held low for a duration of t_{SLEEP} , the AWD8231A enters a low-power consumption sleep mode. During this mode, the outputs are maintained in a high-impedance (High-Z) state, and the current drawn from the supply pin (I_{VMQ}) is minimized. Upon power-up, if all input pins are low, the device will instantaneously transition into sleep mode. Full operational functionality is restored once any of the input pins are set high for longer than the t_{WAKE} period.

Fault Mode

The AWD8231A enters fault mode upon detection of a fault condition, which serves to safeguard both the device and the connected load. The specific behavior in fault mode is outlined in **Table 3** and varies depending on the nature of the fault. The device will exit fault mode and transition back into active mode once the recovery condition has been satisfied.

Table 3 AWD8231A Fault Mode

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
Under-Voltage Protection(UVLO)	$VM < V_{UVLO,falling}$	Disabled	Disabled	$VM > V_{UVLO,rising}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	Operating	$I_{OUT} < I_{OCP}$
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	Disabled	Operating	$T_J < T_{TSD} - T_{HYS}$

Protection Circuits

The AWD8231A device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

Under-Voltage Protection(Uvlo)

If at any time the voltage on the VM pin falls below the under-voltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VM pin voltage rises above the UVLO threshold.

Overcurrent Protection

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG} , all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low side FETs. A short to the VM pin, GND, or from the OUT1 pin to the OUT2 pin results in an overcurrent condition.

Thermal Shutdown

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Application Information

The AWD8231A is used to drive one brushed dc motor. The following design procedure can be used to configure the AWD8231A device.

Design Requirements

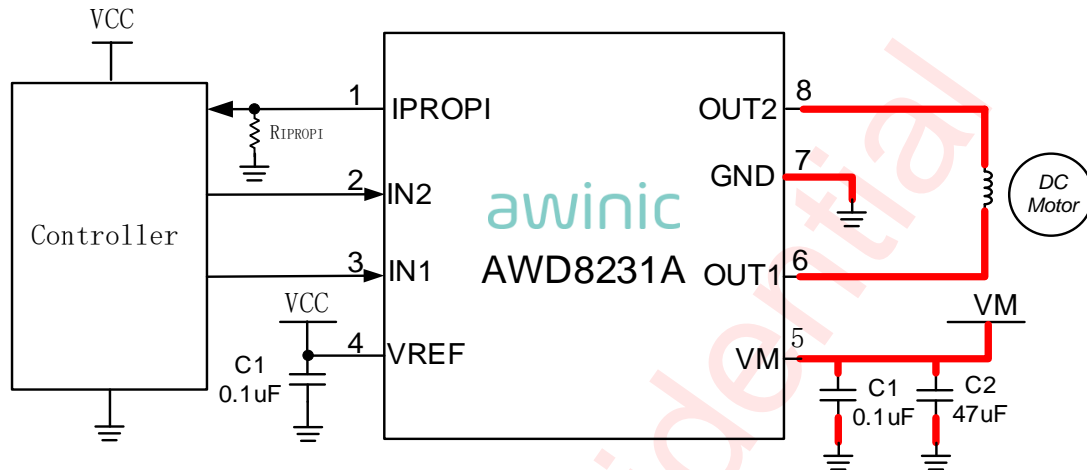


Figure 4 Typical Application Circuit of AWD8231A

Table 4 lists the required parameters for a typical usage case.

Table 4 AWD8231A Required Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V _{VM}	24 V
Motor RMS current	I _{RMS}	0.5 A
Motor startup current	I _{START}	0.8 A
VREF voltage	VREF	3.3 V
IPROPI resistance	R _{IPROPI}	2.2kΩ
Motor current trip point	I _{TRIP}	1 A
PWM frequency	f _{PWM}	5 kHz

Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

Drive Current

The current path is through the high-side sourcing NMOS power driver, motor winding, and low-side sinking NMOS power driver. Power dissipation losses in one source and sink NMOS power driver are shown in Equation 2:

$$P_D(W) = I^2(R_{DS(on)(HS)} + R_{DS(on)(LS)})$$

The AWD8231ASPR device has been measured to be capable of 2.1A RMS current at 25°C on standard FR-4 PCBs. The AWD8231ADNR device has been measured to be capable of 1.2A RMS current at 25°C on

standard FR-4 PCBs. The maximum RMS current varies based on the PCB design, ambient temperature, and PWM frequency.

I_{PROPI} Resistor

Design the I_{TRIP} current to 1.5A according to the application requirements, with V_{REF} = 3.3V and A_{I_{PROPI}} = 1500 (μA/A). Calculate the value of the R_{I_{PROPI}} resistor using the following formula:

$$I_{TRIP} (A) \times A_{I_{PROPI}} (\mu A/A) = V_{VREF} (V) / R_{I_{PROPI}} (\Omega) \quad (4)$$

The calculation results in R_{I_{PROPI}} = 2.2K.

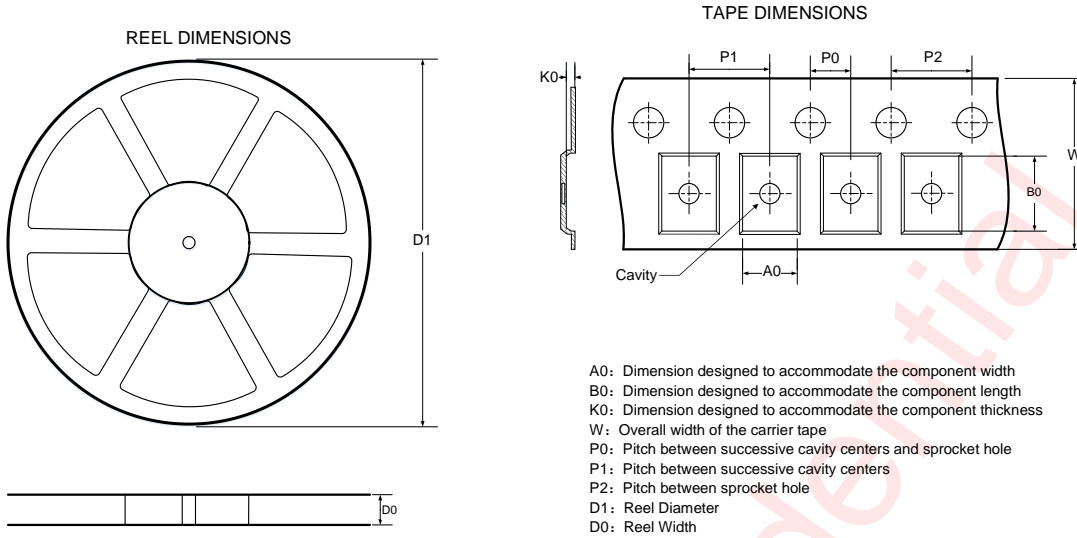
VM Decoupling Capacitor

A 0.1μF and 47μF capacitor should be placed close to the VM pin for power supply filtering and absorbing the pulse voltage generated by the motor's back EMF. For applications with low-temperature requirements, ceramic capacitors are recommended due to their better temperature characteristics compared to aluminum electrolytic capacitors.

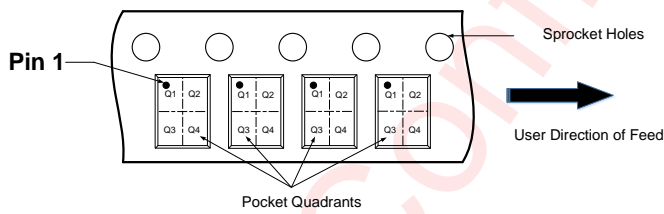
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Tape And Reel Information

AWD8231ASPR



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



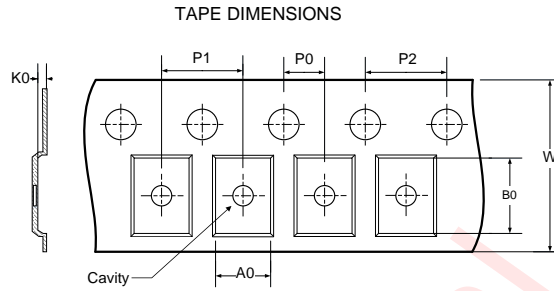
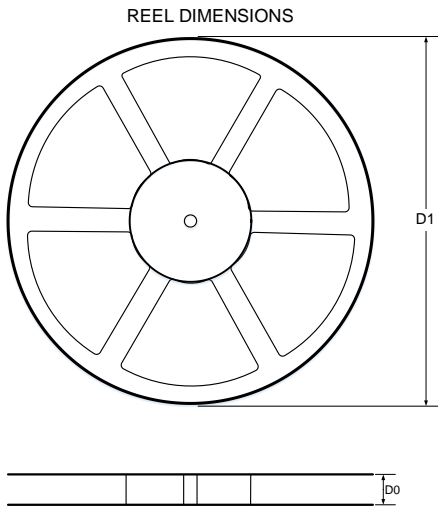
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

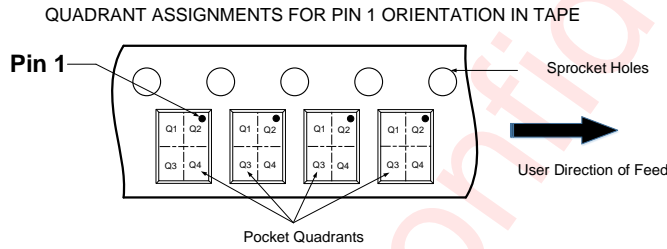
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.0	12.40	6.55	5.30	2.00	2.00	8.00	4.00	12.00	Q1

All dimensions are nominal

AWD8231ADNR



- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P0: Pitch between successive cavity centers and sprocket hole
- P1: Pitch between successive cavity centers
- P2: Pitch between sprocket hole
- D1: Reel Diameter
- D0: Reel Width



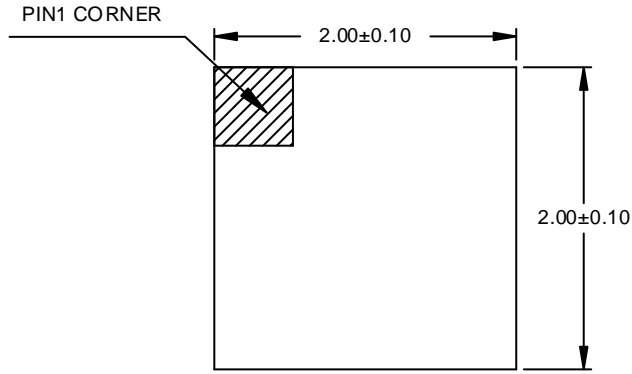
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

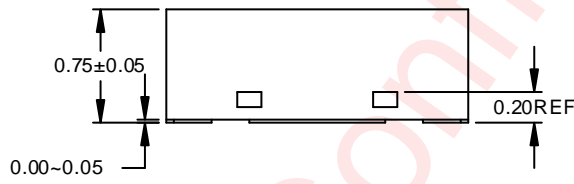
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	2.3	1	2	4	4	8	Q2

All dimensions are nominal

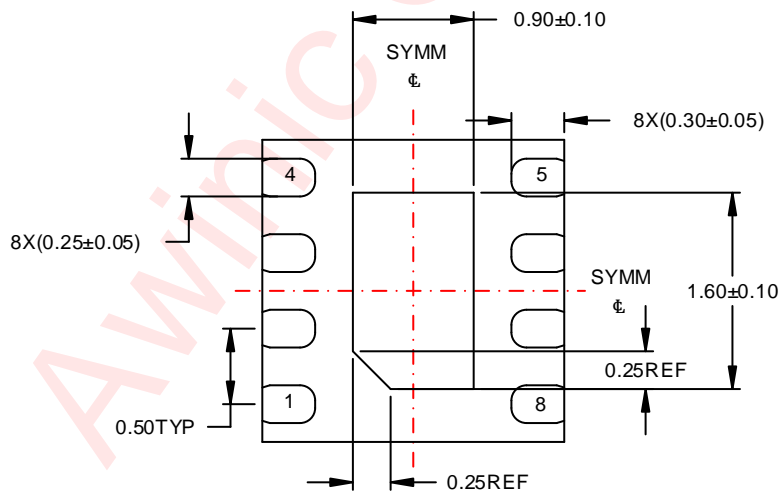
AWD8231ADNR



TOP VIEW



SIDE VIEW

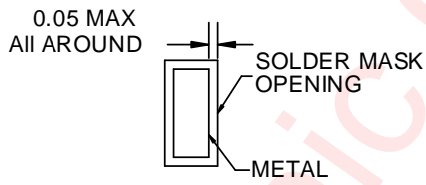
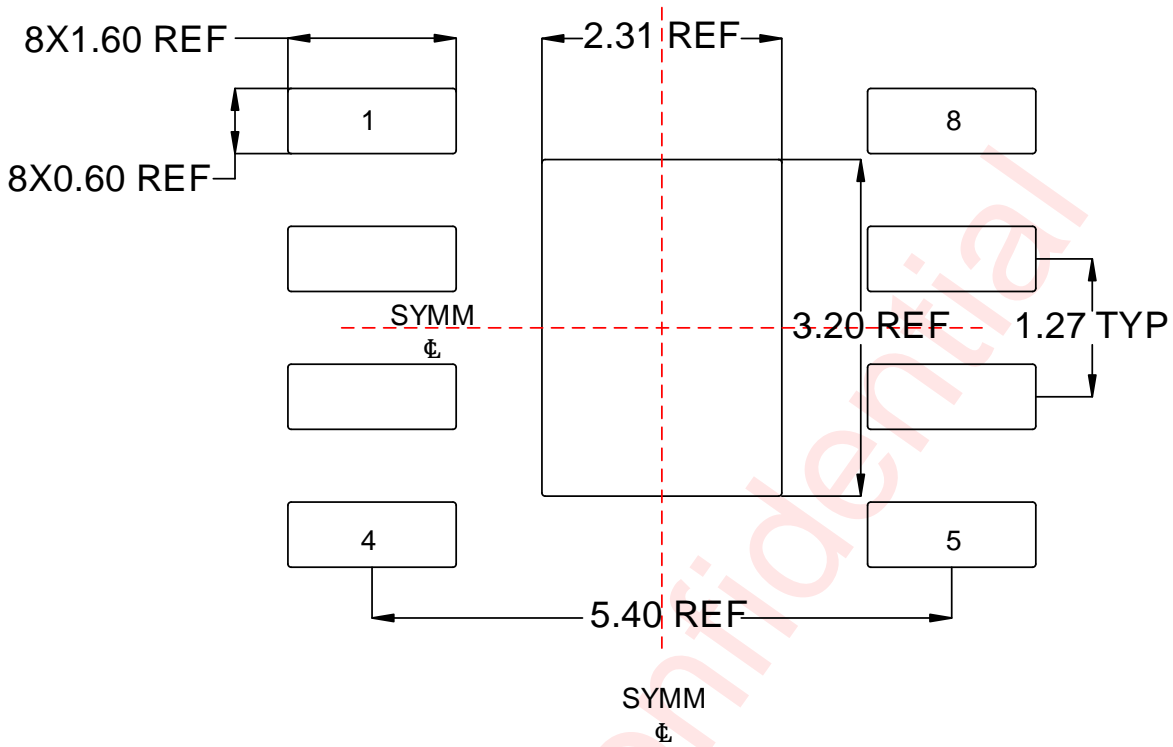


BOTTOM VIEW

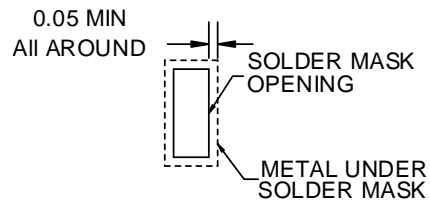
Unit: mm

Land Pattern Data

AWD8231ASPR



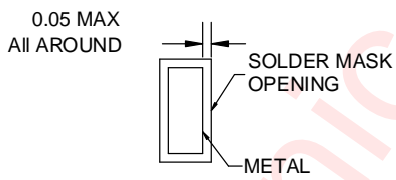
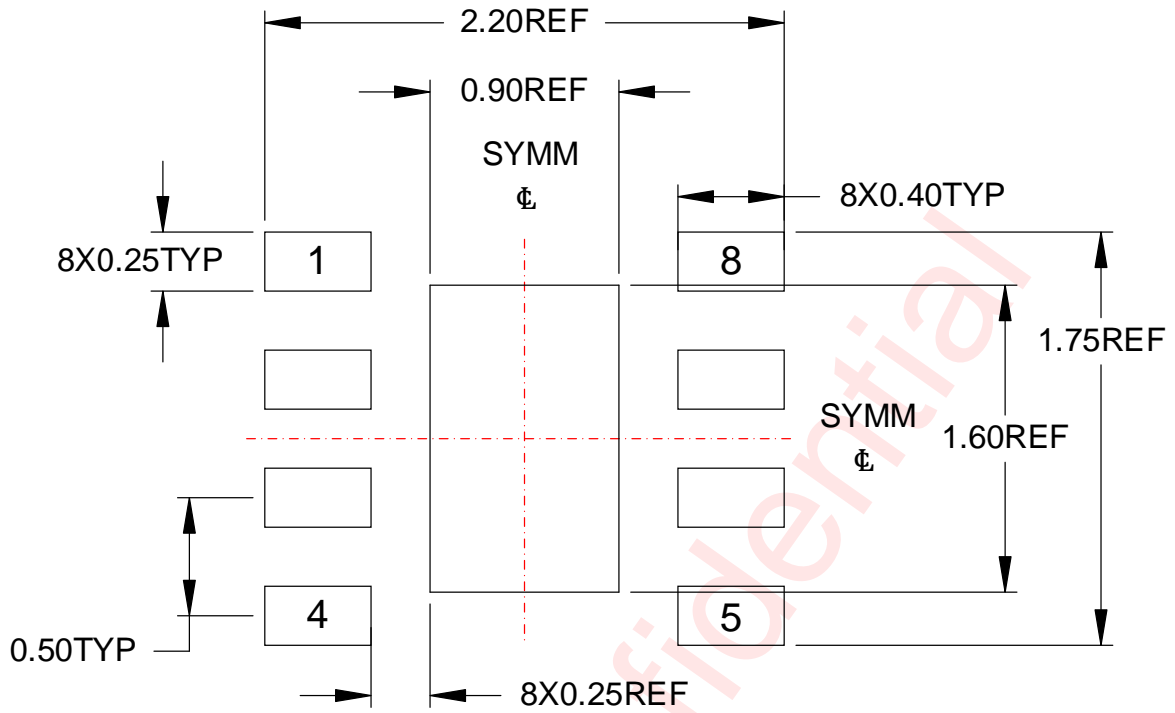
NON SOLDER MASK DEFINED



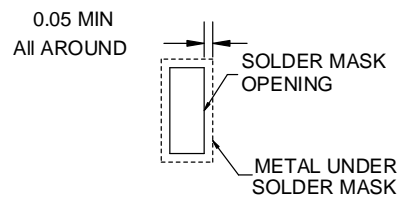
SOLDER MASK DEFINED

Unit: mm

AWD8231ADNR



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Mar. 2025	Officially released
V1.1	Sep. 2025	Add the description of AWD8231ADNR chip

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