AW95124 24-Bit Translating I²C and SMBus I/O Expander with Interrupt Output, Reset, and Agile I/O Configuration Registers

Features

- I²C-bus to 24-bit parallel port expander
- 1MHz I²C interface
- power supply
  - V_{CCI}: 1.08V~3.6V
  - V_{CCP}: 1.08V~3.6V
- Allows bidirectional voltage-level translation and GPIO expansion between 1.2V, 1.8V, 2.5V and 3.3V I²C bus and P ports
- Low standby current consumption of 1.5μA (typical at 3.6V V_{CCI}/V_{CCP})
- Interrupts can be specified by level or edge(rising or falling) triggered
- 3.6V tolerant I/O ports
- Active LOW reset input (RSTN)
- I²C software reset call
- Open-drain active-low interrupt output (INTN)
- Hardware address pin allows four devices on the same I²C, SMBus bus
- Noise filter on SCL/SDA inputs
- Latched outputs with high-current drive capability for directly driving LEDs
- Operation temperature range: -40°C~105°C
- Package:
  - AW95124FOR: FOWLP 2.6X2.6-36B
  - AW95124QNR: QFN 5X5-32L

Applications

Servers

Routers (Telecom Switching Equipment)

Personal Computers

Personal Electronics

Industrial Automation Equipment

Products with GPIO-Limited Processors

General Description

AW95124 device provides general purpose parallel input/output (I/O) expansion for the two-line bidirectional I²C bus (or SMBus) protocol. The device can operate with a power supply voltage ranging from 1.08V to 3.6V on the I²C bus side (V_{CCI}) and a power supply voltage ranging from 1.08V to 3.6V on the P port side (V_{CCP}).AW95124 supports 100kHz, 400kHz, and 1MHz I²C clock frequencies.

AW95124 has Agile I/O plus ports which include additional features designed to enhance the I/O performance. The additional features are: maskable interrupt, latchable inputs, interrupt status register, programmable output drive strength, programmable pull-up and pull-down resistors, programmable open-drain or push-pull outputs, Interrupts can be specified by level or edge(rising or falling) triggered, and can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

The power-on reset puts the registers in their default state and initializes the I²C/SMBus state machine. The RSTN pin causes the same reset/initialization to occur without depowering the part. The system master can also accomplish a reset via an I²C command and initialize all registers to their default state.

Typical Application Circuit

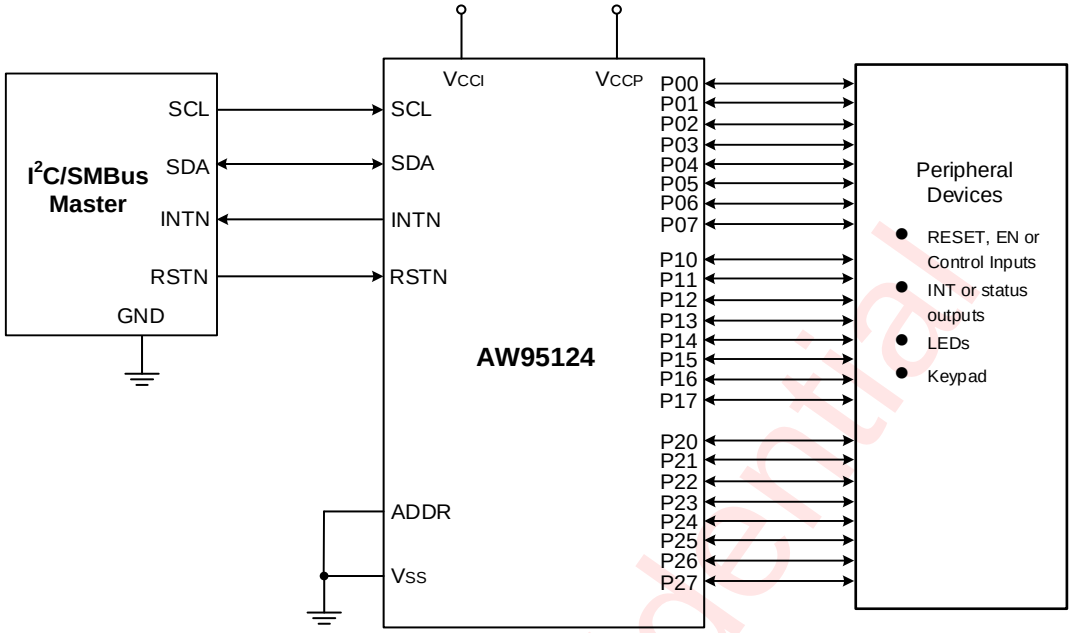
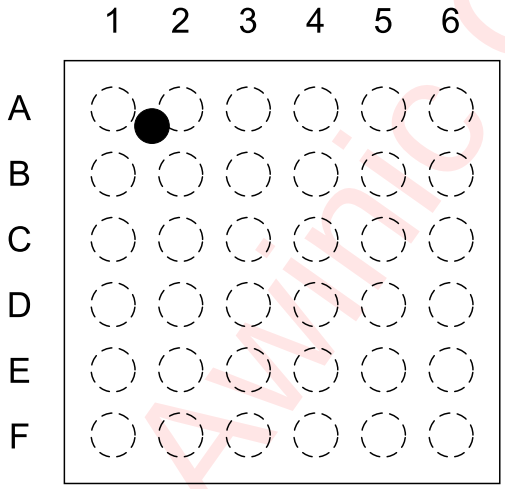


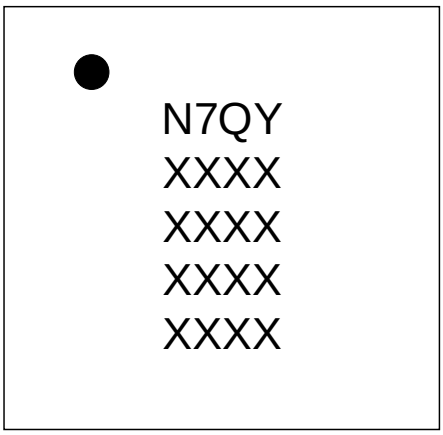
Figure 1 AW95124 Simplified Application Circuit

Pin Configuration And Top Mark

AW95124FOR
(Top View)

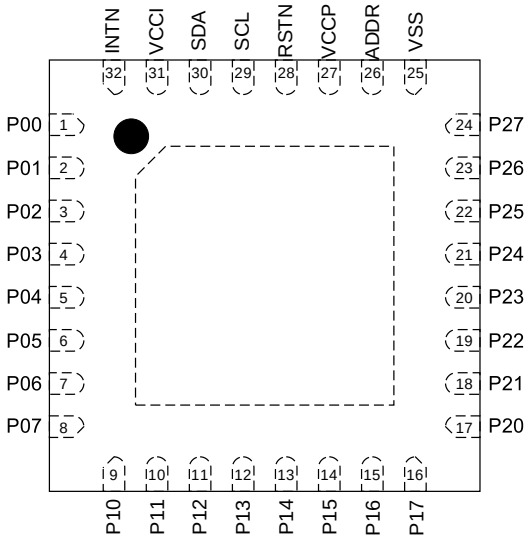


AW95124FOR Marking
(Top View)

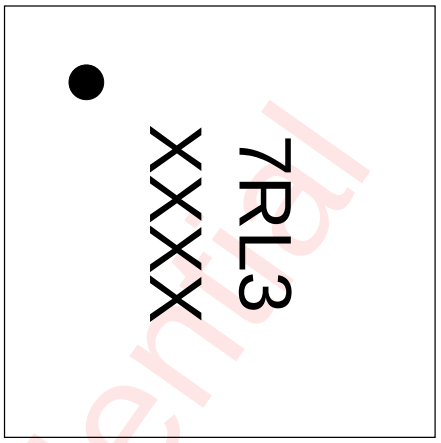


N7QY - AW95124FOR
XXXX/XXXX/XXXX/XXXX - Production Tracing Code

AW95124QNR
(Top View)



AW95124QNR Marking
(Top View)



7RL3 - AW95124QNR
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Figure 2 Pin Configuration and Marking

Pin Definition

Name	Pin No.		Description
	AW95124FOR	AW95124QNR	
SCL	A3	29	Serial clock line. Connect to V_{CCI} through a pull-up resistor
SDA	A2	30	Serial data line. Connect to V_{CCI} through a pull-up resistor
V_{CCI}	A1	31	Supply voltage of I^2C-bus. Connect directly to the VCC of the external I^2C-bus master. Provides voltage-level translation
INTN	C4	32	Interrupt output. Connect to V_{CCI} or V_{CCP} through a pull-up resistor
P00	B1	1	Port 0 input/output 0. At power on, P00 is configured as an input
P01	D4	2	Port 0 input/output 1. At power on, P01 is configured as an input
P02	C1	3	Port 0 input/output 2. At power on, P02 is configured as an input
P03	D2	4	Port 0 input/output 3. At power on, P03 is configured as an input
P04	D1	5	Port 0 input/output 4. At power on, P04 is configured as an input
P05	E1	6	Port 0 input/output 5. At power on, P05 is configured as an input
P06	D3	7	Port 0 input/output 6. At power on, P06 is configured as an input
P07	F1	8	Port 0 input/output 7. At power on, P07 is configured as an input
P10	E2	9	Port 1 input/output 0. At power on, P10 is configured as an input
P11	F2	10	Port 1 input/output 1. At power on, P11 is configured as an input
P12	E3	11	Port 1 input/output 2. At power on, P12 is configured as an input
P13	F3	12	Port 1 input/output 3. At power on, P13 is configured as an input
P14	F4	13	Port 1 input/output 4. At power on, P14 is configured as an input
P15	E4	14	Port 1 input/output 5. At power on, P15 is configured as an input
P16	F5	15	Port 1 input/output 6. At power on, P16 is configured as an input
P17	E5	16	Port 1 input/output 7. At power on, P17 is configured as an input
P20	F6	17	Port 2 input/output 0. At power on, P20 is configured as an input
P21	E6	18	Port 2 input/output 1. At power on, P21 is configured as an input
P22	D5	19	Port 2 input/output 2. At power on, P22 is configured as an input
P23	D6	20	Port 2 input/output 3. At power on, P23 is configured as an input
P24	C5	21	Port 2 input/output 4. At power on, P24 is configured as an input
P25	C6	22	Port 2 input/output 5. At power on, P25 is configured as an input
P26	B5	23	Port 2 input/output 6. At power on, P26 is configured as an input
P27	B6	24	Port 2 input/output 7. At power on, P27 is configured as an input
V_{SS}	A6	25	Supply ground.
ADDR	A5	26	Address input. Connect directly to V_{CCI}, V_{SS}, SCL or SDA.
V_{CCP}	A4	27	Supply voltage for P Port .
RSTN	B4	28	Active LOW reset input. Connect to V_{CCI} through a pull-up resistor if no active connection is used.
NC	B2,B3,C2,C3	-	Not connected

Functional Block Diagram

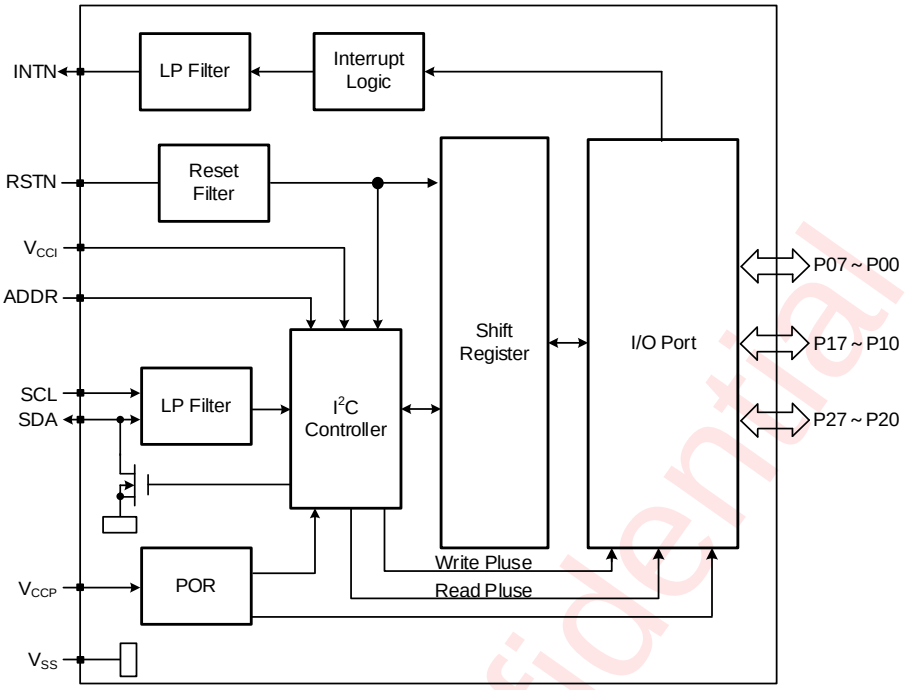


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW95124FOR	-40°C~105°C	FOWLP 2.6X2.6-36B	N7QY	MSL1	RoHS+HF	4500 units/ Tape and Reel
AW95124QNR	-40°C~105°C	QFN 5X5-32L	7RL3	MSL3	RoHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

Parameters		Range
Supply voltage, V_{CCI}, V_{CCP}		-0.5V to 4V
Input voltage, V_I		-0.5V to 4V
Output voltage, V_O		-0.5V to 4V
Continuous output low current, I_{OL}(P port)	V_O=0 to V_{CCP}	50mA
Continuous output low current, I_{OL}(SDA, INTN)	V_O=0 to V_{CCI}	50mA
Continuous output high current, I_{OH}(P port)	V_O=0 to V_{CCP}	-50mA
Continuous current through V_{SS}		-200mA
Continuous current through V_{CCP}		160mA
Continuous current through V_{CCI}		10mA
Operating free-air temperature range T_A		-40°C to 105°C

Parameters	Range
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
Maximum operating junction temperature T_{JMAX}	150°C
ESD(Including CDM HBM)(NOTE2)	
HBM	±4kV
CDM	±1kV
Latch-Up	
Test condition: JESD78F	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method of AW95124FOR and AW95124QNR: ESDA/JEDEC JS-001-2023, the CDM test method of AW95124FOR and AW95124QNR: ESDA/JEDEC JS-002-2022.

Recommended Operating Conditions

Symbol	Parameters		Min.	Typ.	Max.	Unit
V_{CCI}	I^2C-Bus Supply voltage		1.08		3.6	V
V_{CCP}	P port Supply voltage		1.08		3.6	V
V_{IH}	High-level input voltage	SCL,SDA,ADDR,RSTN	0.7×V_{CCI}		3.6	V
		P port	0.7×V_{CCP}		3.6	V
V_{IL}	Low-level input voltage	SCL,SDA,ADDR,RSTN	-0.5		0.3×V_{CCI}	V
		P port	-0.5		0.3×V_{CCP}	V
I_{OH}	High-level output current	continuous; P port; V_O=0~V_{CCP}			-10	mA
I_{OL}	Low-level output current	continuous; P port; V_O=0~V_{CCP}			25	mA
T_A	Operating free-air temperature		-40		105	°C

Electrical Characteristics

V_{CCI}=1.08V to 3.6V, T_A=25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	V_{CCP}	MIN	TYP	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I=-18mA	1.08~3.6V	-1.2			V
V_{PORR}	Power-on reset voltage	V_{CCP} rising			0.85	1	V
V_{PORF}	Power-on reset voltage	V_{CCP} falling		0.6	0.75		V
V_{OH}(NOTE3)	P port high-level output voltage	I_{OH}=–4mA	1.08V	0.75			V
		I_{OH}=–10mA	1.65V	1.4			V
		I_{OH}=–10mA	2.3V	2.1			V
		I_{OH}=–10mA	3V	2.8			V
V_{OL}(NOTE4)	P port low-level output voltage	I_{OL}=8mA	1.08V			0.25	V
		I_{OL}=10mA	1.65V			0.15	V
		I_{OL}=10mA	2.3V			0.1	V
		I_{OL}=10mA	3V			0.1	V

PARAMETER		TEST CONDITION	V_{CCP}	MIN	TYP	MAX	UNIT
I_{OL}	SDA Low-level output current	V_{OL}=0.4V	<1.32V	16			mA
		V_{OL}=0.4V	1.32~3.6V	20			mA
	INTN Low-level output current	V_{OL}=0.4V	1.08~3.6V	4			mA
I_I	P port Input leakage current	V_I=V_{CCP} or V_{SS}	1.08~3.6V			±1	μA
		V_I=3.6V	0V			±1	μA
	SCL, SDA, RSTN, ADDR Input leakage current	V_I=V_{CCI} or V_{SS}	1.08~3.6V			±1	μA
I_{CC} (I_{CCI}+I_{CCP})	Operating mode (1MHz)	SDA, RSTN, ADDR= V_{CCI}; P port=V_{CCP} or V_{SS}; I/O=inputs, f_{SCL}=1MHz	3.6V		22	52	μA
			1.08V		4.3	12	
	Operating mode (400kHz)	SDA, RSTN, ADDR= V_{CCI}; P port=V_{CCP} or V_{SS}; I/O=inputs, f_{SCL}=400kHz	3.6V		9.5	22	μA
			1.08V		1.95	6	
	Standby mode	SDA, RSTN, ADDR= V_{CCI}; P port=V_{CCP} or V_{SS}; I/O=inputs, f_{SCL}=0kHz	3.6V		1.5	3.6	μA
			1.08V		0.4	1.2	
Rpupd(int)	Internal pull-up/pull-down resistance	P port		50	100	200	kΩ
ΔI_{CCI}	Additional quiescent supply current for V_{CCI}	SCL, SDA, RSTN, ADDR; one input at V_{CCI}-0.6V, other inputs at V_{CCI};	1.08~3.6V		12	50	μA
ΔI_{CCP}	Additional quiescent supply current for V_{CCP}	P port; One input at V_{CCP}-0.6V, Other inputs at V_{CCP};	1.08~3.6V		0.1	2	μA
C_I	Input pin capacitance	SCL, V_I=V_{CCI} or V_{SS}	1.08~3.6V		3		pF

PARAMETER		TEST CONDITION	V_{CCP}	MIN	TYP	MAX	UNIT
C_{IO}	Input-output pin capacitance	SDA, V_I=V_{CCI} or V_{SS}	1.08~3.6V		8		pF
		P port, V_I=V_{CCP} or V_{SS}	1.08~3.6V		6		pF

NOTE3: The total current sourced by all I/Os must be limited to 160mA.

NOTE4: Each I/O must be externally limited to a maximum of 25mA, and each octal (P00-P07, P10-P17 and P20-P27) must be limited to a maximum current of 100mA, for a device total of 200mA.

I²C Interface Timing Requirements

Parameters			Standard Mode		Fast Mode		Fast Mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	Interface clock frequency		0	100	-	400	-	1000	kHz
$t_{HD:STA}$	(Repeat-start) START condition hold time		4		0.6	-	0.26		μs
t_{LOW}	Low level width of SCL		4.7		1.3	-	0.5		μs
t_{HIGH}	High level width of SCL		4		0.6	-	0.26		μs
$t_{SU:STA}$	(Repeat-start) START condition setup time		4.7		0.6	-	0.26		μs
$t_{HD:DAT}$	Data hold time		0		0	-	0		μs
$t_{SU:DAT}$	Data setup time		0.25		0.1	-	0.05		μs
t_R	Rising time of SDA and SCL			1000	20	300	-	120	ns
t_F	Falling time of SDA and SCL			300	20× (V_{CCI}/5.5V)	300	20× (V_{CCI}/5.5V)	120	ns
$t_{SU:STO}$	STOP condition setup time		4		0.6	-	0.26		μs
t_{BUF}	Time between start and stop condition		4.7		1.3	-	0.5		μs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	0	50	0	50	ns
$t_{VD:DAT}$	Valid-data time	SCL low to SDA output valid		3.45		0.9		0.45	μs
$t_{VD:ACK}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		3.45		0.9		0.45	μs
C_b	Capacitive load for each bus line			400		400		550	pF

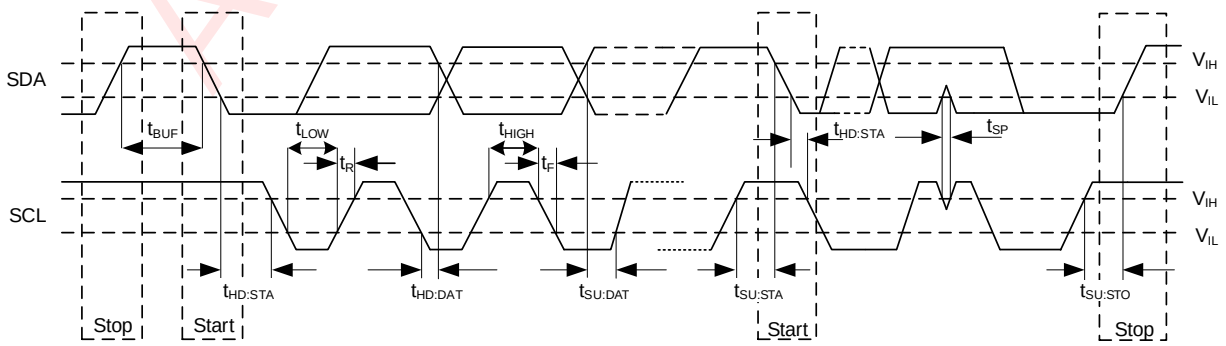


Figure 4 Definition of Timing on The I²C-bus

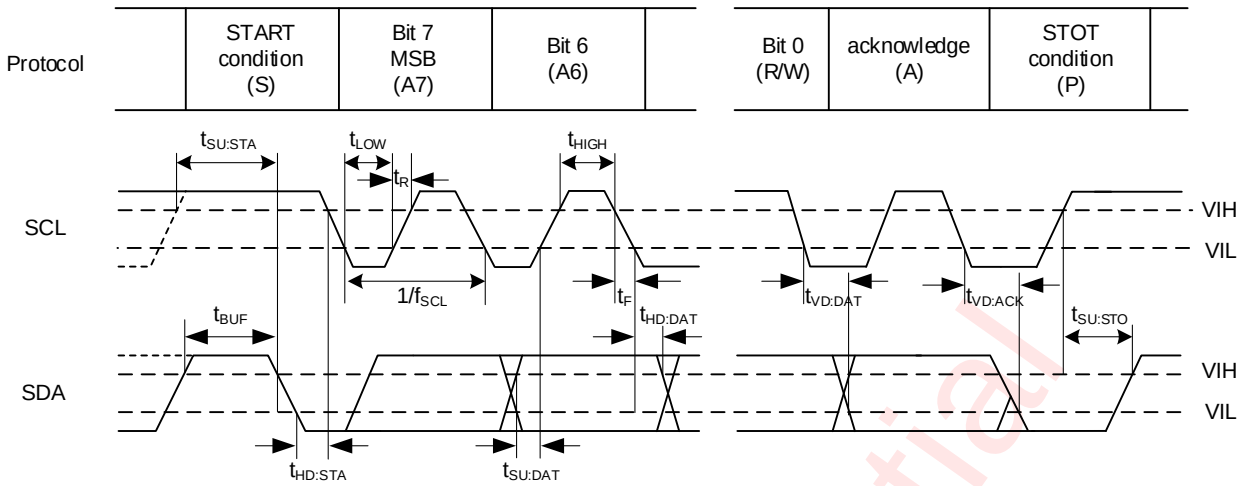


Figure 5 I²C-bus Timing Diagram

Timing Requirements

Over operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_w	Reset pulse width		80		ns
t_{REC}	Reset recovery time		80		ns
t_{RESET}	time to Reset		400		ns

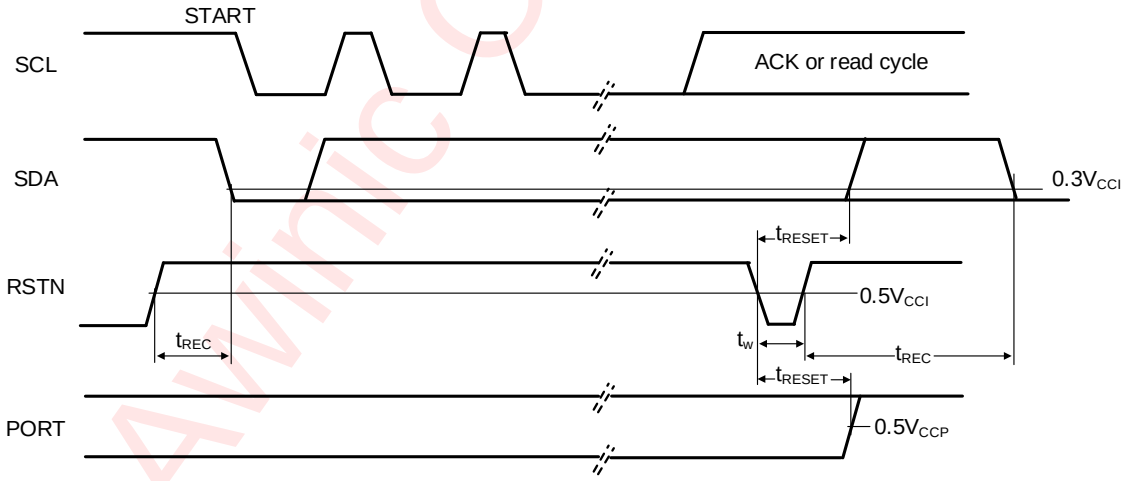


Figure 6 RSTN Timing Diagram

Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	From (Input)	To (Output)	Min.	Max.	Unit
t_{iv}	Interrupt valid time	P port	INTN		500	ns
t_{ir}	Interrupt reset delay time(no_latched)	SCL	INTN		1	μs
	Interrupt reset delay time(latched)				T_{SCL}(NOTE5)	s
t_{pv}	Output data valid time	SCL	P port		400	ns
t_{ps}	Input data setup time	P port	SCL	0		ns
t_{ph}	Input data hold time	P port	SCL	300		ns

NOTE5: T_{SCL} is the period of serial clock line (SCL).

Typical Characteristics

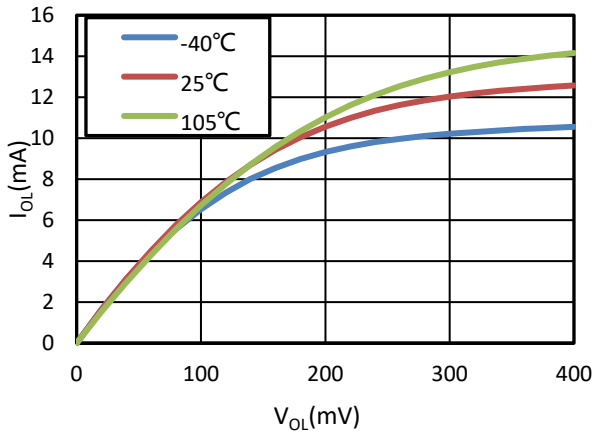


Figure 7 I/O Sink Current vs Output Low Voltage, V_{CCP}=1.08V

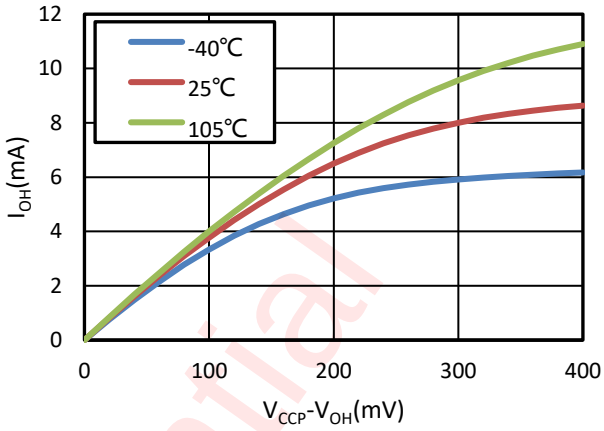


Figure 8 I/O Source Current vs Output High Voltage, V_{CCP}=1.08V

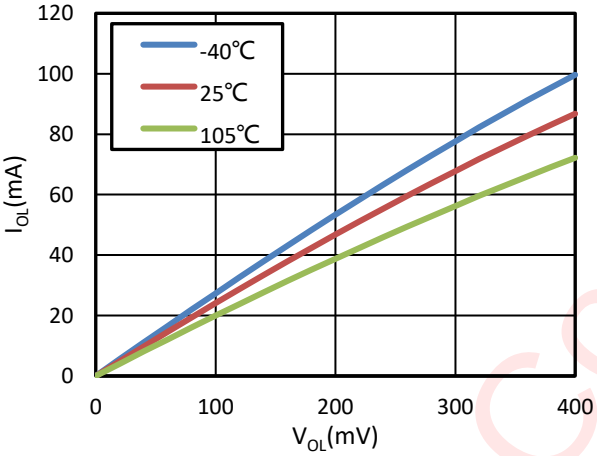


Figure 9 I/O Sink Current vs Output Low Voltage, V_{CCP}=2.3V

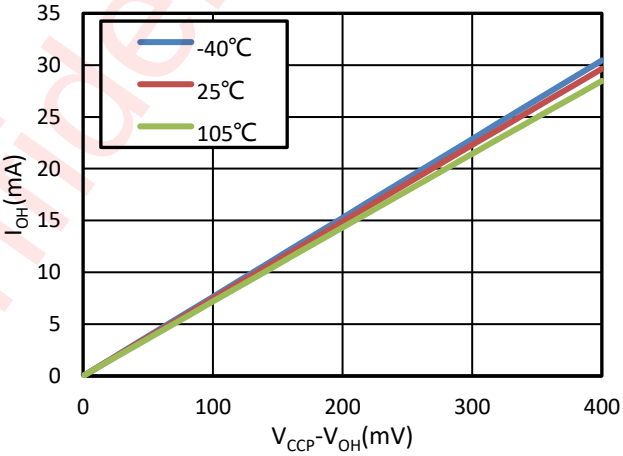


Figure 10 I/O Source Current vs Output High Voltage, V_{CCP}=2.3V

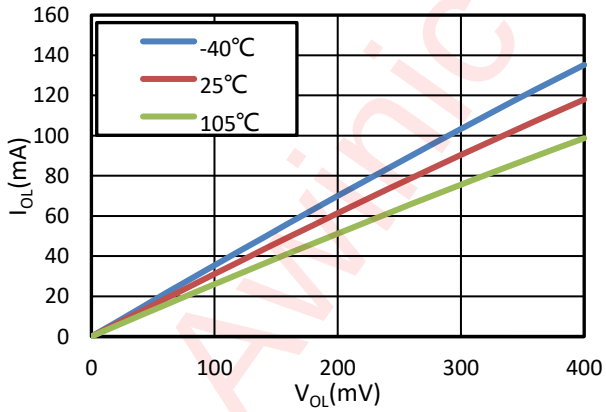


Figure 11 I/O Sink Current vs Output Low Voltage, V_{CCP}=3.6V

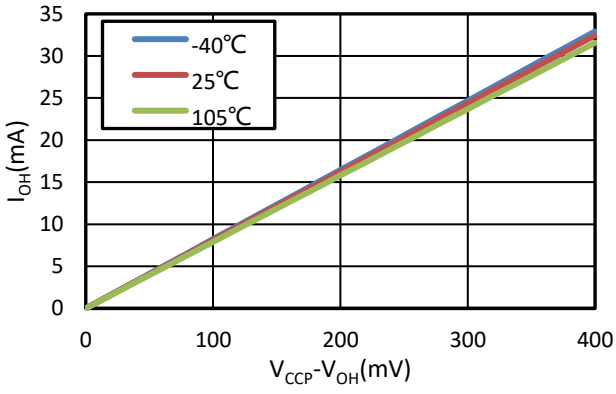


Figure 12 I/O Sink Current vs Output Low Voltage, V_{CCP}=3.6V

Detailed Functional Description

AW95124 is a 24-bit I/O expander that can be controlled through the I²C bus. Each I/O port can be configured as output or input independently. After power-on, all channels are configured as inputs.

The AW95124 supports voltage translation over a of a wide supply voltage range. This allows the device to interface with modern processors on the I²C side, where supply levels are lower to conserve power. In contrast to the dropping power supplies of processors, some PCB components such as LEDs still require a higher voltage power supply.

The V_{CCI} pin is the power supply for the I²C bus, and therefore the pull-up resistors connected to the SCL, SDA, ADDR, and RSTN pins should be terminated at V_{CCI}. The INTN output has an open-drain structure and requires an external pull-up resistor to V_{CCP} or V_{CCI} depending on the application. The V_{CCP} pin is the power supply for the P ports. The device P ports configured as outputs have the ability to sink up to 25mA for directly driving LEDs, but the current must be limited externally with an additional resistance.

The AW95124 digital core consists of 8-bit data registers which allow the user to configure the I/O port characteristics. At power on or after a reset, the I/Os are configured as inputs. However, the system controller can configure the I/Os as either inputs or outputs by writing to the Configuration registers. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller. Additionally, the AW95124 has Agile I/O functionality which is specifically targeted to enhance the I/O ports.

The Agile I/O features and registers include programmable output drive strength, programmable pull-up and pull-down resistors, latchable inputs, maskable interrupts, interrupt status register, and programmable open-drain or push-pull outputs. These configuration registers improve the I/O by increasing flexibility and allowing the user to optimize their design for power consumption, speed, and EMI.

The AW95124 has additional Agile I/O Plus features include I²C software reset. Interrupts can be specified by level or edge, and can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

Other features of the device include an interrupt that is generated on the INTN pin whenever an input port changes state. The device can be reset to its default state by applying a low logic level to the RSTN pin, issuing a software reset command, or by cycling power to the device and causing a power-on reset. The ADDR hardware selectable address pin allows four AW95124 devices to be connected to the same I²C bus.

Device Address

Following a START condition, the bus master must send the target slave address followed by a read (R/W=1) or write (R/W=0) operation bit. The slave address of the AW95124 is shown in Figure 13. One slave address pin ADDR can chooses four slave addresses by connecting the ADDR pin to SCL, SDA, V_{SS}, or V_{CCI}. The following table lists the four device addresses.

Table 1 Device address map

ADDR	Device family high-order address bits					Variable portion of address		R/ W	Address
	A6	A5	A4	A3	A2	A1	A0	R/W	
SCL	0	1	0	0	0	0	0	0/1	20h
SDA	0	1	0	0	0	0	1	0/1	21h
V_{SS}	0	1	0	0	0	1	0	0/1	22h
V_{CCI}	0	1	0	0	0	1	1	0/1	23h

The permitted I²C addresses are 0x20(7-bit) through 0x23(7-bit). The last bit of the first byte defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

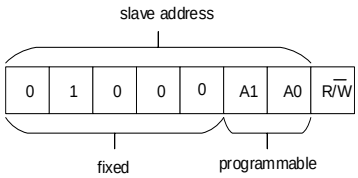


Figure 13 AW95124 Device Address

Software Reset Call

The Software Reset Call allows all the devices in the I²C to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.

2. The reserved General Call I²C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I²C-bus master.

3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.

4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it. If more than 1 byte of data is sent, the device does not acknowledge any more.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 14.

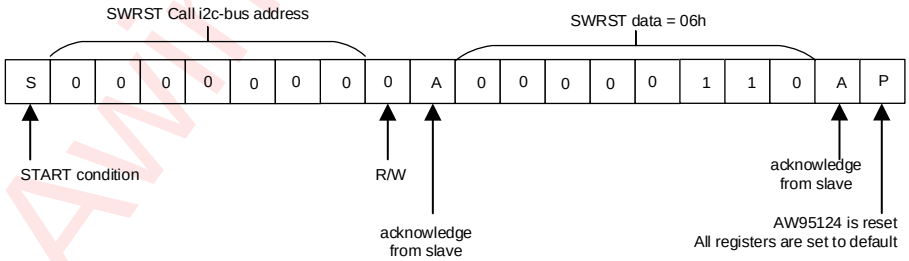


Figure 14 Software Reset

Power On Reset

When power (from 0V) is applied to V_{CCP}, an internal power-on reset circuit holds the AW95124 in a reset condition until V_{CCP} has reached V_{PORR}. At that time, the reset condition is released, and the AW95124 registers and I²C/SMBus state machine initialize to their default states. After that, V_{CCP} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

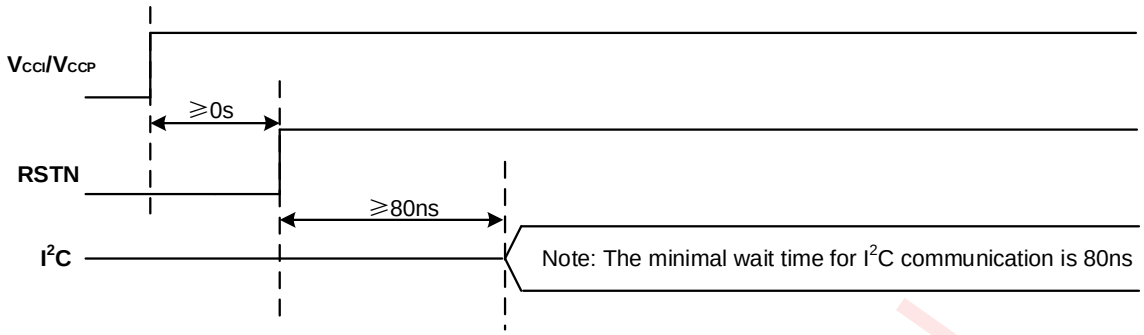


Figure 15 AW95124 Power On

Reset input(RSTN)

The RSTN input can be asserted to initialize the system while keeping the V_{CCP} at its operating level. A reset can be accomplished by holding the RSTN pin LOW for a minimum of tw. The AW95124 registers and I^2C/SMBus state machine are changed to their default state once RSTN is LOW (0). When RSTN is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to V_{CCI} if no active connection is used.

The function of RSTN input can be changed. When the last bit of F9h register is set to 0 (default value), once RSTN is LOW (0), both the registers and I^2C/SMBus state machine are changed to their default state; When the last bit of the F9h register is set to 1, once RSTN is LOW (0), only the I^2C/SMBus state machine will be restored to the default state, while the state of the registers remains unchanged.

Feature Description

I/O Port

When an I/O is configured as an input on AW95124, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage of AW95124 may be raised above V_{CCP} to a maximum of 3.6V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CCP} or V_{SS}. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation. Figure 16 shows the simplified schematic of I/Os.

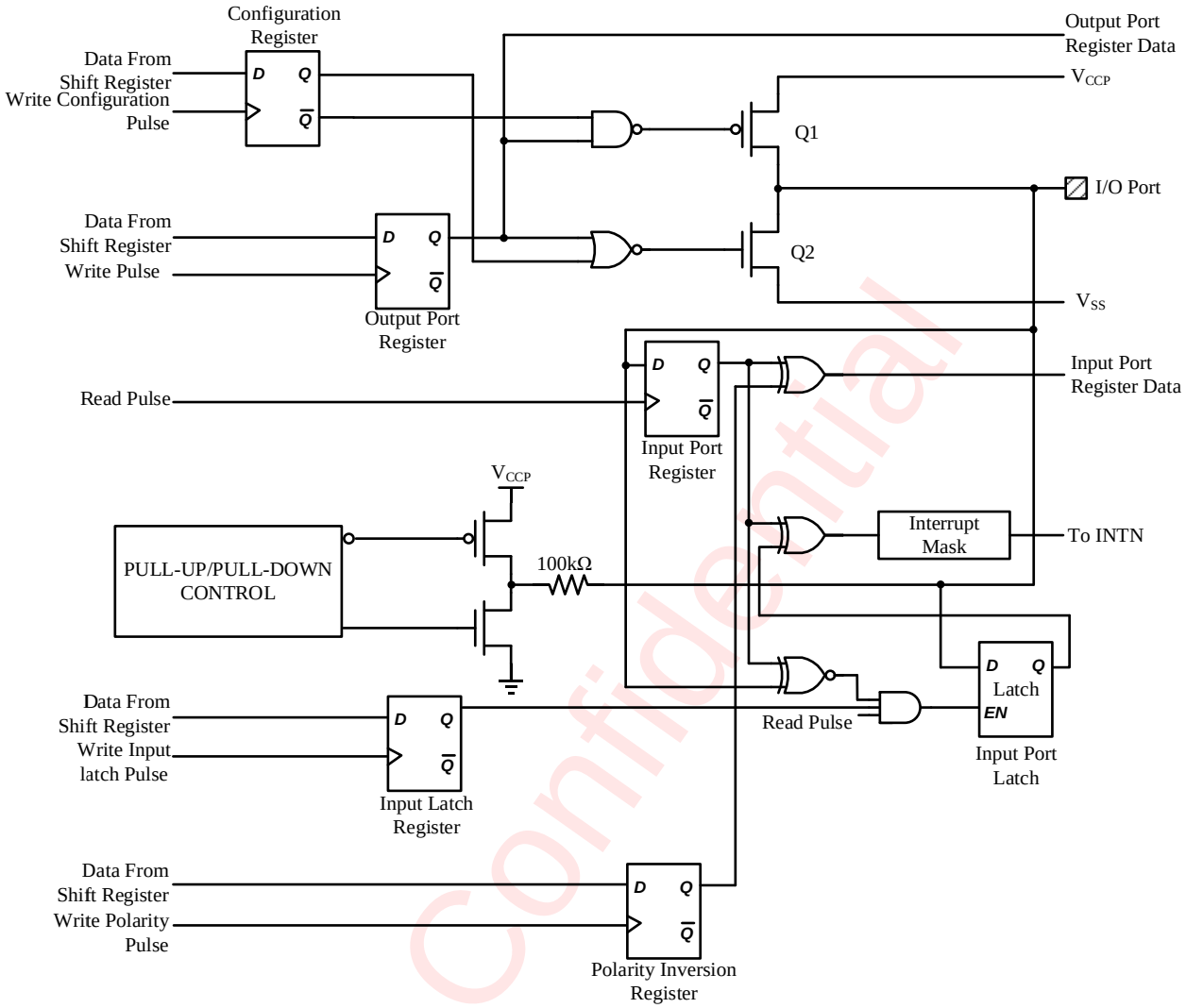


Figure 16 Simplified Schematic of I/Os

Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Figure 17 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the Output drive strength register. When the Output drive strength register bits are programmed to 01b, then only two of the fingers are active, reducing the current drive capability by 50%.

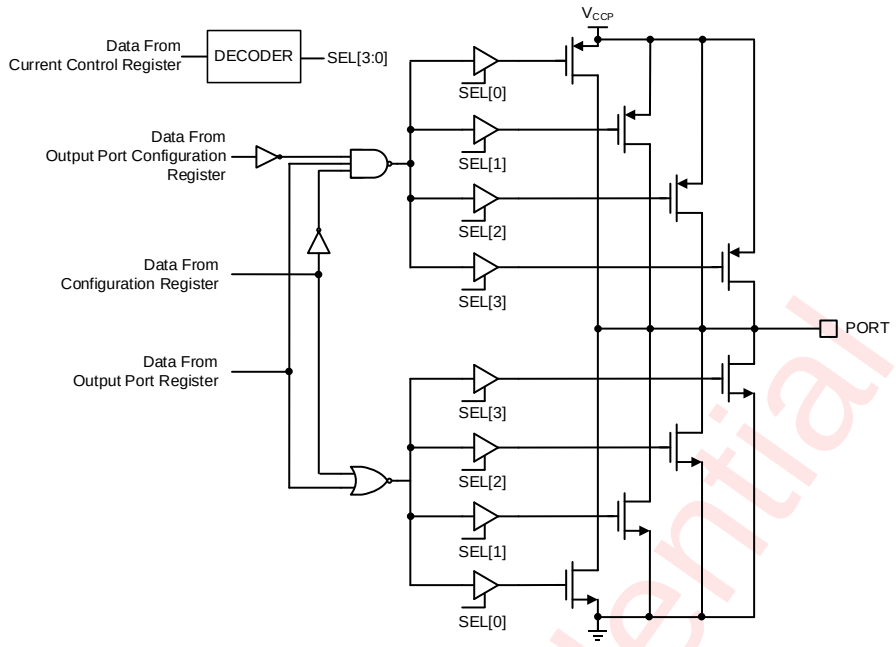


Figure 17 simplified output stage

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{CCP} and V_{SS} package inductance and will create noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

Interrupt Output

The INTN output has an open-drain structure and requires pull-up resistor to V_{CCP} or V_{CCI} depending on the application. When any current input port state differs from its corresponding input port register state, the INTN is asserted (logic 0) to indicate the system master (MCU) that one of input port states has changed. A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

In order to enable the interrupt output, the following three conditions must be satisfied:

• The GPIO must be configured as an input port by writing '1' to configuration port registers (0Ch, 0Dh, 0Eh)

• The interrupt mask registers (54h, 55h, 56h) must set to '0' to unmask interrupt sources.

• The interrupt edge registers (60h to 65h) select what action on each input pin will cause an interrupt; there are four different interrupt trigger modes: level trigger, rising-edge trigger, falling-edge trigger, or any edge trigger.

The input latch registers (48h, 49h, 4Ah) control each input pin either to enable latched input state or non-latched input state. When input pin is set to latch state, it will hold or latch the input pin state (keep the logic value) and generate an interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

Any interrupt status bit can be cleared and INTN pin de-asserted by using one of the following methods and conditions:

- Power on reset (POR), hardware reset from RSTN pin, or software reset call
- Read input port registers (00h, 01h, 02h)
- Write logic 1 to interrupt clear registers (68h, 69h, 6Ah)
- Write logic 1 to interrupt mask registers (54h, 55h, 56h)

- Write logic 0 to configuration registers (0Ch, 0Dh, 0Eh), set pin as output port.
- Input pin goes back to its initial state in level trigger and non-latch mode
- Input pin goes back to its initial state in level trigger and change latch to non-latch mode
- Change the interrupt trigger mode from level trigger to edge trigger or vice versa in interrupt edge registers

When using the input latch feature, the input pin state is latched. The interrupt is de-asserted only when data is read from the port that generated the interrupt. When the latch is disabled, an interrupt reset occurs in read mode with the SCL signal rising edge after the acknowledge (ACK) bit or not acknowledge (NACK) bit, and when the latch is enabled, an interrupt reset occurs in read mode with the next SCL signal rising edge after the acknowledge (ACK) bit or not acknowledge (NACK) bit . Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the inputs after resetting is detected and is transmitted as INTN.

Switch debounce circuitry

The AW95124 implements hardware to ease the hardware interface by debouncing switch closures with dedicated circuitry. P01 to P07, P10 to P17 can connect to this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods. The output does not change until the input is stable for a programmable duration. The circuit block diagram (Figure 18) shows the functional blocks consisting of an external oscillator, counter, edge detector, and D flip-flop. When the switch input state changes, the edge detector will reset the counter. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output.

To use the debounce circuitry, set the port pins (P01 to P07, and P10 to P17) with switches attached in the Switch Debounce Enable 0 and 1 registers (74h, 75h). Connect an external oscillator signal on P00, which serves as a time base to the debounce timer. Finally, set a delay time in the Switch Debounce Count register (76h). The combination of time base of the external oscillator and the debounce count sets the qualification debounce period. Note that all debounce counters will use the same time base and count, but they all function independently. The first time external clock is connected, external clock is required to wait 9 clock cycles for the debounce circuit in normal operation.

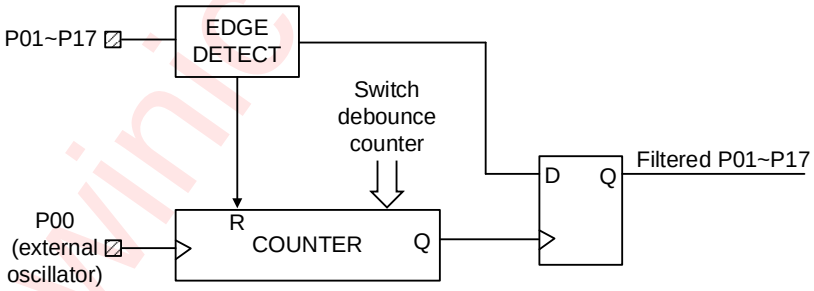


Figure 18 Switch debounce circuitry

Each channel of P00~P27 has an independent analog filter that can filter out glitch signals below 20ns. The filter is turned off by default, and the filter of the port can be enabled by configuring the last bit of the filter configuration register (F7h) to be 1.

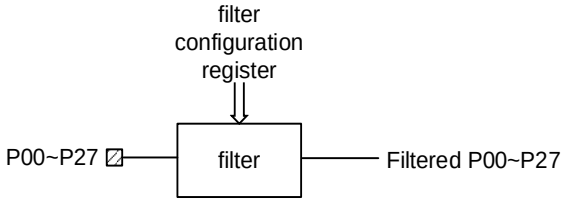


Figure 19 P port analog filter circuitry

Writing To The Port Registers

Data is transmitted to the AW95124 by sending the device address and setting the least significant bit to a logic 0. The command byte is sent after the address and determines which register will receive the data following the command byte.

Many registers in AW95124 are configured to operate as register triples. These groups include input port, output port, polarity inversion and configuration registers, as well as input latch, pull-up/pull-down enable and selection registers, interrupt mask and interrupt state, interrupt clear and input status (ports) without interrupt clear registers (states), Individual pin output configuration registers, and switch debounce enable registers. After sending data to one register, the next data byte will be sent to the other register in the pair. For example, if the first byte is sent to Output Port 2 (06h), then the next byte will be stored in Output Port 0 (04h). The next byte sent is stored in Output Port 1 (05h). Since every new write access after a STOP condition requires a Command byte, which sets the Pointer register, the next new write access will be to an arbitrary register.

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register group independently of the other registers or the host can simply update a single register.

There are two 6-register groups: Output drive strength (40h to 45h) and interrupt edge (60h to 65h) registers which can be programmed continuously in this group.

There is two registers that is not part of a register group: Output port configuration (5Ch) and switch debounce count (76h). When this register is accessed multiple times, the register address remains fixed on the same address.

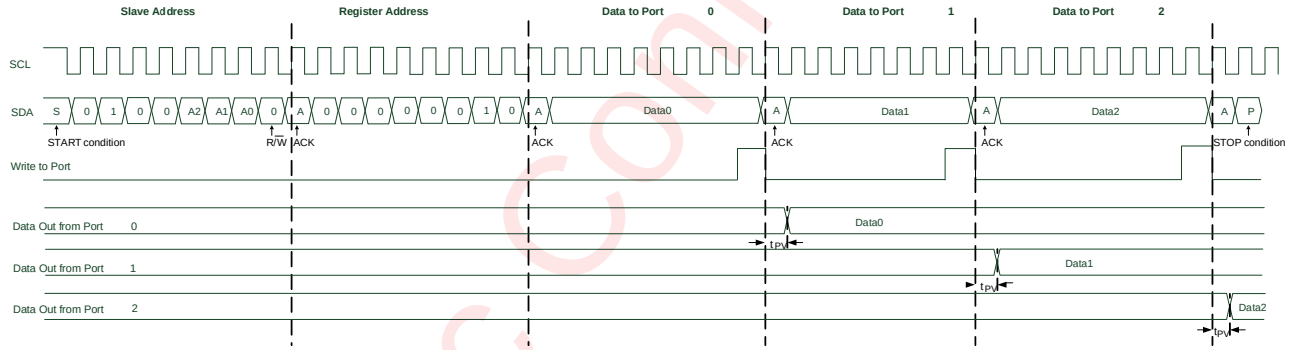
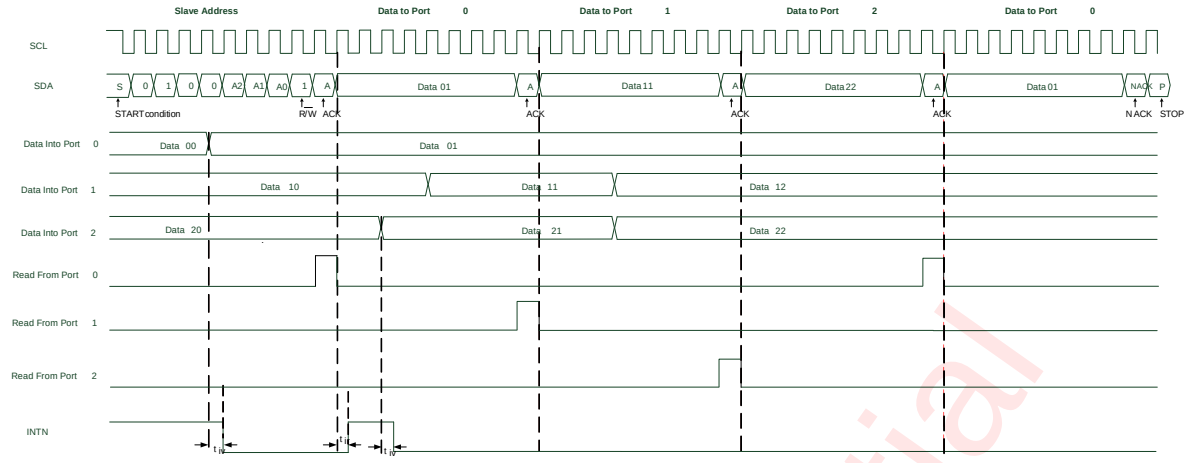


Figure 20 Write to Output Port Registers

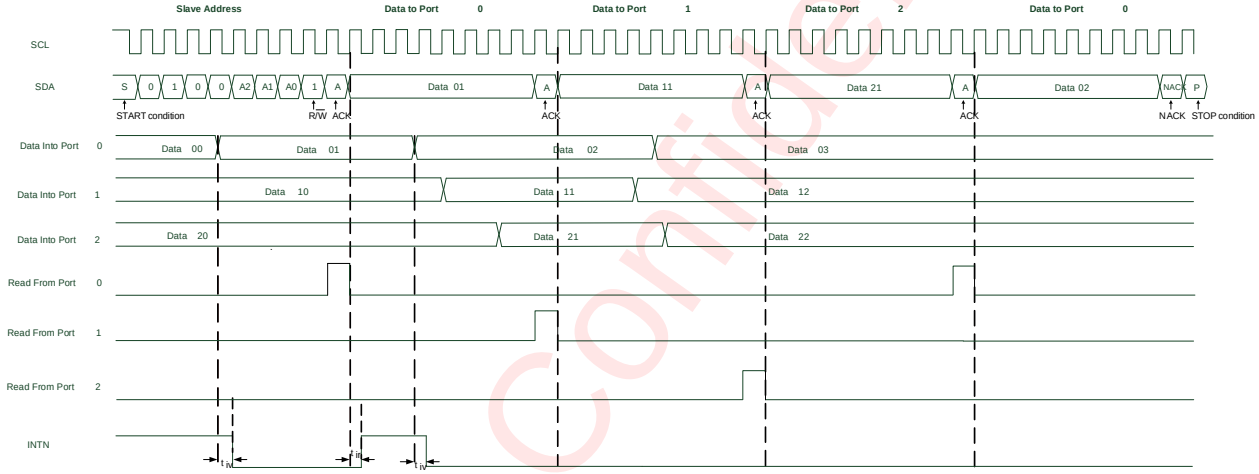
Reading The Port Registers

Reading from a slave is very similar to writing, but requires some additional steps. In order to read data from the AW95124, the bus master must first send the AW95124 address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the AW95124 (Figure 21 and Figure 22). Data is clocked into the register on the rising edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 2 (02h), then the next byte read would be Input Port 0 (00h). The next byte read would be Input Port 1 (01h).There is no limitation on the number of data bytes received in one read transmission, but the final byte received, the bus master must not acknowledge the data.



- Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
- This figure eliminates the command byte transfer from the P port, a restart, and slave address call between the initial slave address call and actual data transfer

Figure 21 Read Input Port Register(no_latched), Scenario 1



- Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
- This figure eliminates the command byte transfer from the P port, a restart, and slave address call between the initial slave address call and actual data transfer

Figure 22 Read Input Port Register(latched), Scenario 2

General I²C Operation

AW95124 supports the serial I²C-bus and data transmission protocol in fast mode plus at 1000kHz. It operates as a slave on the I²C bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. The size of the pull-up resistor is determined by the amount of capacitance on the I²C lines. The I²C interface supports 1.2V pull-up voltage values. Additionally, the I²C device supports continuous read and write operations. The I²C register address is 8-bit and register data is 8-bit, and the data transmission is in big-endian mode. Data transfer may be initiated only when the bus is not busy.

Data Validation

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

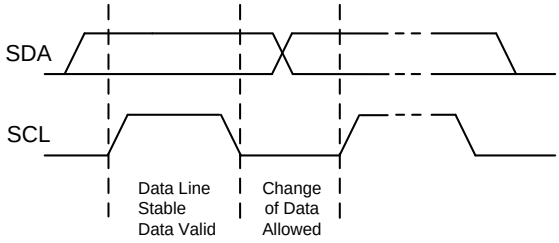


Figure 23 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

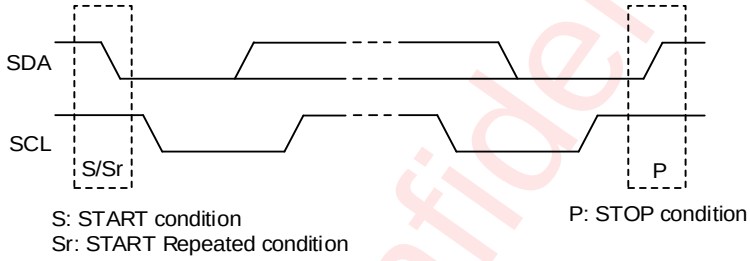


Figure 24 I²C Start/Stop Condition Timing

Acknowledge(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to V_{SS} by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

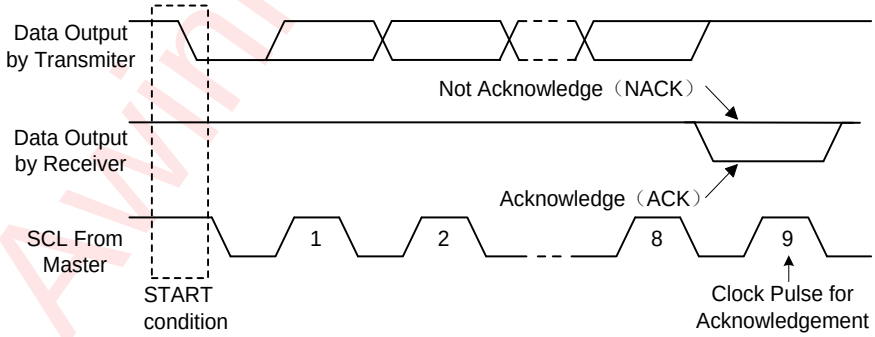


Figure 25 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The “START” signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit (R/W=0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends command byte(8-bit).
e) Slave sends acknowledge signal.
f) Master sends data byte to be written to the addressed register.
g) Slave sends acknowledge signal.
h) Master generates STOP condition to indicate write cycle end.

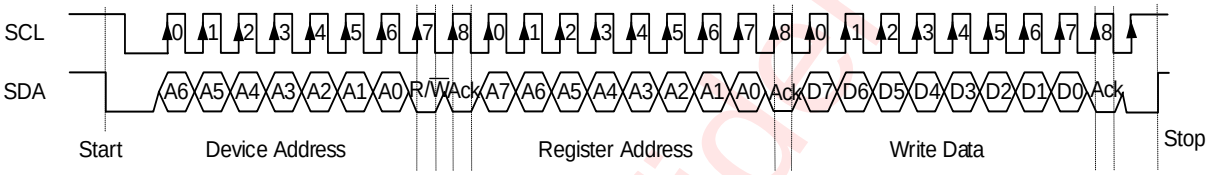


Figure 26 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition.
b) Master device sends slave address (7-bit) and the data direction bit (R/W=0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends command byte(8-bit).
e) Slave sends acknowledge signal.
f) Master generates STOP condition followed with START condition or REPEAT START condition.
g) Master device sends slave address (7-bit) and the data direction bit (R/W=1).
h) Slave device sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) If the master device generates STOP condition, the read cycle is ended.

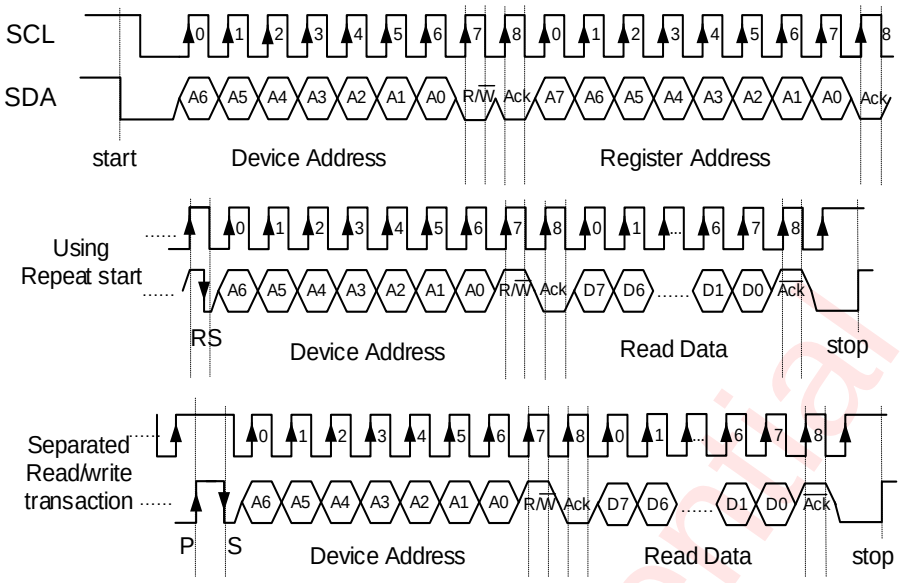


Figure 27 I²C Read Byte Cycle

Register Configuration

Following the successful acknowledgement of the slave address byte, the bus master sends a command byte, which is write only and stored in the pointer register in the AW95124. The lowest 7 bits are used as a pointer to determine which register is accessed and the highest bit is used as Auto-Increment (AI) as shown in Figure 28. At power-up, hardware or software reset, the pointer register defaults to 00h, with the AI bit set to '0' and the lowest seven bits set to '000 0000'.

When the Auto-Increment bit is set (AI=1), the seven low-order bits of the pointer register are automatically incremented after a read or write until a STOP condition is encountered. This allows the user to program the registers sequentially without modifying the pointer register. The contents of these bits will roll over to '000 0000' after the last register (76h) is accessed. Unimplemented register addresses (reserved registers) and global config registers (F7h, F8h or F9h) are skipped. If more than 52 bytes are written, the address will loop back to the register which is indicated by the seven low-order bits in the pointer register, and previously-written data will be overwritten. A STOP condition will keep the pointer register value in the last read or write location.

When the Auto-Increment bit is cleared (AI=0), the 2 least significant bits are automatically incremented after a read or write for 3-register group which allows the user to program each of the 3-register group sequentially. If more than 3 bytes of data are read or written when AI is 0, previous data in the selected registers will be overwritten. For example: if input port 1 is read first, the next 2nd byte will be input port 2, and next 3nd byte will be input port 0, there is no limit on the number of data bytes for this read operation. There are some special groups: output drive strength (40h~45h) and interrupt edge (60h~65h) registers will allow user to program each of the 6-register group sequentially. Switch debounce enable (74h~75h) registers will allow user to program each of the 2-register group sequentially. Output port configuration register (5Ch) and Switch debounce count register (76h) remains in the same location after a successive read or write.

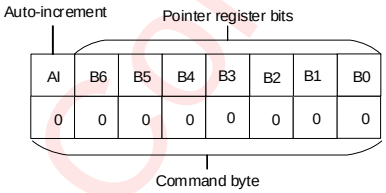


Figure 28 I²C Read Byte Cycle

Pointer register bits	R/W	NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
00h	R	P0DI	P0_DI								xxh
01h	R	P1DI	P1_DI								xxh
02h	R	P2DI	P2_DI								xxh
04h	W/R	P0DO	P0_DO								FFh
05h	W/R	P1DO	P1_DO								FFh
06h	W/R	P2DO	P2_DO								FFh
08h	W/R	P0INV	P0_INV								00h
09h	W/R	P1INV	P1_INV								00h
0Ah	W/R	P2INV	P2_INV								00h
0Ch	W/R	P0OEN	P0_OEN								FFh
0Dh	W/R	P1OEN	P1_OEN								FFh
0Eh	W/R	P2OEN	P2_OEN								FFh
40h	W/R	P0DSR1	P0_DSR1								FFh

Pointer register bits	R/W	NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
41h	W/R	P0DSR2	P0_DSR2								FFh
42h	W/R	P1DSR1	P1_DSR1								FFh
43h	W/R	P1DSR2	P1_DSR2								FFh
44h	W/R	P2DSR1	P2_DSR1								FFh
45h	W/R	P2DSR2	P2_DSR2								FFh
48h	W/R	P0LE	P0_LE								00h
49h	W/R	P1LE	P1_LE								00h
4Ah	W/R	P2LE	P2_LE								00h
4Ch	W/R	P0PE	P0_PE								00h
4Dh	W/R	P1PE	P1_PE								00h
4Eh	W/R	P2PE	P2_PE								00h
50h	W/R	P0PMD	P0_PMD								FFh
51h	W/R	P1PMD	P1_PMD								FFh
52h	W/R	P2PMD	P2_PMD								FFh
54h	W/R	P0MSK	P0_MSK								FFh
55h	W/R	P1MSK	P1_MSK								FFh
56h	W/R	P2MSK	P2_MSK								FFh
58h	R	P0INST	P0_INST								00h
59h	R	P1INST	P1_INST								00h
5Ah	R	P2INST	P2_INST								00h
5Ch	W/R	OPC						ODEN2	ODEN1	ODEN0	00h
60h	W/R	P0EDGE1	P0_EDGE1								00h
61h	W/R	P0EDGE2	P0_EDGE2								00h
62h	W/R	P1EDGE1	P1_EDGE1								00h
63h	W/R	P1EDGE2	P1_EDGE2								00h
64h	W/R	P2EDGE1	P2_EDGE1								00h
65h	W/R	P2EDGE2	P2_EDGE2								00h
68h	W	P0INTCLR	P0_INTCLR								00h
69h	W	P1INTCLR	P1_INTCLR								00h
6Ah	W	P2INTCLR	P2_INTCLR								00h
6Ch	R	P0DIST	P0_DIST								xxh
6Dh	R	P1DIST	P1_DIST								xxh
6Eh	R	P2DIST	P2_DIST								xxh
70h	W/R	P0DOMD	P0_DOMD								00h
71h	W/R	P1DOMD	P1_DOMD								00h
72h	W/R	P2DOMD	P2_DOMD								00h
74h	W/R	P0DEBEN	P0_DEBEN								00h
75h	W/R	P1DEBEN	P1_DEBEN								00h

Pointer register bits	R/W	NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
76h	W/R	DEBCNT	DEBCNT_CODE								00h

ADDR	R/W	NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
F7h	W/R	PDEG_EN	-					INT_DEG_SET		DIN_DEG_SET	00h
F8h	W/R	SOFT_RSTN	SOFT_RSTN_EN								01h
F9h	W/R	I2C_RSTEN								IIC_RST_EN	00h
FBh	R	CHIPID						CHIPID			0Xh

Register Detailed Description

P0DI/P1DI/P2DI: Input Port Registers (Address 00h/01h/02h)

Bit	Register	R/W	Description	Default
7:0	P0_DI	R	P07~P00 input state 0: low level 1: high level	xxh
7:0	P1_DI	R	P17~P10 input state 0: low level 1: high level	xxh
7:0	P2_DI	R	P27~P20 input state 0: low level 1: high level	xxh

The Input Port registers reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, x, is determined by the externally applied logic level.

If a pin is configured as an output (04h, 05h, 06h), the port value is equal to the actual voltage level on that pin. If the output is configured as open-drain (5Ch, 70h, 71h, 72h), the input port value is forced to 0. After reading input port registers, all interrupts will be cleared.

P0DO/P1DO/P2DO: Output Port Registers (Address 04h/05h/06h)

Bit	Register	R/W	Description	Default
7:0	P0_DO	W/R	P07~P00 output state 0: low level 1: high level	FFh
7:0	P1_DO	W/R	P17~P10 output state 0: low level 1: high level	FFh

7:0	P2_DO	W/R	P27~P20 output state 0: low level 1: high level	FFh

The Output Port registers show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value.

P0INV/P1INV/P2INV: Polarity Inversion Enable Registers (Address 08h/09h/0Ah)

Bit	Register	R/W	Description	Default
7:0	P0_INV	W/R	P07~P00 input state invert enable 0: disable 1: enable	00h
7:0	P1_INV	W/R	P17~P10 input state invert enable 0: disable 1: enable	00h
7:0	P2_INV	W/R	P27~P20 input state invert enable 0: disable 1: enable	00h

The Polarity Inversion registers allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in these registers is cleared (written with a 0), the corresponding port pin's original polarity is retained.

P0OEN/P1OEN/P2OEN: Configuration Registers (Address 0Ch/0Dh/0Eh)

Bit	Register	R/W	Description	Default
7:0	P0_OEN	W/R	P07~P00 input/output direction 0:output 1:input	FFh
7:0	P1_OEN	W/R	P17~P10 input/output direction 0:output 1:input	FFh
7:0	P2_OEN	W/R	P27~P20 input/output direction 0:output 1:input	FFh

The Configuration registers configure the directions of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is set to 0, the corresponding port pin is enabled as an output.

P0DSR1/P0DSR2: Port 07~00 Output drive strength registers (Address 40h~41h)

Bit	Register	R/W	Description	Default
7:6	P0_DSR1	W/R	P03 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh

5:4	P0_DSR1	W/R	P02 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
3:2	P0_DSR1	W/R	P01 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
1:0	P0_DSR1	W/R	P00 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
7:6	P0_DSR2	W/R	P07 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
5:4	P0_DSR2	W/R	P06 GPIO output drive strength of the I/O. 00 : 0.25x, 01 : 0.5x, 10 : 0.75x, 11 : 1x	FFh
3:2	P0_DSR2	W/R	P05 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
1:0	P0_DSR2	W/R	P04 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh

P1DSR1/P1DSR2: Port 17~10 Output drive strength registers (Address 42h~43h)

Bit	Register	R/W	Description	Default
7:6	P1_DSR1	W/R	P13 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
5:4	P1_DSR1	W/R	P12 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh

3:2	P1_DSR1	W/R	P11 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
1:0	P1_DSR1	W/R	P10 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
7:6	P1_DSR2	W/R	P17 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
5:4	P1_DSR2	W/R	P16 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
3:2	P1_DSR2	W/R	P15 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
1:0	P1_DSR2	W/R	P14 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh

P2DSR1/P2DSR2: Port 27~20 Output drive strength registers (Address 44h~45h)

Bit	Register	R/W	Description	Default
7:6	P2_DSR1	W/R	P23 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
5:4	P2_DSR1	W/R	P22 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
3:2	P2_DSR1	W/R	P21 GPIO output drive strength of the I/O 00 : 0.25x	FFh

			01 : 0.5x 10 : 0.75x 11 : 1x	
1:0	P2_DSR1	W/R	P20 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
7:6	P2_DSR2	W/R	P27 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
5:4	P2_DSR2	W/R	P26 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
3:2	P2_DSR2	W/R	P25 GPIO output drive strength of the I/O 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh
1:0	P2_DSR2	W/R	P24 GPIO output drive strength of the I/O. 00 : 0.25x 01 : 0.5x 10 : 0.75x 11 : 1x	FFh

P0LE/P1LEP2LE: Input latch registers (Address 48h/49h/4Ah)

Bit	Register	R/W	Description	Default
7:0	P0_LE	W/R	P07~P00 input state latch enable 0: disable 1: enable	00h
7:0	P1_LE	W/R	P17~P10 input state latch enable 0: disable 1: enable	00h
7:0	P2_LE	W/R	P27~P20 input state latch enable 0: disable 1: enable	00h

The input latch registers (48h, 49h, 4Ah) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (00h, 01h, 02h). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt.

For example, if the P04 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read '1'. The next read of the input port register bit 4 should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is cleared if the input latch register changes from latched to non-latched configuration and I/O pin returns to its original state.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level.

P0PE/P1PE/P2PE: Pull Up/Down Enable Register (Address 4Ch/4Dh/4Eh)

Bit	Register	R/W	Description	Default
7:0	P0_PE	W/R	P07~P00 pull up /down resistors enable 0: disable 1: enable	00h
7:0	P1_PE	W/R	P17~P10 pull up /down resistors enable 0: disable 1: enable	00h
7:0	P2_PE	W/R	P27~P20 pull up/down resistors enable 0: disable 1: enable	00h

The pull-up and pull-down enable registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs.

P0PMD/P1PMD/P2PMD: Pull Up/Down selection registers (Address 50h/51h/52h)

Bit	Register	R/W	Description	Default
7:0	P0_PMD	W/R	P07~P00 pull up/down selection registers 0: pull down 1: pull up	FFh
7:0	P1_PMD	W/R	P17~P10 pull up/down selection registers 0: pull down 1: pull up	FFh
7:0	P2_PMD	W/R	P27~P20 pull up/down selection registers 0: pull down 1: pull up	FFh

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin.

P0MSK/P1MSK/P2MSK: Interrupt mask register (Address 54h/55h/56h)

Bit	Register	R/W	Description	Default
7:0	P0_MSK	W/R	P07~P00 interrupt mask 0: disable 1: enable	FFh
7:0	P1_MSK	W/R	P17~P10 interrupt mask 0: disable 1: enable	FFh
7:0	P2_MSK	W/R	P27~P20 interrupt mask 0: disable 1: enable	FFh

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted. When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted.

P0INST/P1INST/P2INST: Interrupt state register (Address 58h/59h/5Ah)

Bit	Register	R/W	Description	Default
7:0	P0_INST	R	P07~P00 interrupt state 0: no interrupt occurred 1: interrupt occurred	00h
7:0	P1_INST	R	P17~P10 interrupt state 0: no interrupt occurred 1: interrupt occurred	00h
7:0	P2_INST	R	P27~P20 interrupt state 0: no interrupt occurred 1: interrupt occurred	00h

The read-only interrupt status registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt. When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0.

OPC: Output port configuration register (Address 5Ch)

Bit	Register	R/W	Description	Default
7:3	Reserved	RW	Not used	
2	ODEN2	W/R	P27~P20 output mode 0: push-pull 1: open-drain	0

1	ODEN1	W/R	P17~P10 output mode 0: push-pull 1: open-drain	0
0	ODEN0	W/R	P07~p00 output mode 0: push-pull 1: open-drain	0

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull . A logic 1 configures the I/O as open-drain and the recommended command sequence is to program this register (5Ch) before the Configuration register (0Ch, 0Dh, 0Eh) sets the port pins as outputs. ODEN0 configures Port 0, ODEN1 configures Port 1, and ODEN2 configures Port 2. Individual pins may be programmed as open-drain or push-pull by programming Individual Pin Output Configuration registers (70h, 71h, 72h).

P0EDGE1/P0EDGE2: Port 07~00 Interrupt edge registers (Address 60h~61h)

Bit	Register	R/W	Description	Default
7:6	P0_EDGE1	W/R	P03 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
5:4	P0_EDGE1	W/R	P02 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
3:2	P0_EDGE1	W/R	P01 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
1:0	P0_EDGE1	W/R	P00 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
7:6	P0_EDGE2	W/R	P07 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
5:4	P0_EDGE2	W/R	P06 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
3:2	P0_EDGE2	W/R	P05 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered	00h

			11: any edge triggered	
1:0	P0_EDGE2	W/R	P04 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h

P1EDGE1/P1EDGE2: Port 17~10 Interrupt edge registers (Address 62h~63h)

Bit	Register	R/W	Description	Default
7:6	P1_EDGE1	W/R	P13 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
5:4	P1_EDGE1	W/R	P12 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
3:2	P1_EDGE1	W/R	P11 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
1:0	P1_EDGE1	W/R	P10 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
7:6	P1_EDGE2	W/R	P17 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
5:4	P1_EDGE2	W/R	P16 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
3:2	P1_EDGE2	W/R	P15 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
1:0	P1_EDGE2	W/R	P14 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered	00h

			10: negative-going edge triggered 11: any edge triggered	

P2EDGE1/P2EDGE2: Port 27~20 Interrupt edge registers (Address 64h~65h)

Bit	Register	R/W	Description	Default
7:6	P2_EDGE1	W/R	P23 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
5:4	P2_EDGE1	W/R	P22 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
3:2	P2_EDGE1	W/R	P21 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered210: negative-going edge triggered 11: any edge triggered	00h
1:0	P2_EDGE1	W/R	P20 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
7:6	P2_EDGE2	W/R	P27 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
5:4	P2_EDGE2	W/R	P26 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
3:2	P2_EDGE2	W/R	P25 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h
1:0	P2_EDGE2	W/R	P24 interrupt triggering mode 00: level-triggered 01: postive-going edge triggered 10: negative-going edge triggered 11: any edge triggered	00h

The interrupt edge registers determine what action on an input pin will cause an interrupt along with the

Interrupt Mask registers (54h, 55h and 56h). If the Interrupt is enabled (set '0' in the Mask register) and the action at the corresponding pin matches the required activity, the INTN output will become active. The default value for each pin is 00b or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH-to-LOW or LOW-to-HIGH), since the last read of the Input port (00h, 01h, 02h) which can be latched with a corresponding '1' set in the Input Latch register (48h, 49h, 4Ah). If the Interrupt edge register entry is set to 11b, any edge, positive-going or negative-going, causes an interrupt event. If an entry is 01b, only a positive-going edge will cause an interrupt event, while a 10b will require a negative-going edge to cause an interrupt event.

P0INTCLR/P1INTCLR/P2INTCLR: Interrupt clear registers (Address 68h/69h/6Ah)

Bit	Register	R/W	Description	Default
7:0	P0_INTCLR	W	P07~P00 Clear individual interrupt 0: not clear 1: clear	00h
7:0	P1_INTCLR	W	P17~P10 Clear individual interrupt 0: not clear 1: clear	00h
7:0	P2_INTCLR	W	P27~P20 Clear individual interrupt 0: not clear 1: clear	00h

The write-only interrupt clear registers clear individual interrupt sources (status bit). Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the INTN will be cleared. After writing a logic 1 the bit returns to logic 0.

P0DIST/P1DIST/P2DIST: Input status registers (Address 6Ch/6Dh/6Eh)

Bit	Register	R/W	Description	Default
7:0	P0_DIST	R	P07~P00 actual input state 0: low level 1: high level	00h
7:0	P1_DIST	R	P17~P10 actual input state, 0: low level 1: high level	00h
7:0	P2_DIST	R	P27~P20 actual input state 0: low level 1: high level	00h

The read-only input status registers function exactly like Input Port 0, 1 and 2 (00h, 01h, 02h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. If the pin is configured as an input, the port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. If a pin is configured as an output by the Configuration register (0Ch, 0Dh, 0Eh), and is also configured as open-drain (5Ch, 70h, 71h, 72h), the read for that pin will always return 0, otherwise that state of that pin is returned.

P0DOMD/P1DOMD/P2DOMD: Individual pin output configuration registers (Address 70h/71h/72h)

Bit	Register	R/W	Description	Default
7:0	P0_DOMD	W/R	P07~P00 individual output configuration 0: keep the ODEN0 configuration	00h

			1: reverse the ODEN0 configuration	
7:0	P1_DOMD	W/R	P17~P10 individual output configuration 0: keep the ODEN1 configuration 1: reverse the ODEN1 configuration	00h
7:0	P2_DOMD	W/R	P27~P20 individual output configuration 0: keep the ODEN2 configuration 1: reverse the ODEN2 configuration	00h

The individual pin output configuration registers modify output configuration (push-pull or open-drain) set by the Output Port Configuration register (5Ch). If the ODENx bit is set at logic 0 (push-pull), any bit set to logic 1 in the DOMDx register will reverse the output state of that pin only to open-drain. When ODENx bit is set at logic 1 (open-drain), a logic 1 in DOMDx will set that pin to push-pull.

The recommended command sequence to program the output pin is to program ODENx (5Ch), the DOMDx, and finally the Configuration register (0Ch, 0Dh, 0Eh) to set the pins as outputs.

P0DEBEN/P1DEBEN: Switch decounce enable registers (Address 74h/75h)

Bit	Register	R/W	Description	Default
7:0	P0_DEBEN	W/R	P07~P00 switch debounce function 0: disable 1: enable	00h
7:0	P1_DEBEN	W/R	P17~P00 switch debounce function 0: disable 1: enable	00h

The switch debounce enable registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the Switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P00 is designated as the oscillator input. If P00 is not configured as input and if P0DEBEN.0 is not set to logic 1, then switch debounce logic is not connected to any pin.

DEBCNT: Switch debounce count register (Address 76h)

Bit	Register	R/W	Description	Default
7:0	DEBCNT_CODE	W/R	switch debounce count	00h

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 or Port 1 pins finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P00, determines the debounce time (for example, the debounce time will be 5us if this register is set to 05h and external oscillator frequency is 1 MHz).

PDEG_EN: filter configuration register (Address F7h)

Bit	Register	R/W	Description	Default
7:3	Reserved	W/R	Not used	0
2:1	INT_DEG_SET	W/R	INTN internal analog filter deglitch time 00: 0ns 01: 60ns 10: 120ns 11: 180ns	0

0	DIN_DEG_EN	W/R	P27~P00 input analog filter（20ns deglicth） 0:disable 1:enable	0

SOFT_RSTN: Soft Reset register (Address F8h)

Bit	Register	R/W	Description	Default
7:0	SOFT_RSTN_EN	W/R	write 16h to this register will reset all registers and I²C/SMBus state machine	0

I2C_RSTEN: RSTN Configuration register (Address F9h)

Bit	Register	R/W	Description	Default
7:1	Reserved	W/R	Not used	0
0	IIC_RST_EN	W/R	configure the function of the hardware reset pin RSTN 0: when RSTN Pin is LOW(0), both the registers and I²C/SMBus state machine will be reset 1: when RSTN Pin is LOW(0), only the I²C/SMBus state machine will be reset, while the state of the registers remains unchanged	0

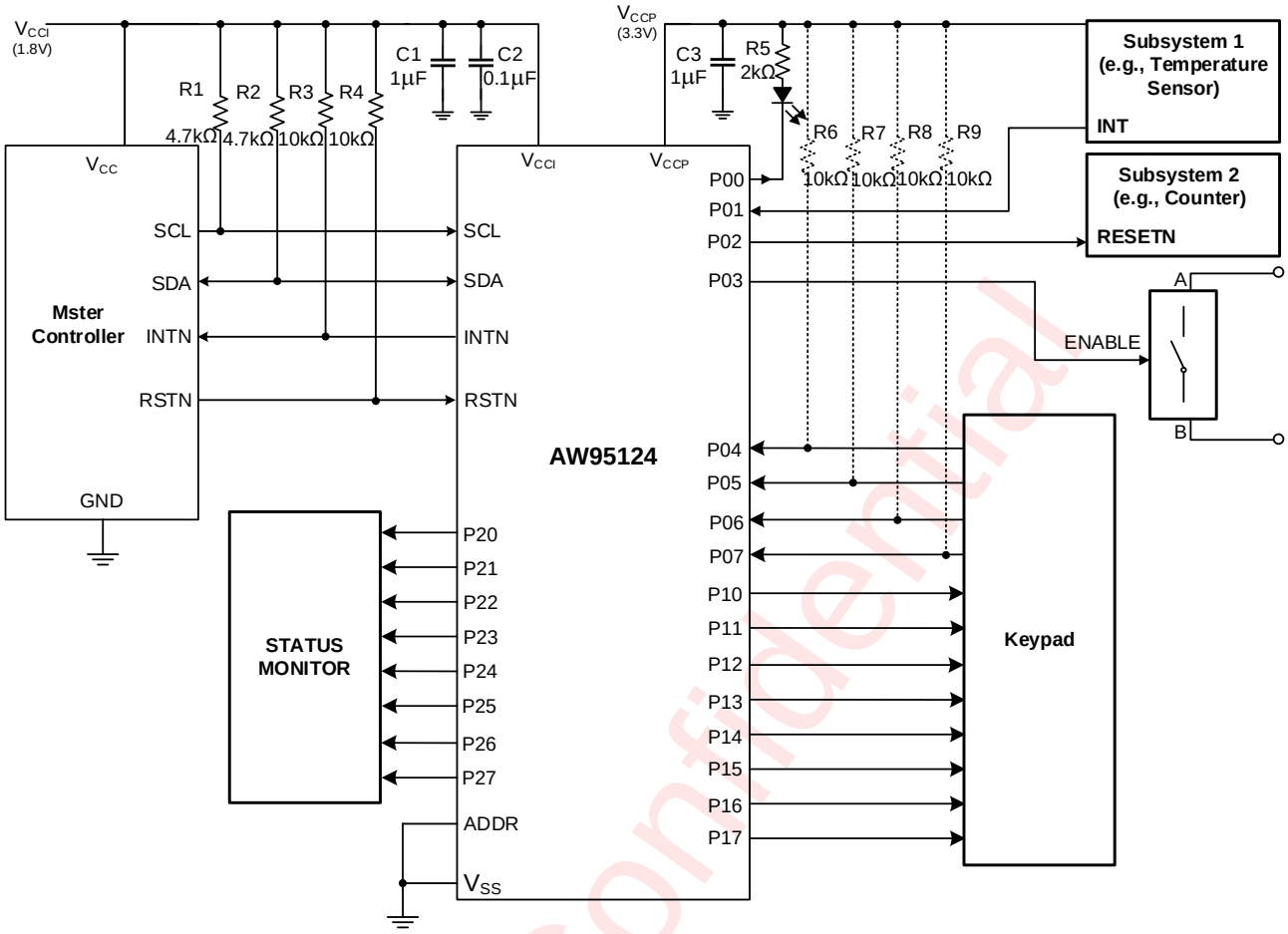
CHIPID: ID register (Address FBh)

Bit	Register	R/W	Description	Default
7:3	Reserved	R	Not used	0
2:0	CHIPID	R	ID register, read only; the readout value is 05h for AW95124FOR; the readout value is 04h for AW95124QNR;	0Xh

Application Information

Applications of the AW95124 has this device connected as a slave to an I²C master (processor), and the I²C bus may contain any number of other slave devices. The AW95124 is typically be in a remote location from the master, placed close to the GPIOs to which the master needs to monitor or control.

A typical application of the AW95124 operates with a lower voltage on the controller side (V_{CCI}), and a higher voltage on the P port side (V_{CCP}). The P ports can be configured as outputs connected to inputs of devices such as enable, reset, power select, the gate of a switch, and LEDs. The P ports can also be configured as inputs to receive data from interrupts, alarms, status outputs, or push buttons.



(1) In this application schematic, P00, P02, P03 andP10~P27 are configured as outputs.
(2) P01 and P04~P07 are configured as inputs.
(3) Device address is configured as 0100010 for this example.

Figure 29 AW95124 Application Circuit

Minimizing I_{CC} When I/O is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CCP} through a resistor as shown in Figure 29. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2V less than V_{CCP}. The ΔI_{CC} parameter in the Electrical Characteristics table shows how I_{CCP} increases as V_{IN} becomes lower than V_{CCP}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CCP} when the LED is off to minimize current consumption.

Figure 30 shows a high-value resistor in parallel with the LED. Figure 31 shows V_{CCP} less than the LED supply voltage by at least 1.2V. Both of these methods maintain the I/O V_{IN} at or above V_{CCP} and prevent additional supply current consumption when the LED is off.

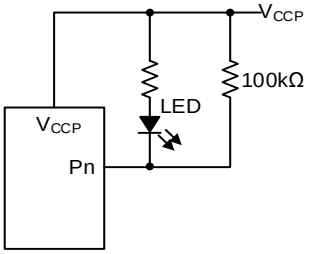


Figure 30 High-Value Resistor in Parallel With LED

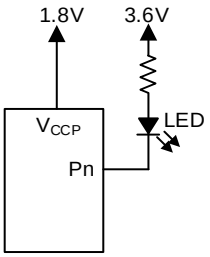


Figure 31 Device Supplied by Lower Voltage

Pull-up Resistor Calculation

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I²C bus. The minimum pull-up resistance is a function of pull-up reference voltage (V_{CC}), V_{OL}(max), and I_{OL} as shown in Equation 1.

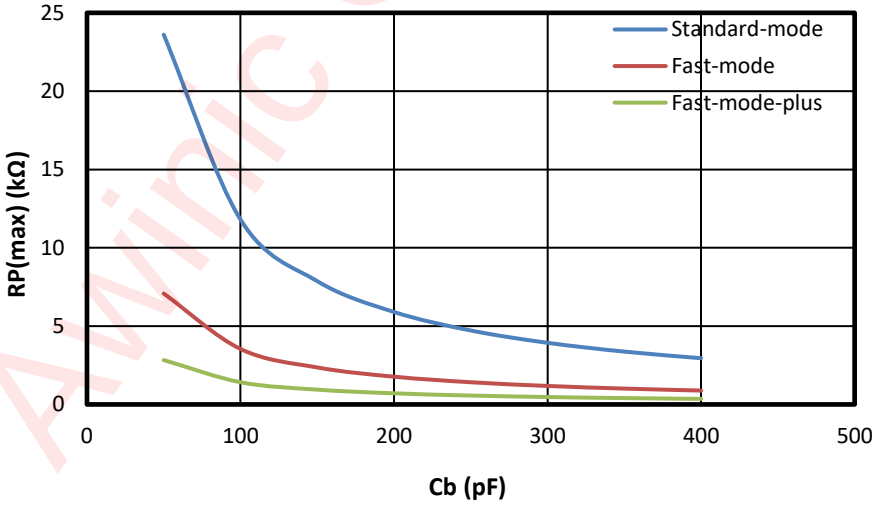
$$R_{p(min)} = \frac{V_{CC}-V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (120ns for fast-mode-plus operation, f_{SCL}=1000kHz) and bus capacitance, C_b as shown in Equation 2.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

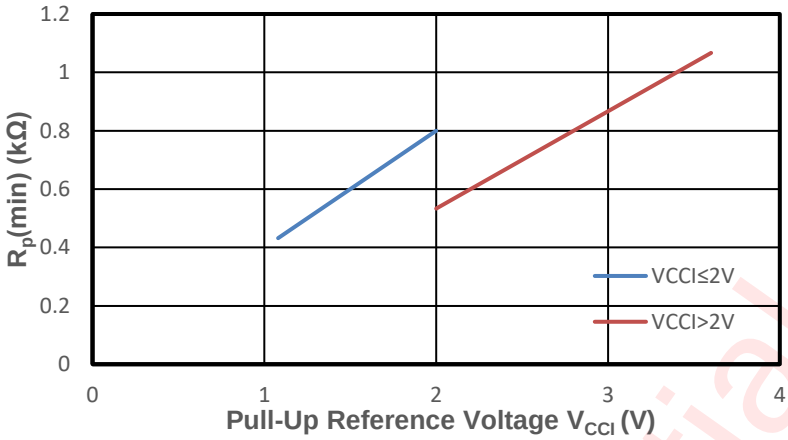
The maximum bus capacitance for an I²C bus must not exceed 400pF for standard-mode or fast-mode operation, or 550pF for fast-mode-plus. The bus capacitance can be approximated by adding the capacitance of the AW95124, C_i for SCL or C_{io} for SDA, the capacitance of wires, connections and traces, and the capacitance of additional slaves on the bus.

Application Curves



Standard-mode (f_{SCL}=100kHz, t_r=1μs) Fast-mode (f_{SCL}=400kHz, t_r=300ns) Fast-mode-plus (f_{SCL}=1000kHz, t_r=120ns)

Figure 32 Maximum Pull-Up Resistance (Rp(max)) vs Bus Capacitance (Cb)



V_{OL}=0.2*V_{CCI}, I_{OL}=2mA when V_{CCI}⩽2V

V_{OL}=0.4V, I_{OL}=3mA when V_{CCI}>2V

Figure 33 Minimum Pull-up Resistance (Rp(min)) vs Pull-up Reference Voltage (V_{CCI})

Power Supply Recommendations

In the event of a glitch (data output or input or even power) or data corruption, the AW95124 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 33 and Figure 34.

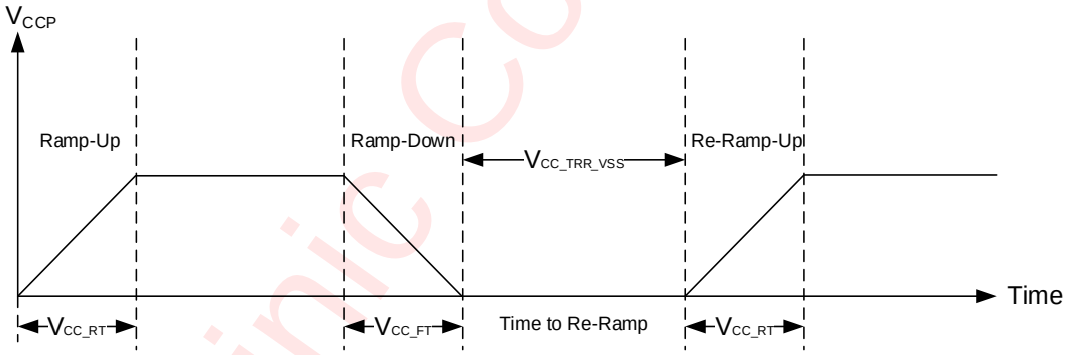


Figure 33 V_{CCP} is Lowered Below 0.2V or 0V and Then Ramped Up to V_{CCP}

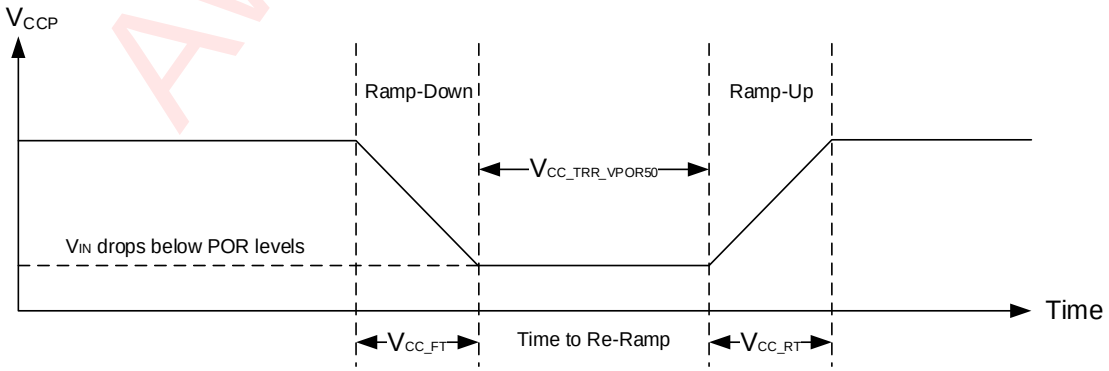


Figure 34 V_{CCP} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CCP}

Table 2 specifies the performance of the power-on reset feature for AW95124 for both types of power-on reset.

Table 2 Recommended Supply Sequencing and Ramp Rates

Parameter			Min.	Typ.	Max.	Unit
V_{CC_FT}	Fall rate of V_{CCP}	See Figure 33	0.1		2000	ms
V_{CC_RT}	Rise rate of V_{CCP}	See Figure 33	0.1		2000	ms
$V_{CC\_TRR\_VSS}$	Time to re-ramp (when V_{CCP} drops below 0.2V or to V_{SS})	See Figure 33	1			μs
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CCP} drops to $V_{POR(MIN)}$ – 50mV)	See Figure 34	1			μs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CC_GW}=1μs	See Figure 35			1	V
V_{CC_GW}	Glitch width that does not cause a functional disruption when V_{CC_GH}=0.5×V_{CC} (For V_{CCP}>1.65V)	See Figure 35			10	μs

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 35 and Table 2 provide more information on how to measure these specifications.

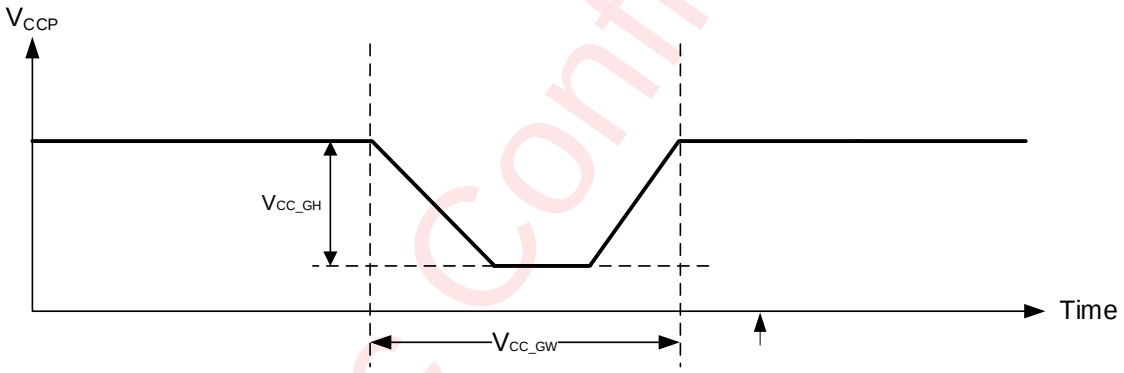


Figure 35 Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CCP} being lowered to or from 0V. Figure 36 and Table 2 provide more details on this specification.

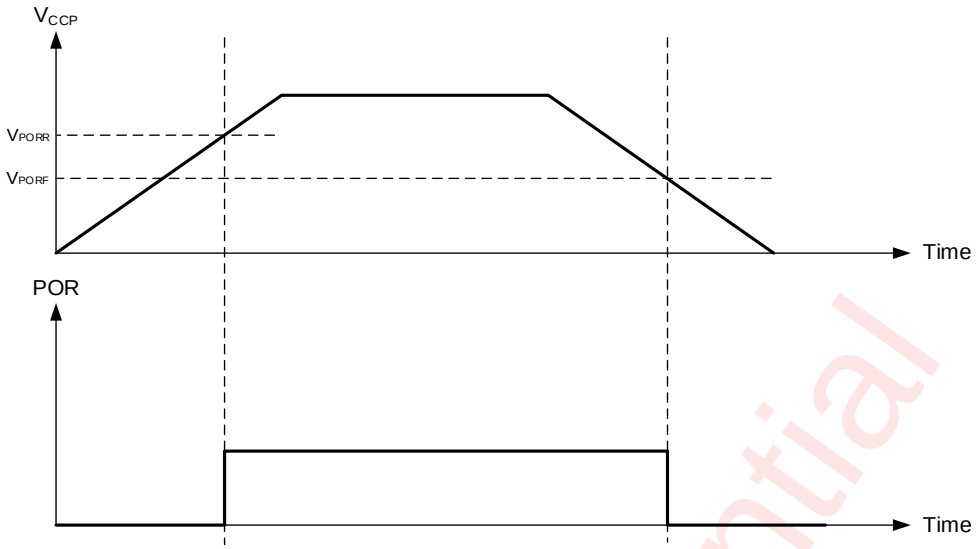


Figure 36 V_{POR}

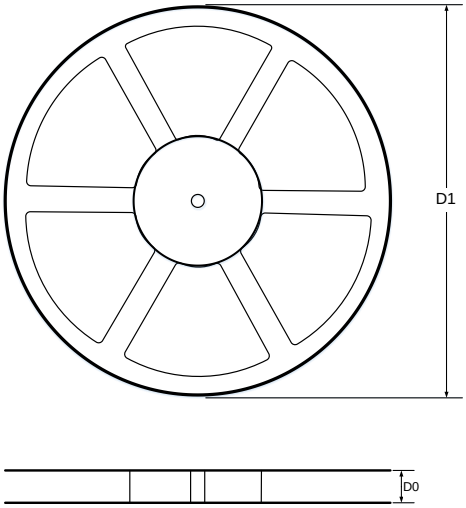
PCB Layout Consideration

AW95124 is a 24-bit I/O expander that can be controlled through the I^2C bus. To obtain the good thermal performance, PCB layout should be considered carefully. Here are some guidelines:

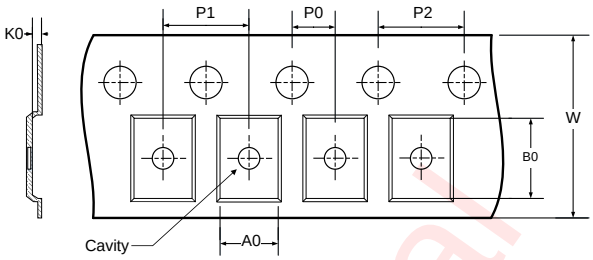
1. The C1, C2 should be placed as close to the V_{CCI} pin as possible, the C3 should be placed as close to the V_{CCP} pin as possible.
2. I^2C wiring follows impedance matching.
3. The GND pad must be well connected to the ground of the PCB, and add as many thermal vias as possible near the GND on the PCB for the heat conductivity of the device and PCB.

Tape And Reel Information

REEL DIMENSIONS

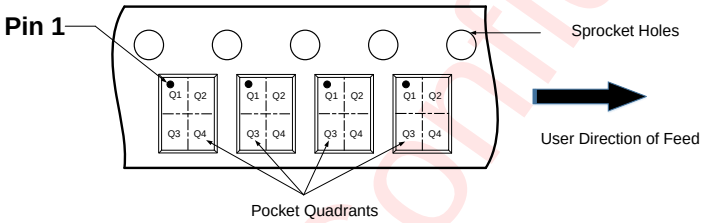


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



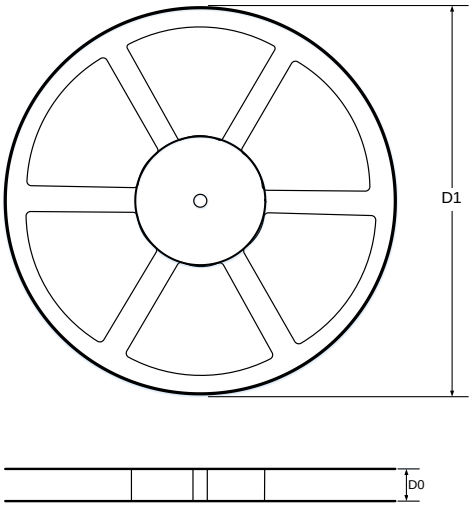
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

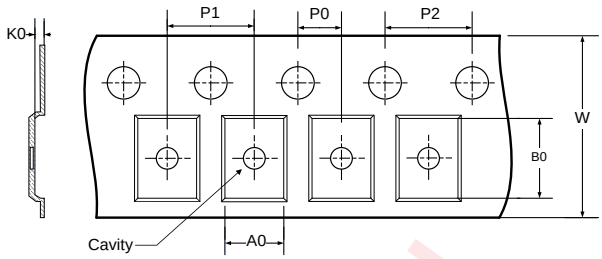
Device Name	D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
AW95124FOR	178.0	8.40	2.73	2.73	0.68	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

REEL DIMENSIONS

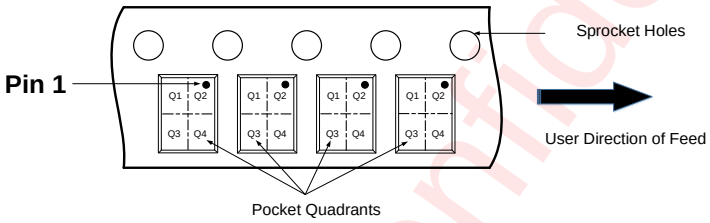


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



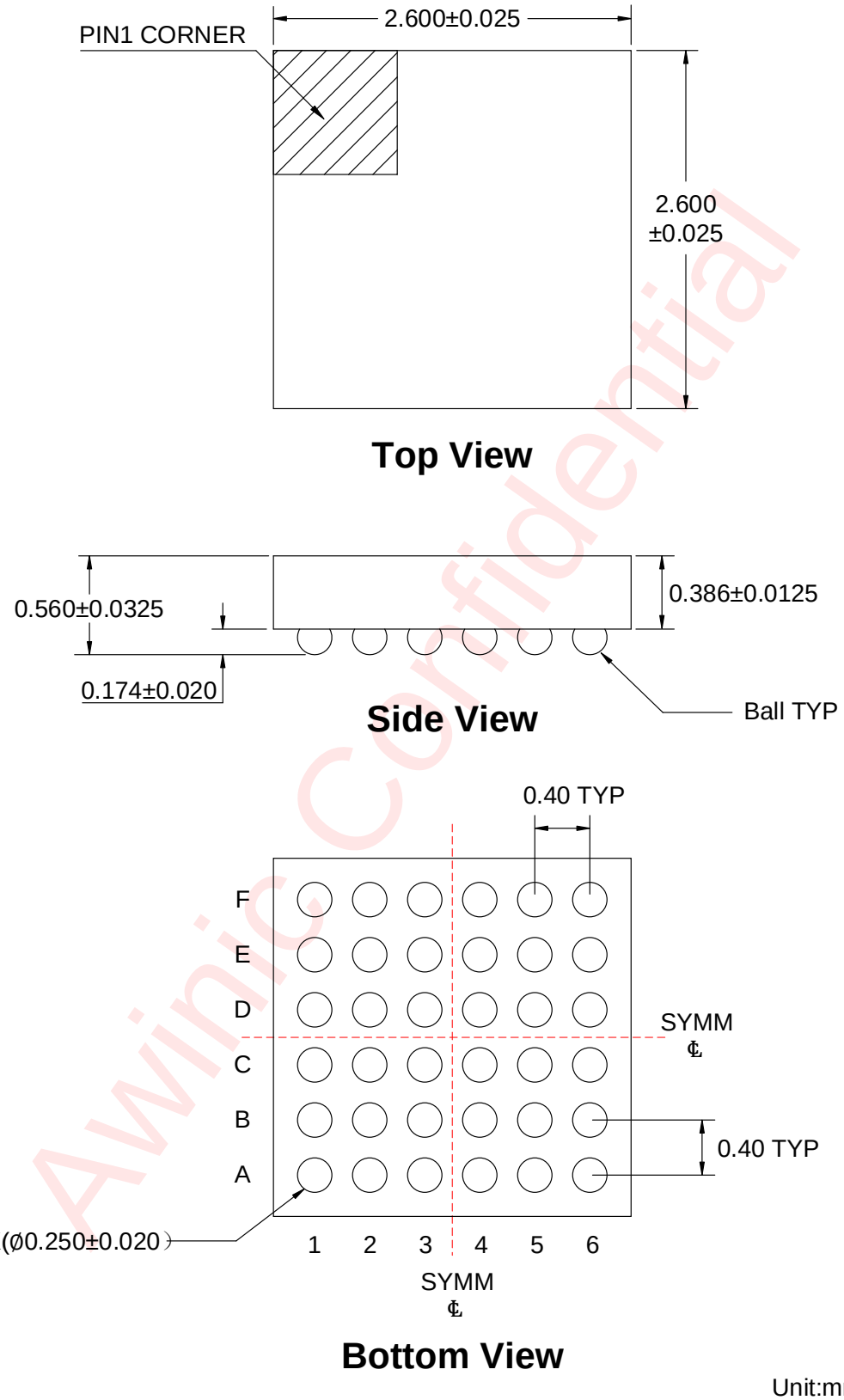
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

Device Name	D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
AW95124QNR	330.0	12.40	5.25	5.25	0.75	2.00	8.00	4.00	12.00	Q2

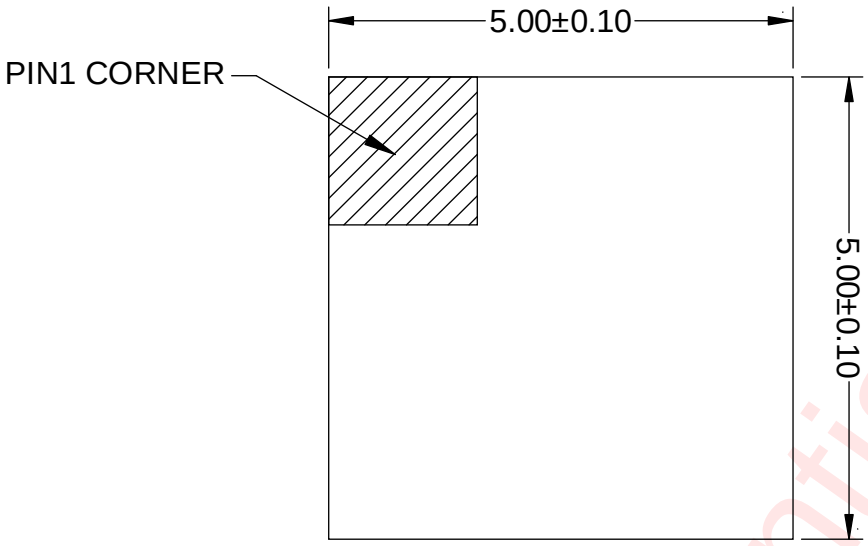
All dimensions are nominal

Package Description

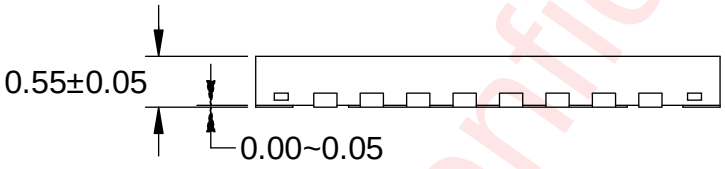


Unit:mm

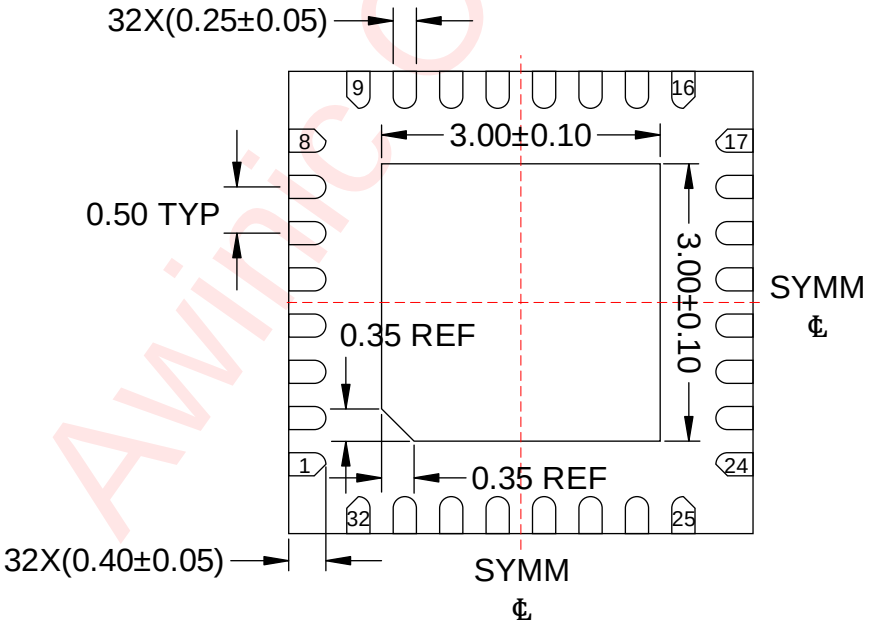
AW95124FOR Package Description



Top View



Side View

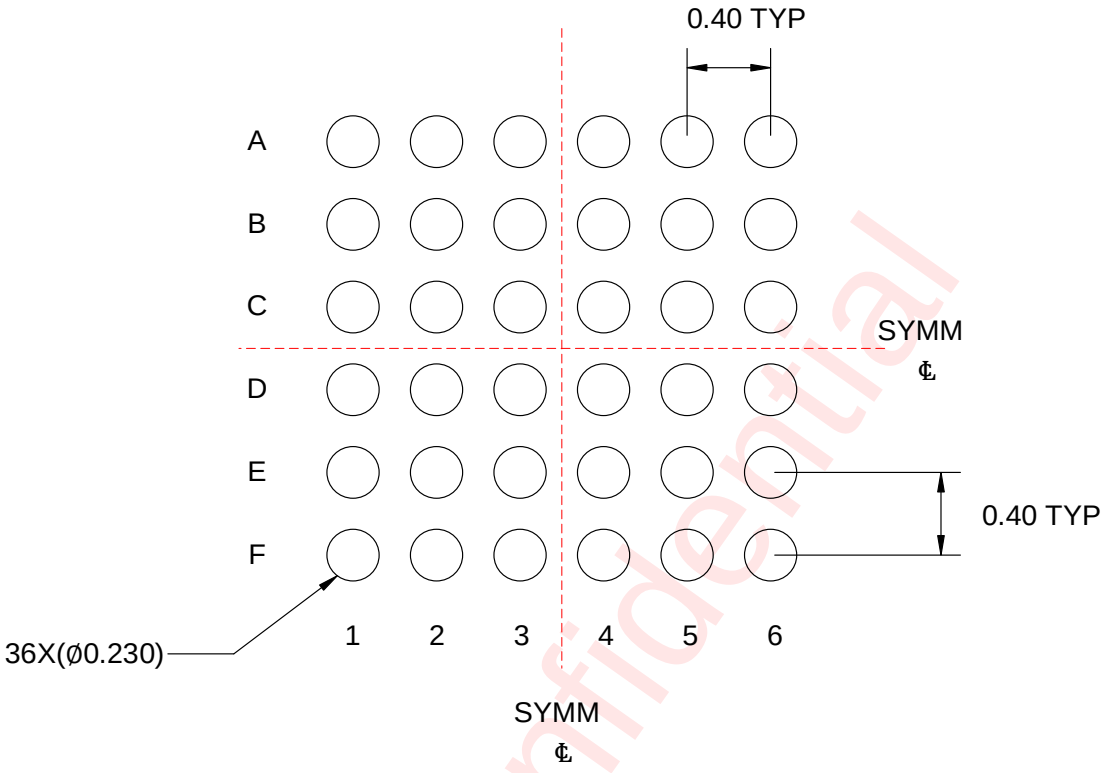


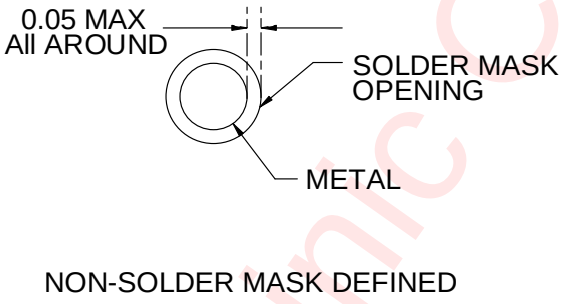
Bottom View

Unit:mm

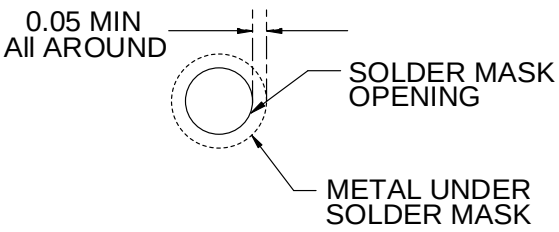
AW95124QNR Package Description

Land Pattern Data





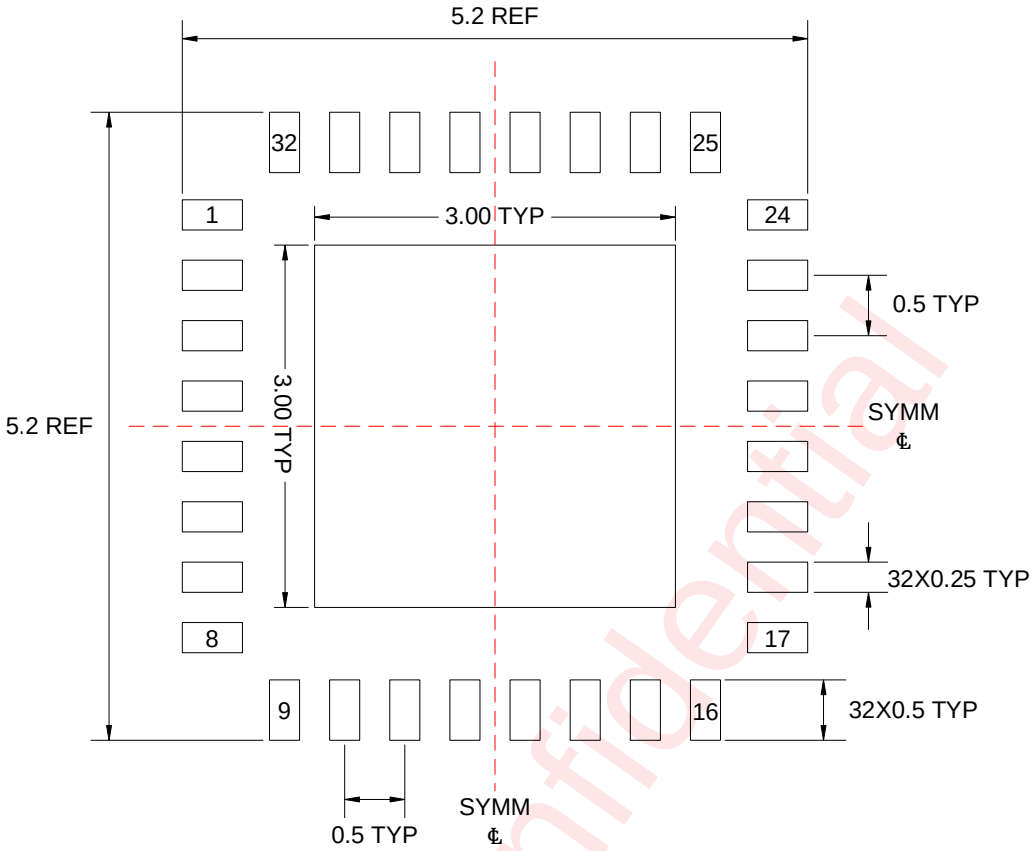
NON-SOLDER MASK DEFINED

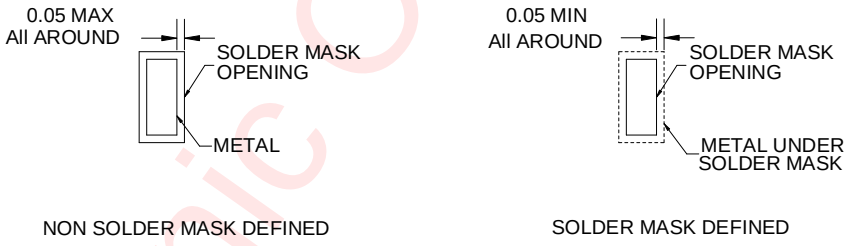


SOLDER MASK DEFINED

Unit: mm

AW95124FOR Land Pattern Data





Unit：mm

AW95124QNR Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Oct.2024	Officially released
V1.1	May.2025	Add AW95124QNR
V1.2	Jun.2025	Update the tape information of AW95124QNR

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