I²S/TDM Input, High Efficiency, 10.25V BOOST Digital Smart K Audio Amplifier

FEATURES

- **Smart amplifier with total efficiency up to 85%**
- **High RF noise suppression, eliminate the TDD noise completely**
- **Output noise：**
  - **Speaker mode: 10.5μV**
  - **Receiver mode: 7.2μV**
- **THD+N: 0.02%**
- **Speaker Voltage and Current monitor and feedback with I2S/TDM interface**
- Supports 4Ω Speaker
- Extensive Pop-Click Suppression
- Volume control (from -96dB to 0dB)
- I2S/TDM interface：
  - I²S, Left-Justified and Right-Justified
  - Supports 1/2/4/6/8/16 slots TDM
  - Input Sample Rates from 8kHz to 192kHz
  - Data Width: 16, 20, 24, 32 Bits
- Ultrasonic support with sample frequency greater than or equal to 96kHz
- I2C-bus control interface
- Power Supplies：
  - VBAT: 2.5V-5.5V
  - DVDD: 1.65V~1.95V
  - VDDIO: 1.2V / 1.8V
- Battery Brown Out Protection
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- WLCSP 2.2mmX2.2mm-36B Package

APPLICATIONS

- Mobile phones
- Tablets
- Portable Audio Devices

DESCRIPTION

The AW88460CSR is an I2S/TDM input, high efficiency digital Smart K audio amplifier with an integrated 10.25V smart boost converter. Due to its 7.2μV noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 5.2W output power into an 8Ω speaker at a battery voltage of 4.2V.

The AW88460CSR integrates a high-efficiency smart boost converter as the Class-D amplifier supply rail. The output voltage of boost converter can be adjusted smartly according to the input amplitude, which extremely improves the efficiency without clipping distortion.

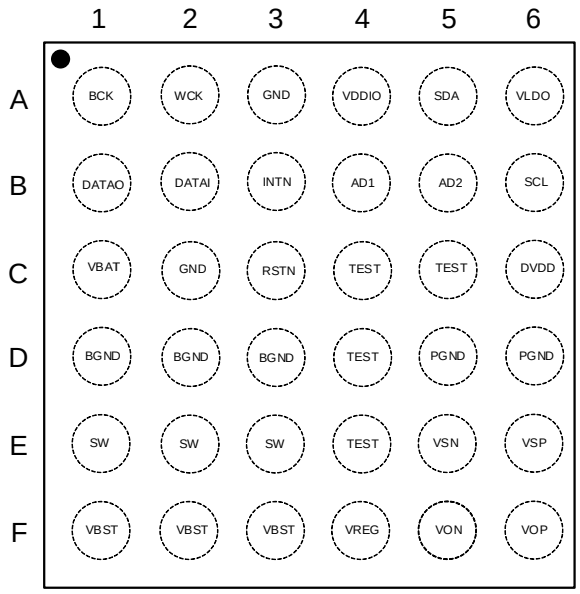
The AW88460CSR features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface. General settings are communicated via an I2C-bus interface, and the device address is configurable.

The AW88460CSR offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

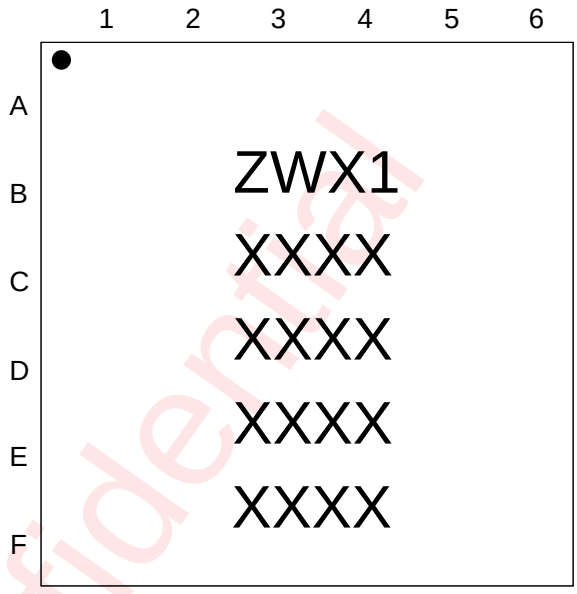
AW88460CSR is available in a WLCSP 2.2mmX2.2mm-36B Package.

PIN CONFIGURATION AND TOP MARK

AW88460CSR (Top View)



AW88460CSR Marking (Top View)



ZWX1：AW88460CSR

XXXX/XXXX/XXXX/XXXX：Production Tracing Code

Figure 1 AW88460CSR pin diagram top view and device marking

PIN DESCRIPTION

Pin No	Pin Name	Description
A1	BCK	I2S/TDM bit clock input
A2	WCK	I2S word select input / TDM frame sync signal
A3, C2	GND	GND
A4	VDDIO	Digital I/O supply voltage
A5	SDA	I2C data IO
A6	VLDO	Digital core voltage regulator output
B1	DATAO	I2S/TDM data out
B2	DATAI	I2S/TDM data input
B3	INTN	Interrupt output
B4	AD1	I2C device address selection
B5	AD2	I2C device address selection
B6	SCL	I2C clock input
C1	VBAT	Battery power supply
C3	RSTN	Active low hardware reset
C4, C5, D4, E4	TEST	Test signal, connected to GND

Pin No	Pin Name	Description
C6	DVDD	Digital power supply
D1, D2, D3	BGND	Boost GND
D5, D6	PGND	Power GND
E1, E2, E3	SW	Boost switch pin
E5	VSN	Voltage sense inverting
E6	VSP	Voltage sense non-inverting
F1, F2, F3	VBST	Boost output
F4	VREG	Voltage output of regulator
F5	VON	Inverting Class-D output
F6	VOP	Non-inverting Class-D output

FUNCTIONAL BLOCK DIAGRAM

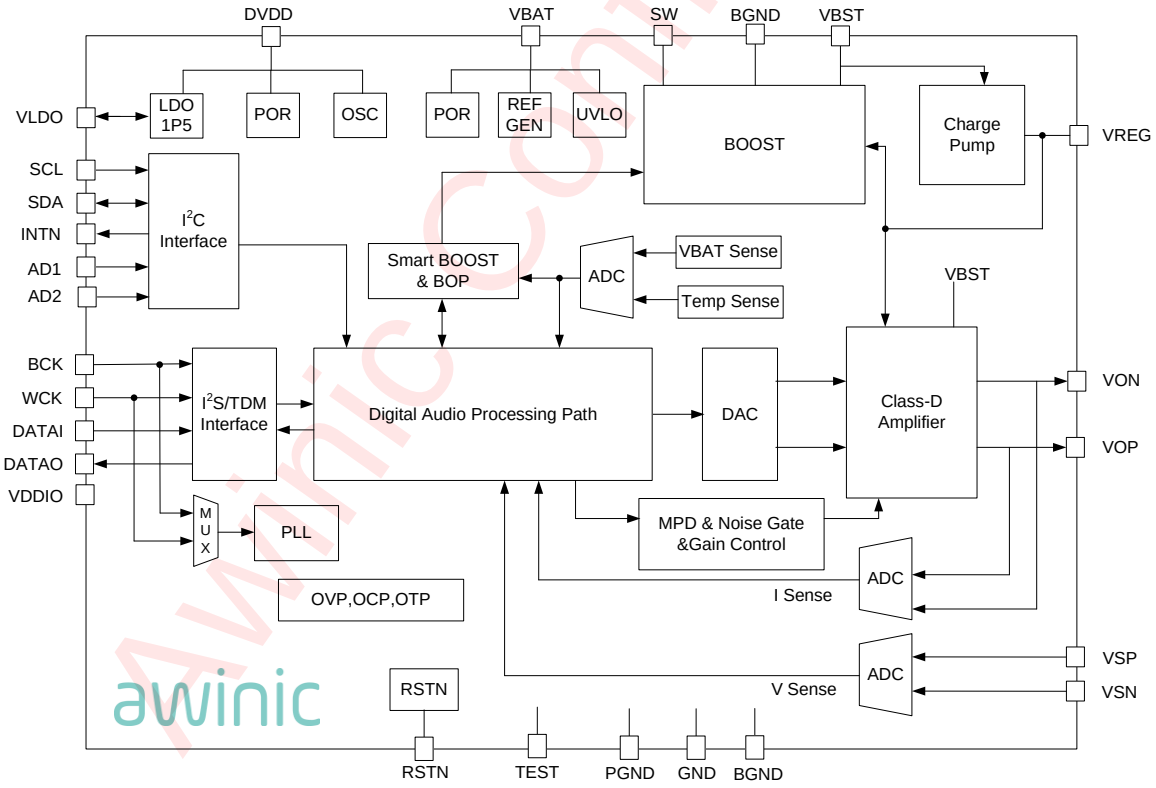


Figure 2 FUNCTIONAL BLOCK DIAGRAM

APPLICATION DIAGRAM

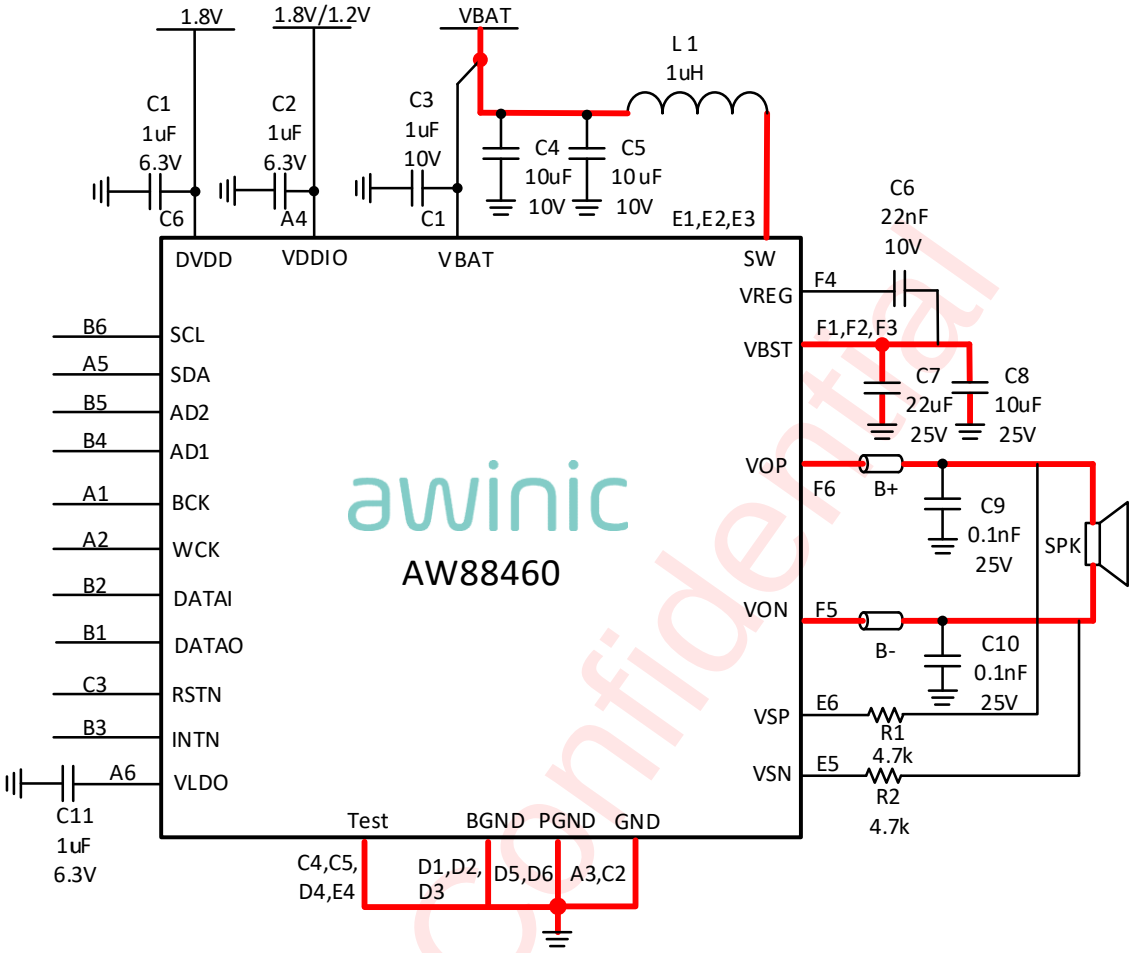


Figure 3 AW88460 Application Circuit

Note: *Traces carry high current are marked in red in the above figure*

ORDERING INFORMATION

Product Type	Temperature	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW88460CSR	-40°C～85°C	WLCSP 2.2mmX2.2mm-36B	ZWX1	MSL1	ROHS+HF	4500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATING(NOTE1)

Parameter	Range
Battery Supply Voltage V_{VBAT}	-0.3V to 7V
Digital Supply Voltage V_{DVDD}	-0.3V to 2V
Digital Supply Voltage V_{VDDIO}	-0.3V to 2V
Boost output voltage V_{VBST}	-0.3 to 14V
Boost SW pin voltage	-0.3 to V_{VBST} (Note 2)
VOP/VON pin voltage	-0.3 to V_{VBST} (Note 2)
Minimum load resistance R_L	3.2Ω
Package Thermal Resistance θ_{JA}	40.88°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating (Note 3,4)	
HBM (Human Body Model)	±2000V
CDM (Charge Device Model)	±1500V
Latch-up	
Test Condition：JEDEC STANDARD NO.78E SEPTEMBER 2016	+IT：200mA -IT：-200mA

Note 1：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2：*Using Awinic demo board, with a 1mm wire/PCB track length, SW/VOP/VON pins can handle -5V and +16V transients for less than 5ns without damaging the chip.*

Note 3：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9*

Note 4：*Test method: JEDEC EIA/JESD22-C101F*

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS

Test condition： T_A=25°C， VBAT=4.2V， VDDIO=1.8V, DVDD=1.8V, VBST=10.25V, R_L=8Ω+33μH ，f=1kHz(unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{VBAT}	Battery supply voltage(Note1)	On pin VBAT(Note2)	2.5		5.5	V
V_{DVDD}	Digital supply voltage(Note1)	On pin DVDD	1.65	1.8	1.95	V
V_{VDDIO}	IO supply voltage(Note1)	On pin VDDIO	1.1	1.2	1.3	V
			1.65	1.8	1.95	V
I_{VBAT}	Battery supply current	Idle mode		4.2		mA
		Idle mode, noise gate ON		1.3		mA
		Standby mode		5		μA
		Power down mode, RSTN=0V		0.6		μA
I_{DVDD}	Digital supply current	Idle mode		1.5		mA
		Idle mode, noise gate ON		1.5		mA
		Standby mode		5		μA
		Power down mode		4		μA
Boost						
V_{VBST}	Boost output voltage			10.25(Note3)		V
V_{OVP}	Over-voltage threshold(Note1)		V_{VBST}+0.8	V_{VBST}+1	V_{VBST}+1.2	V
	OVP hysteresis voltage			400		mV
I_{L_PEAK}	Inductor peak current limit		1.5	4(Note3)	4.25	A
F_{BST}	Operating Frequency(Note1)	fs = 48kHz	1.8	2	2.1	MHz
η_{BST}	Boost converter efficiency	VBAT=4.2V, I_{load} = 0.5A		88.5		%
Class-D						
R_{dson}	Drain-Source on-state resistance(Note1)	High side MOS + Low side MOS	200	280	430	mΩ
Po	Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, VBAT=4.2V, VBST =10.25V		5.2		W
		THD+N=10%, R_L=8Ω+33μH, VBAT=4.2V, VBST =10.25V		6.5		W
		THD+N=1%, R_L=6Ω+33μH, VBAT=4.2V, VBST =10.25V		5.4		W
		THD+N=10%, R_L=6Ω+33μH, VBAT=4.2V, VBST =10.25V		6.7		W
V_{OS}	Output offset voltage	I^2S signal input 0	-1	0	1	mV
F_{PWM}	PWM Switching frequency	Typical Sample Rate: 48kHz	365	384	420	kHz

Symbol	Description	Test Conditions		Min	Typ.	Max	Units
η	Total efficiency (Class-D)	VBAT=4.2V, Po=0.91W, R_L=8Ω+33μH			91		%
	Total efficiency (SmartBoost+Class-D)	VBAT=4.2V, Po=2W, R_L=8Ω+33μH			85		%
THD+N	Total harmonic distortion plus noise	VBAT=4.2V, Po=1W, R_L=8Ω+33μH, f=1kHz，VBST =10.25V			0.02		%
E_N	Speaker Mode Output noise	A-weighting			10.5		μV
	Speaker Mode Output noise	A-weighting, noise gate ON			1.3		μV
	Receiver Mode Output noise	A-weighting			7.2		μV
	Receiver Mode Output noise	A-weighting, noise gate ON			1.3		μV
SNR	Signal-to-noise ratio	VBAT=4.2V, VBST =10.25V, Po=5.2W, R_L=8Ω+33μH, MPD OFF, A-weighting			108		dB
		VBAT=4.2V, VBST =10.25V, Po=5.2W, R_L=8Ω+33μH, MPD ON, A-weighting			116		dB
DNR	Dynamic Range	-60dBFS Method, A-weighting			111		dB
PSRR	Power supply rejection ratio	Receiver Mode, VBAT=4.2V, V_{p-p_sin}=200mV	217Hz		90		dB
			1kHz		89		dB
Current Sense							
I_{SNS_FS}	Current sense full scale				2.92		A
SNR	Signal-to-noise ratio	Ipeak=1A, R_L=8Ω+33μH, A-weighting			69		dB
THD+N	Total harmonic distortion plus noise	Po=1W, R_L=8Ω+33μH			0.2		%
ΔI_{SNS}	Current sense accuracy	Po=1W, R_L=8Ω+33μH			2		%
Voltage Sense							
V_{SNS_FS}	Voltage sense full scale				23.4		V
SNR	Signal-to-noise ratio	Ipeak=1A, R_L=8Ω+33μH, A-weighting			65		dB
THD+N	Total harmonic distortion plus noise	Po=1W, R_L=8Ω+33μH			0.1		%
ΔV_{SNS}	Voltage sense accuracy	Po=1W, R_L=8Ω+33μH			2		%

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
Digital Logical Interface						
V_{IL}	Logic input low level	BCK, WCK, DATAI Pin			0.3 x V_{VDDIO}	V
V_{IH}	Logic input high level		0.7 x V_{VDDIO}		V_{VDDIO}	V
V_{IL}	Logic input low level	SCL, SDA, AD Pin			0.3 x V_{VDDIO}	V
V_{IH}	Logic input high level		0.7 x V_{VDDIO}		V_{VDDIO}	V
V_{OL}	Logic output low level	I_{OUT}=2mA			0.2	V
V_{OH}	Logic output high level	I_{OUT}=-2mA	V_{VDDIO} - 0.2		V_{VDDIO}	V
Protection						
T_{SD}	Over temperature protection threshold			150		°C
T_{SDR}	Over temperature protection recovery threshold			130		°C
UVP	Under-voltage protection voltage			2.4(Note4)		V
	Under-voltage protection hysteresis voltage			200	300	mV

Note1：*Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.*

Note2：*Device performance will degreed below 3V.*

Note3：*Registers are adjustable; Refer to the list of registers.*

Note4：*Under-voltage protection voltage is set by register*

I²C INTERFACE TIMING

Parameter			Fast mode			Fast mode plus			Units
No.	Sym	Name	Min	Typ.	Max	Min	Typ.	Max	
1	f_{SCL}	SCL Clock frequency			400k			1M	Hz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.26			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			0.26			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05			μs
11	$t_{HD:DAT}$	SDA hold time	10			10			ns

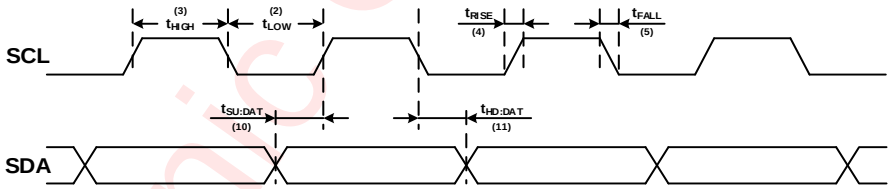


Figure 4 SCL and SDA timing relationships in the data transmission process

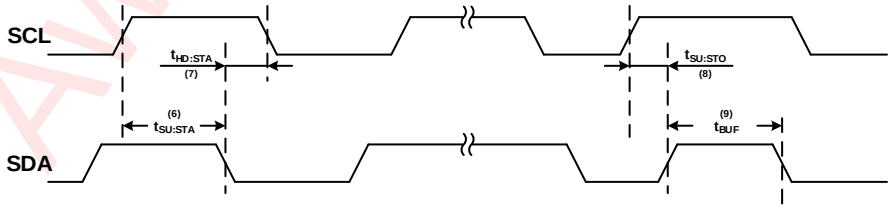


Figure 5 The timing relationship between START and STOP state

DIGITAL AUDIO INTERFACE TIMING

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WCK	8		192(Note1)	kHz
f_{bck}	Bit clock frequency, on pin BCK	16*fs		12.288M(Note1)	Hz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns
t_d	DATAO output delay time to BCK			50	ns

Note 1：*Test condition: VDDIO=1.8V; The BCK frequency f_{bck} is determined by sampling frequency, slot number and slot length, please make sure f_{bck} is less than 12.288MHz.*

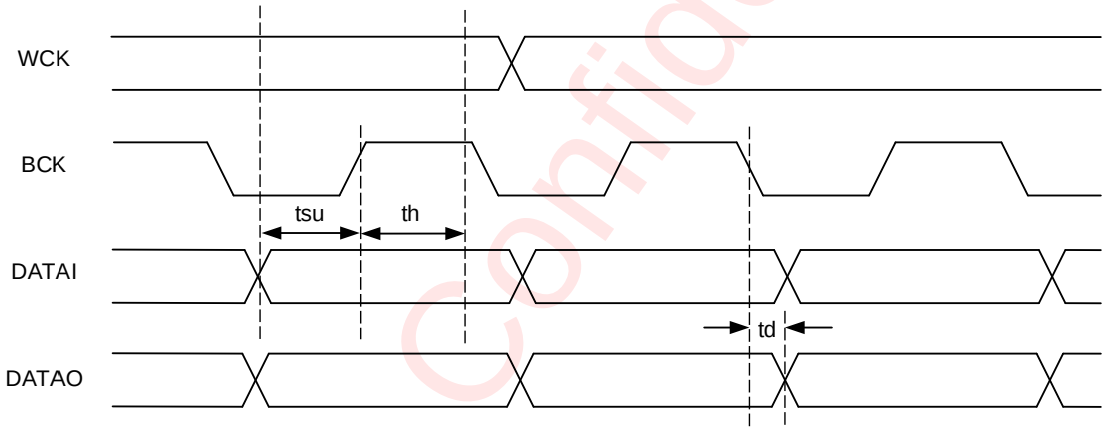
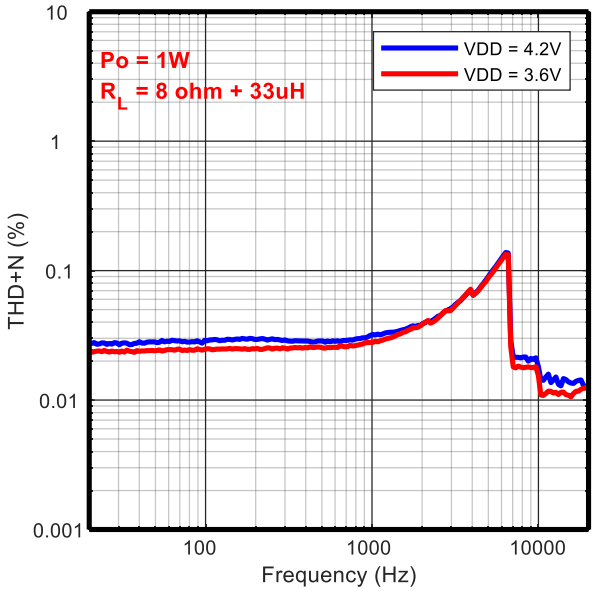


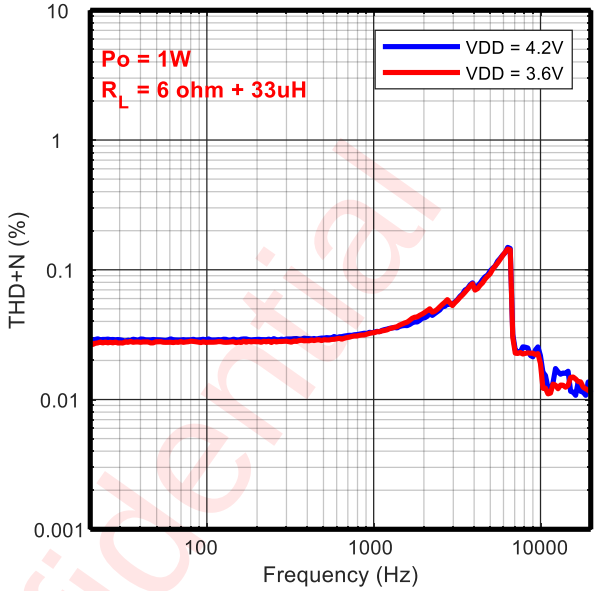
Figure 6 Digital Audio Interface Timing

TYPICAL CHARACTERISTIC CURVES

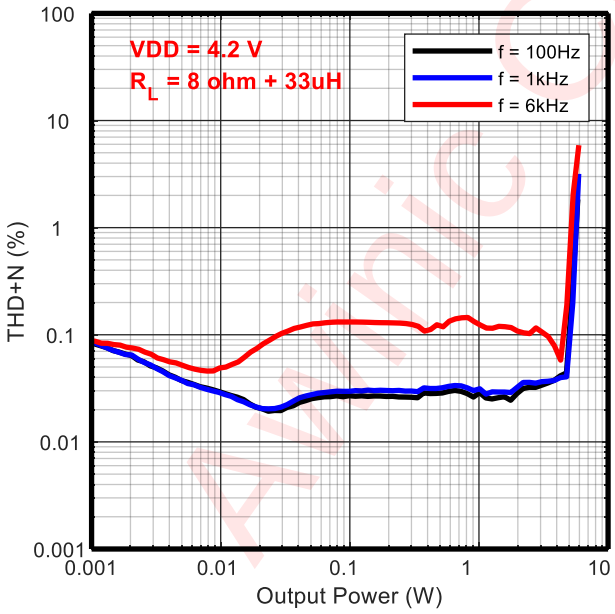
THD+N VS. FREQUENCY



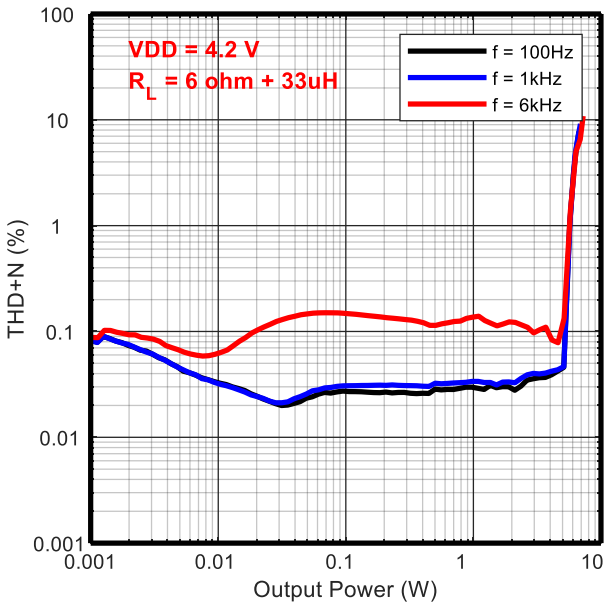
THD+N VS. FREQUENCY



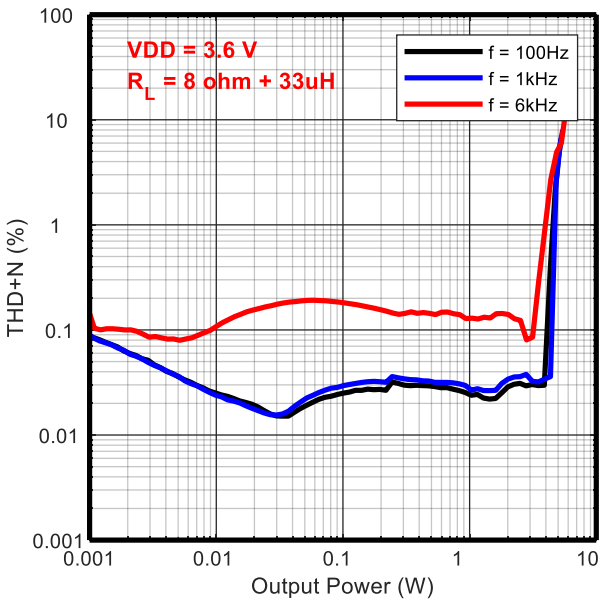
THD+N VS. OUTPUT POWER



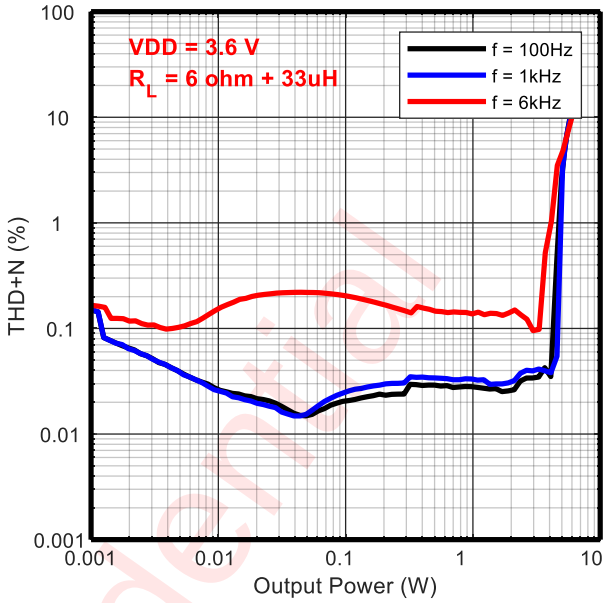
THD+N VS. OUTPUT POWER



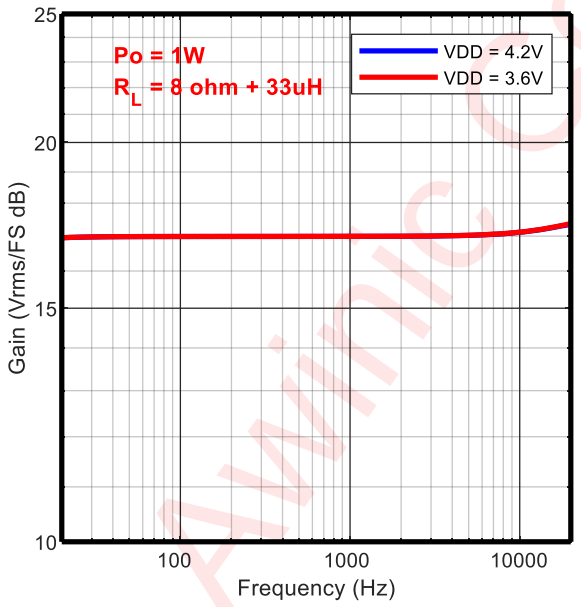
THD+N VS. OUTPUT POWER



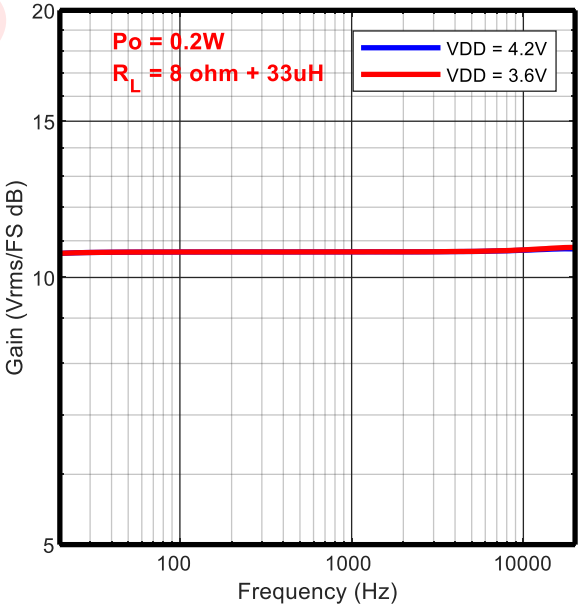
THD+N VS. OUTPUT POWER



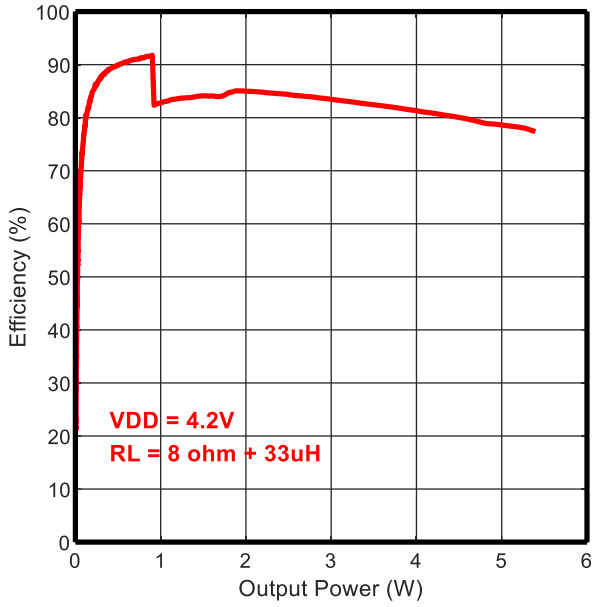
SPEAKER GAIN VS. FREQUENCY



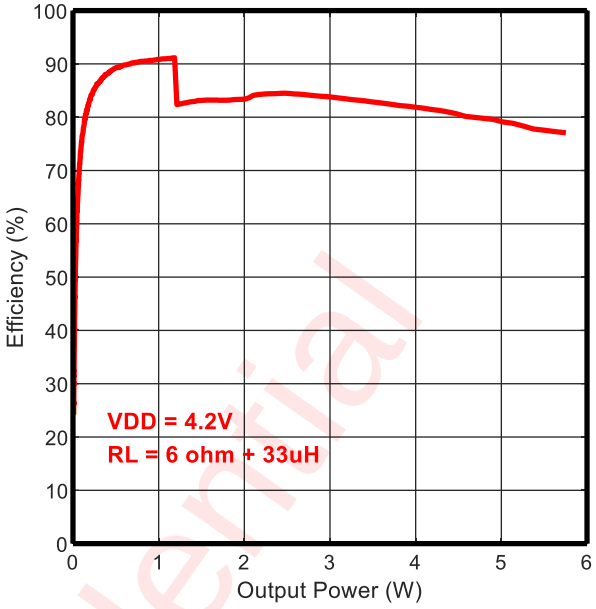
RECEIVER GAIN VS. FREQUENCY



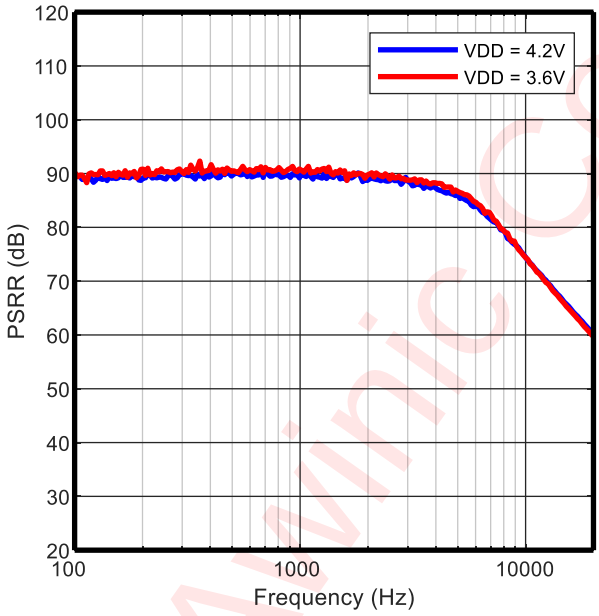
EFFICIENCY VS. OUTPUT POWER



EFFICIENCY VS. OUTPUT POWER



VBAT PSRR VS. FREQUENCY



DETAIL FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VBAT, DVDD and VDDIO supply voltage. When the VBAT supply voltage raises from 0V to 2.1V, DVDD supply voltage raises from 0V to 1.4V, and VDDIO supply voltage raises from 0V to 1.1V, the internal reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 4 operation modes.

Mode	Condition	Description
Power-Down	V_{VBAT} < 2.1V V_{DVDD} < 1.4V V_{VDDIO} < 0.7V	Power supply is not ready, chipset is power down.
Stand-By	V_{VBAT} > V_{UVL} V_{DVDD} > 1.65V V_{VDDIO} > 1.1V	Power supply is ready, most parts of the device are power down for low power consumption except I^2C interface
Configuring	PWDN = 0	Device is biased while boost and Class-D output is floating. System configuration carried out in this mode
Operating	AMPPD = 0	Amplifier is fully operating

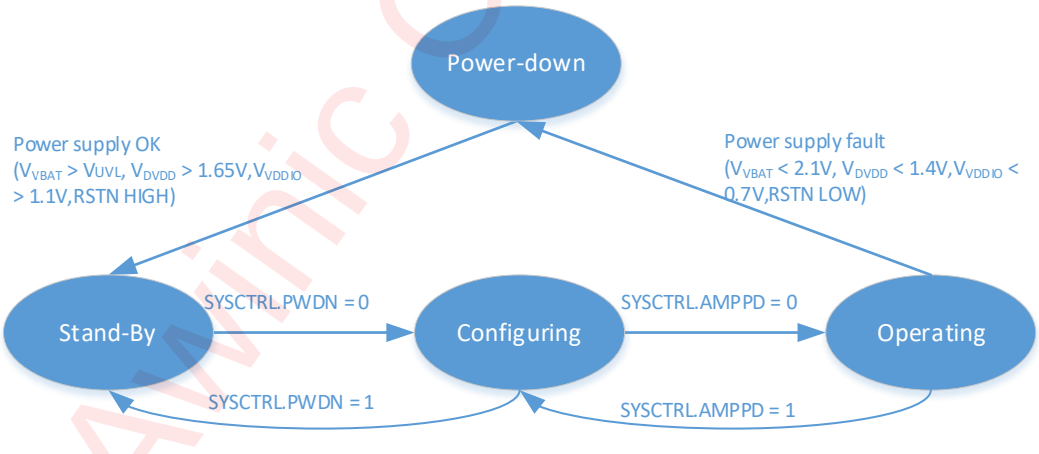


Figure 7 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- V_{DVDD} < 1.4 V
- V_{VDDIO} < 0.7 V
- V_{VBAT} < 2.1 V
- RSTN pin goes LOW

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

V_{DVDD} > 1.65 V, V_{VDDIO} > 1.1 V, V_{VBAT} > V_{UVL} and RSTN goes HIGH.

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are right and RSTN pin is HIGH. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to Stand-By mode when the device is no needed to work.

CONFIGURING MODE

The device switches to Configuring mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.AMPPD = 1;

In this mode the internal bias, OSC, PLL will start to work

OPERATING MODE

The device is fully operational in this mode. Boost, amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.AMPPD = 0 to make device in this mode.

This device power up sequence is illustrated in the following figure:

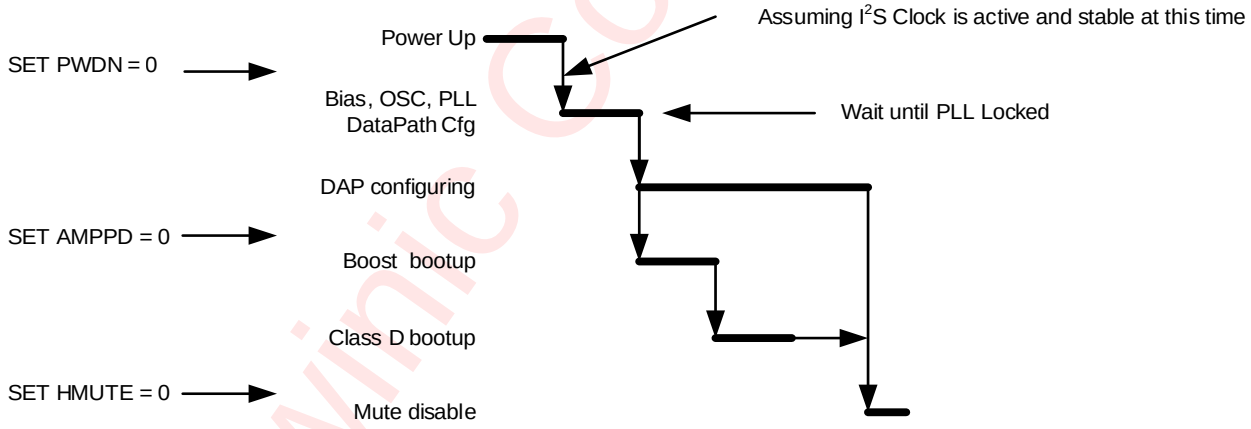


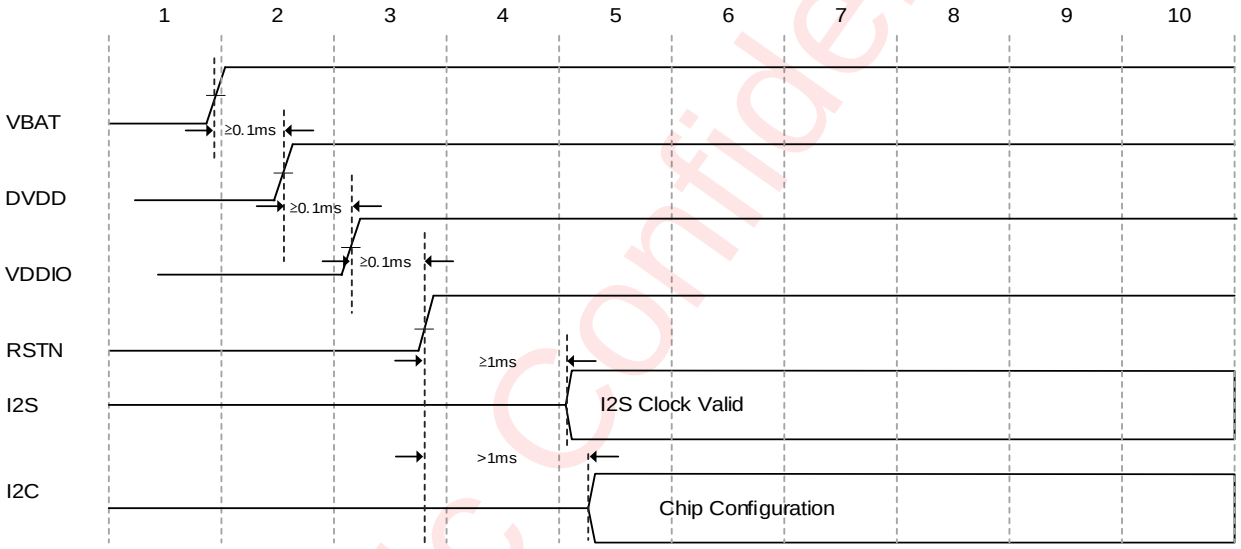
Figure 8 Power up sequence

Detail description for each step is listed in the following table.

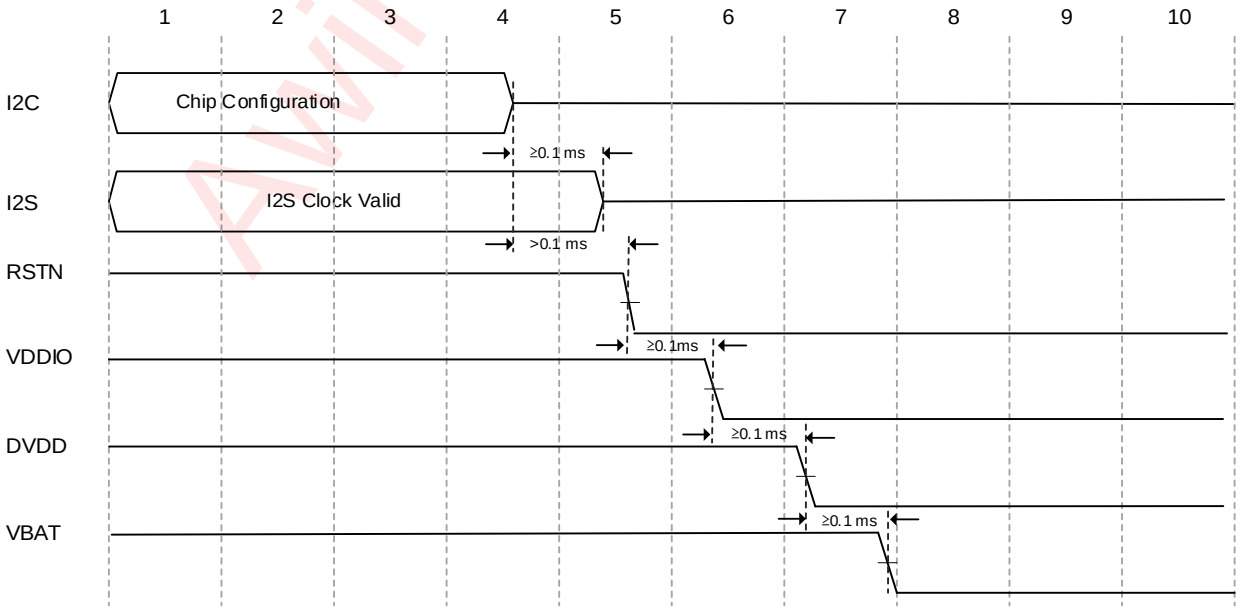
Detail Description of Power up sequence

Index	description	Mode
1	Wait for VBAT, DVDD, VDDIO supply power up	Power-Down
2	I²S + Data Path Configuration	Stand-By
3.1	Enable system (SYSCTRL.PWDN = 0)	Configuring
3.2	Active Bias, OSC and PLL	
3.3	Wait for PLL to be locked	
4	Enable Boost and amplifier (SYSCTRL.AMPPD =0) Boost and Amplifier boot up	Operating
5	Release Hard-Mute Data Path active	

Power up sequence considering I²S, I²C timing shows as below:



Power down sequence considering I²S, I²C timing shows as below:



SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers.

DIGITAL AUDIO INTERFACE

The state of each digital input and output are shown in below table. After power on, the input signal pin BCK, WCK, DATAI are set to high impedance by default. If I2STXEN bit is enabled, DATAO is actively driven when outputting data otherwise it is high impedance by default.

Digital I/O	Type	Description (Default State)
SCL	Input	Hi-Z
SDA	Input	Hi-Z
INTN	Output	Hi-Z
AD1	Input	Weak pull down
AD2	Input	Weak pull down
BCK	Input	Hi-Z
WCK	Input	Hi-Z
DATAI	Input	Hi-Z
DATAO	Output	Hi-Z

DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 4 dedicated pins:

- BCK
- WCK
- DATAI
- DATAO

Two-slot I²S and 1/2/4/6/8/16-slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL1.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL1.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz and 192kHz. The max output signal frequency is 40kHz. It is selected via configurable register I2SCTRL1.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL1.I2SBCK. The frequency of BCK can be calculated according to the following equation:

BCK frequency = ***SampleRate*** * ***SlotLength*** * ***SlotNumber***

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 1/2/4/6/8/16-slot supported in TDM mode.

The word selects and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL1.CHSEL.

Interface format(MSB first)	Data width	BCK frequency
Standard I²S	16b/20b/24b/32b	32fs/48fs /64fs
left-justified	16b/20b/24b/32b	32fs/48fs /64fs
right-justified	16b/20b/24b/32b	32fs /48fs /64fs

The output port DATAO, can be enabled or disabled via bit SYSCTRL.I2STXEN. The unused slots can be set to Hi-z or zero, which is controlled by I2SCTRL3.DOHZ.

STANDARD I²S MODE

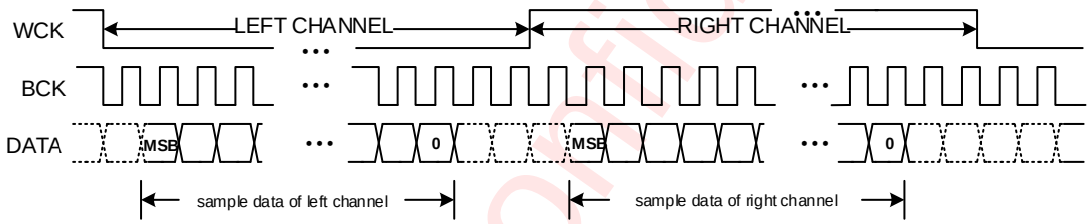


Figure 9 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

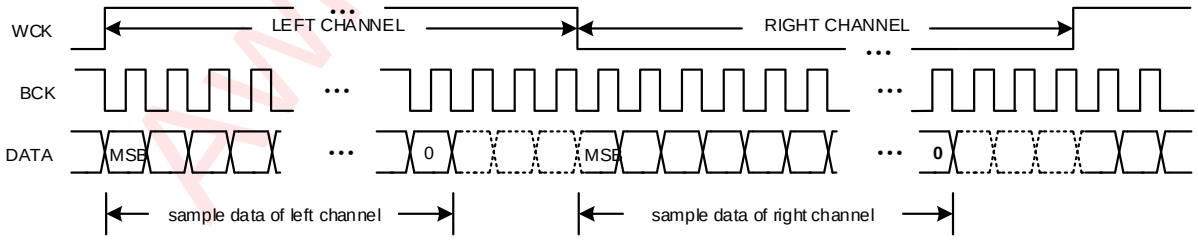


Figure 10 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

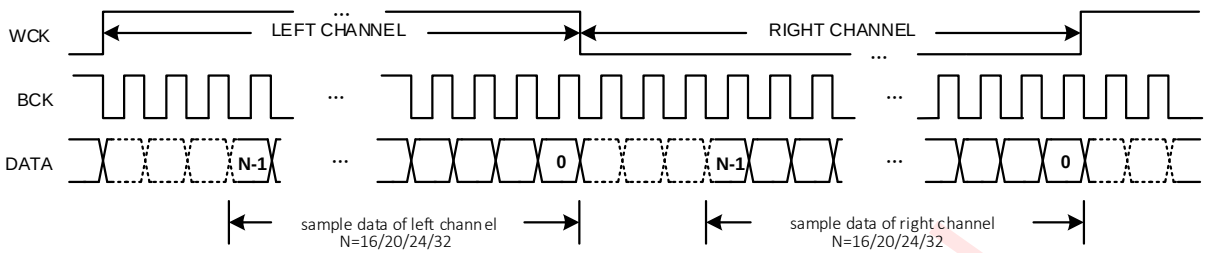


Figure 11 I²S Timing for Right-Justified Mode

- When WCK is high indicating the left channel data, and WCK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

TDM MODE

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 1/2/4/6/8/16-slot is supported in TDM mode, while 2-slot is supported in I²S mode. 4-slot in TDM mode for example:

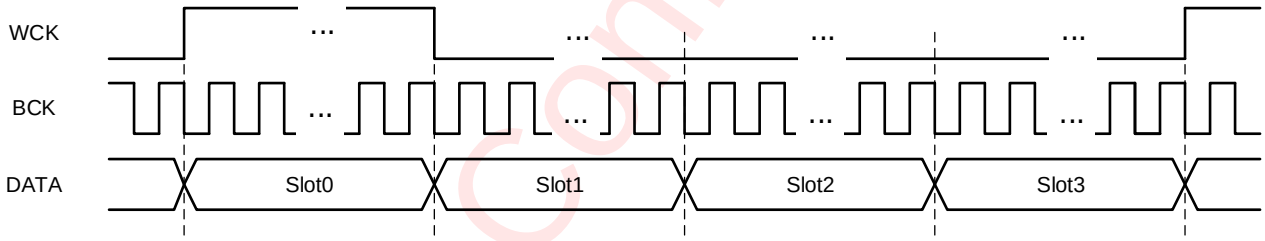


Figure 12 TDM Timing

Note: The high level pulse width of WCK signal can be one slot time or one period of BCK.

DIGITAL AUDIO PROCESSING

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- HDCC
- Hardware AGC
- Volume control
- Mute

The signal processing flow in the DAP (Digital Audio Processor) is illustrated in the following figure.

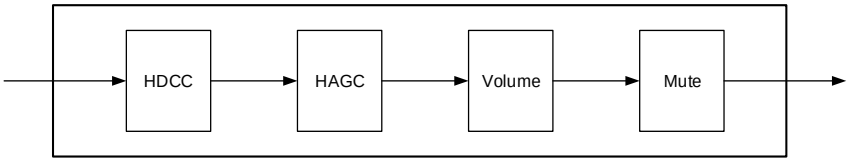


Figure 13 Block Diagram of DAP

HDCC

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

HAGC

System output power tends to be more than rated power of speaker, such as in the 10.25V power supply, as for 8Ω speaker, the maximum undistorted power is about 5.2W, but many speakers' rated power is about 1W, if there is no output power control, the overload signal can cause damage to the speaker. The audio power amplifier with hardware AGC can protect the speaker effectively, When the output power is not exceeding the setting threshold, the hardware AGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the hardware AGC module will reduce the internal gain of amplifier and restricts the output power under the setting threshold.

VOLUME CONTROL

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0db to -96db with 0.094db/step

MUTE

This module performs mute control for the audio stream

DC-DC CONVERTER

This device using smart boost converter generates the amplifier supply rail. The DC-DC converter can work in different mode via BSTCTRL1.BST_MODE:

- **Pass-through mode**: the voltage of VBAT is transparently passed to output of converter VBST
- **Smart boost 1 mode**: the output voltage can be switch between VBAT and programmed output voltage according to the input audio level.
- **Smart boost 2 mode**: the output voltage can be dynamically adjusted according to the amplifier output's signal swing requirements in order to maximize efficiency.

Pass-through mode

The internal boost circuit is not working; the voltage of VBAT is passed to VBST directly.

Smart boost 1 mode

Smart boost 1 mode can dynamically turn on or off the boost according to the amplifier output's signal swing requirements in order to maximize efficiency.

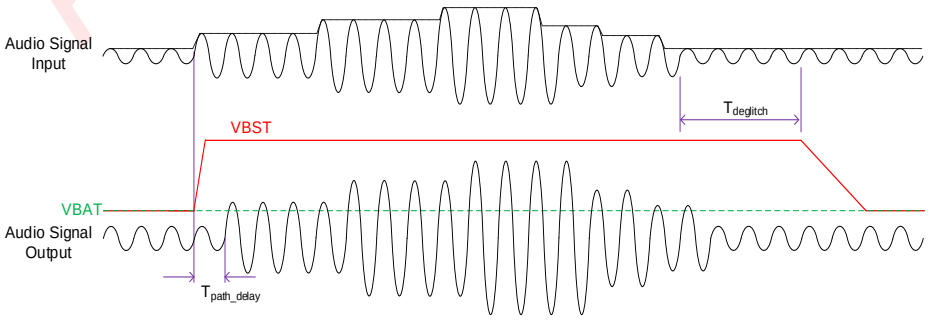


Figure 14 Boost Circuit Behavior in Smart Boost 1 Mode

Smart boost 2 mode

The boost circuit works dynamically according to the output audio level. When the level of output audio signal is below the setting threshold, the boost circuit will not be activated. Till the level of output audio signal is above the threshold, the boost circuit starts to work before the audio stream arriving at amplifier power stage. The output voltage VBST is dynamically adjusted to meet the requirement of output audio signal.

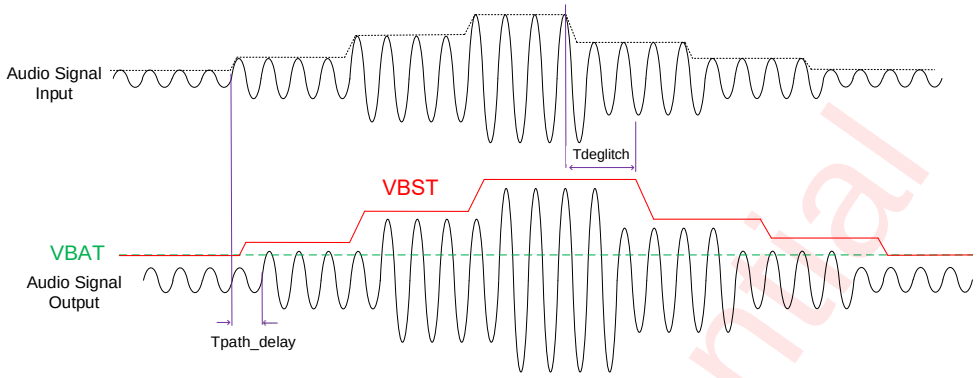


Figure 15 Boost Circuit Behavior in Smart Boost 2 Mode

PROTECTION MECHANISMS

Over Voltage Protection (OVP)

The boost circuit has integrated the over voltage protection control loop. When the output voltage VBST is above the threshold, the boost circuits will stop working, until the voltage of VBST going down and under the normal fixed working voltage.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

Over Current (short) Protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to VBST /GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

Under Voltage Detection (UVL)

The interrupt bit SYSINT.UVLI will be set to 1 when under voltage occurs, which will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected under-voltage event has taken place.

Direct-Current Detection (DCD)

The interrupt bit SYSINT.ODCI will be set to 1 when there is DC current on the output and then turn off the output, which will be cleared by a read operation of SYSINT register. Usually the SYSINT. ODCI bit can be used to check whether an unexpected direct-current event has taken place.

BROWN OUT PROTECTION

The brown out protection (BOP) function reduces the device power consumption in order to prevent the system from collapsing when the battery is in a weakened condition. There is a total of eight low battery voltage thresholds, which divide the low battery condition into eight levels (as shown in the below table). When battery voltage drops in BOP level, the BOP function would either applies smooth digital gain reduction or limits the peak input current of boost to help prevent the system battery supply form drooping. The max attenuation level of digital gain and the limitation of boost peak input current are individually configurable for each BOP level. The digital gain and the boost peak current limit can be automatically recovered to its programmed value after VBAT rises.

Threshold	Battery Condition
BOP Level 0	VBAT > Low_bat_avth1
BOP Level 1	Low_bat_avth2 < VBAT <= Low_bat_avth1
BOP Level 2	Low_bat_avth3 < VBAT <= Low_bat_avth2
BOP Level 3	Low_bat_avth4 < VBAT <= Low_bat_avth3
BOP Level 4	Low_bat_avth5 < VBAT <= Low_bat_avth4
BOP Level 5	Low_bat_avth6 < VBAT <= Low_bat_avth5
BOP Level 6	Low_bat_avth7 < VBAT <= Low_bat_avth6
BOP Level 7	VBAT <= Low_bat_avth7

NOISE GATE

The noise gate functionality allows the amplifier to stop switching in order to reduce power consumption during passages of ultra-low input signal, When the input audio signal keep smaller than the noise gate threshold for more than deglitch time, the amplifier enters noise-gated condition, then the amplifier's output (VOP/VON) switching is disabled and tied to a programmable value (Hi-Z / Low). This eliminates the power consumption of the output switching, produces a state of very low idle noise and idle current. When exiting the noise-gated condition, the simplifier immediately resumes normal operation.

MULTI-LEVEL POWER DRIVING(MPD)

In order to operate with lowest achievable noise floor, the multi-level MPD maintains the analog-gain as low as possible based on the input audio signal Din. The digital-gain is synchronously adjusted to compensate for analog-gain so that the total-gain of audio path always remains constant.

BATTERY VOLTAGE MONITORING

The device monitors the voltage on the VBAT pin, which is most commonly the battery for the system. The battery voltage level is available via bits VBAT_DET in the Battery Supply Voltage register VBAT. Status bits VBAT_DET can be used to calculate the battery voltage. The battery voltage level V_{VBAT} is:

$$V_{VBAT} = \frac{VBAT\_DET}{2^{10} - 1} \times 6.025V$$

For example, if VBAT_DET = 1001100011, the battery voltage level V_{VBAT} is equal to 3.6V.

VBST VOLTAGE MONITORING

The device monitors the voltage on the VBST pin, which is most commonly the VBST voltage level for the system. The VBST pin voltage level is available via bits VBST_DET in the Power Supply Voltage monitor register VBST. Status bits VBST_DET can be used to calculate the VBST voltage. The VBST voltage level V_{VBST} is:

$$V_{VBST} = \frac{VBST\_DET}{2^{10} - 1} \times 14.13V$$

For example, if VBST_DET = 1001100011, the VBST voltage level V_{VBST} is equal to 8.44V.

DIE TEMPERATURE MONITORING

The device monitors the die temperature and the result is available via bits TEMP_DET in the Temperature register TEMP. The TEMP_DET is a two's complement value. For example, if TEMP_DET = 00011001, the die temperature is 25°C.

CURRENT SENSING

The device provides speaker current sense for real time monitoring of loudspeaker behavior. Current sensing is not disturbed by capacitance(<1nF) on the output lines or on the long speaker tracks. The current sensing transfer function I_{SNS} is:

$$I_{SNS} = \frac{D_{OUT}}{2^{15} - 1} \times 2.92A$$

D_{OUT}: the current sense I²S output stream

VOLTAGE SENSING

The device provides speaker voltage sense for real time monitoring of loudspeaker behavior. The voltage sensing transfer function V_{SNS} is:

$$V_{SNS} = \frac{D_{OUT}}{2^{15} - 1} \times 23.4V$$

D_{OUT}: the voltage sense I²S output stream

AMPLIFIER TRANSFER FUNCTION

The transfer function from the input to the amplifier PWM output (when no gain and attenuation is applied in digital signal domain) is:

$$V_o = AMP\_NORM\_V \times D_{in}$$

D_{in}: the level of input signal with a range from -1 to +1

AMP_NORM_V: the equivalent amplifier output voltage when D_{in} is 1. In receiver mode the AMP_NORM_V is 10dBV, in speaker mode it's 19dBV.

RECEIVER MODE

The device built-in Receiver mode is easy to realize the Speaker and Receiver combo applications, it saves the system cost and board space. If the receiver magnification is one times, the noise floor will be 7.2μV. Speaker and Receiver combo applications can be realized without changing any hardware.

When the device is set to receiver mode, the power supply of Class D driver stage is from VBAT directly without boost.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode plus at 1MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the AD pin according to the following table: The AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7-bit) through 0x37(7-bit).

AD2	AD1	Address(7-bit)
GND	GND	0x34
GND	VDDIO	0x35
VDDIO	GND	0x36
VDDIO	VDDIO	0x37

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

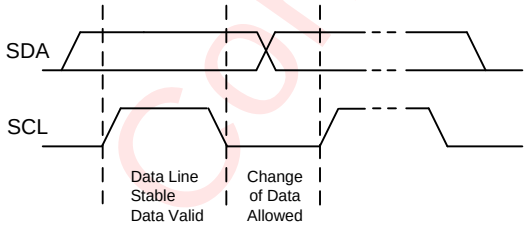


Figure 16 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

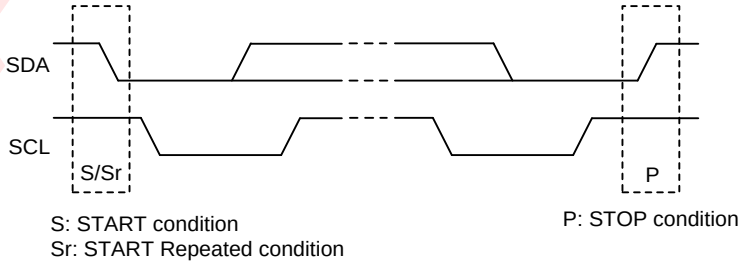


Figure 17 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

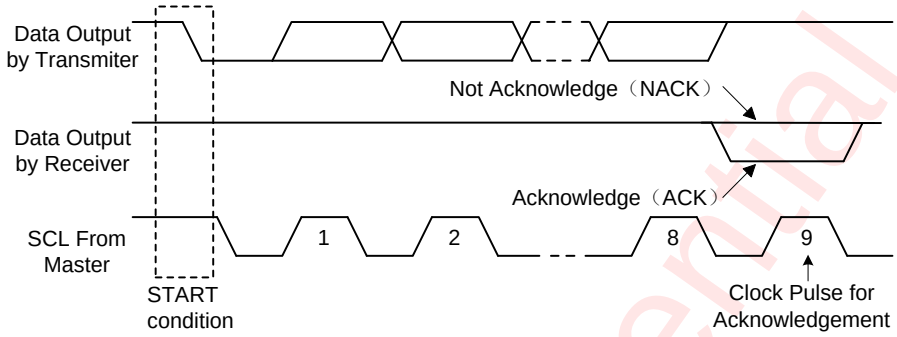


Figure 18 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends high data byte of 16-bit data to be written to the addressed register

g) Slave sends acknowledge signal

h) Master sends low data byte of 16-bit data to be written to the addressed register

i) Slave sends acknowledge signal

j) If master will send further 16-bit data bytes, the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g)

k) Master generates STOP condition to indicate write cycle end

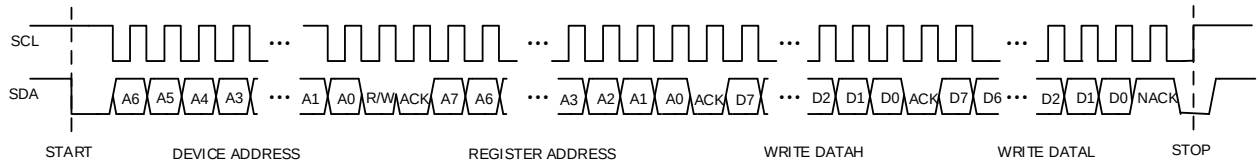


Figure 19 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 16-bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 16-bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.

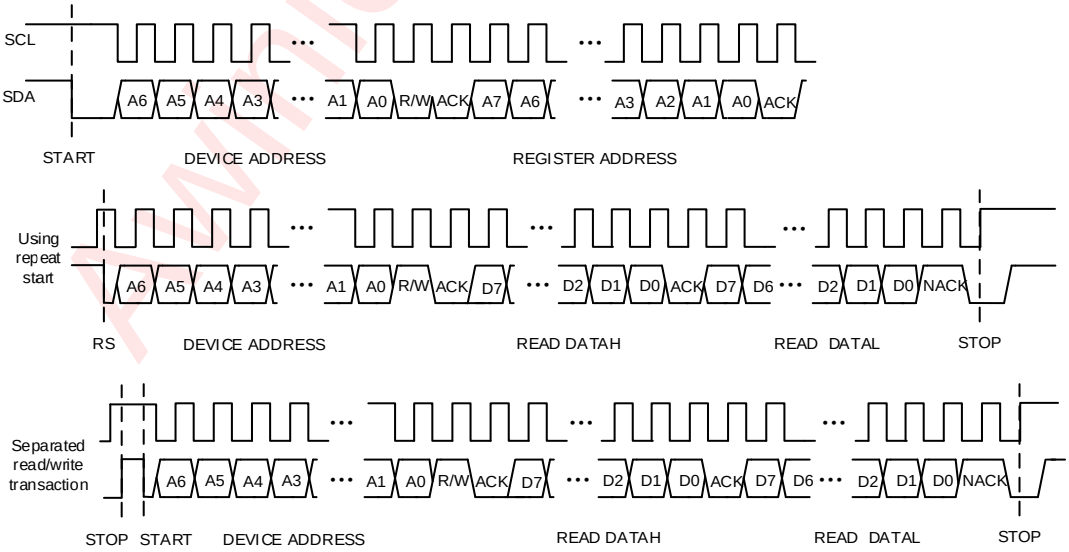


Figure 20 I²C Read Byte Cycle

REGISTER MAP

REGISTER DESCRIPTION

REGISTER LIST

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	ID	RO	IDCODE															
0x01	SYSST	RO	OVP2S	UVLS	ADPS		BSTOCS	OVPS	BSTS	SWS	ODCS		NOCLKS	CLKS	OCDS	BROWN_OUTS	OTHS	PLLS
0x02	SYSINT	RC	OVP2I	UVLI	ADPI		BSTOCI	OVPI	BSTI	SWI	ODCI		NOCLKI	CLKI	OCDI	BROWN_OUTI	OTHI	PLLI
0x03	SYSINTM	RW	OVP2M	UVLM	ADPM		BSTOCM	OVPM	BSTM	SWM	ODCM		NOCLKM	CLKM	OCDM	BROWN_OUTM	OTHM	PLLM
0x04	SYSCTRL	RW	ULS_HMUTE	I2SRXEN	I2STXEN	BOP_EN	RMSE	HAGCE	HDCCE	HMUTE	RCV_MODE	I2SEN	WSINV	BCKINV	IPLL		AMPPD	PWDN
0x05	SYSCTRL2	RW	EN_MPD		INTMODE	INTN	VOL_ADD		VOL									
0x06	I2SCTRL1	RW	TX_EDGE	CFSEL			CHSEL		I2SMD		I2SFS		I2SBCK		I2SSR			
0x07	I2SCTRL2	RW	IV2CH	SLOT_NUM			I2S_TX_SLOTVLD				I2S_RXR_SLOTVLD				I2S_RXL_SLOTVLD			
0x08	I2SCTRL3	RW		RCV_GAIN0				SPK_GAIN0			FSYNC_TYPE	DOHZ	DRVSTREN	I2SDOSEL	I2SCHS	LPBK		ULS_MODE
0x09	DACCFG1	RW	RVTH								AVTH							
0x0A	DACCFG2	RW	ATTH															
0x0B	DACCFG3	RW	RTTH															
0x0C	DACCFG4	RW									HOLDTH							
0x12	PWMCTRL2	RW		SET_UVLO														
0x21	VBAT	RO									VBAT_DET							

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x22	TEMP	RO							TEMP_DET									
0x23	VBST	RO							VBST_DET									
0x60	BSTCTRL1	RW	BST_MODE			BST_RTH						BST_ATH						
0x61	BSTCTRL2	RW	BST_IPEAK				BST_TDEG				BST_VOUT_SET							

DETAILED REGISTER DESCRIPTION

ID: (Address 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:0	IDCODE	RO	Chip ID will be returned after read. All configuration registers will be reset to default Value after 0x55aa is written	0x2308

SYSST: (Address 01h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	OVP2S	RO	Boost OVP2 status indicator 0: Normal 1: OVP	0
14	UVLS	RO	VBAT under voltage indicator 0: Normal 1: UVLO	0
13	ADPS	RO	Boost Adaptive status. 0: Pass Through 1: Boost	0
12	Reserved	RO	Not used	0
11	BSTOCS	RO	Boost over current indicator 0: Normal 1: Over Current	0
10	OVPS	RO	Boost OVP status indicator 0: Normal 1: OVP	0
9	BSTS	RO	Boost start up finished. 0: Not finished 1: Finished	0
8	SWS	RO	Amplifier switching status. 0: Not switching 1: Switching	0
7	ODCS	RO	Attack DC_PRO function status indicator 0: normal 1: ODC	0
6	Reserved	RO	Not used	0
5	NOCLKS	RO	The reference clock of PLL is not available 0: Clock Ok 1: No Clock	0

4	CLKS	RO	Internal clocks status flag, status 0 means At least one clock are not stable 0: Not stable 1: Stable	0
3	OCDS	RO	Over current status in amplifier 0: Normal 1: OC	0
2	BROWN_OUTS	RO	Brownout protection status 0: Not Activated 1: Activated	0
1	OTHS	RO	Die Temperature is higher than 150°C 0: Normal 1: OT	0
0	PLLS	RO	PLL locked status. 0: Unlocked 1: Locked	0

SYSINT: (Address 02h)

Bit	Symbol	R/W	Description	Default
15	OVP2I	RC	Interrupt indicator for OVP2S.	0
14	UVLI	RC	Interrupt indicator for Power On and UVLS	0
13	ADPI	RC	Interrupt indicator for ADPS	0
12	Reserved	RC	Not used	0
11	BSTOCI	RC	Interrupt indicator for BSTOCS.	0
10	OVPI	RC	Interrupt indicator for OVPS.	0
9	BSTI	RC	Interrupt indicator for BSTS.	0
8	SWI	RC	Interrupt indicator for SWS.	0
7	ODCI	RC	Interrupt indicator for oRodc	0
6	Reserved	RC	Not used	0
5	NOCLKI	RC	Interrupt indicator for NOCLKS.	0
4	CLKI	RC	Interrupt indicator for CLKS.	0
3	OCDI	RC	Interrupt indicator for OCDS	0
2	BROWN_OUTI	RC	Interrupt indicator for BROWN_OUTS	0
1	OTHI	RC	Interrupt indicator for OTHS.	0
0	PLLI	RC	Interrupt indicator for PLLS.	0

SYSINTM: (Address 03h)

Bit	Symbol	R/W	Description	Default
15	OVP2M	RW	Interrupt mask for OVP2I	1

14	UVLM	RW	Interrupt mask for UVLI.	1
13	ADPM	RW	Interrupt mask for ADPI	1
12	Reserved	RW	Not used	0
11	BSTOCM	RW	Interrupt mask for BSTOCI.	1
10	OVPM	RW	Interrupt mask for OVPI	1
9	BSTM	RW	Interrupt mask for BSTI.	1
8	SWM	RW	Interrupt indicator for SWI.	1
7	ODCM	RW	Interrupt mask for oRodc	1
6	Reserved	RW	Not used	0
5	NOCLKM	RW	Interrupt mask for NOCLKI.	1
4	CLKM	RW	Interrupt mask for CLKI.	1
3	OCDM	RW	Interrupt mask for OCDI.	1
2	BROWN_OUTM	RW	Interrupt mask for BROWN_OUTI	1
1	OTHM	RW	Interrupt mask for OTHI.	1
0	PLLM	RW	Interrupt mask for PLLI.	1

SYSCTRL: (Address 04h)

Bit	Symbol	R/W	Description	Default
15	ULS_HMUTE	RW	Ultrasonic data path mute control 0: Normal 1: Mute	1
14	I2SRXEN	RW	Disable/Enable I2S receiver module 0: Disable 1: Enable	1
13	I2STXEN	RW	Disable/Enable I2S transmitter module 0: Disable 1: Enable	0
12	BOP_EN	RW	Enable/Disable Brownout protection module 0: Disable 1: Enable	0
11	RMSE	RW	Hardware AGC mode selection 0: Peak AGC 1: RMS AGC	0
10	HAGCE	RW	Disable/Enable Hardware AGC 0: Disable 1: Enable	0
9	HDCCE	RW	Disable/Enable Hardware DC Canceling module 0: Disable 1: Enable	1

8	HMUTE	RW	Disable/Enable Hardware mute module 0: Disable 1: Enable	1
7	RCV_MODE	RW	Receiver mode enable, active "1". 0: Speaker 1: Receiver	0
6	I2SEN	RW	Disable/Enable whole I2S interface module 0: Disable 1: Enable	0
5	WSINV	RW	I2S Left/Right channel switch control 0: Not switch 1: Switch	0
4	BCKINV	RW	I2S bit clock invert control 0: Not invert 1: Inverted	0
3	IPLL	RW	PLL reference clock selection 0: BCK 1: WCK	0
2	Reserved	RW	Not used	0
1	AMPPD	RW	Amplifier power down control bit, Power Down until system configuration finished 0: Working 1: Power Down	1
0	PWDN	RW	System power down control bit 0: Working 1: Power Down	1

SYSCTRL2: (Address 05h)

Bit	Symbol	R/W	Description	Default
15	EN_MPD	RW	Disable/Enable MPD multi stage power mode, Gain will be automatically adjusted only when EN_MPD is high. It can enable the small-signal detection or not, based on the audio input, so that the quiescent current could be reduced and the noise level will be smaller. 0: Disable 1: Enable	1
14	Reserved	RW	Not used	0
13	INTMODE	RW	Interrupt pad INTN output mode selection 0: Open-drain 1: Push&Pull	0

12	INTN	RW	Interrupt pad INTN pin-source selection 0: SYSINT 1: SYSST	0
11:10	VOL_ADD	RW	Vol positive gain value 00: 0dB 01: +6dB 10: +12dB reserved	0
9:0	VOL	RW	Volume control, from 0 to -96.2259375dB, in unit of -0.0940625dB	0

I2SCTRL1: (Address 06h)

Bit	Symbol	R/W	Description	Default
15	TX_EDGE	RW	I2S TX clock edge selection 0: negedge 1: posedge	0
14:12	CFSEL	RW	I2S legacy path output data selection 000: HAGC 010: ivbt_txdout 011: iv_txdout 101: ivbt_dout_24k Others: reserve	0
11:10	CHSEL	RW	Left/right channel selection for I2S input 00: Reserved 01: Left 10: Right 11: Mono	1
9:8	I2SMD	RW	I2S interface mode selection 00: Philip Standard 01: MSB justified 10: LSB justified 11: Reserved	0
7:6	I2SFS	RW	I2S data resolution selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits	3
5:4	I2SBCK	RW	I2S BCK mode 00: 32*fs 01: 48*fs 10: 64*fs 11: Reserved	2

3:0	I2SSR	RW	I2S interface sample rate configuration 0000: 8 kHz 0001: 11.025 kHz 0010: 12 kHz 0011: 16 kHz 0100: 22.05 kHz 0101: 24 kHz 0110: 32 kHz 0111: 44.1 kHz 1000: 48 kHz 1001: 96 kHz 1010: 192 kHz Others: Reserved	8

I2SCTRL2: (Address 07h)

Bit	Symbol	R/W	Description	Default
15	IV2CH	RW	I2S TX channel data packing mode control. When I2SBCK is set to 32*fs mode, Current & Voltage data could be transmitted to I2S Left & Right channels by Using Special Mode. 0: Legacy 1: Special	0
14:12	SLOT_NUM	RW	I2S TDM mode control. 000: I2S mode 001: TDM1s 010: TDM2s 011: TDM4s 100: TDM6s 101: TDM8s 110: TDM16s 111: Reserved	0
11:8	I2S_TX_SLOTVLD	RW	TX slot selection, data will be sent to one of the slots. 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 …… 1111: Slot 15	0
7:4	I2S_RXR_SLOTVLD	RW	RX right channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 …… 1111: Slot 15	1

3:0	I2S_RXL_SLOTVLD	RW	RX left channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 …… 1111: Slot 15	0

I2SCTRL3: (Address 08h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14:12	RCV_GAIN0	RW	Receiver Mode gain setting 010: 6dB 011: 10.4dB 100: 12.5dB 101: 17dB 110: 17dB 111: 17dB Others: Reserved	4
11	Reserved	RW	Not used	0
10:8	SPK_GAIN0	RW	Speaker Mode gain setting 010: 12dB 011: 15dB 100: 18.5dB 101: 19dB 110: 20dB 111: 20dB Others: Reserved	5
7	FSYNC_TYPE	RW	Audio Frame synchronization signal (WCK) pulse width configuration 0: One-slot 1: One-bck	0
6	DOHZ	RW	Unused channel Data control, when it is set to 0, all Channels are available. Otherwise Unused channel is set to be HiZ. 0: All 1: HiZ	1
5	DRVSTREN	RW	I2S_DATAO PAD driving strength setting 0: 4mA 1: 12mA	1
4	I2SDOSEL	RW	I2S unused channel data selection 0: Zeros 1: TX Data	0

3	I2SCHS	RW	I2S Tx Channel selection 0: Left 1: Right	0
2:1	LPBK	RW	I2S data Loopback control bits 00: Disable 01: Far-Back 10: Near-Back 11: Reserved	0
0	ULS_MODE	RW	Ultrasonic mode control 0: Low Pass 1: TDM	0

DACCFG1: (Address 09h)

Bit	Symbol	R/W	Description	Default
15:8	RVTH	RW	Release Amplitude threshold, in percent of signal full scale	0x39
7:0	AVTH	RW	Attack Amplitude threshold, in percent of signal full scale RMSE = 0 (Peak AGC): Po= ((i/256*Gain)**2)/RLoad/2 RMSE = 1 (RMS AGC): Po=(i/256)*(Gain**2)/RLoad i is the register value, default 0x40 Gain is the Speaker Gain can be configured. RLoad is 8Ω	0x40

DACCFG2: (Address 0ah)

Bit	Symbol	R/W	Description	Default
15:0	ATTH	RW	Attack time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	0x0030

DACCFG3: (Address 0bh)

Bit	Symbol	R/W	Description	Default
15:0	RTTH	RW	Release time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	0x01E0

DACCFG4: (Address 0ch)

Bit	Symbol	R/W	Description	Default
15:8	Reserved	RW	Not used	0

7:0	HOLDTH	RW	Hold time before release control, in unit of about 1.33ms 0: Reserved n: n*1.33ms	0x64

PWMCTRL2: (Address 12h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14:13	SET_UVLO	RW	The UVLO threshold voltage settings as follow: 00: 2.1V 01: 2.2V 10: 2.3V 11: 2.4V	3
12:0	Reserved	RW	Not used	0

VBAT: (Address 21h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	VBAT_DET	RO	Detected Voltage of battery, and the full range is 6.025V V_BATS=(VBAT)/1023×6.025	0x2EB

TEMP: (Address 22h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	TEMP_DET	RO	Detected Die Temperature (Two's Complement), typical Values are as follows. 0x3D8 : -40 °C 0x00 : 0 °C 0x01 : 1 °C 0x19 : 25 °C 0x37 : 55 °C Please convert it to decimal number.	0x019

VBST: (Address 23h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	VBST_DET	RO	Detected Voltage of VBST, and the full range is 14.13V VBST=(VBST_DET)/1023×14.13	0x13E

BSTCTRL1: (Address 60h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:14	BST_MODE	RW	BOOST mode selection. 00: Pass Through 10: Smart Boost 1 11: Smart Boost 2	0x3
13:7	BST_RTH	RW	Smart boost release threshold setting, When signal is above over the threshold, the voltage of VBST will be raised up higher than VDD in smart boost mode Release threshold = ((BST_RTH /128 * SET_GAIN)**2)/2/Rload, which SET_GAIN represents actual gain of Class-D.	40
6:0	BST_ATH	RW	Smart boost attack threshold setting. When signal is below the threshold, the voltage of VBST will be equal to VDD in smart boost mode. Attack threshold = ((BST_ATH/128 * SET_GAIN)**2)/2/Rload, which SET_GAIN represents actual gain of Class-D.	38

BSTCTRL2: (Address 61h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:12	BST_IPEAK	RW	Boost peak current limiter threshold 0000: 1.5A 0001: 1.75A 0010: 2.0A 0011: 2.25A 0100: 2.5A 0101: 2.75A 0110: 3.0A 0111: 3.25A 1000: 3.5A 1001: 3.75A 1010: 4A 1011: 4.25A others: Reserved	5

11:8	BST_TDEG	RW	Smart Boost small signal level detection deglitch time 0000: 0.50 ms 0001: 1.00 ms 0010: 2.00 ms 0011: 4.00 ms 0100: 8.00 ms 0101: 10.7 ms 0110: 13.3 ms 0111: 16.0 ms 1000: 18.6 ms 1001: 21.3 ms 1010: 24.0 ms 1011: 32.0 ms 1100: 64.0 ms 1101: 128 ms 1110: 256 ms 1111: 1200 ms	11
7:0	BST_VOUT_SET	RW	BOOST max output voltage control bits (41.7mV/Step) 00000000: 3.5V 00000001: 3.5417V 00000010: 3.5834V 00000011: 3.6251V 00000100: 3.6668V 00000101: 3.7085V …... 10101000: 10.5056V others: Reserved	0xA2

APPLICATION INFORMATION

EXTERNAL COMPONENTS

BOOST INDUCTOR SELECTION

Inductance value is limited by the boost converter's internal loop compensation, a large L_{SW} will reduce the phase margin of the DC-to-DC converter. Also, the inductor should have low core loss at 1MHz (Min.) and low DCR for better efficiency under all operating conditions, the recommended value of inductor is 1μH.

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, inductance value will decline since the magnetic core begins to saturate; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. The inductor saturation current rating could to be considered with the following equation:

$$I_{L\_PEAK} = \frac{2 * P_{OUT}}{\eta * VBAT} + \frac{VBAT * (VBST - VBAT)}{2 * L_{SW} * F_{BST} * VBST}$$

Following is the inductor selection reference for typical speaker impedances.

V_{VBAT} (V)	VBST (V)	R_L (Ω)	Efficiency (%)	P_{OUT} (W)	I_{L_PEAK} (A)	I_{SAT_min} (A)
4.2	10.25	8	78%	5.2	3.79	4.0
4.2	10.25	6	77%	5.4	3.96	4.2

BOOST CAPACITOR SELECTION

Boost output capacitor is usually within the range 0.1μF~47μF. The ceramic capacitors with low ESR are recommended for low ripple voltage which is determined as following equation:

$$\Delta VBST = \frac{(VBST - VBAT) * I_{OUT}}{\eta * VBST * F_{BST} * C_{OUT}} + \left(\frac{I_{OUT} * VBST}{VBAT} + \frac{VBAT * (VBST - VBAT)}{2 * L_{SW} * F_{BST} * VBST}\right) * R_{C\_ESR}$$

Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the material, size, capacitor voltage, and capacitance values. It is suggested to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically $BaTiO_3$), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance.

Please notice the DC bias characteristics when selecting capacitors. For typical applications, it is necessary to ensure that the residual capacitance is higher than 3.3μF**.** Take the following capacitances as the output capacitor of boost for example:

Value	Material	Size (mm^3)	Rated Voltage	Quantity	Value@10.25V
10μF	X5R	1.00×0.50×0.50 (0603)	25V	2	3.6μF
22μF	X5R	2.00×0.80×0.85 (0805)	25V	1	3.7μF

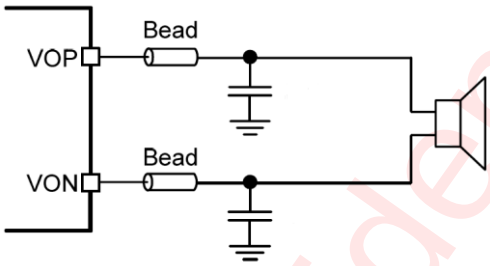
SUPPLY DECOUPLING CAPACITOR

The device is a high-performance audio amplifier that requires adequate power supply decoupling. A 1μF low equivalent-series-resistance (ESR) ceramic capacitor is recommended. This choice of capacitor and

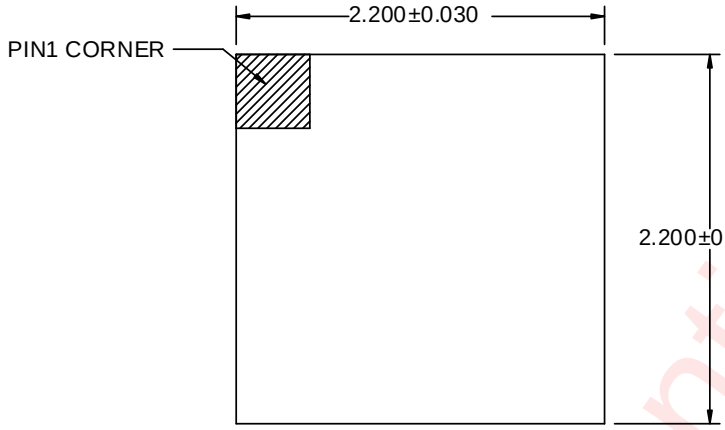
placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 1μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any drop in the supply voltage.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

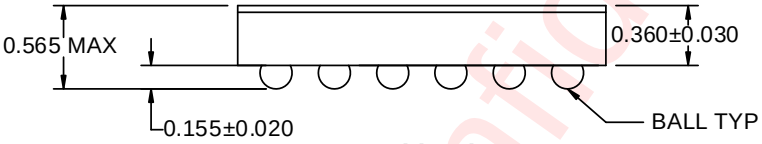
If the PA is close to the EMI sensitive circuits and/or there are long leads from amplifier to speaker, a ferrite bead filter could be used, and placed as close as possible to the output pins of the PA. When choosing a ferrite bead, select a ferrite bead with adequate current rating to prevent distortion of the output signal. In addition, a 0.1nF ceramic capacitor is typically recommended, and its rated voltage should be above 25V.



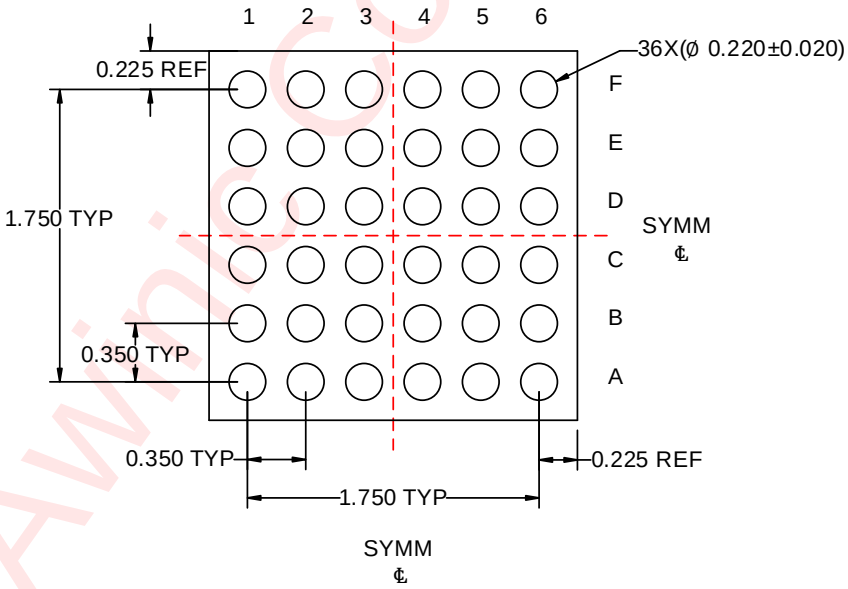
PACKAGE DESCRIPTION



Top View



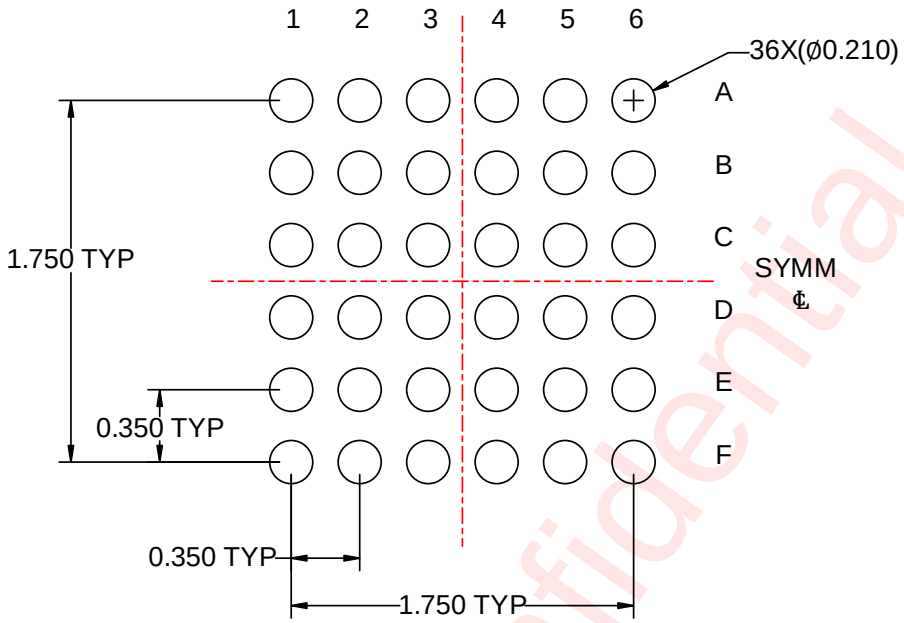
Side View

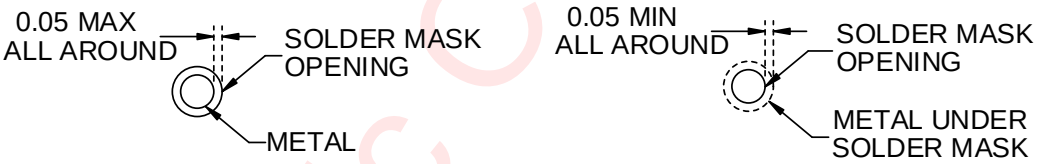


Bottom View

Unit:mm

LAND PATTERN DATA





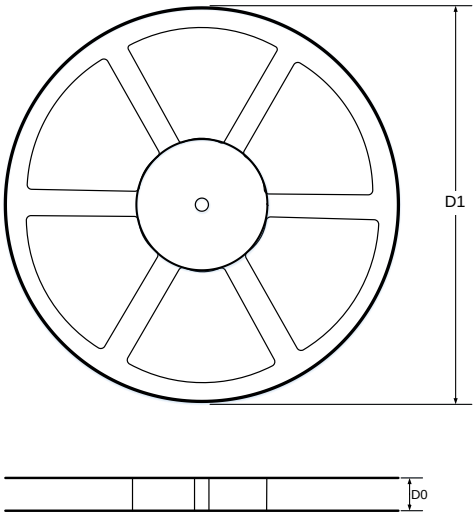
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

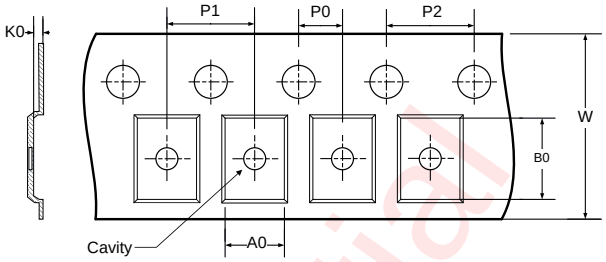
Unit: mm

TAPE AND REEL INFORMATION

REEL DIMENSIONS

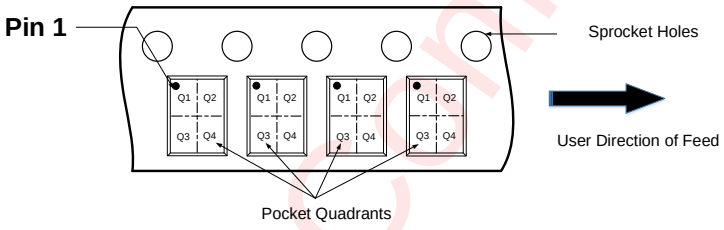


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179	9.2	2.33	2.33	0.66	2	4	4	8	Q1

All dimensions are nominal

REVISION HISTORY

Version	Date	Change Record
V1.0	Jan.2024	Officially Released
V1.1	May.2024	Add max value of EC and AMR, update application diagram
V1.2	Feb.2025	Add the description of the min/max value in the EC table Modify the default timing of I2S DATAO sending at the falling edge of BCK Modify the timing of DVDD and VDDIO

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