XPA5355

16-V Input, 20-A, 3mΩ R_{DS_ON}, Hot-Swap Efuse

FEATURES

- 2.7V to 16V Operating Input Range
- Maximum 20A Output Current
- Integrated 3mΩ Power FET
- Adjustable Over-current Limit and Fault Regulation Time
- Adjustable Short-circuit Current Limit
- 3.3V LDO Output
- ±1% Current Monitor Accuracy
- Fast Response (<200ns) for Short Protection
- PG Detector and FLTB Indication
- PG De-assert Low at VIN = 0
- Input-to-Output Short-Circuit Detection
- External adjustable Soft Start (SS)
- Programmable LOADEN Blanking Time
- Configurable Input Over-Voltage (OV) Threshold
- Under-Voltage Lockout (UVLO)
- Output Short-circuit Protection (SCP)
- Thermal Protection (OTP)
- Efuse Health Reporting
- Available in TLGA (4mmx4mm)Package

APPLICATIONS

- Servers
- Hot Swap
- Laptops
- Disk Drives

DESCRIPTION

The XPA5355 is a hot-swap/Efuse device designed to protect its load circuitry from input transients. It also protects the input from unwanted shorts and transients coming from the output.

During start-up, the inrush current is limited by the output slew rate, which is in turn controlled by an external capacitor on pin SS.

The maximum load current is limited by a built-in current-sense circuitry, and a low-power resistor from ISET to ground sets the current limit.

The gate of the power device is driven by a built-in charge pump, enabling a very low RDS_ON of 3mΩ.

Connect a resistor from IMON to ground to generate a voltage signal that is proportional to the current through the power device.

Full protection features include current limit (OCP), short-circuit protection (SCP), thermal shutdown (TSD), damaged MOSFET detection, over-voltage protection (OVP), and under-voltage lockout (UVLO).

XPA5355 is available in TLGA-26 (4mmx4mm) package.

FUNCTIONAL BLOCK DIAGRAM

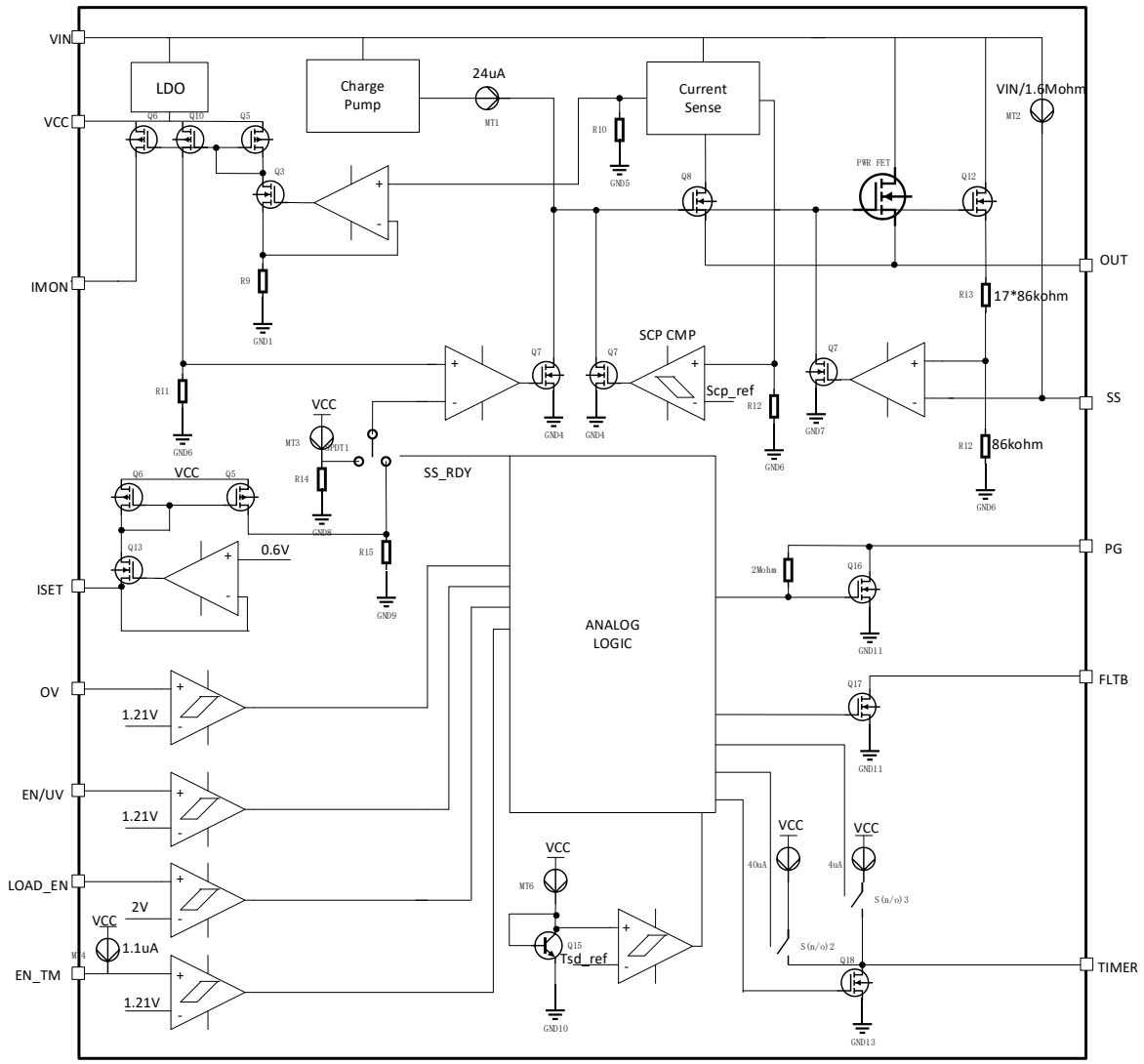


Fig.1 Functional Block Diagram

TYPICAL APPLICATION

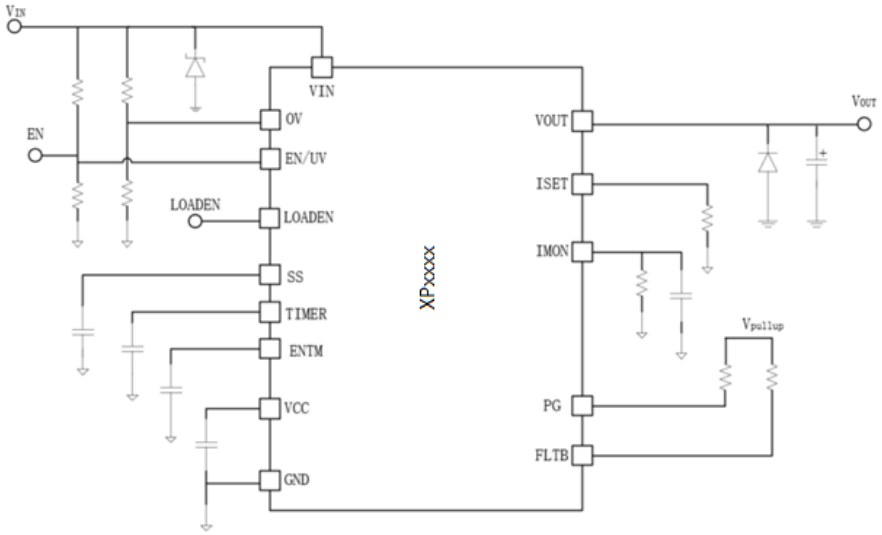


Fig. 2 Typical Application Diagram of XPA5355

REVISION HISTORY

Release	Rev	Changes	Date
Released	1.0	Finalized	2025.02

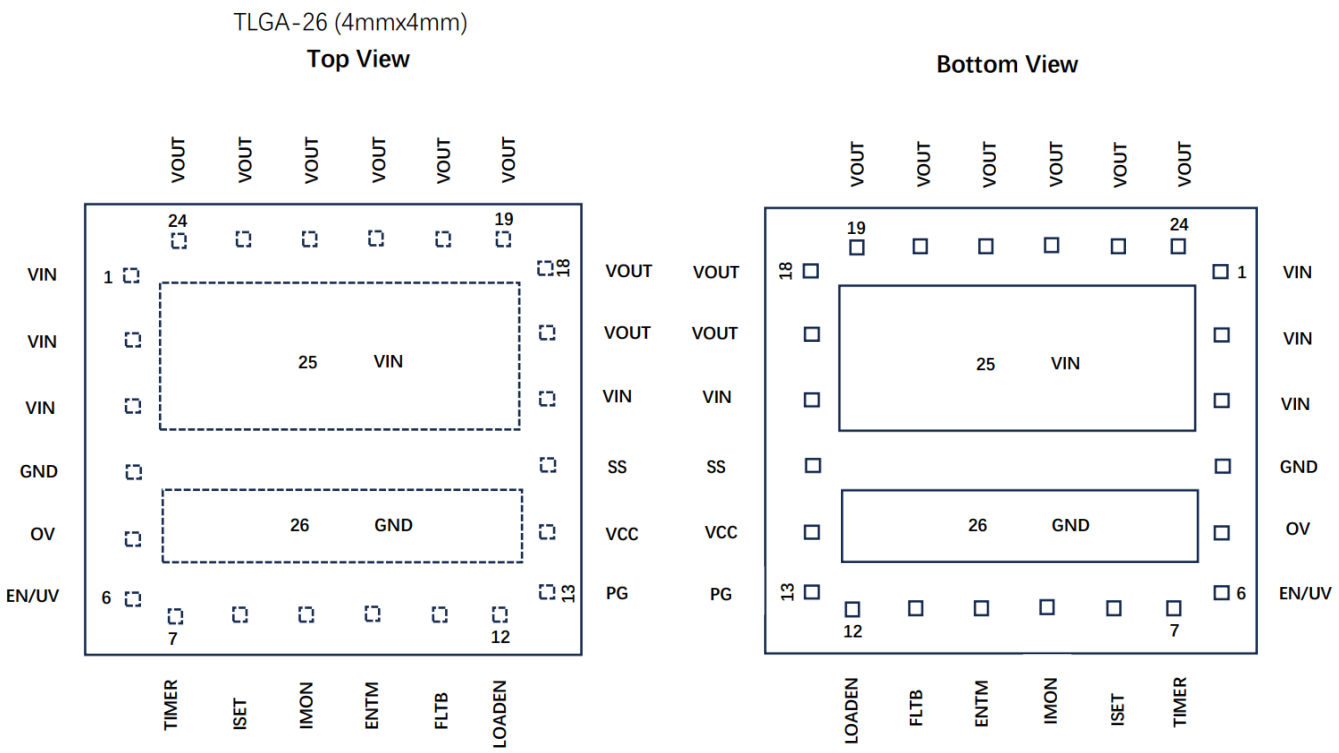
ORDERING INFORMATION

Part Number	Output Current (A)	VOUT (V)	Top Marking	MPQ
XPA5355G26R	20	E-fuse	A5355	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN CONFIGURATION AND DESCRIPTION

TLGA-26 (4mmx4mm)



Pin Description

Pin Number	Pin Name	Description
1,2,3,16,25	VIN	Main power input.
4,26	GND	Ground.
5	OV	Over-voltage enable input. OV=high turns off the internal MOSFET. Set the OV disable threshold by connecting an external resistive divider to OV pin.
6	EN/UV	Enable control and input UVLO setting. EN is the control input that turns on/off the device, including the logic and power FET. EN=high turns on the device. EN=low turns it off. Input UVLO threshold is set by connecting the tap-point of a resistive divider between VIN and GND. EN doesn't control the VCC LDO. Don't float EN/UV.
7	TIMER	Timer set. Hot-swap insertion delay time and fault time-out period are set by an external capacitor on pin TIMER.
8	ISET	Current Limit set. Over-current limit is set by connecting a resistor from ISET to GND.
9	IMON	Output current monitor. Connecting a resistor (R_{IMON}) from IMON to GND to generate a voltage proportional to the power FET current. A capacitor of no less than 10nF should be placed in parallel with R_{IMON}.
10	ENTM	Sets the LOADEN blanking time. Connect an external capacitor to ENTM pin to set the LOADEN blanking time. Once EN is active, the timer starts and the LOADEN de-assertion is blanked. The device shuts down in case of a fault or EN low condition, however, LOADEN low alone during the blanking time is not enough to turn off the device.

11	FLTB	Fault bar. FLTB is an open-drain output, which is pulled up to an external power supply through a 10-100kΩ resistor. It latches following an over-current fault, short-circuit fault, over-temperature fault, OV fault, and FET health fault.
12	LOADEN	Load enable input. LOADEN and EN together can be used to turn on or off the power device (see Table 1). LOADEN is also used to shut down the device after the LOADEN blanking time expired but cannot turn XPA5355 back on by recycling LOADEN alone.
13	PG	Power good. Open-drain output, which should be pulled up to an external power supply through a 10-100kΩ resistor. PG=high indicates power good.
14	VCC	Output of internal 3.3V LDO. Place a 1uF capacitor close to VCC and GND.
15	SS	Soft start. The soft-start time of the VOUT is set by an external capacitor connected to SS. An internal circuit controls the slew rate of the output voltage at start-up. Min. soft-start time (1ms) is obtained by floating SS.
17-24	VOUT	Output voltage. VOUT is the output voltage controlled by XPA5355. A Schottky diode should be placed between VOUT and GND to absorb potential negative voltage spikes.

ABSOLUTE MAXIMUM RATINGS

VIN	DC	-0.3V ~ +20V
	1us	+24V
	25ns	+29V
VOUT		-0.3V ~ +20V
All other pins		-0.3V ~ +4.2V
Continuous power dissipation (T_A=25°C) (2)		5.16W
Junction temperature	T_J	–40°C to 150°C
Storage temperature	T_{stg}	–65°C to 155°C
Lead soldering temperature	T_s(10s)	280°C
Junction-to-ambient thermal resistance	θ_{JA}	24.2°C/W
Junction-to-case thermal resistance	θ_{JC}	10.5°C/W
ESD	HBM	2kV
ESD	CDM	1kV

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VIN	Input voltage	2.7	16	V
T_J	Operating junction temperature	-40	125	°C

Notes

(1) Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.

(2) The max allowable continuous power dissipation at any ambient temperature is defined by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Excessive die temperature will cause the device to go into thermal shutdown, hence protects it from permanent damage.

(3) The device is not guaranteed to function outside of its operating conditions.

ELECTRICAL SPECIFICATIONS

VIN = 12V, R_{ISET} = 12k, T_A = 25°C, unless otherwise noted

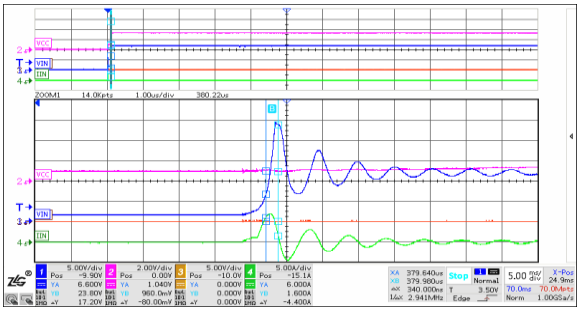
Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	EN = high, no load		1.5	1.8	mA
		Fault latch off		0.38	0.5	mA
		EN = 0, V_{IN} = 12V		0.38	0.5	mA
		EN = 0, V_{IN} = 16V		0.39	0.5	mA
Power FET						
On resistance	R_{DS_ON}	TJ = 25°C, Iout=2A, VIN=12V		2.8		mΩ
		TJ = 25°C, Iout=2A, VIN=2.7V		4.2		
		TJ = 125°C, Iout=2A, VIN=12V		3.8		
		TJ =125°C, Iout=2A, VIN=2.7V		5.4		
Off-state leakage current	I_{OFF}	V_{IN} = 16V, EN = 0V			5	μA
VCC Regulator and Under-Voltage Protection (UVLO)						
VCC regulator output voltage	VCC	I_{VCC}=0mA	3.1	3.37	3.5	V
		I_{VCC}=10mA		3.36		V
		I_{VCC}=20mA		3.35		V
VCC UVLO threshold, rising	VCC_{VTH_R}		2.26	2.46	2.66	V
VCC UVLO threshold, falling	VCC_{VTH_F}		2.1	2.3	2.5	V
VCC UVLO threshold, hysteresis	VCC_{HYS}			160		mV
Thermal Shutdown						
Shutdown temperature (4)	T_{STD}			150		°C
VIN Under-Voltage Protection (UVLO)						
VIN UVLO threshold, rising	VIN_{VTH_R}		2.46	2.56	2.66	V
VIN UVLO threshold, falling	VIN_{VTH_F}		2.3	2.4	2.5	V
VIN UVLO hysteresis	VIN_{HYS}			160		mV
LOADEN						
Low-level input voltage	V_{LOADEN_L}				0.8	V
High-level input voltage	V_{LOADEN_H}		2.0			V
ENTM (LOADEN Blanking Time)						
Upper threshold voltage	V_{ENTMRH}		1.19	1.21	1.23	V
Charge current	I_{ENTMCC}		0.8	1	1.2	μA
FET Short Detection						
FET drain-to-source short entry threshold	V_{DSTH_ENT}	V_{IN} = 12V	85%	90%	95%	VIN
		V_{IN} = 2.7V		VIN-0.5		V
FET drain-to-source short recovery threshold	V_{DSTH_EXT}	V_{IN} = 12V	70%	75%	80%	VIN
		V_{IN} = 2.7V		VIN-0.7		V
Gate-to-source short protection delay time (4)	T_{GS_ST}	V_{SS} > VCC-0.7	150	200	250	ms

Parameters	Symbol	Condition	Min	Typ	Max	Units
Current Limit						
ISET Voltage	V_{ISET}		-3%	0.6	+3%	V
OC internal current sensing gain		1/10 of IMON gain		2		μA/A
Current limit at normal operation	I_{OC_NOR}	R_{ISET} = 12k	-6%	24.5	+6%	A
Current limit at soft start	I_{OC_SS}	I_{OC_NOR}<20A, VOUT<90%VIN		80%* I_{OC_NOR}		A
		I_{OC_NOR}>20A, VOUT<90%VIN		15.6		A
OC regulation time at soft start	t_{OC_REG}			1.5		ms
Short-circuit current limit	I_{SC}			50		A
Short-circuit protection response time (4)	t_{SC}			200		ns
Current Monitor Output (IMON)						
IMON sense gain	A_{IMON}	I_{OUT} > 5A	19.8	20	20.2	μA/A
IMON sense offset		I_{OUT} > 5A	-0.5		0.5	μA
Timer						
Upper threshold voltage	V_{TMR_H}		1.11	1.21	1.31	V
Insertion delay charge current	I_{INSERT}		3.35	4	4.65	μA
OCP fault timeout charge current	I_{FLT_TMR}		33.5	40	46.5	μA
Discharge $R_{DS(ON)}$	R_{FLT}			5.9		Ω
Soft Start (SS)						
SS pull-up current	I_{SS}	V_{SS} = 12V	6.5	7.5	8.5	μA
EN/UV (Enable and VIN UVLO)						
EN/UV input Rising threshold	V_{EN_R}		1.15	1.21	1.27	V
EN/UV input Falling threshold	V_{EN_F}		1.05	1.1	1.17	V
EN/UV Hysteresis	V_{ENHYS}			110		mV
EN/UV blanking time	t_{EN_BLANK}	EN recycling. High level trig mode		1.3		ms
Over-Voltage (OV)						
Input OV threshold, rising	V_{OV_R}		1.15	1.21	1.27	V
Input OV threshold, falling	V_{OV_F}		1.075	1.135	1.195	
Input OV threshold hysteresis	V_{OV_HYS}			75		mV
Fault Bar (FLTB)						
Low-level output voltage	V_{OL}	Sink current 10mA			0.3	V
Off-state leakage current	I_{FLT_LKG}	V_{FLTB} = 3.3V			1	μA
Power Good Output (PG)						
Power good rising threshold	PG_{Vth_R}	V_{IN} = 12V	85%	90%	95%	V_{IN}
		V_{IN} = 2.7V		VIN-0.5		V
Power good falling threshold	PG_{Vth_F}	V_{IN} = 12V	70%	75%	80%	V_{IN}
		V_{IN} = 2.7V		VIN-0.7		V
Power good off-state leakage current	I_{PG_LKG}	V_{FLT} = 3.3V			2	μA
PG output low voltage	V_{OL}	Sink current 10mA			0.3	V

TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

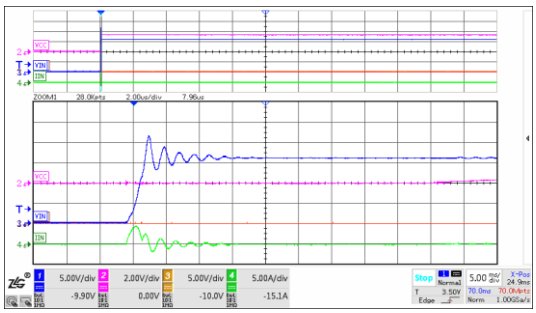
Hot Plug In

Test Conditions: Cin=0.47uF



VIN=12V, Cin=0.47uF

CH1=VIN, CH2=VCC, CH3=OUT, CH4=IIN

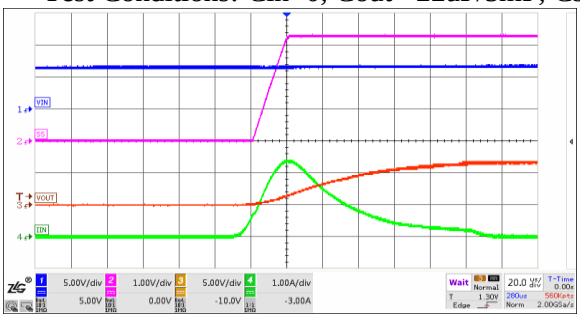


VIN=16V, Cin=0.47uF

CH1=VIN, CH2=VCC, CH3=OUT, CH4=IIN

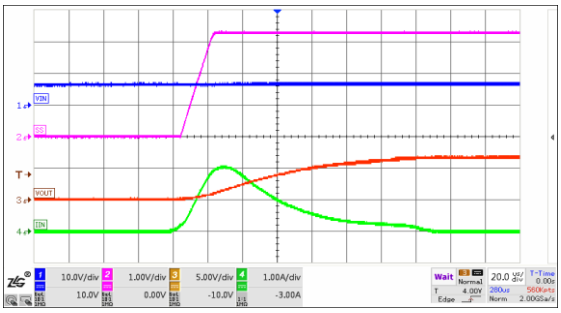
Power Up

Test Conditions: Cin=0, Cout =22uF/5mF, Css =Open/47nF/220nF



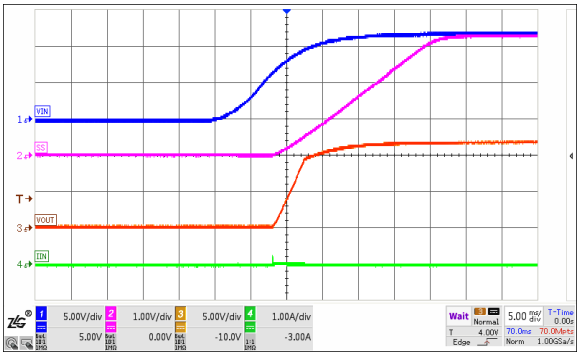
VIN=12V, Cout =22uF, Css =Open

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN



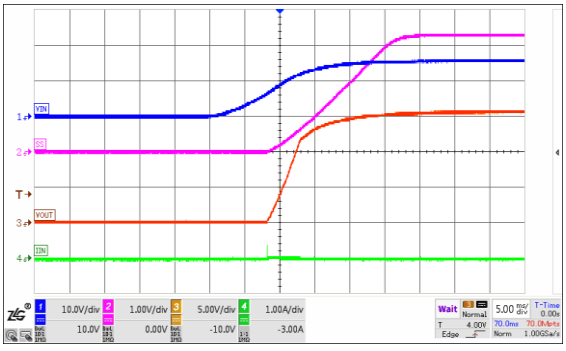
VIN=16V, Cout =22uF, Css =Open

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN



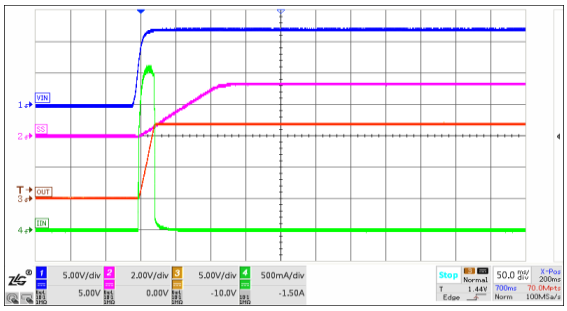
VIN=12V, Cout =22uF, Css =47nF

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN



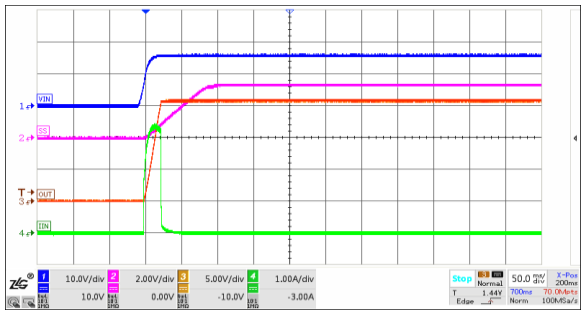
VIN=16V, Cout =22uF, Css =47nF

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN



VIN=12V, Cout =5mF, Css =220nF

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN

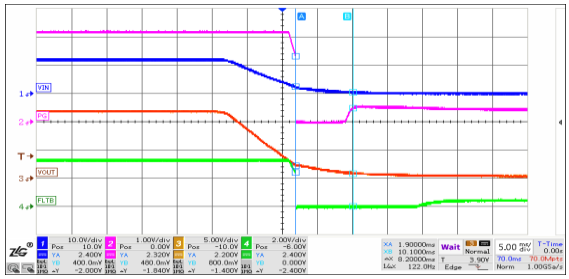


VIN=16V, Cout =5mF, Css =220nF

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN

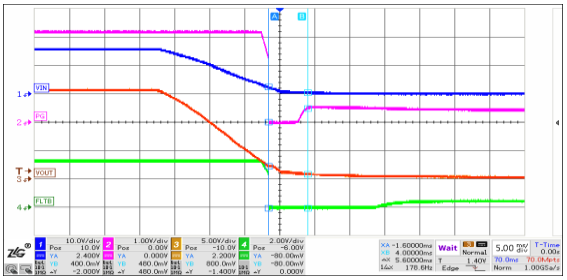
Power Down

Test Conditions: Cin=0, Cout =22uF/5mF, Css = 47nF/220nF



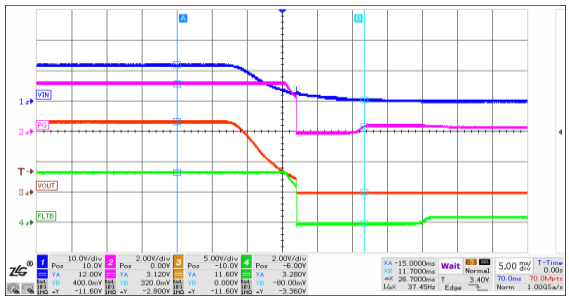
VIN=12V, Cout =22uF, Css =47nF, empty load

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB



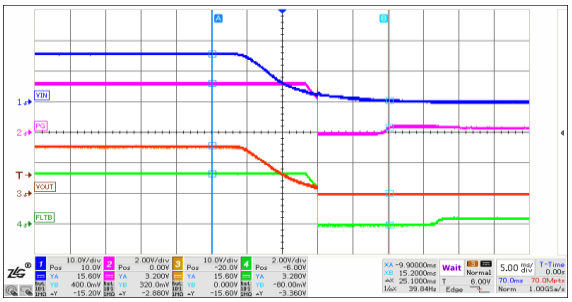
VIN=16V, Cout =22uF, Css =47nF, empty load

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB



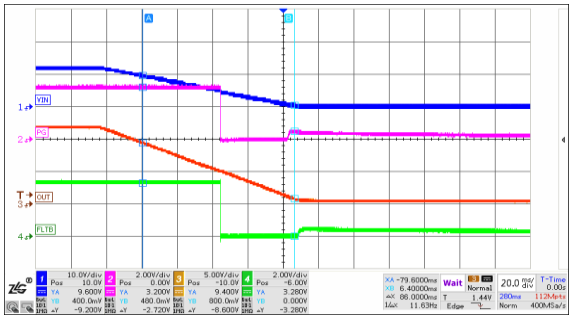
VIN=12V, Cout =22uF, Css =47nF, Full load

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB



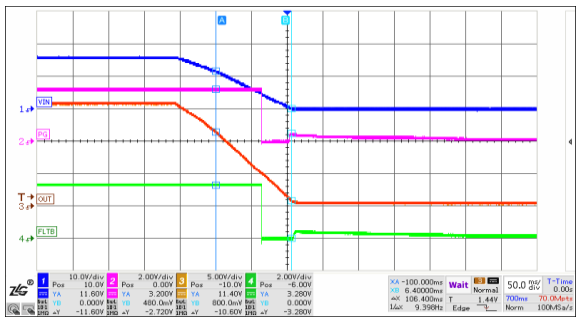
VIN=16V, Cout =22uF, Css =47nF, Full load

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB



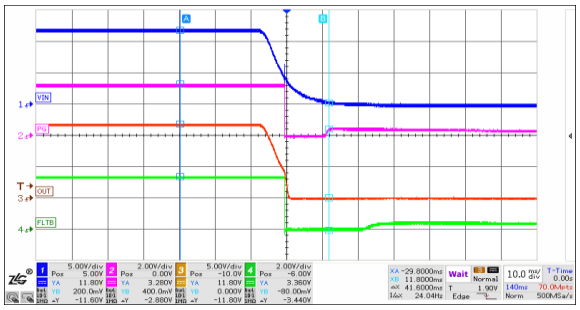
VIN=12V, Cout =5mF, Css =220nF, empty load

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB



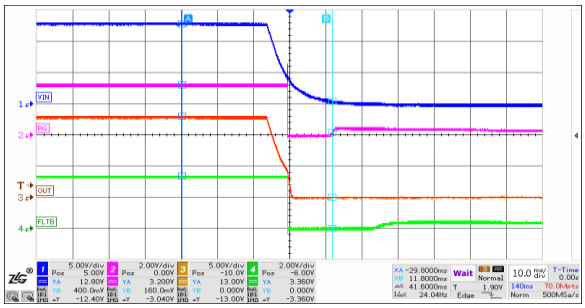
VIN=16V, Cout =5mF, Css =220nF, empty load

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB



VIN=12V, Cout =5mF, Css =220nF, Full load

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB

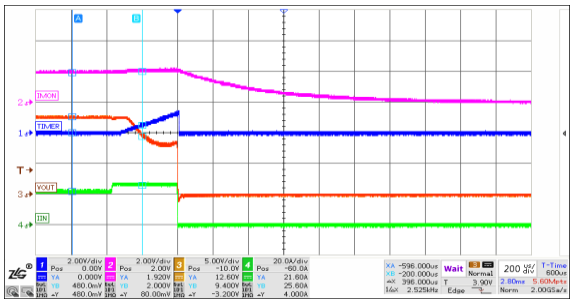


VIN=16V, Cout =5mF, Css =220nF, Full load

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB

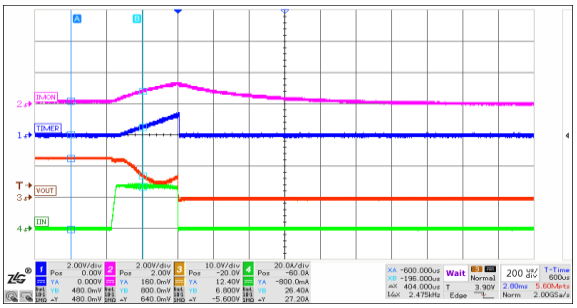
OCP

Test Conditions: Cout=22uF/5mF, Riset=12k



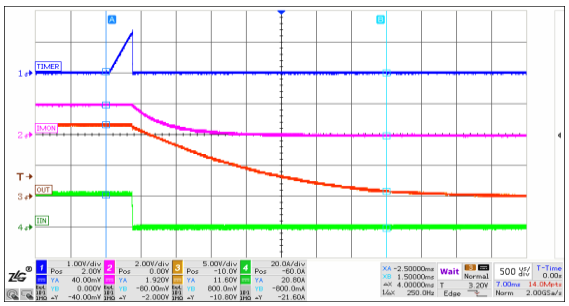
VIN=12V, Cout =22uF, Slow load, after SS

CH1=TIMER, CH2= IMON, CH3= VOUT, CH4=IIN



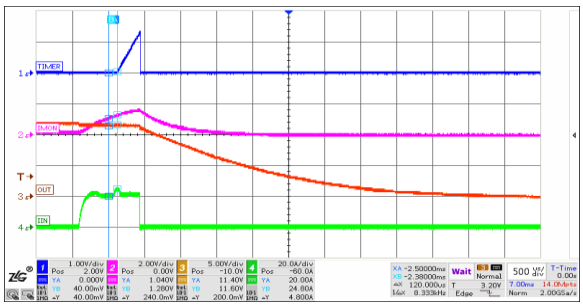
VIN=12V, Cout =22uF, load Jump, after SS

CH1=TIMER, CH2= IMON, CH3= VOUT, CH4=IIN



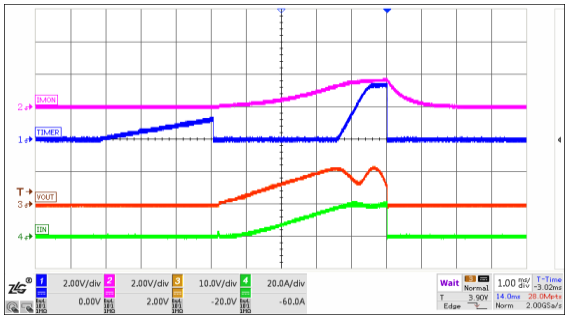
VIN=12V, Cout =5mF, Slow load, after SS

CH1=TIMER, CH2= IMON, CH3= VOUT, CH4=IIN



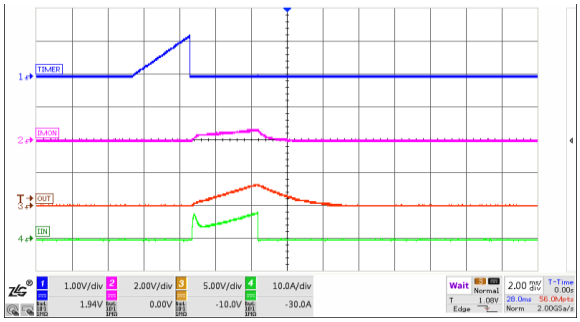
VIN=12V, Cout =5mF, load Jump, after SS

CH1=TIMER, CH2= IMON, CH3= VOUT, CH4=IIN



VIN=12V, Cout =22uF, Slow load, at SS

CH1=TIMER, CH2= IMON, CH3= VOUT, CH4=IIN

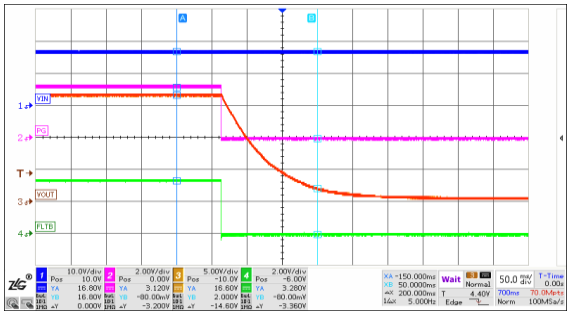


VIN=12V, Cout =5mF, load Jump, at SS

CH1=TIMER, CH2= IMON, CH3= VOUT, CH4=IIN

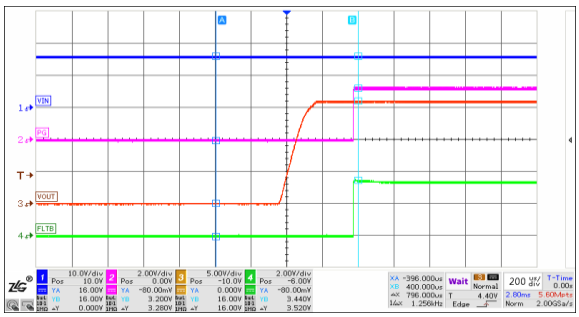
OV

Test Conditions: Cout=470uF



VIN=12V-17V, Cout =470uF

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB

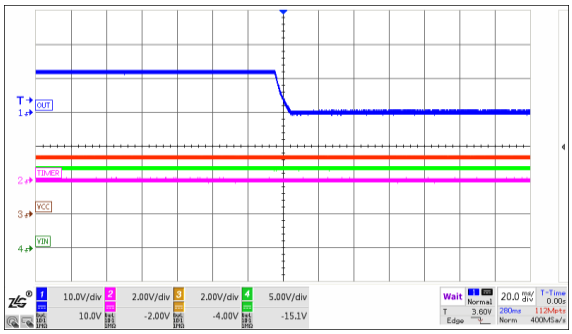


VIN=20V-16V, Cout =470uF

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB

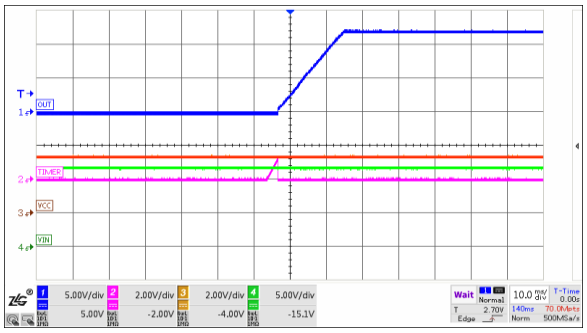
OT

Test Conditions: Cout=470uF



VIN=12V, Cout =470uF, Ta=147.6℃

CH1=VOUT, CH2= TIMER, CH3= VCC, CH4=VIN

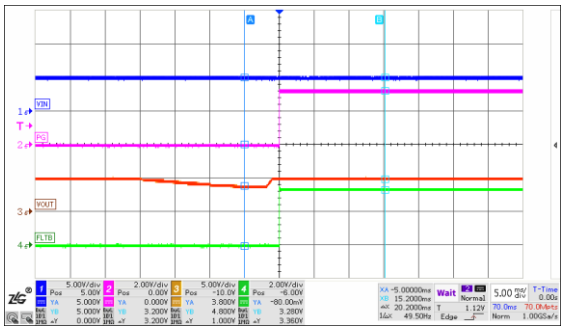


VIN=12V, Cout =470uF, Ta=94.5℃

CH1=VOUT, CH2= TIMER, CH3= VCC, CH4=VIN

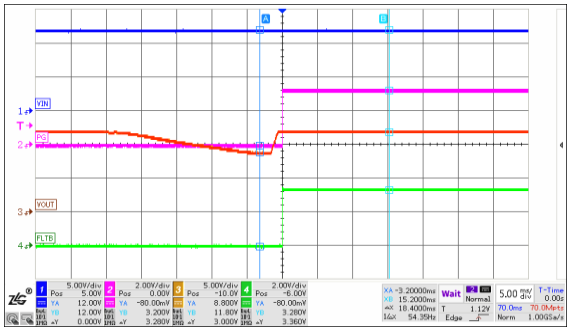
DS Short

Test Conditions: Cin=0, Cout=22uF



VIN=5V

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB

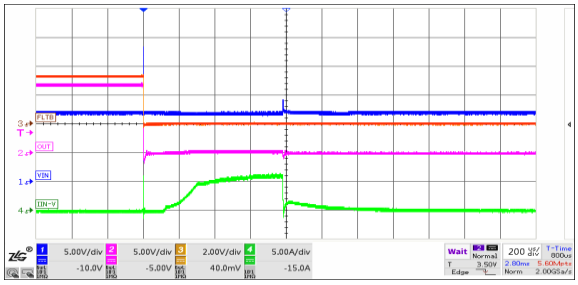


VIN=12V

CH1=VIN, CH2= PG, CH3= VOUT, CH4=FLTB

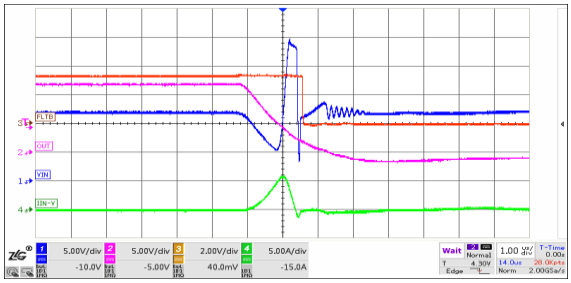
SCP

Test Conditions: Vin=12V/16V, Cin=220uF+TVS, Cout=22uF, Riset=12k, Schottky on Vout



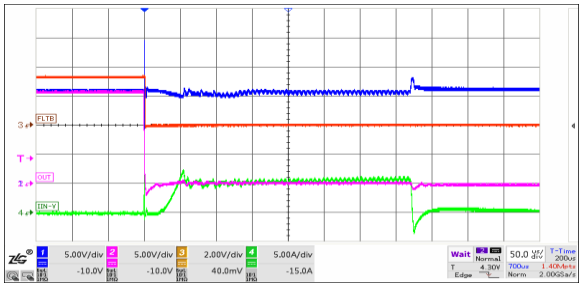
VIN=12V

CH1=VIN, CH2= OUT, CH3= FLTB, CH4=IIN



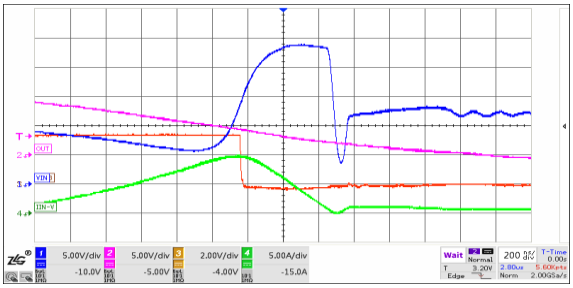
VIN=12V

CH1=VIN, CH2= OUT, CH3= FLTB, CH4=IIN



VIN=16V

CH1=VIN, CH2= OUT, CH3= FLTB, CH4=IIN

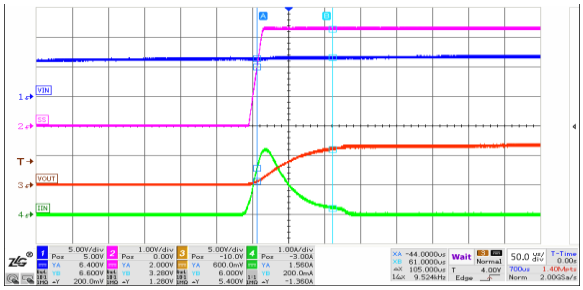


VIN=16V

CH1=VIN, CH2= OUT, CH3= FLTB, CH4=IIN

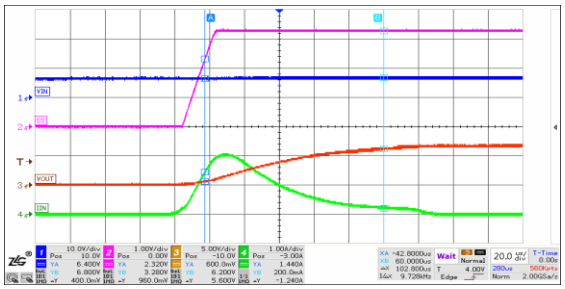
Tss vs Css

Test Conditions: Vin=12V/16V, Cout=22uF, Css= Open/220nF



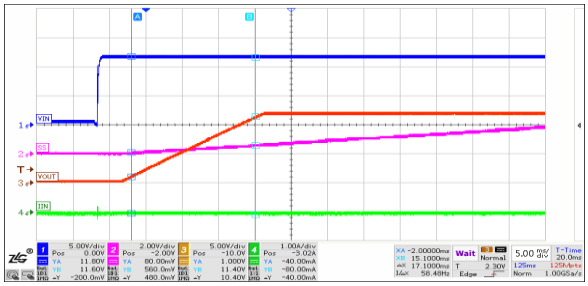
VIN=12V, Css= Open, Tss=105us

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN



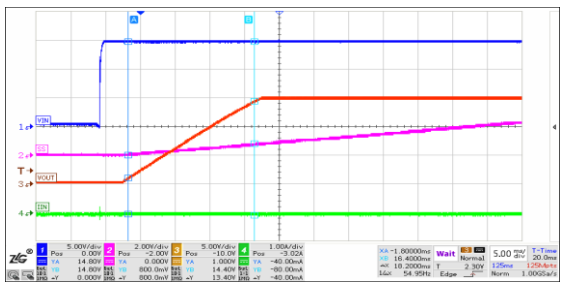
VIN=16V ,Css= Open, Tss=161.2us

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN



VIN=12V, Css= 220nF, Tss=17.1ms

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN

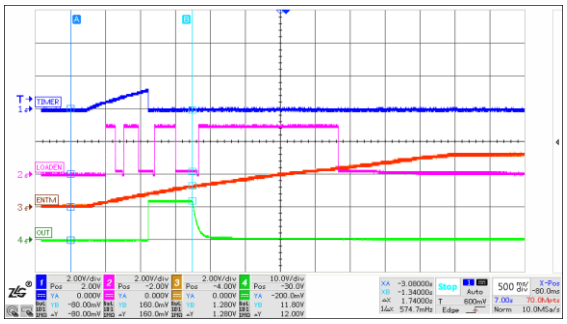


VIN=16V ,Css= 220nF, Tss=18.2ms

CH1=VIN, CH2= SS, CH3= VOUT, CH4=IIN

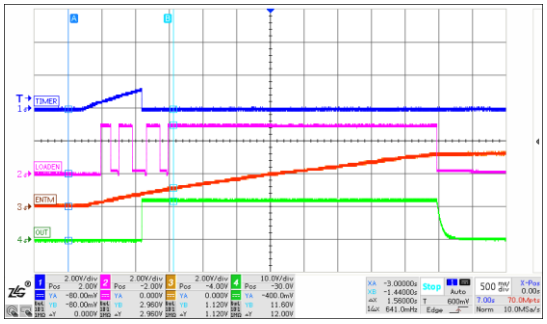
Blanking Time

Test Conditions: Vin=12V, Cout=22uF, Ctimer=2.2uF



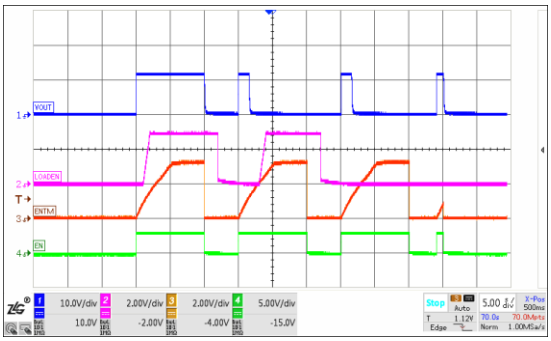
VIN=12V, VEN=VLOADEN=3.3V, Ctimer=2.2uF

CH1=TIMER, CH2= LOADEN, CH3= ENTM, CH4=OUT



VIN=12V, VEN=VLOADEN=3.3V, Ctimer=2.2uF

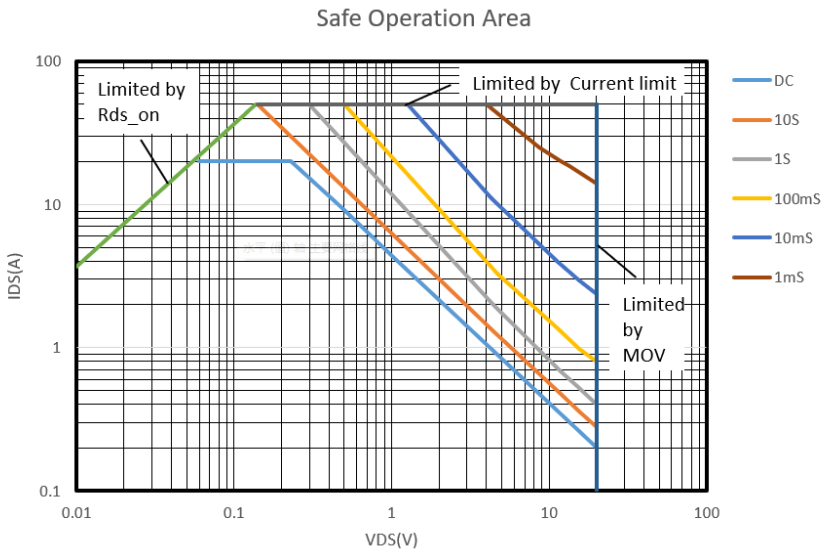
CH1=TIMER, CH2= LOADEN, CH3= ENTM, CH4=OUT



VIN=12V, VEN=VLOADEN=3.3V, Ctimer=2.2uF

CH1=VOUT, CH2= LOADEN, CH3= ENTM, CH4=EN

SOA



FUNCTIONAL DESCRIPTION

The XPA5355 limits the inrush current to the load when a circuit card is inserted into a live backplane power source, thus limiting the voltage drop seen on the backplane and the dV/dt of the voltage to the load. XPA5355 provides an integrated solution that monitors the input/output voltages, output current, and die temperature, eliminating the external current sense power resistor, power MOSFET, and thermal sense device.

The XPA5355 limits the integrated MOSFET's current by controlling its gate voltage through the reference input on ISET and soft-start ramp.

Current Limit

A constant current limit is set by an external resistor. Once the current-limit threshold is reached, gate voltage of the power FET is regulated to hold its current constant. The typical response time is around 20us, during which a small overshoot might be observed on the output current.

XPA5355 operates in start-up mode if VOUT < max (VIN-0.5V, 80% of VIN). In case the current through the power FET is greater than the start-up current limit for 1.5ms typical, the soft-start OC fault is triggered, and the device is shut down.

The start-up OC limit depends on the normal OC limit, which is set by the external resistor on ISET pin. When 80%*I_{OC_NOR} < 16A, I_{OC_SS} is equal to 80%*I_{OC_NOR}, otherwise, I_{OC_SS} is clamped to 16A, as illustrated in Fig. 3.

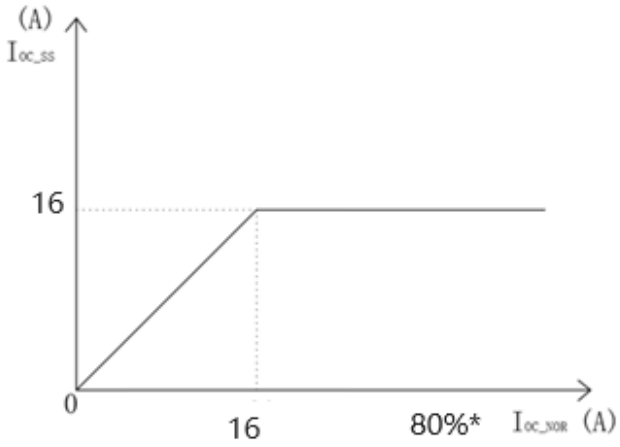


Fig. 3 Soft-start current limit vs normal OC limit

The device leaves start-up mode after VOUT > max (VIN-0.5V, 80% of VIN), and V_{GS} of the power FET gets close to the internal charge pump output voltage. The device operates normally once the start-up has finished, and the OC limit is now decided by the ISET resistor, with the following equation:

$$I_{OC_{NOR}} = \frac{0.3*10^6}{R_{ISET}} \text{-0.5(A)} \qquad (1)$$

Where R_{ISET} (Ω) is the resistor connected from ISET pin to ground.

The fault timer starts once the current limit is triggered. The device will resume normal operation if the output current falls below the OC threshold before the fault timeout period. The power FET latches off if the OC duration exceeds the fault timeout period. The fault timeout period is decided by the following equation:

$$t_{fault} = \frac{1.21}{40} * C_T \qquad (2)$$

Where t_{fault} is the fault timer (ms), and C_T (nF) is the timer capacitor. As an example, a 10nF capacitor generates 0.3ms fault timer. When an OC fault occurs, FLTB is driven LOW at a propagation delay of 8μs.

Short-circuit Protection (SCP)

If a short-circuit fault happens, the load current may increase rapidly and exceed the current limit threshold before the hot-swap control loop kicks in. In case the SC current limit is reached, a fast-off circuit is activated to turn off the power FET. This limits the peak device current and hence the input-voltage drop, with a typical response time (t_{SC}) of around 200ns.

After the power FET's V_{GS} drops low, the device attempts to start up again immediately to avoid an input voltage line transient event. An internal charge pump charges up the gate of the power FET. If the short-circuit has been induced by the input line transient, the part should work normally thereafter. In case a real short circuit occurs, the load current limit is set by ISET as normal, and if the fault persists, the fault timer will ramp up to 1.21V, to help turn OFF the power FET.

When a real hard-short occurs, the input voltage is pulled below VCC rapidly. Therefore, the gate volage of the power FET will be pulled low immediately, regardless of the whether 50A short-circuit limit has been reached or not. Note that the power FET will retry one more time even if the short-circuit condition is there (Fig. 4). If the short-circuit stays after the timer expires, FLTB switches LOW.

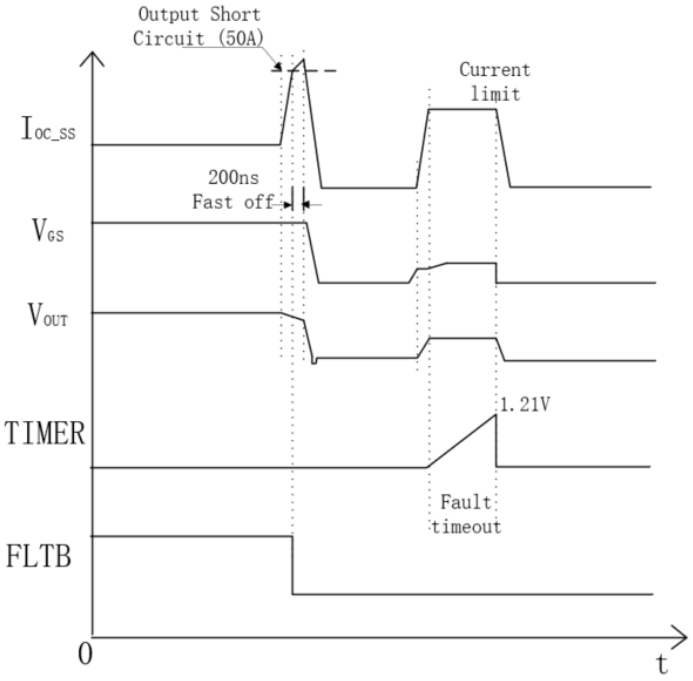


Fig. 4 Waveforms during short-circuit protection

Power-up Sequence

For hot-swap applications, the input of XPA5355 might see a voltage spike or transient during the hot-plug procedure, due to parasitic inductance of the input trace and the input capacitor. To help stabilize the input voltage, an insertion delay is necessary before the main FET is turned on. The is realized by TIMER pin charging an external capacitor (C_T), through a 4μA constant current source when VIN reaches the UVLO threshold. The capacitance of C_T can be determined with the following Equation:

$$t_{delay} = \frac{1.21}{4} * C_T \qquad (3)$$

Where C_T is the insertion delay timer capacitance (nF), and tdelay is the insertion delay (ms). For example, a 10nF capacitor corresponds to an insertion delay of 3.025ms.

Soft Start (SS)

When EN is pulled high and the insertion delay time ends, a constant-current source proportional to the input voltage charges up the capacitor connected to the SS pin, which determines the soft- start time. The output voltage rises at a similar slew rate to the SS voltage.

The SS capacitor value can be calculated with Equation:

$$\boldsymbol{C_{SS} = 18 * \frac{t_{SS}}{R_{SS}}} \qquad (4)$$

Where t_{SS} is the soft-start time, and R_{SS} is 1.6MΩ. For example, a 100nF capacitor gives a soft-start time of 8.9ms.

If the load capacitance is extremely large, the current required to maintain the preset soft-start time exceeds the current limit. In this case, the rise time is controlled by the load capacitor and the current limit.

A 24μA current source pulls up the gate of the power FET, and the gate charge current controls the output voltage rise time. A floating SS leads to the fastest ramp-up voltage.

Enable and LOADEN

Table 1 shows how EN and LOADEN are used in combination to control the on/off status of XPA5355.

During the LOADEN blanking time, EN = 1 alone can turn on the device. After the LOADEN blanking time expires, both EN = 1 and LOADEN = 1 are needed to turn on the device. EN = 0 can always turn off the power FET. Recycling EN or VIN will restart the device once it is latched off.

LOADEN is used to shut down the device after the LOADEN blanking time, however, recycling LOADEN alone can't turn on the device (see Fig. 5).

Table 1: Function of EN/LOADEN Blanking Time

LOADEN blanking time expires?	EN	LOADEN	On/off Status
Y	0	0	Off
Y	0	1	Off
Y	1	0	Off
Y	1	1	On
N	0	0	Off
N	0	1	Off
N	1	0	On
N	1	1	On

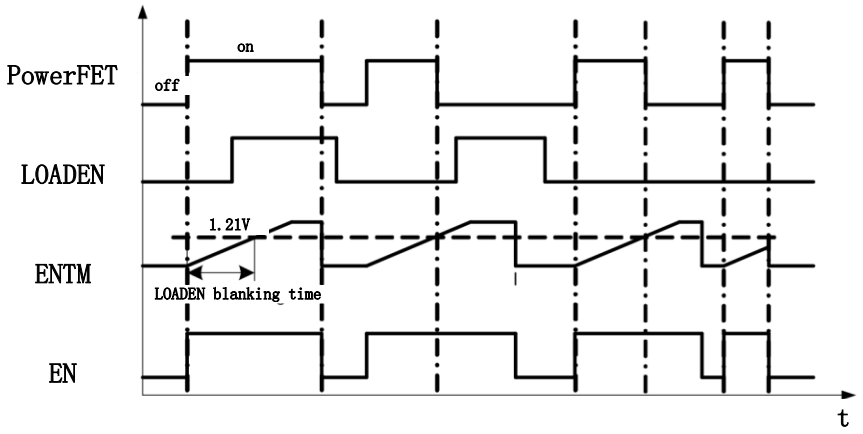


Fig. 5 EN/LOADEN Timing Diagram

The insertion delay timer starts once the device is enabled. Upon the end of the insertion delay time, an internal 24μA current source starts charging up the power FET's V_{GS}, and it takes around 1ms for V_{GS} to reach its threshold. The output voltage then rises following the slew rate controlled by SS.

LOADEN Blanking Time (ENTM)

When EN is high, a programmable blanking time can prevent LOADEN from undesired de-assertion (see Fig. 6). All fault functionality works during start-up, so the power FET can still shut down if a fault is detected. LOADEN going low during the blanking time will not turn off the power FET. After the blanking time ends, LOADEN can then operate normally.

A capacitor connected to ENTM is used to set the blanking time, and the capacitor is calculated with Equation (5):

$$C_{ENTM} = \frac{1.1}{1.24} * t_{LDNB} \qquad (5)$$

Where t_{LDNB} is the LOADEN blanking time, and C_{ENTM} is the LOADEN blanking time capacitor (μF). For example, a 1μF ENTM capacitor sets a blanking time of 1.1s.

Short ENTM to GND if the LOADEN function is not used.

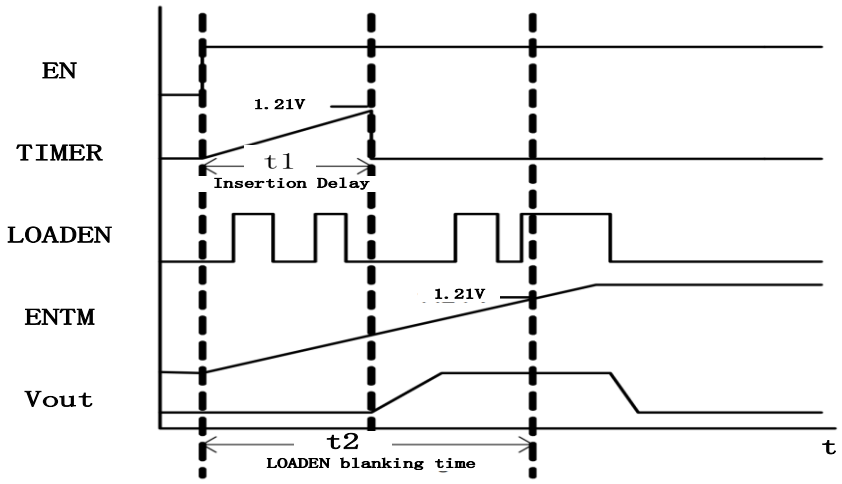


Fig. 6 LOADEN Blanking Time

Power Good (PG)

Power good (PG) indicates whether the VOUT is in the normal range relative to VIN. PG is an open drain output. Pull PG up to the external power supply througha 10-100kΩ resistor. During start-up, the power good output is driven low. This keeps the system off and minimize the load on VOUT, in order to reduce inrush current and power dissipation at start-up.

When the device meets the following conditions, the PG signal is pulled HIGH, and the output can start to draw full power:

- $V_{OUT} > V_{IN} * 90\%$
- $V_{EN} > 2V$
- $V_{OUT} > V_{IN} – 0.5V$

PG signal is switched LOW, if any of the below occurs：

- $V_{OUT} < 75\% * V_{IN}$
- EN=0
- Any faults occurred.

With VIN=0, PG stays LOW even if a pull-up supply exists.

Fault Bar (FLTB)

Fault bar (FLTB) is an open-drain output used to indicate that a fault has occurred. Pull FLTB up to an external power supply through a 10-100kΩ resistor.

FLTB is driven low with an 8μs propagation delay for the following faults:

- Over-current of short circuit
- Over-temperature
- Power FET drain-source short
- OV/UV

Note that if a short circuit occurs and the 50A secondary current limit is reached, the FLTB is switched low immediately.

FLTB goes high when the XPA5355 resumes normal operation. This means that VOUT is higher than the setting voltage of the PG rising threshold, and the power FET is fully on (VGS > 3V).

Fault Protections

Over-current Protection (OCP)

During soft-start, if VOUT< max (VIN-0.5V, 80% of VIN), and the output current is regulated by IOC_SS for 1.5ms, the power FET's gate is pulled low to stop regulating. Meanwhile, FLTB and SS are pulled LOW to indicate that a fault has occurred.

ISET determines the current limit level for over-current protection of XPA5355. During normal operation, if the load current exceeds IOC_NOR, the power FET's gate keeps regulate until the OCP fault timeout, upon which the power FET turns off, FLTB and SS are switched LOW immediately.

Short-circuit Protection (SC)

Short-circuit protection is provided to protect the device from serious over-current faults, including a hard-short event between VOUT and GND. The power FET is turned OFF quickly within 200ns, if the output current exceeds 50A.

After VGS drops low, the device attempts to start up again immediately to avoid an input voltage line transient event. In case the short is real, the fault timer will start to ramp up, and once it reaches 1.21V, FLTB is asserted LOW and the power FET is turned OFF.

Over-temperature Protection (OTP)

XPA5355 monitors the junction temperature Tj with internal sense circuitry. Once Tj exceeds its threshold of 150°C, FLTB is asserted LOW and the device is shut down.

VIN Over-voltage Protection (VIN OVP)

OV pin sets the VIN OVP threshold, to help protect the device from an over-voltage event. Once OVP triggers, both SS and FLTB are asserted LOW and the power FET is turned off.

Drain-source Short Detection

Regardless of the status of EN, if VOUT > min (V_{IN} - 0.5V, VIN*90%) before the insertion delay timer expires, XPA5355 determines that the power FET drain-source is shorted. Both PG and FLTB go LOW, and the power switch is held off. Once $V_{OUT} \leq$ min (V_{IN} - 0.7V, VIN*75%), the part then starts up normally.

Note that the drain-source short detection is enabled as EN goes HIGH, so the check is continuous. If DS short is detected during normal operation, PG and FLTB are both pulled low. Upon the removal of this short, the device then continues to work normally.

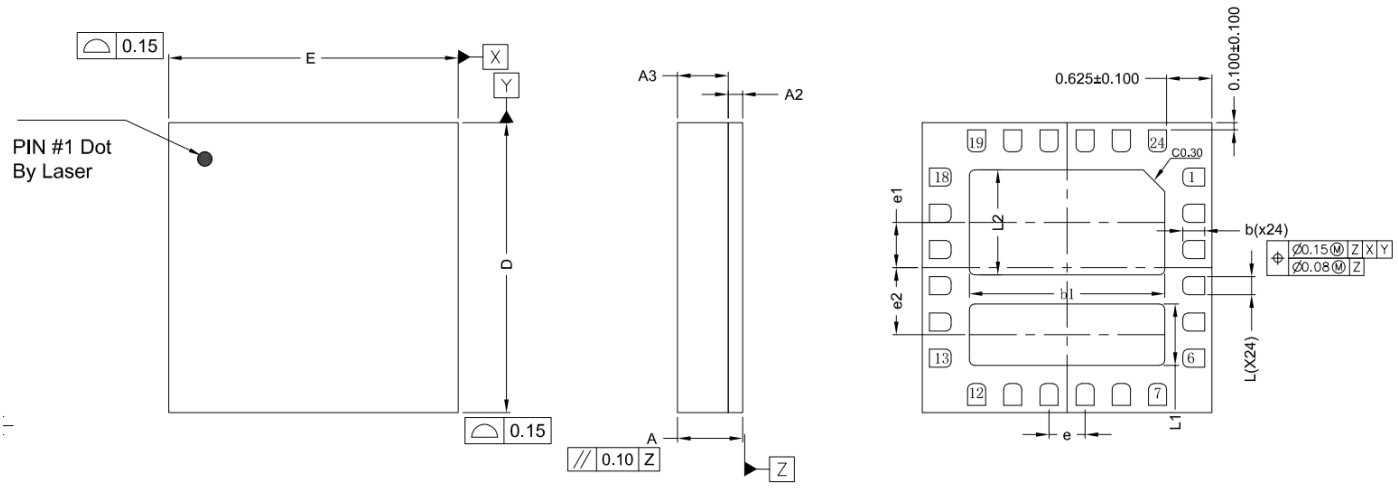
Gate-source Short Detection

If the following conditions happen, the power FET constitutes a gate-source short and is shut down:

- V_{GATE} < VCP – 0.9V
- V_{GS} > VCC – 0.7V
- No OC faults
- Delay 200ms

PHYSICAL DIMENSIONS

Package: TLGA-26 (4mmX4mm)



TOP VIEW SIDE VIEW BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom	Max.
D	3.900	4.000	4.100
E	3.900	4.000	4.100
A	0.830	0.900	0.970
A2	0.170	0.200	0.230
A3	0.700 BASIC		
b	0.250	0.300	0.350
L	0.200	0.250	0.300
e	0.450	0.500	0.550
b1	2.650	2.700	2.750
L1	0.800	0.850	0.900
L2	1.400	1.450	1.500
e1	0.575	0.625	0.675
e2	0.875	0.925	0.975

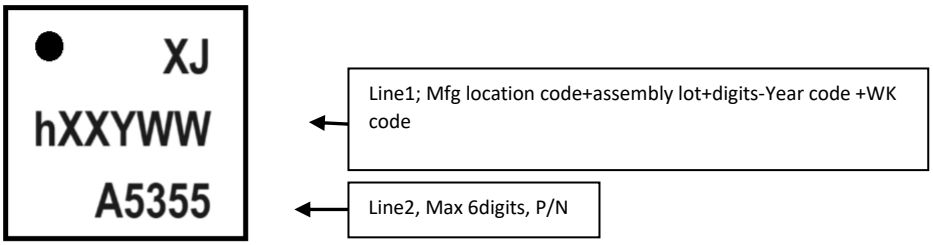
NOTES :
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSIONS ARE IN MM.
3. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
4. CUSTOMER'S SPECIFIC DRAWING.
5. TOLERANCE X.XXX =±0.05mm, X.XX=±0.10mm.

TOP MARKINGS

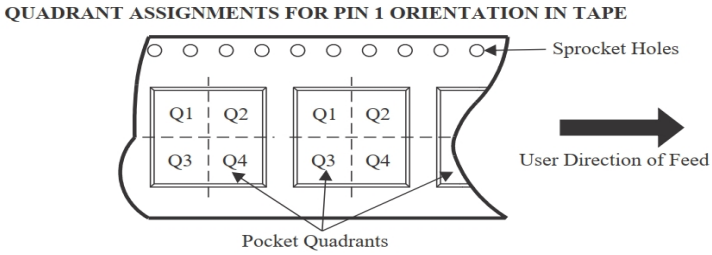
Package Marking & PQ information

XPA5355G26R Marking

Format:



Pin 1 located in Q2 direction in T&R (follow EIA-418)



Remark :

Font: Arial

Letter height of 160um, wide of 120um

Letter pitch of 50um

Line space of 50um

LOGO Line 1 right

Logo of XJ should be required and placed on assigned Logo position as upside illustration.

Pin 1 Line 1 left

Pin 1 should be designed at left of line 1 for recognition.

Traceability Code: Line 2 and Line 3

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code

a) 1st digit: Assembly location code: h
b) 2nd & 3rd digit: Assembly lot number
c) 4th digit: Year code.

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d) 5th & 6th digit: Week code, 01 means the 1st Work Week based on XinJi's calendar.

WK01 means the 1st Work Week based on XinJi's calendar.

2.Product Number Code: Line 3

Product Name	P/N Code	Remark
XPA5355G26R	A5355	

3. Packing: 3K/Reel