

16 Multi-Function LED Driver And GPIO Controller With I²C Interface

Features

- 16 multi-function I/O, each for LED drive (current-source dimming) or GPIO mode
- 256 steps linear dimming in LED drive mode
- Any GPIO can be configured as an input or an output independently
- Support interrupt, 8 μ s deglitch, low-level active
- Standard I²C interface, AD1/AD0 select I²C device address
- SDA, SCL, RSTN, and all GPIO can accept in 1.8V logic input
- Supply shutdown function, low-level active
- 2.5V~5.5V power supply
- QFN 4mmx4mm-24L package

Applications

Cell Phone
PDA/MP3/MP4/CD/Mini display
Automotive

General Description

AW9523Q is a 16 multi-function LED driver and GPIO controller. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently.

After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I²C device address selection inputs, AD0 and AD1. All I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When AW9523Q reads GPIO state through the I²C interface, the interrupt is cleared. Interrupt has 8 μ s deglitch.

When the I/O ports are configured as LED drive mode, AW9523Q can set the current of LED drive between 0~IMAX by I²C interface, which is divided by 256 steps linear dimming. The default maximum current (IMAX) is 37mA, and IMAX can be changed in GCR register.

The operating voltage range of AW9523Q is 2.5V~5.5V.

Typical Application Circuits

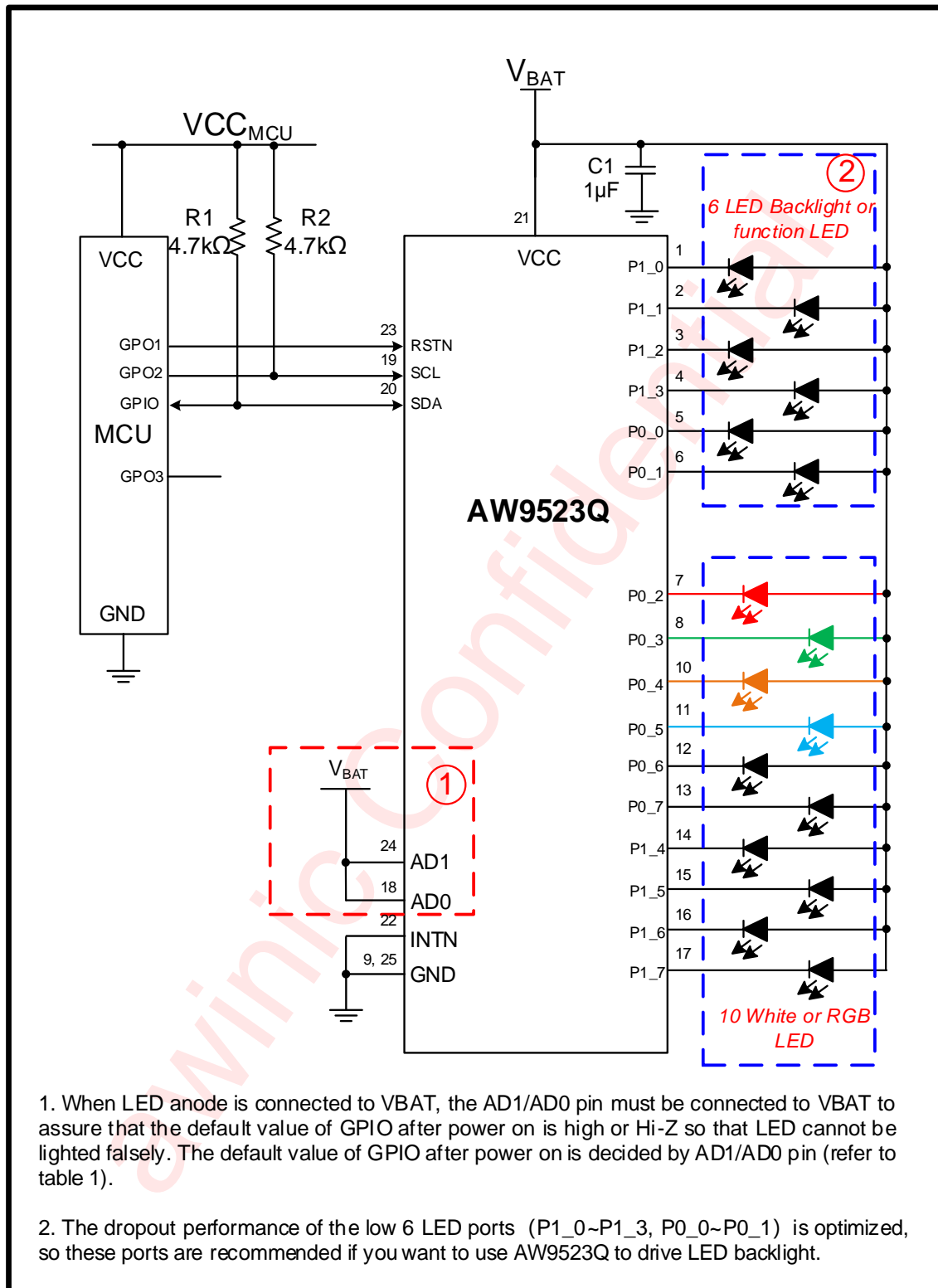


Figure 1 Drive 16 Function LEDs, Including 6 Ports Feasible for LED Backlight

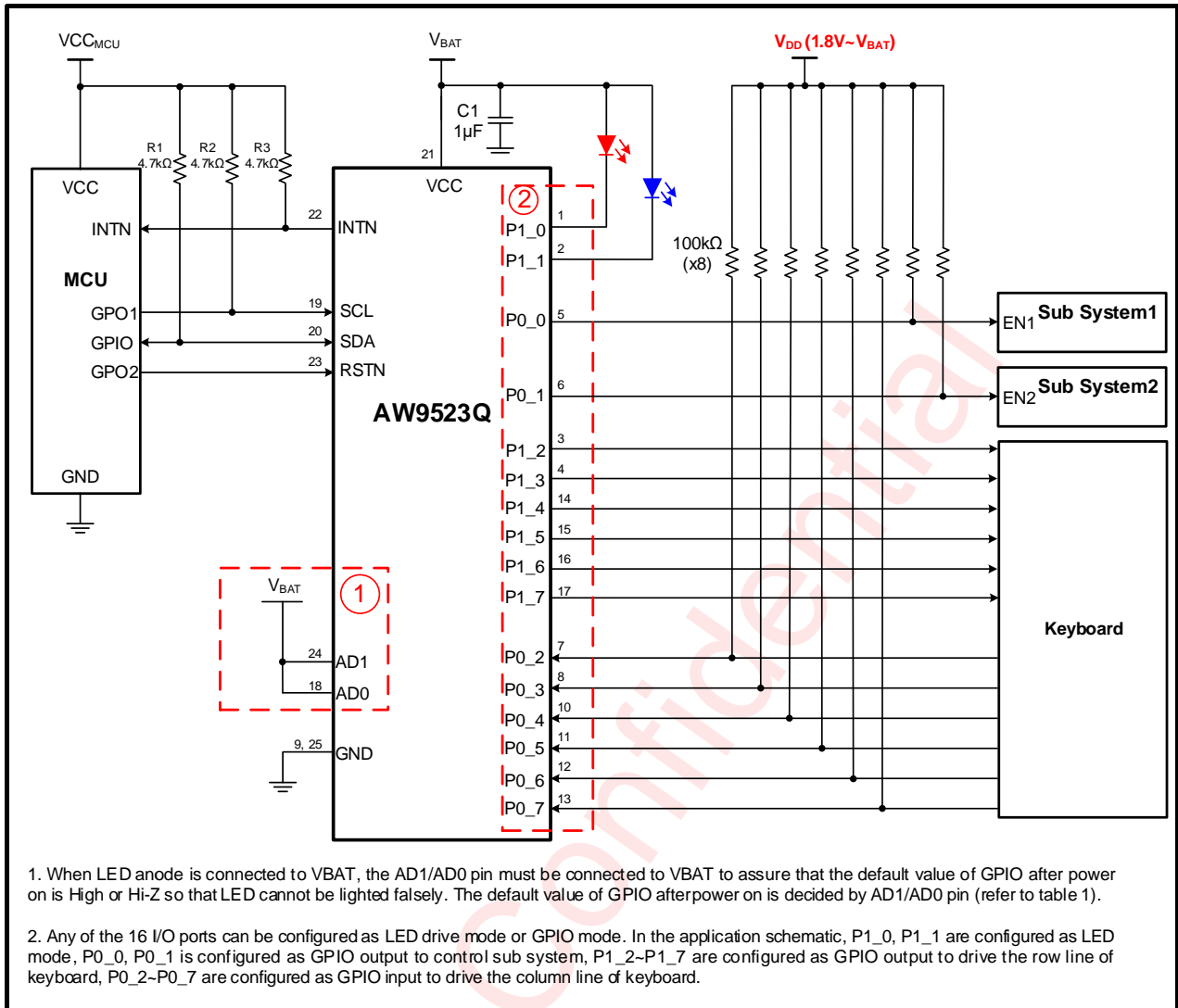


Figure 2 Function LED + Keyboard/IO Extended

Pin Configuration And Top Mark

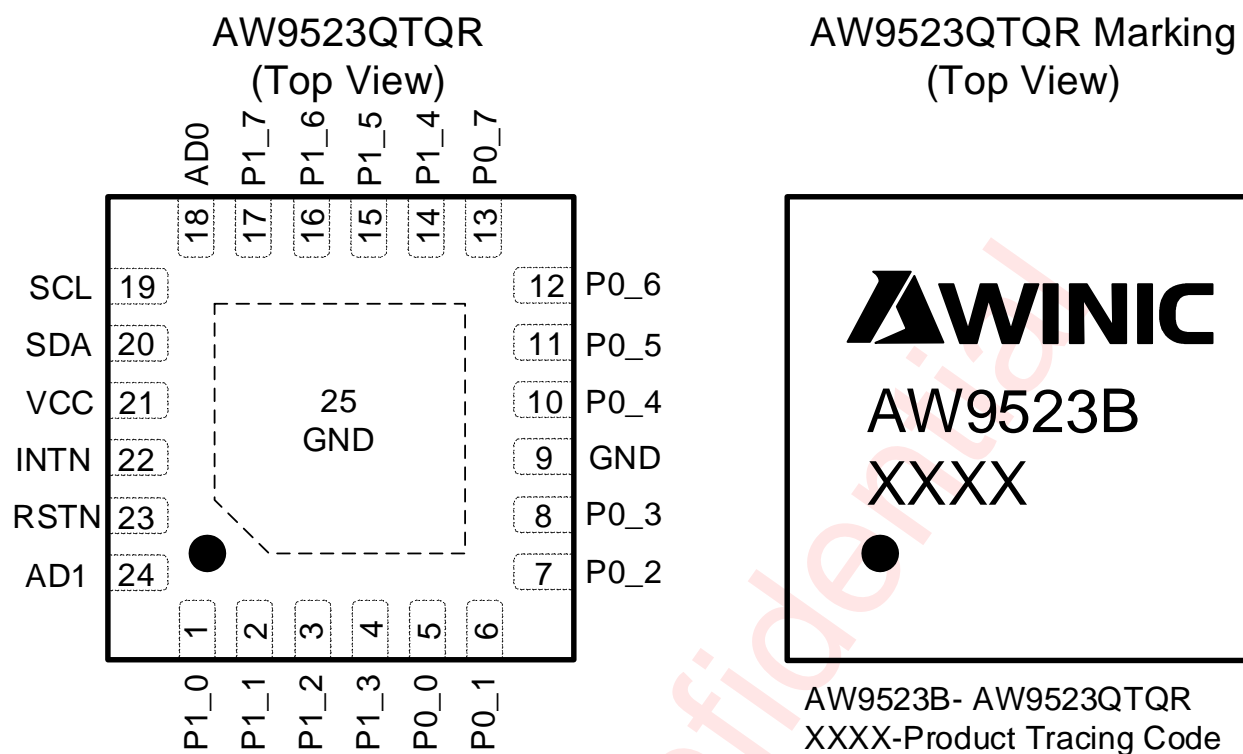


Figure 3 AW9523Q Pin Configuration and Marking

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Pin Definition

Pin No.	Name	Description
1	P1_0	GPIO output mode default, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
2	P1_1	GPIO output mode default, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
3	P1_2	GPIO output mode default, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
4	P1_3	GPIO output mode default, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
5	P0_0	GPIO output mode default, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
6	P0_1	GPIO output mode default, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
7	P0_2	GPIO output mode default, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
8	P0_3	GPIO output mode default, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
9	GND	Ground supply
10	P0_4	GPIO output mode default, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.

Pin No.	Name	Description
11	P0_5	GPIO output mode default, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
12	P0_6	GPIO output mode default, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
13	P0_7	GPIO output mode default, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
14	P1_4	GPIO output mode default, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
15	P1_5	GPIO output mode default, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
16	P1_6	GPIO output mode default, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
17	P1_7	GPIO output mode default, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 pin.
18	AD0	I ² C interface device address, connect to VCC or GND, and control the default state of output pin (refer to table 1).
19	SCL	I ² C interface clock bus
20	SDA	I ² C interface data bus
21	VCC	Power supply
22	INTN	Interrupt output pin, open-drain mode, need external pull-up resistor. Interrupt low active.
23	RSTN	Hardware reset pin, low reset. It has an internal 100kΩ(typical) pull-low resistor.
24	AD1	I ² C interface device address, connect to VCC or GND, and control the default state of output pin (refer to table 1).
25	GND	Ground supply

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9523QTQR	-40°C~105°C	QFN 4mm×4mm- 24L	AW9523B	MSL3	RoHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply voltage, VCC	-0.3V to 6V
SCL, SDA, AD0, AD1, INTN, RSTN, P0_0~P0_7, P1_0~P1_7	-0.3V to 6V
Max power (P _{Dmax} , package@ T _A =25°C)	3.2W
Package thermal impedance, θ_{JA}	31°C/W
Max junction temperature, T _{Jmax}	150°C
Storage Temperature, T _{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD(NOTE2)	
HBM	±2kV
CDM	±1.5kV
Latch-Up	
Test Condition: JEDEC EIA/JESD78E	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9. JEDEC EIA/JESD22-C101F(CDM).

Electrical Characteristics

$V_{CC}=3.8V$, $T_A=25^{\circ}C$ for typical values (unless otherwise noted).

Parameter	Test Condition	Min.	Typ.	Max.	Unit		
Supply Voltage and Current							
VCC	Supply voltage	2.5		5.5	V		
I _{shutdown}	Shutdown current	RSTN=GND		0.1	5	μA	
I _{CC}	Standby mode	RSTN=1.8V; V _I =GND or VCC; AD0=AD1=GND; I _O =0mA; F _{SCL} =0kHz	VCC=5.5V	30	60	μA	
			VCC=3.6V	10	20	μA	
			VCC=2.7V	2	5	μA	
		RSTN=1.8V V _I =GND or VCC; AD0=AD1=GND; I _O =0mA; F _{SCL} =400kHz	VCC=5.5V	50	80	μA	
			VCC=3.6V	12	24	μA	
			VCC=2.7V	6	10	μA	
LED Driver							
I _{MAX}	Max current of LED drive	Configure DIMx Reg. as FFH		25.9	37	48.1	mA
V _{drop1}	Dropout voltage on low 6 ports (P1_0~P1_3, P0_0~P0_1)	I _{OUT} =20mA			60		mV
V _{drop2}	Dropout voltage on high 10 ports (P0_2~P0_7, P1_4~P1_7)	I _{OUT} =20mA			80		mV
Digital Pin Output							
V _{OH}	High-level output voltage (P0_7~P0_0, P1_7~P1_0)	VCC=2.5V, I _{SOURCE} =10mA			VCC-170		mV
		VCC=3.6V, I _{SOURCE} =20mA			VCC-250		mV
		VCC=5V, I _{SOURCE} =20mA			VCC-200		mV
V _{OL}	Low-level output voltage (P0_7~P0_0, P1_7~P1_0)	VCC=2.5V, I _{SINK} =20mA			90		mV
		VCC=3.6V, I _{SINK} =20mA			70		mV
		VCC=5V, I _{SINK} =20mA			60		mV
V _{OL}	Low-level output voltage (SDA, INTN)	VCC=2.5V, I _{SINK} =6mA			150		mV
		VCC=3.6V, I _{SINK} =6mA			100		mV
		VCC=5V, I _{SINK} =6mA			75		mV
Digital Pin Input							
V _{IH}	High-level input voltage (SCL, SDA, RSTN, AD0, AD1, P0_7~P0_0, P1_7~P1_0)		1.4				V
V _{IL}	Low-level input voltage (SCL, SDA, RSTN, AD0, AD1, P0_7~P0_0, P1_7~P1_0)				0.4		V

Parameter		Test Condition	Min.	Typ.	Max.	Unit
I _{IH} , I _{IL}	Input current (SCL, SDA, AD0, AD1, P0_7~P0_0, P1_7~P1_0)	V _I =VCC or GND	-0.2		0.2	μA
R _{RSTN}	Internal pull-low resistor in RSTN pin			100		kΩ
C _i	Input capacitance (SCL, SDA, RSTN, AD0, AD1, P0_7~P0_0, P1_7~P1_0)	V _I =VCC or GND		3		pF
t _{SP_RSTN}	Pulse width that RSTN pin can filter	RSTN=VCC		10		μs

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I²C Interface Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL I ² C clock frequency	f _{SCL}			400	kHz
I ² C Start or repeated Start condition hold time	t _{HD:STA}	0.6			μs
SCL I ² C clock low time	t _{LOW}	1.3			μs
SCL I ² C clock high time	t _{HIGH}	0.6			μs
I ² C Start or repeated Start condition setup time	t _{SU:STA}	0.6			μs
I ² C serial-data hold time	t _{HD:DAT}	0			μs
I ² C serial-data setup time	t _{SU:DAT}	0.1			μs
I ² C rise time	t _R			0.3	μs
I ² C fall time	t _F			0.3	μs
I ² C Stop condition setup time	t _{SU:STO}	0.6			μs
I ² C bus free time between a STOP and START condition	t _{BUF}	1.3			μs
I ² C spike time	t _{SP}	0		50	ns
I ² C bus capacitive load	C _b			400	pF

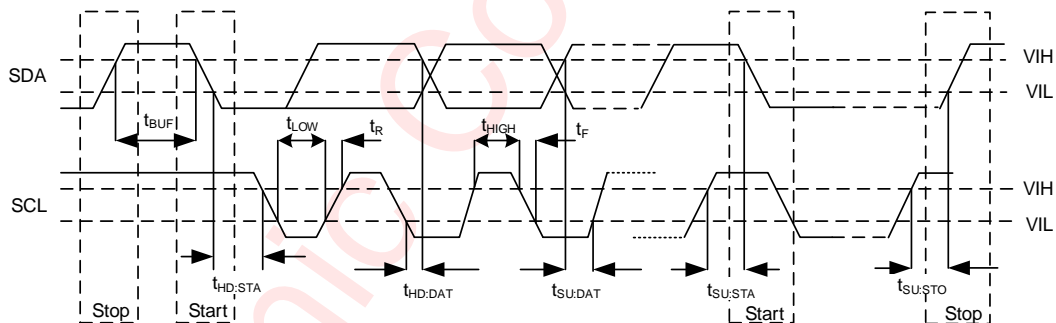
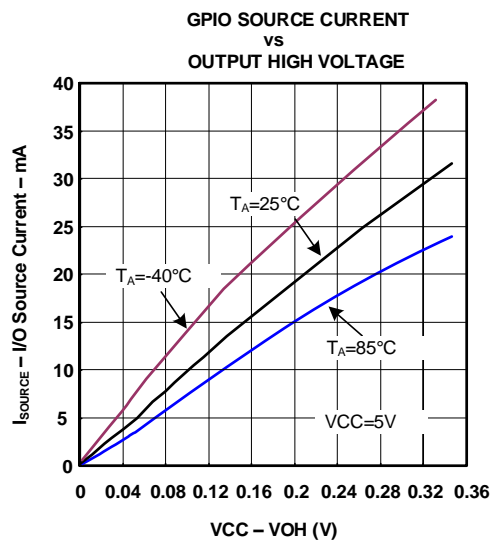
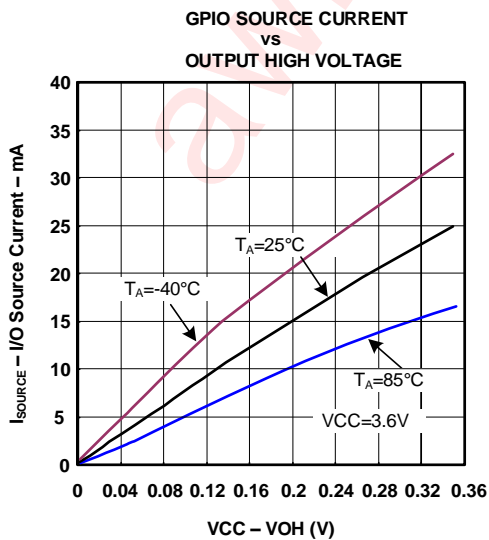
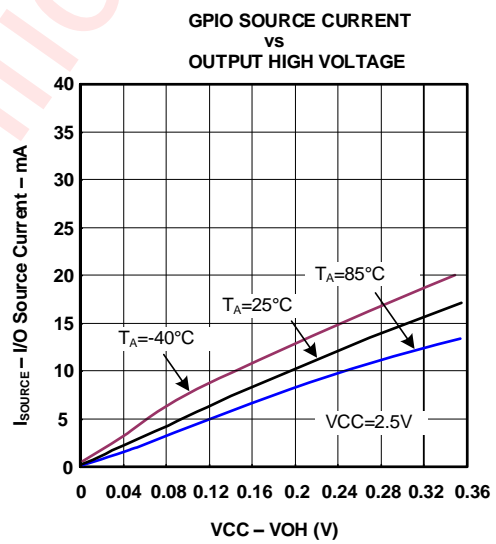
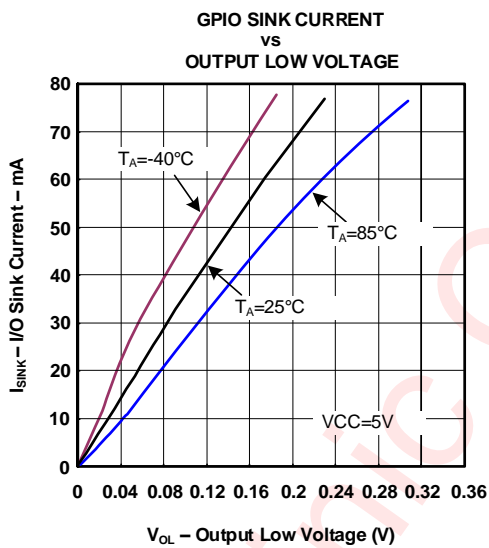
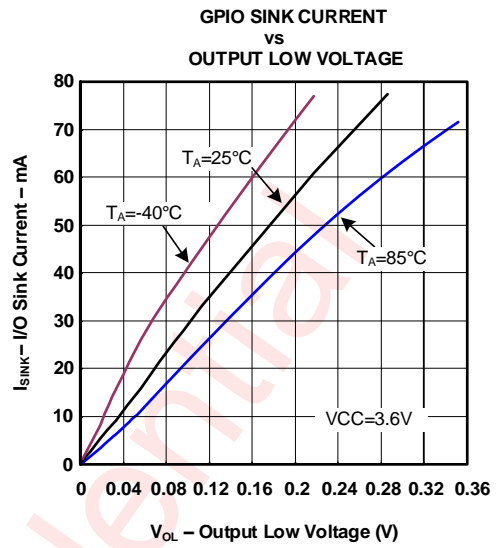
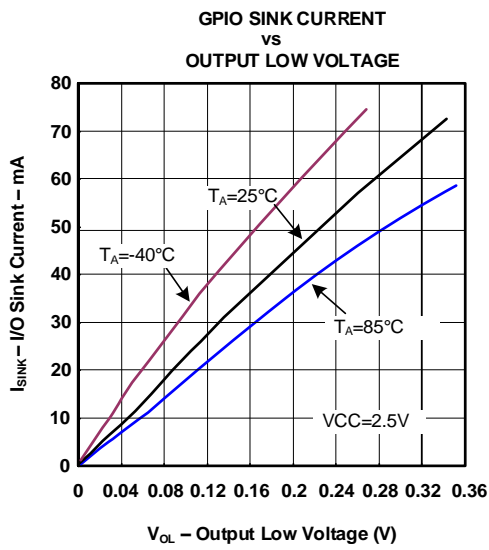


Figure 4 I²C Interface Timing

Typical Characteristics

Ambient temperature is 25°C, input voltage is 3.6V, unless otherwise noted .



Functional Block

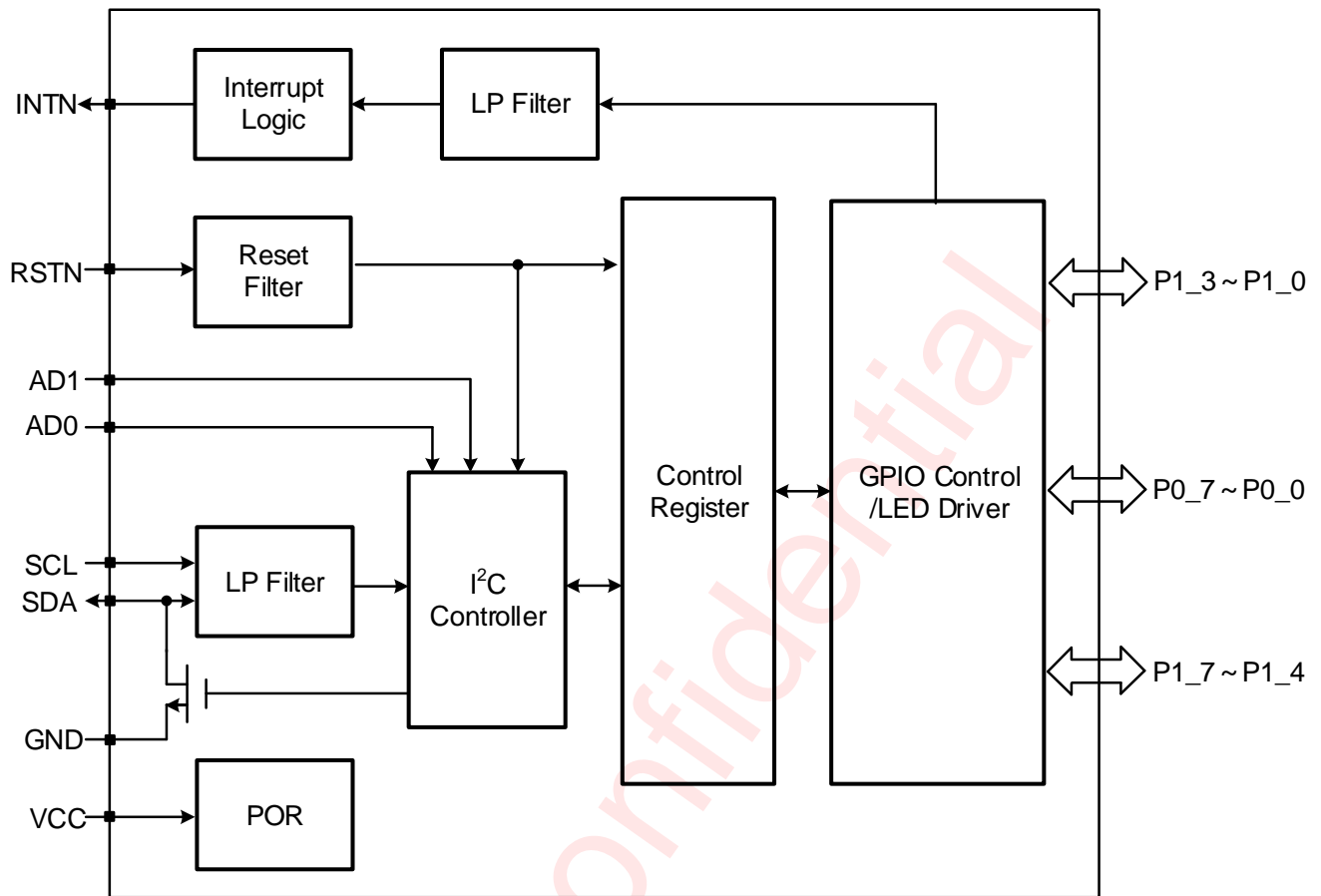


Figure 5 AW9523Q Functional Block

Detailed Description

AW9523Q is a 16 multi-function IO controller, which is applied for LED drive or GPIO. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently.

When configured as GPIO mode, all I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When AW9523Q read GPIO state through the I²C interface, the interrupt is cleared.

When configured as LED drive, drive current range is 0~IMAX, which has 256 steps. Default IMAX is 37mA, and it can be changed in GCR register.

Power On

After power-up, about 100 μ s delay is required before RSTN set to high, otherwise, the device may work incorrectly. The minimal wait time for I²C communication is 5ms, during this period, some internal modules (such as LDO) start to work and reach a stable state.

Below is the recommended operation timing:

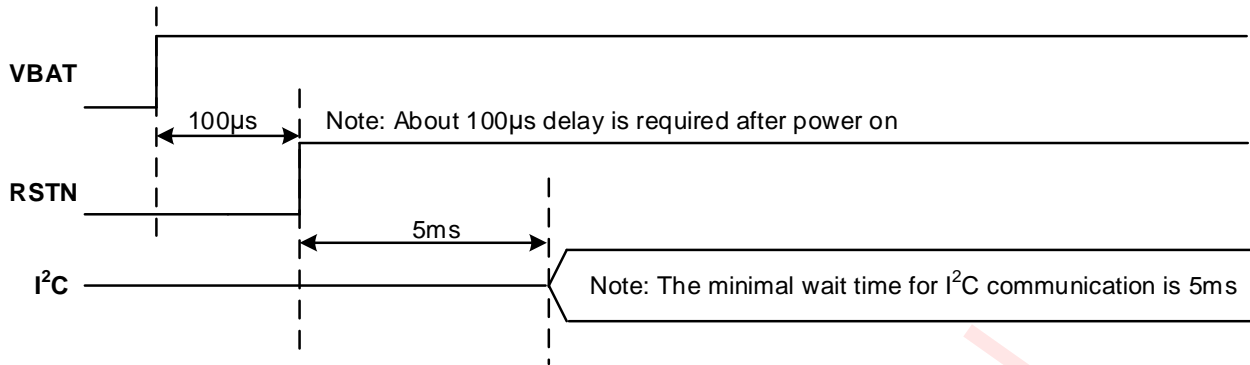


Figure 6 AW9523Q Power On

GPIO Output

After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I²C slave address selection inputs, AD0 and AD1, refer to table 1 for detail. The P1 port is Push-Pull mode; P0 port is Open-Drain mode (default) and can be configured as Push-Pull mode. When P0 port is Open-Drain mode, it need pull-up resistor.

Table 1. Default state of IO ports, AD1/AD0 and P0_x/P1_x

AD1	AD0	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GND	VBAT	0	0	0	0	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VBAT	GND	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	0	0	0	0
VBAT	VBAT	1	1	1	1	1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

GPIO Input/Output Direction Select

The register Config_Port0 and Config_Port1 can configure a port as input or output. Each bit of the register is corresponding to each port, the bit set '1' as input, '0' as output. The default value is '0' as output.

GPIO Input

User can get the current state of GPIO through reading the register Input_Port0 and Input_Port1 by I²C Interface. AW9523Q GPIO support 1.8V logic input.

Interrupt

AW9523Q can monitor IO state to generate interrupt when configure port as GPI and GPIO interrupt enabled. External MCU is required acknowledge by INTN pin. INTN is open-drain output, low-level active, and need external pull-up resistor.

When AW9523Q detect port change, any input state from high-level to low-level or from low-level to high-level will generate interrupt after 8µs internal deglitch. External MCU read Input_Port0/1 register to clear interrupt. P1 port state change must clear interrupt by read Input_Port1 register; P0 port state change must clear interrupt by read Input_Port0 register.

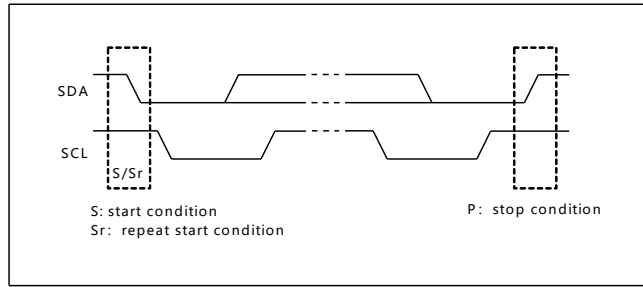


Figure 8 Start and Stop Condition

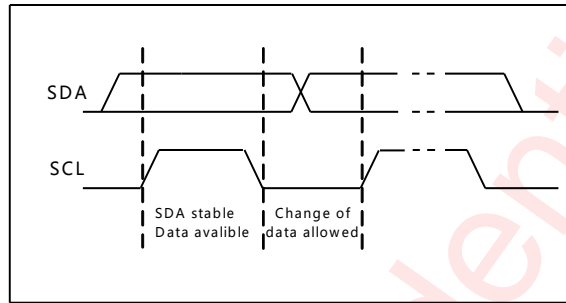


Figure 9 Bit Transfer

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

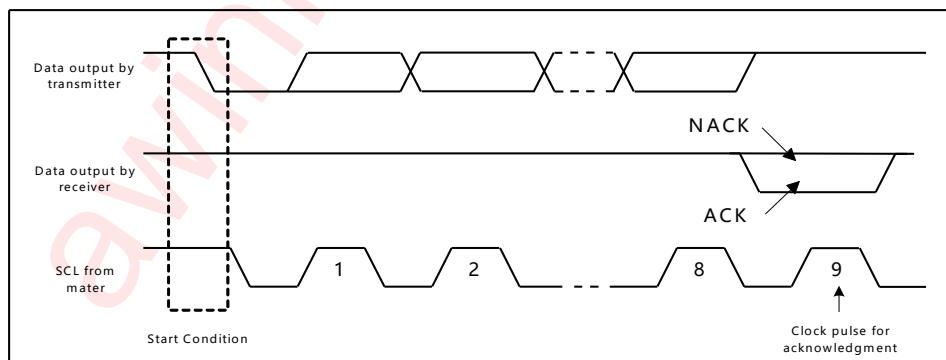
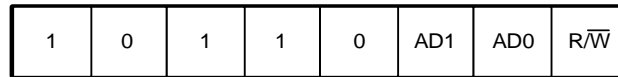


Figure 10 Acknowledgment on I²C Bus

Device Address

Below is the device address of AW9523Q. AD1/AD0 bit in device address match with AD1/AD0 pin respectively.



AD1/AD0 value match with AW9523Q pin AD1/AD0 respectively

Figure 11 AW9523Q Device Address

Write

Data is transmitted to the AW9523Q by sending the device address and setting the least-significant bit to a logic 0. The register address byte is sent after the device address and determines which register receives the data that follows the command byte.

After sending data to one register, the next data byte is sent to the other register. There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

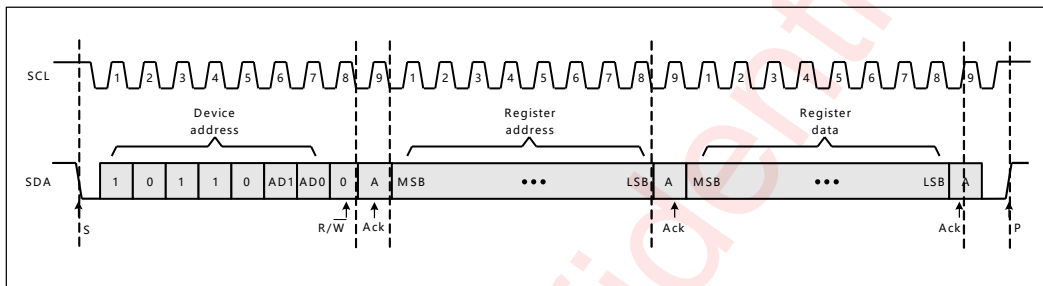


Figure 12 AW9523Q Write Operation

Read

The bus master first must send the AW9523Q address with the least-significant bit set to a logic 0. The register address byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the register address byte then is sent by the AW9523Q.

After a restart, the value of the register defined by the register address byte matches the register being accessed when the restart occurred. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

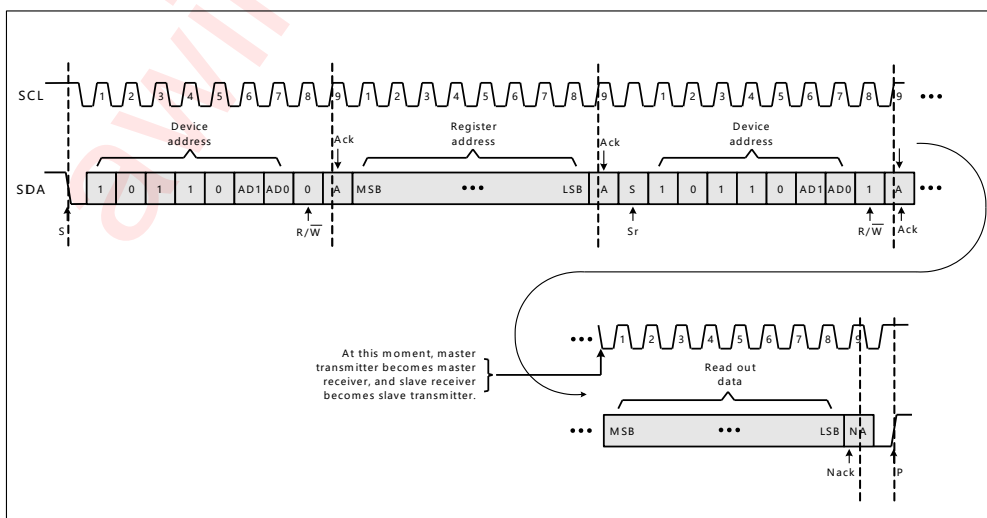


Figure 13 AW9523Q Read Operation

Reset Function

AW9523Q supports 3 reset mode: power on reset, hardware reset, software reset. Each reset mode can reset registers to default value.

Hardware Reset

Hardware reset timing is as the following figure.

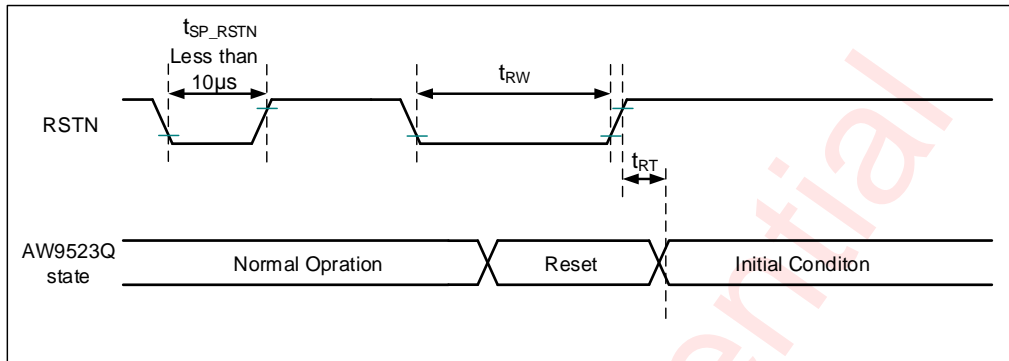


Figure 14 Hardware Reset Timing

Table 3. Hardware Reset Parameter

Parameter	Condition	Min	Typ	Max	Unit
t_{RW}	Reset pulse low level width	20			μs
t_{RT}	Reset recovery time	1			μs

Note:

- The hardware reset pin (RSTN) has a built-in deglitch block. Spike due to an electrostatic discharge on RSTN line does not cause irregular system reset according to the table below:

Reset Pulse (RSTN)	AW9523Q Action
Shorter than $10\mu s$ (typical)	Reset Rejected
Longer than $20\mu s$	Reset

- After reset, AW9523Q is in default state. All GPIO are configured as output, which value is decided by 2 device address (AD1/AD0) (refer to table 1). The interrupt (INTN) is cleared and pulled up by external pull-up resistor.
- Spike Rejection also applies during a valid reset pulse as shown below:

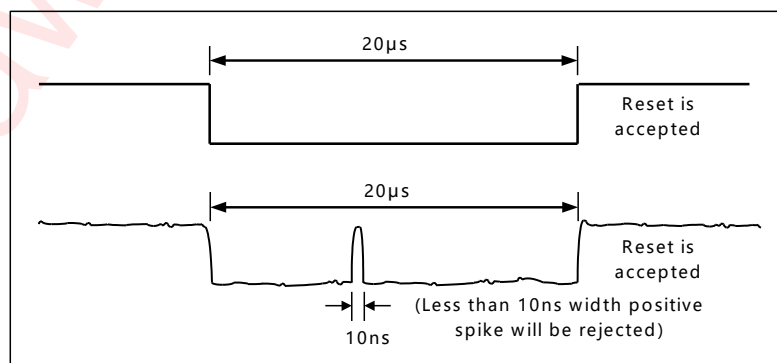


Figure 15 Operation When RSTN Low

Software Reset

AW9523Q support software reset mode. Writing 00H to the software register(7FH) will generate a reset pulse. After software reset, AW9523Q is in default state, which is the same as hardware reset. The software reset timing is as below. After the software reset command is send through the I²C interface, it takes at least 1ms for chip to acknowledge the new I²C command.

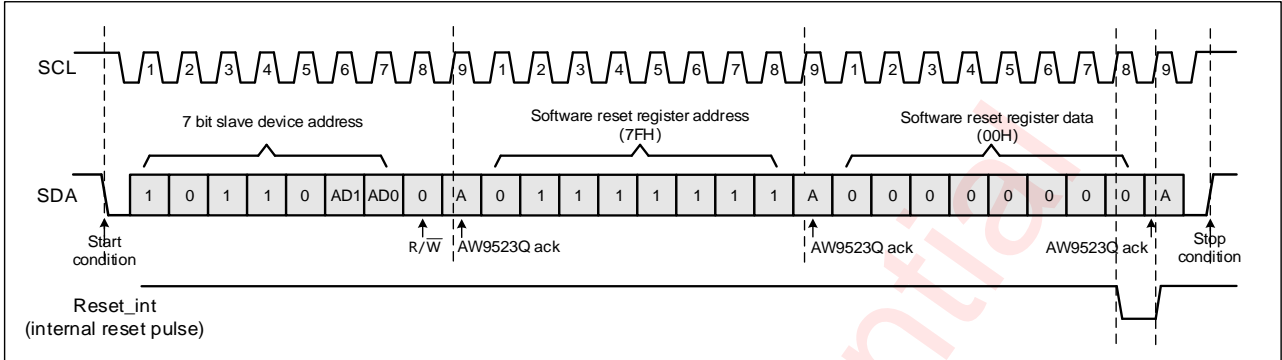


Figure 16 Software Reset Timing

Registers

Table 4. AW9523Q register list

Address	W/R	Default Value	Function	Description
00H	R	Equal to P0	Input_Port0	P0 port input state
01H	R	Equal to P1	Input_Port1	P1 port input state
02H	W/R	Refer to table 1	Output_Port0	P0 port output state
03H	W/R	Refer to table 1	Output_Port1	P1 port output state
04H	W/R	00H	Config_Port0	P0 port direction configure
05H	W/R	00H	Config_Port1	P1 port direction configure
06H	W/R	00H	Int_Port0	P0 port interrupt enable
07H	W/R	00H	Int_Port1	P1 port interrupt enable
10H	R	23H	ID	ID register (read only)
11H	W/R	00H	GCR	Global control register
12H	W/R	FFH	LED Mode Switch	P0 port mode configure
13H	W/R	FFH	LED Mode Switch	P1 port mode configure
20H	W	00H	DIM0	P1_0 LED current control
21H	W	00H	DIM1	P1_1 LED current control
22H	W	00H	DIM2	P1_2 LED current control
23H	W	00H	DIM3	P1_3 LED current control
24H	W	00H	DIM4	P0_0 LED current control
25H	W	00H	DIM5	P0_1 LED current control
26H	W	00H	DIM6	P0_2 LED current control
27H	W	00H	DIM7	P0_3 LED current control
28H	W	00H	DIM8	P0_4 LED current control
29H	W	00H	DIM9	P0_5 LED current control
2AH	W	00H	DIM10	P0_6 LED current control
2BH	W	00H	DIM11	P0_7 LED current control
2CH	W	00H	DIM12	P1_4 LED current control
2DH	W	00H	DIM13	P1_5 LED current control
2EH	W	00H	DIM14	P1_6 LED current control
2FH	W	00H	DIM15	P1_7 LED current control
7FH	W	00H	SW_RSTN	Soft reset
Other	-	-	-	Reserved

Register Detail Description

Table 5. Input state register (00H, 01H)

Address	Name	Description	Default
00H	Input_Port0	P0 port current logic state, 0-low level; 1-high level	X
01H	Input_Port1	P1 port current logic state, 0-low level; 1-high level	X

The Input state registers (00H,01H) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I²C device know that the Input Port registers will be accessed next.

Table 6. Output state register (02H, 03H)

Address	Name	Description	Default
02H	Output_Port0	Set P0 port output value. 0-low level; 1-high level	Refer to table1
03H	Output_Port1	Set P1 port output value. 0-low level; 1-high level	Refer to table1

The Output state register (02H, 03H) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 7. Configuration register (04H, 05H)

Address	Name	Description	Default
04H	Config_Port0	P0 port input/output mode select. 0-output; 1-input	00H
05H	Config_Port1	P1 port input/output mode select. 0-output; 1-input	00H

The Configuration registers (04H, 05H) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 8. Interrupt enable register (06H, 07H)

Address	Name	Description	Default
06H	Int_Port0	P0 port interrupt enable. 0-enable; 1-disable	00H
07H	Int_Port1	P1 port interrupt enable. 0-enable; 1-disable	00H

The Interrupt enable register (06H, 07H) are used to configure the interrupt enable or disable of GPIO. If a bit in this register is set to 1, the interrupt function of the corresponding port pin is disabled. If a bit in this register is cleared to 0, the interrupt function of corresponding port pin is enabled.

Table 9. ID register (10H)

Address	Name	Description	Default
10H	ID	ID register, read only, the readout value is 23H	23H

ID register (10H) is a read only register which stores the device ID. The ID read value of AW9523Q is 23H.

Table 10. GCR, Global control register (11H)

Address	Name	Description	Default
D[7:5]	reserved	-	-
D[4]	GPOMD	Set P0 port GPIO output drive mode. if D[4]=0, P0 port is Open-Drain mode; if D[4]=1, P0 port is Push-Pull mode.	0
D[3:2]	reserved	-	-
D[1:0]	ISEL	256 step dimming range select 00: 0~ I_{MAX} 01: 0~($I_{MAX} \times 3/4$) 10: 0~($I_{MAX} \times 2/4$) 11: 0~($I_{MAX} \times 1/4$)	00

D[4] is used to configure P0 port output drive as Open-Drain or Push-Pull mode. When P0 port use as output with Open-Drain mode, it needs pull-up resistor. If in Push-Pull mode, it needs no pull-up resistor.

D[1:0] is used to configure the max drive current of LED. AW9523Q set max current I_{MAX} to 37mA(typical) default, and through register ISEL[1:0] can set to $I_{MAX} \times 1/4$, $I_{MAX} \times 2/4$, $I_{MAX} \times 3/4$, I_{MAX} , so the 256 step dimming range changes.

Except D4, D[1:0], other bits (D[7:5]\D[3:2]) are used for test purpose and the default value is 0. If user needs to configure register 11H, then the bits D[7:5]\D[3:2] must configure to 0, or system function error may occur.

Table 11. LED mode switch register (12H)

Address	Name	Description	Default
12H	LED Mode Switch	Configure P0_7~P0_0 as LED or GPIO mode. 1: GPIO mode 0: LED mode	FFH

LED mode switch register (12H) can configure P0 port as LED or GPIO mode. After reset, it is GPIO mode as default. Set a bit of 12H[7:0] to 0 so the corresponding port is LED mode, and set to 1 so the corresponding port is GPIO mode.

Table 12. LED mode switch register (13H)

Address	Name	Description	Default
13H	LED Mode Switch	Configure P1_7~P1_0 as LED or GPIO mode. 1: GPIO mode 0: LED mode	FFH

LED mode switch register (13H) can configure P1 port as LED or GPIO mode. After reset, it is GPIO mode as default. Set a bit of 13H[7:0] to 0 so the corresponding port is LED mode, and set to 1 so the corresponding port is GPIO mode.

Table 13. 256 step dimming control register (20H~2FH)

Address	Name	Description	Default
20H	DIM0	P1_0 port LED current control	00H
21H	DIM1	P1_1 port LED current control	00H
22H	DIM2	P1_2 port LED current control	00H
23H	DIM3	P1_3 port LED current control	00H
24H	DIM4	P0_0 port LED current control	00H

Address	Name	Description	Default
25H	DIM5	P0_1 port LED current control	00H
26H	DIM6	P0_2 port LED current control	00H
27H	DIM7	P0_3 port LED current control	00H
28H	DIM8	P0_4 port LED current control	00H
29H	DIM9	P0_5 port LED current control	00H
2AH	DIM10	P0_6 port LED current control	00H
2BH	DIM11	P0_7 port LED current control	00H
2CH	DIM12	P1_4 port LED current control	00H
2DH	DIM13	P1_5 port LED current control	00H
2EH	DIM14	P1_6 port LED current control	00H
2FH	DIM15	P1_7 port LED current control	00H

The dimming control register (20H~2FH) are used to configure P0 port and P1 port LED current. Each port supports 256 step dimming. For the detailed configuration, refer to table 2.

Table 13. Soft reset register (7FH)

Address	Name	Description	Default
7FH	Software Reset	Write 00H to generate a reset pulse	X

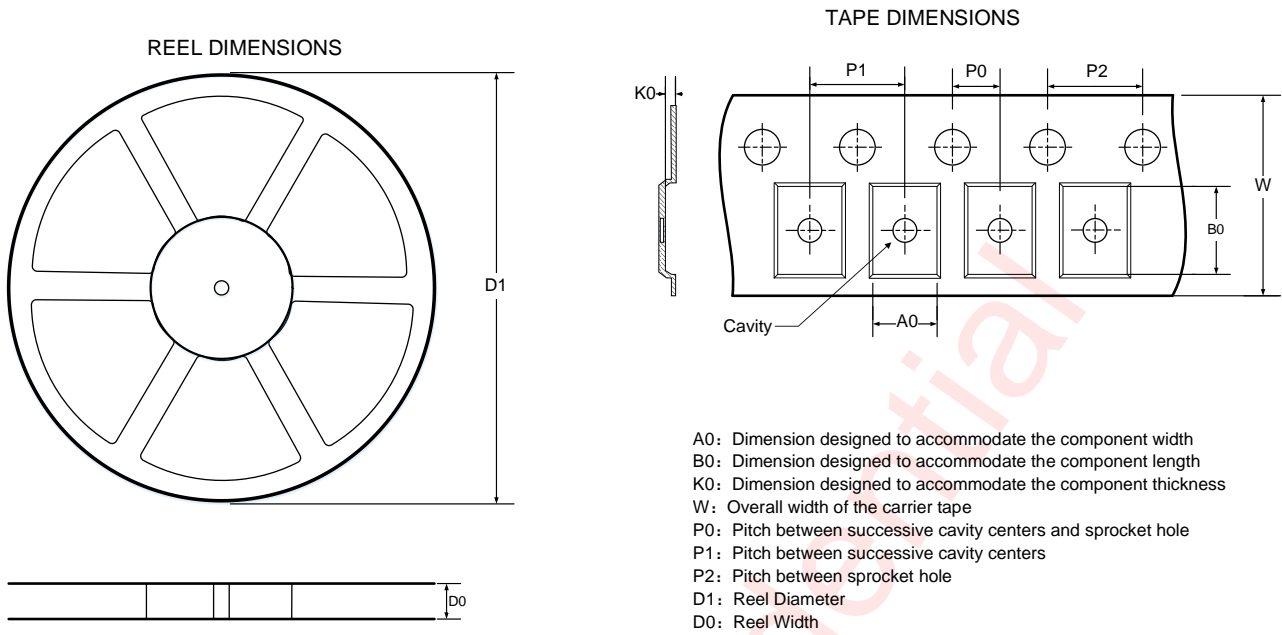
The soft reset register (7FH) support software reset function, which brings convenience to software engineer. Every time write 00H to this register, it generate a reset pulse. The software reset timing, please refer to figure 14.

Table 14. Reserve register

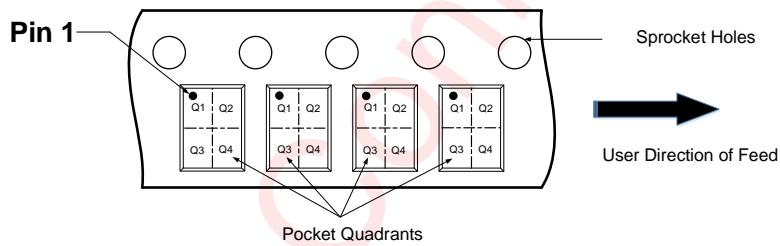
Address	Name	Description
08H~0FH 14H~1FH 30H~7EH 80H~FFH		Reserve register, for test purpose or not defined.

Reserve register (08H~0FH, 14H~1FH, 30H~7EH, 80H~FFH) are for test purpose or not defined, user should not write these registers, or may cause function error.

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



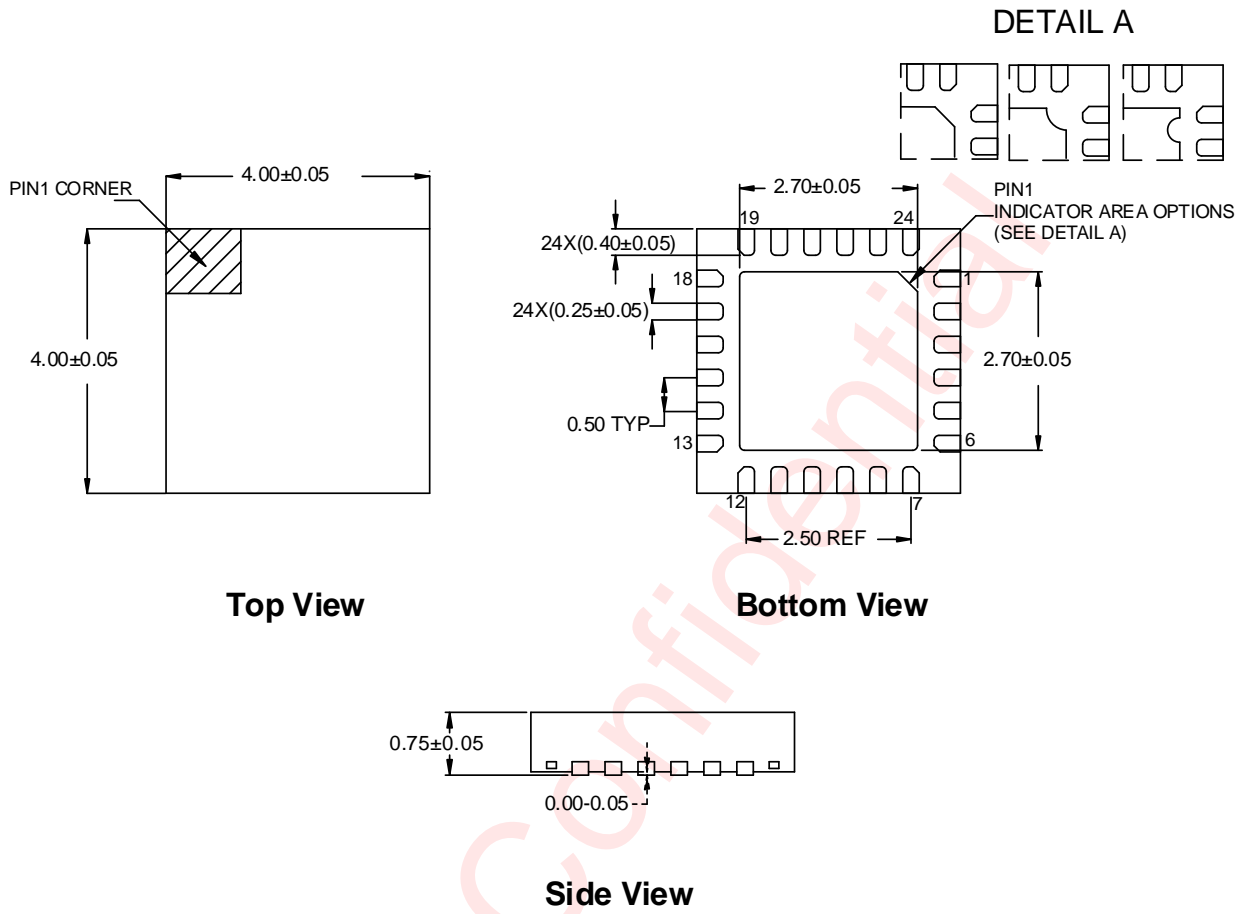
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	4.3	4.3	1.1	2	8	4	12	Q1

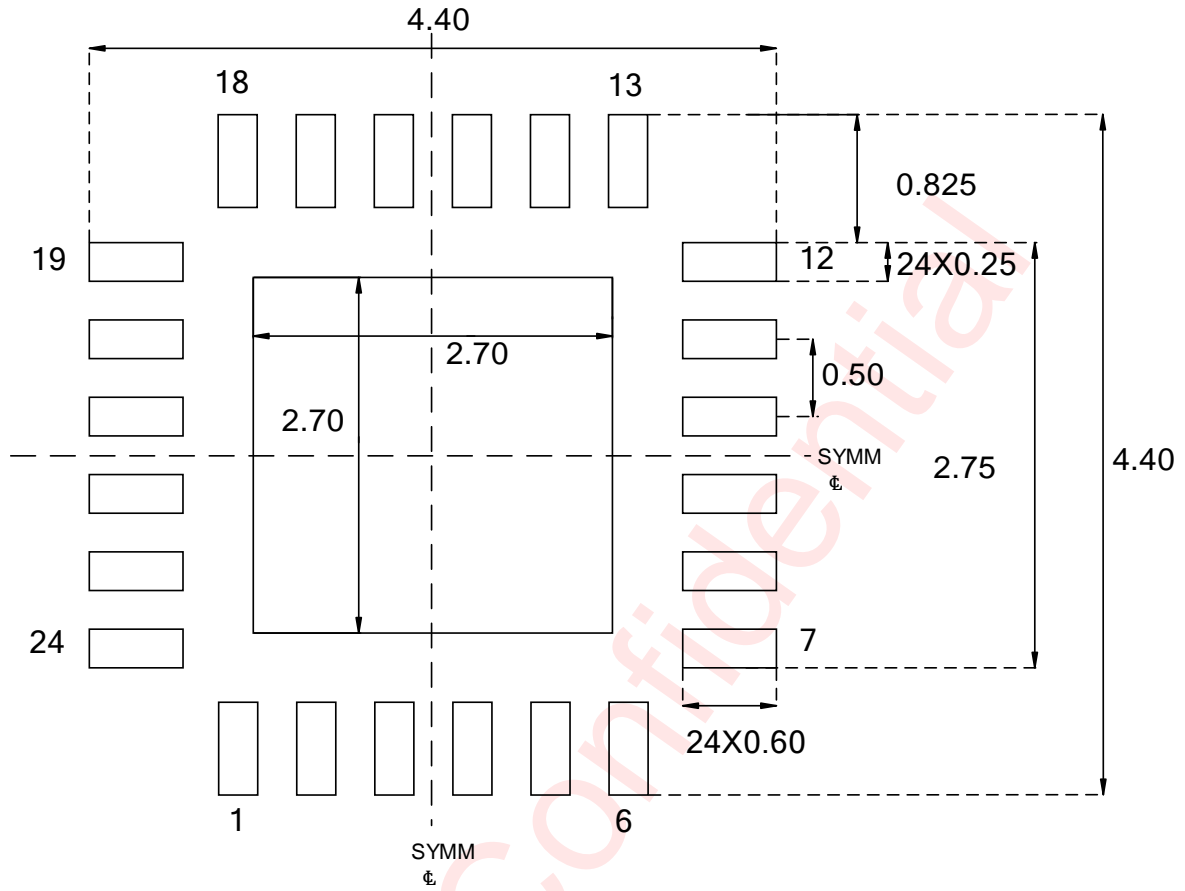
All dimensions are nominal

Package Description



All Dimensions are in Millimeters

Land Pattern Data



All Dimensions are in Millimeter

Revision History

Version	Date	Change Record
V1.0	Sep 2023	Officially Released

awinic Confidential

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