

## 8.5V Smart Adaptive DO-Charge pump High Efficiency Low Noise Multi-Level AGC Smart K Audio Amplifier

### FEATURES

- Multi-Level AGC audio algorithm, effectively eliminates noise and makes sound smooth
- Smart Adaptive DO-Charge pump technology(Patented):
  - Low Quiescent current: 4.5mA@3.6V
  - Overall efficiency up to 88%
- Output Power: 2.8W@8Ω ; 3.1W@6Ω
- Low Noise:
  - RCV: 7μV
  - SPK: 20μV
- Low THD+N: 0.03%
- Support high power receiver stereo application
- Support D speaker , D receiver 2-in-1 application
  - LRCV receiver: 0dB, En=7μV, 0.14W@THD+N=1%
  - SRCV receiver: 0dB, En=8μV, 0.56W@THD+N=1%
- Support 1.8V I<sup>2</sup>C Control
- Over current protection, over-temperature protection and short-circuit protection
- Super TDD-Noise suppression
- Excellent pop-click suppression
- High PSRR: 85dB (217Hz)
- FCQFN 2.5mmX2.0mmX0.55mm-16L package

### APPLICATIONS

- Smart phone、Tablet PC、Tactile feedback

### DESCRIPTION

AW87392E is specifically designed to improve the musical output dynamic range, enhance the overall sound quality, which is a new high efficiency, low noise, constant large volume, Smart K audio amplifier. AW87392E integrates awinic's proprietary Multi-Level AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87392E integrated efficiency up to 95.4% of Adaptive DO-Charge pump technology, significantly improving the dynamic range of the music output and power consumption of audio system. AW87392E noise floor is as low as to 20μV at speaker mode, with 105dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.03% and unique Multi-Level AGC technology bring high quality music enjoyment.

AW87392E controls internal registers through the I<sup>2</sup>C interface. Register parameters include output voltage, power amplifier gain, Multi-Level AGC parameters etc.

AW87392E built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87392E features small FCQFN 2.5mmX2.0mmX0.55mm-16L package.

### TYPICAL APPLICATION CIRCUIT

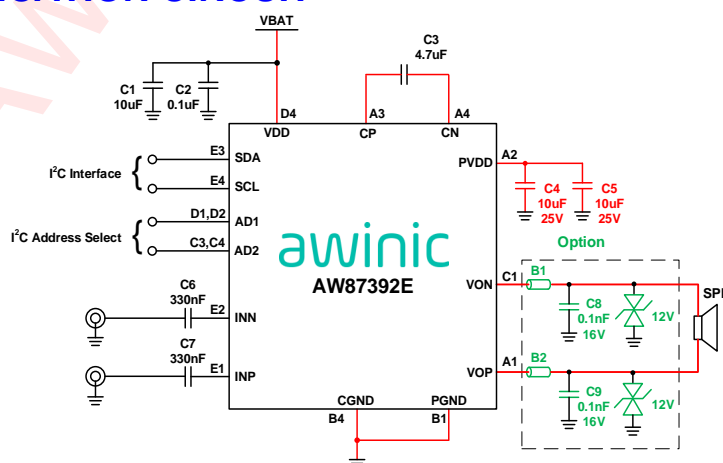


Figure 1 AW87392E Typical Application Diagram

Note: Traces carry high current are marked in red in the above figure

## PIN CONFIGURATION AND TOP MARK

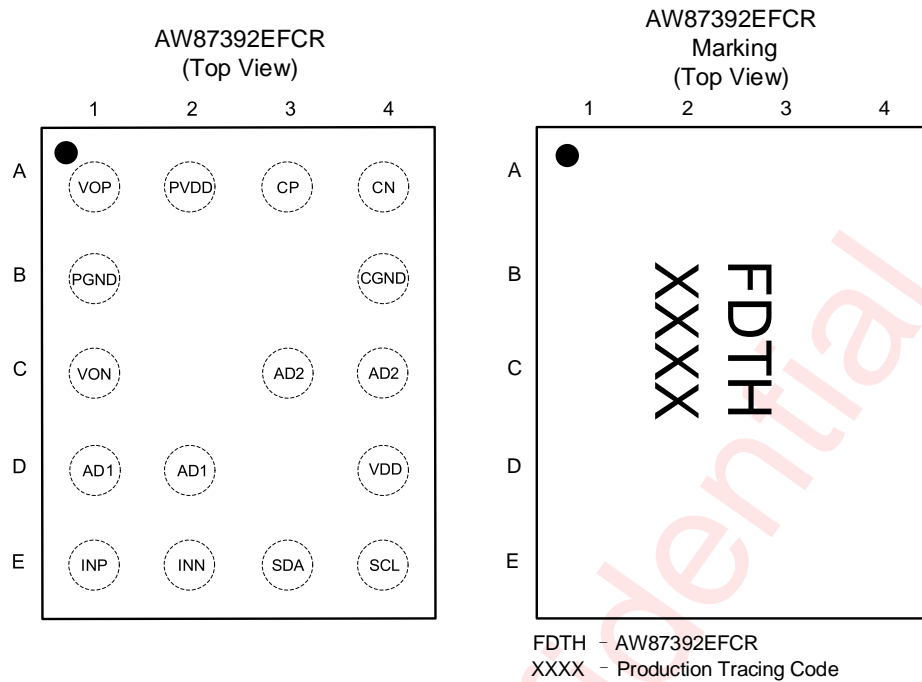


Figure 2 AW87392E Pin configuration and Top Mark

## PIN DEFINITION

No.	NAME	DESCRIPTION
A1	VOP	Positive audio output terminal
A2	PVDD	Charge Pump output voltage
A3	CP	Positive input Charge Pump Flying Capacitance
A4	CN	Negative input Charge Pump Flying Capacitance
B1	PGND	Amplifier power ground
B4	CGND	Charge Pump power ground
C1	VON	Negative audio output terminal
C3,C4	AD2	I <sup>2</sup> C address pin2
D1,D2	AD1	I <sup>2</sup> C address pin1
D4	VDD	Power supply
E1	INP	Positive audio input terminal
E2	INN	Negative audio input terminal
E3	SDA	I <sup>2</sup> C-bus data input/output
E4	SCL	I <sup>2</sup> C-bus clock input

FUNCTIONAL DIAGRAM

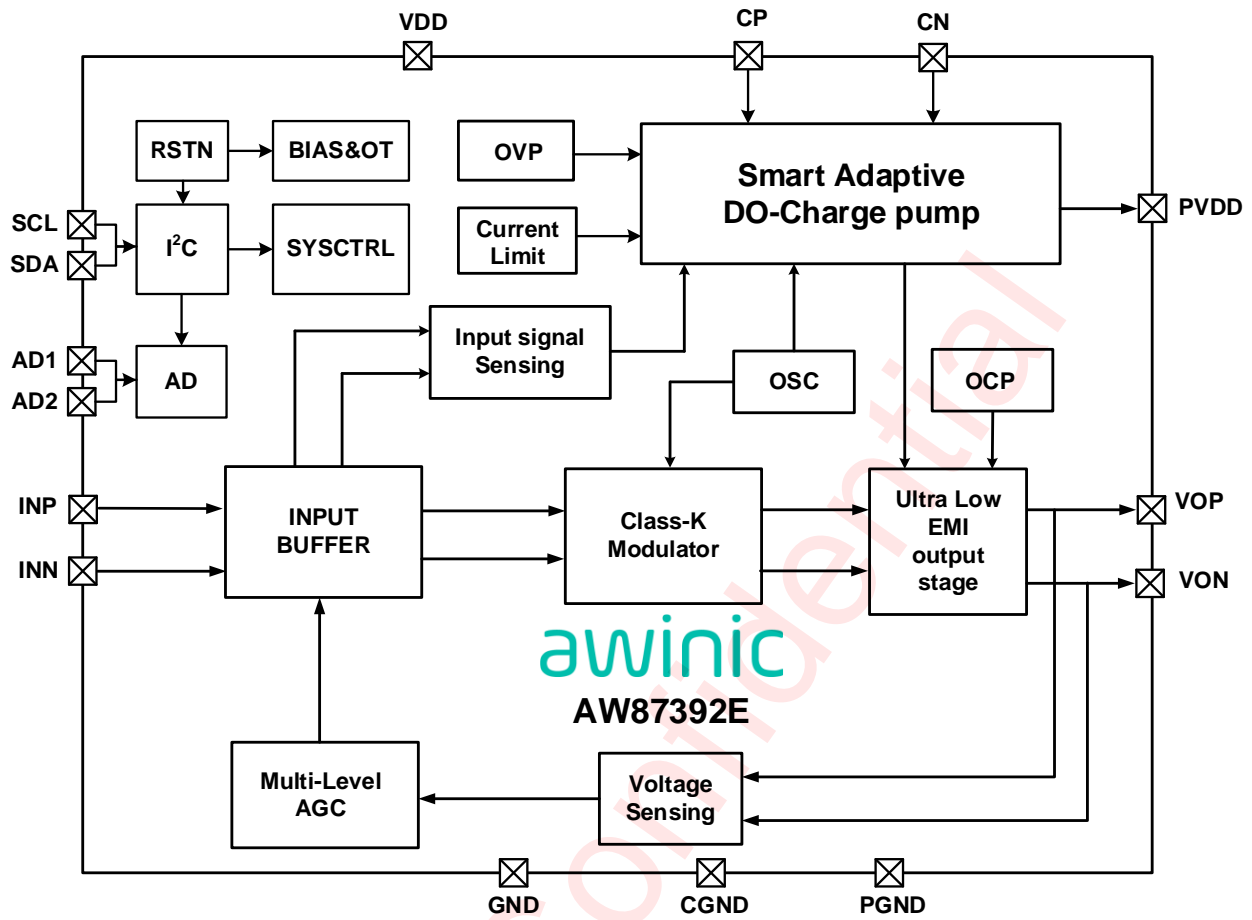
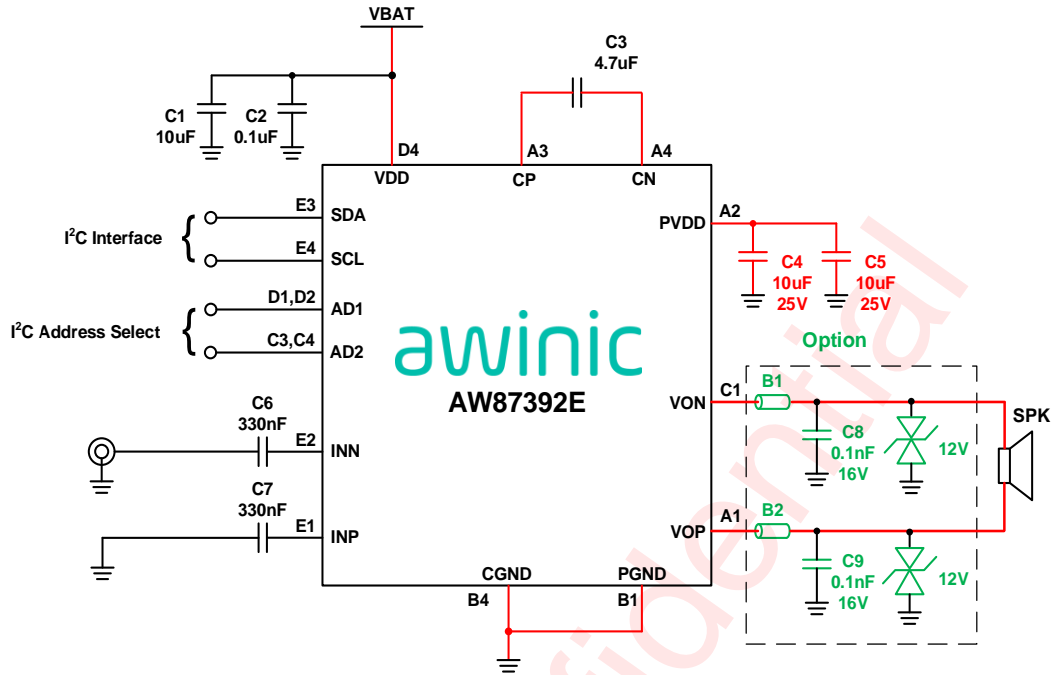


Figure 3 AW87392E Functional Diagram

## Typical Application Circuits

Figure 4 AW87392E Single-ended Input Mode Application Diagram<sup>(Note 1)</sup>

**Note1:** When single-ended input, audio signal line from audio DAC (HPL or HPR) can arbitrarily connected to either of INN or INP input terminal. The other terminal must be connected to reference ground (HPREF) through input capacitor and resistor.

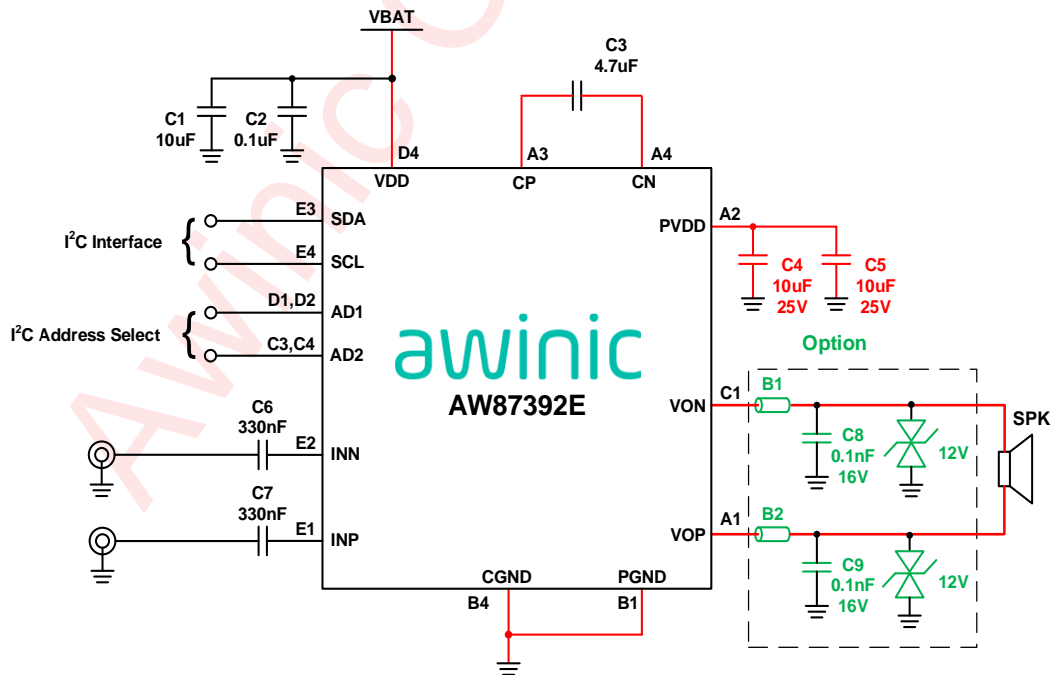


Figure 5 AW87392E Differential Inputs Mode Application Diagram

## ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW87392EFCR	-40°C~85°C	FCQFN 2.5x2-16L(0.55)	FDTH	MSL1	ROHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS<sup>(NOTE1)</sup>

Parameter	Range
Supply Voltage $V_{DD}$	-0.3V to 6V
INN,INP	-0.3V to $V_{DD}+0.3V$
Charge pump output voltage $PV_{DD}$	-0.3V to 9.5V
VOP,VON	-0.6V to $PV_{DD}+0.6V$
CP	-0.3V to $PV_{DD}+0.3V$
CN	-0.3V to $V_{DD}+0.3V$
Minimum load resistance $R_L$	5Ω
Package Thermal Resistance $\theta_{JA}$	60.64°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature $T_{JMAX}$	165°C
Storage Temperature Range $T_{STG}$	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating <sup>(Note 3)</sup>	
HBM (human body model)	±2kV
CDM (charged-device model)	±1.5kV
Latch-up	
Test Condition: JEDEC STANDARD NO.78E	+IT: 200mA -IT: -200mA

**NOTE2:** Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

**NOTE3:** The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2024.

Test method of the charge device model: ESDA/JEDEC JS-002-2025.

## Electrical Characteristics

Test condition:  $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=3.6\text{V}$ ,  $PVDD\text{ OVP}=8.5\text{V}$ ,  $R_L=8\Omega+33\mu\text{H}$ ,  $f=1\text{kHz}$  (unless otherwise noted)

Parameter		Test conditions	Min	Typ	Max	Units
$V_{DD}$	Power supply voltage		2.5		5.5	V
UVLO	Under-voltage protection voltage			2.0		V
	Under-voltage protection hysteresis voltage			90		mV
$V_{IH}$	SCL, SDA, AD1, AD2 high-level input voltage		1.3		VDD	V
$V_{IL}$	SCL, SDA, AD1, AD2 low-level input voltage		0		0.45	V
$I_{SB}$	Standby current	$V_{DD}=3.6\text{V}$		3		$\mu\text{A}$
$T_{SD}$	Over temperature protection threshold			160		$^{\circ}\text{C}$
$T_{SDR}$	Over temperature protection recovery threshold			130		$^{\circ}\text{C}$
$T_{ON}$	Turn-On time	$C_{in}=330\text{nF}$		45		ms
<b>ADP DO-Charge pump</b>						
PVDD	The maximum Output voltage	$V_{DD}=2.5\text{V to }4.25\text{V}$ , $PVDD\text{ OVP}=8.5\text{V}$		$2*V_{DD}$		V
		$V_{DD} > 4.25\text{V}$		8.5 <sup>(Note4)</sup>		V
OVP	OVP voltage	$V_{DD} > 4.25\text{V}$		8.5 <sup>(Note4)</sup>		V
	OVP hysteresis voltage	$V_{DD} > 4.25\text{V}$		50		mV
$F_{CP}$	Charge pump operating frequency	$V_{DD}=2.5\text{V to }5.5\text{V}$	1.53		1.9	MHz
$\eta_{CP}$	Charge pump efficiency	$V_{DD} = 4.25\text{V}$ , $I_{load} = 200\text{mA}$		95.4		%
$T_{ST}$	Softstart Time	No load, $C_{OUT}=4.7\mu\text{F}$		1		ms
<b>LSPK MODE</b>						
$V_{OS}$	Output offset voltage	No input	-6		6	mV
$I_q$	Speaker quiescent current	$V_{DD}=3.6\text{V}$ , input ac grounded, $R_L=8\Omega+33\mu\text{H}$		11.3		mA
$\eta$	Total efficiency(CP+Class D)	$V_{DD}=4.25\text{V}$ , $P_o=1.2\text{W}$ , $R_L=8\Omega+33\mu\text{H}$ , $PVDD\text{ OVP}=8.5\text{V}$		83		%
$V_{inp}$	Recommended input signal amplitude				1.414	Vp
$F_{osc}$	Modulation frequency	$V_{DD}=2.5\text{V to }5.5\text{V}$	764		950	kHz
P <sub>agc</sub>	Multi-Level AGC power	$R_L=8\Omega+33\mu\text{H}$	0.72	0.8 <sup>(Note4)</sup>	0.88	W
		$R_L=6\Omega+33\mu\text{H}$	0.96	1.067 <sup>(Note4)</sup>	1.17	W
PSRR	Power supply rejection ratio	$V_{DD}=4.2\text{V}$ , $V_{pp\_sin}=200\text{mV}$	217Hz		85	dB
			1kHz		80	dB
SNR	Signal-to-noise ratio	$V_{DD}=4.2\text{V}$ , $PVDD\text{ OVP}=8.5\text{V}$ , $A_v=18\text{dB}$ , $THD+N=1\%$ , $R_L=8\Omega+33\mu\text{H}$ ,		105		dB
		$V_{DD}=4.2\text{V}$ , $PVDD\text{ OVP}=8.5\text{V}$ , $A_v=18\text{dB}$ , $P_o=0.8\text{W}$ , $R_L=8\Omega+33\mu\text{H}$		100		dB
$E_N$	Speaker Output noise	$A_v=24\text{dB}$ , LSPK Mode	20Hz to 20kHz, input ac grounded, A-weighting		30	$\mu\text{V}$
		$A_v=18\text{dB}$ , LSPK Mode			20	$\mu\text{V}$
		$A_v=18\text{dB}$ , NSPK Mode			30	$\mu\text{V}$
$A_v$	Speaker gain	$V_{DD}=2.5\text{V to }5.5\text{V}$		18 <sup>(Note4)</sup>		dB
R <sub>ini</sub>	Speaker Inner input resistance	$A_v=24\text{dB}$ , LSPK Mode		2.5		k $\Omega$
		$A_v=18\text{dB}$ , LSPK Mode		5		k $\Omega$
		$A_v=18\text{dB}$ , NSPK Mode		18		k $\Omega$
$F_{in}$	Speaker input Cut-off frequency	$C_{in}=330\text{nF}$ , $A_v=24\text{dB}$ , LSPK Mode		192.9		Hz

Parameter		Test conditions	Min	Typ	Max	Units
		Cin=330nF, Av=18dB, LSPK Mode		96.5		Hz
		Cin=100nF, Av=18dB, NSPK Mode		88.4		Hz
THD+N	Total harmonic distortion + noise	VDD=4.2V, Po=0.6W, RL=8Ω+33μH, f=1kHz, PVDD OVP=8.5V		0.03		%
Rdson	Drain-Source on-state resistance	High side MOS + Low side MOS		400		mΩ
Po	Speaker Output Power	THD+N=1%, RL=8Ω+33μH, VDD=4.3V, PVDD OVP=8.5V		2.8		W
		THD+N=1%, RL=8Ω+33μH, VDD=4.2V, PVDD OVP=8.5V		2.7		W
		THD+N=10%, RL=8Ω+33μH, VDD=4.2V, PVDD OVP=8.5V		3.3		W
		THD+N=1%, RL=6Ω+33μH, VDD=4.3V, PVDD OVP=8.5V		3.1		W
		THD+N=1%, RL=6Ω+33μH, VDD=4.2V, PVDD OVP=8.5V		3.0		W
		THD+N=10%, RL=6Ω+33μH, VDD=4.2V, PVDD OVP=8.5V		3.6		W
		THD+N=1%, RL=8Ω+33μH, VDD=3.6V, PVDD OVP=8.5V		1.9		W
		THD+N=10%, RL=8Ω+33μH, VDD=3.6V, PVDD OVP=8.5V		2.4		W
		THD+N=1%, RL=6Ω+33μH, VDD=3.6V, PVDD OVP=8.5V		2.2		W
		THD+N=10%, RL=6Ω+33μH, VDD=3.6V, PVDD OVP=8.5V		2.6		W
<b>ADP MODE</b>						
V <sub>OS</sub>	Output offset voltage	No input	-6		6	mV
I <sub>q</sub>	Speaker quiescent current	V <sub>DD</sub> =3.6V, input ac grounded, R <sub>L</sub> =8Ω+33μH		4.5		mA
P <sub>th</sub>	Adaptive power threshold	V <sub>DD</sub> =3.5V to 4.25V		0.04*V <sub>DD</sub> <sup>2</sup> (Note4)		W
η	Total efficiency (CP+Class D)	V <sub>DD</sub> =4.25V, Po=0.65W, R <sub>L</sub> =8Ω+33μH, PVDD OVP=8.5V		88		%
		V <sub>DD</sub> =3.6V, Po=0.45W, R <sub>L</sub> =8Ω+33μH, PVDD OVP=8.5V		88		%
PSRR	Power supply rejection ratio	V <sub>DD</sub> =4.2V, V <sub>pp_sin</sub> =200mV	217Hz	80		dB
			1kHz	80		dB
E <sub>N</sub>	Speaker Output noise	Av=24dB, LADP Mode	20Hz to 20kHz, input ac grounded, A-weighting	30		μV
		Av=18dB, LADP Mode		20		μV
		Av=18dB, NADP Mode		30		μV
THD+N	Total harmonic distortion + noise	VDD=4.2V, Po=0.6W, RL=8Ω+33μH, f=1kHz, PVDD OVP=8.5V		0.03		%
<b>Receiver MODE (1X Charge pump)</b>						
V <sub>OS</sub>	Output offset voltage	No input	-6		6	mV
I <sub>q</sub>	Receiver quiescent current (overall)	V <sub>DD</sub> =3.6V, input ac grounded, R <sub>L</sub> =8Ω+33μH		4.5		mA
η	SRCV efficiency	V <sub>DD</sub> =4.25V, Po=0.5W, Av=9dB, R <sub>L</sub> =8Ω+33μH		88.5		%
	LRCV efficiency	V <sub>DD</sub> =4.25V, Po=0.1W, Av=0dB, R <sub>L</sub> =8Ω+33μH		78		%
Av	Receiver gain	V <sub>DD</sub> =2.5V to 5.5V		0 <sup>(Note4)</sup>		dB
R <sub>ini</sub>	SRCV Inner input resistance	Av=0dB		8		kΩ
		Av=6dB		8		kΩ

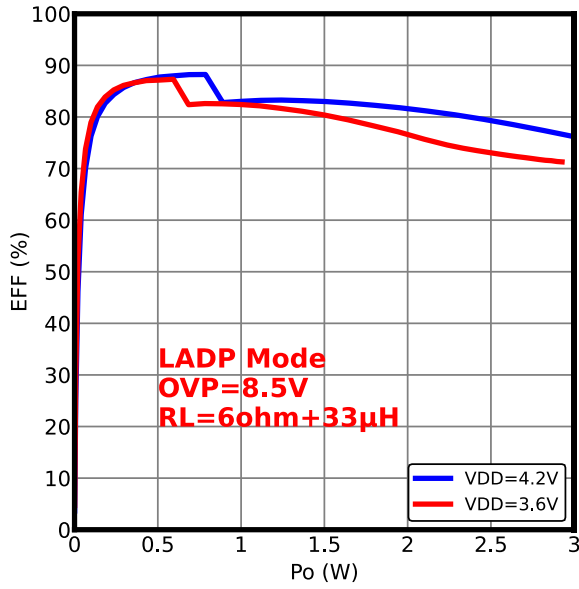
Parameter		Test conditions	Min	Typ	Max	Units
	LRCV Inner input resistance	Av=0dB		8		kΩ
	NRCV Inner input resistance	Av=0dB		8		kΩ
Fin	SRCV input cut-off frequency	Cin=330nF, Av=0dB		60		Hz
		Cin=330nF, Av=6dB		60		Hz
	LRCV input cut-off frequency	Cin=330nF, Av=0dB		60		Hz
	NRCV input cut-off frequency	Cin=100nF, Av=0dB		33.2		Hz
EN	SRCV Output noise	Av=0dB		8		μV
		Av=6dB	20Hz to 20kHz, input ac grounded, A-weighting	11.5		μV
	LRCV Output noise	Av=0dB		7		μV
	NRCV Output noise	Av=0dB		10		μV
THD+N	Total harmonic distortion + noise	VDD=4.2V, Po=0.1W, RL=8Ω+33μH, f=1kHz		0.01		%
PSRR	Receiver Power supply rejection ratio	VDD=4.2V, Vp-p_sin=200mV	217Hz	82		dB
			1kHz	81		dB
Po	SRCV Output Power	Av=0dB, THD+N=1%, RL=8Ω+33μH, VDD=4.25V, single-ended input		0.32		W
		Av=9dB, THD+N=1%, RL=8Ω+33μH, VDD=4.25V, single-ended input		0.96		W
		Av=0dB, THD+N=1%, RL=8Ω+33μH, VDD=4.25V, differential input		0.56		W
		Av=9dB, THD+N=1%, RL=8Ω+33μH, VDD=4.25V, differential input		0.96		W
	LRCV Output Power	Av=0dB, THD+N=1%, RL=8Ω+33μH, VDD=4.25V, single-ended input		0.15		W
		Av=0dB, THD+N=1%, RL=8Ω+33μH, VDD=4.25V, differential input		0.15		W
	NRCV Output Power	Av=0dB, THD+N=1%, RL=8Ω+33μH, VDD=4.25V, single-ended input		0.38		W
		Av=0dB, THD+N=1%, RL=8Ω+33μH, VDD=4.25V, differential input		0.57		W
<b>Multi-Level AGC</b>						
TAT1	AGC1 Attack Time			0.16 (Note4)		ms/dB
TAT2	AGC2 Attack Time			41 (Note4)		ms/dB
TRLT	Release time			21 (Note4)		ms/dB
AMAX	The maximum attenuation gain	VDD=2.5V to 5.5V		-13.5		dB

**Note 4:** Registers are adjustable; Refer to the list of registers.

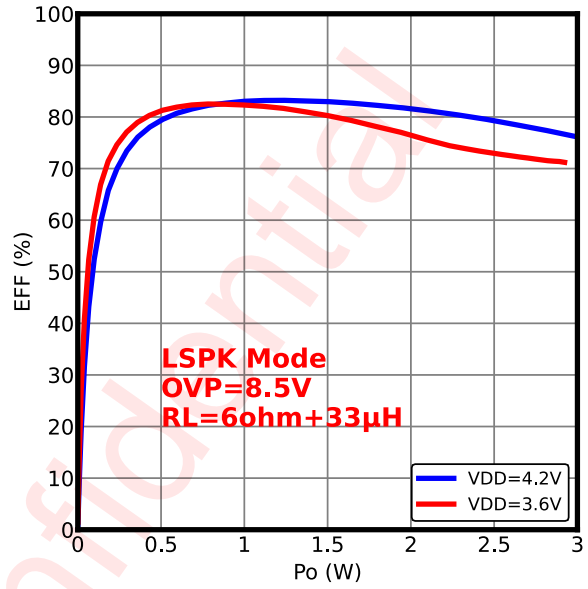
## Typical Characteristics

T<sub>A</sub>=25°C

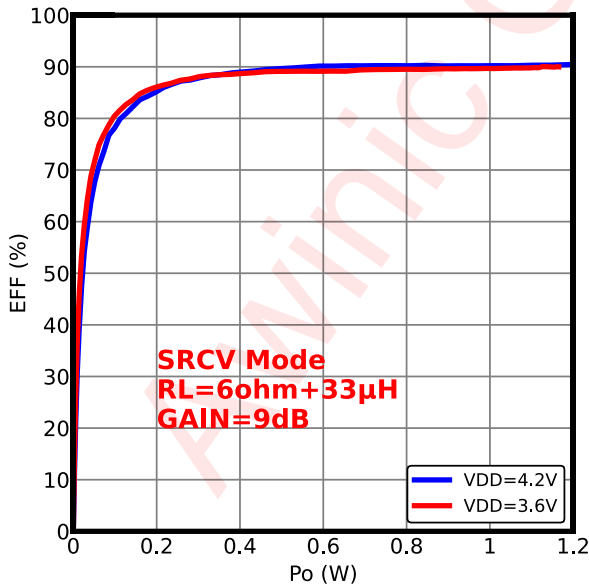
Efficiency VS. Output Power



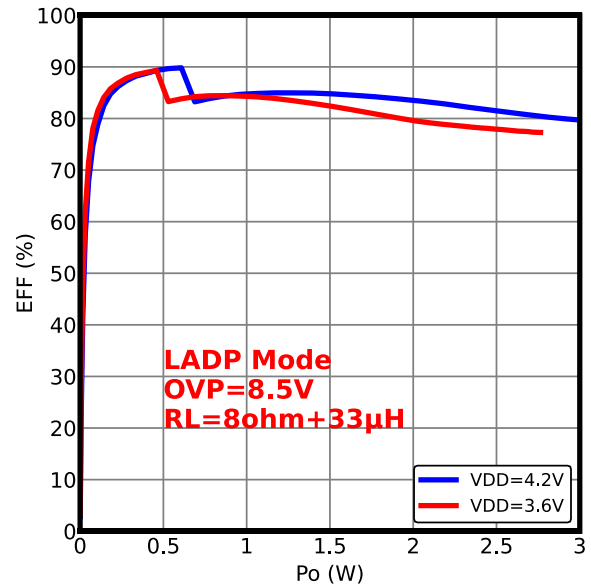
Efficiency VS. Output Power



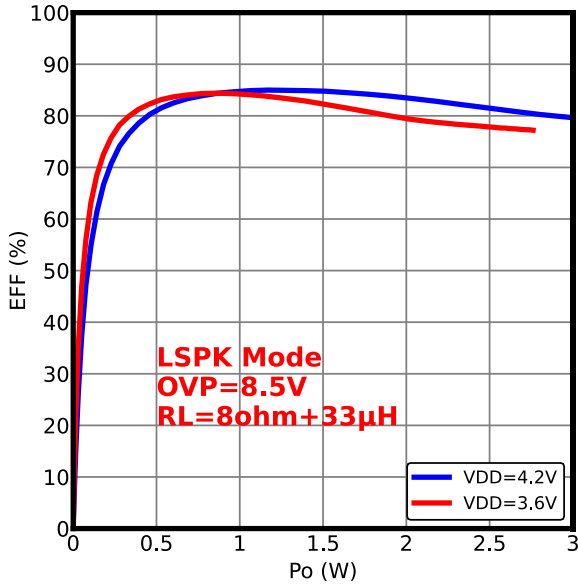
Efficiency VS. Output Power



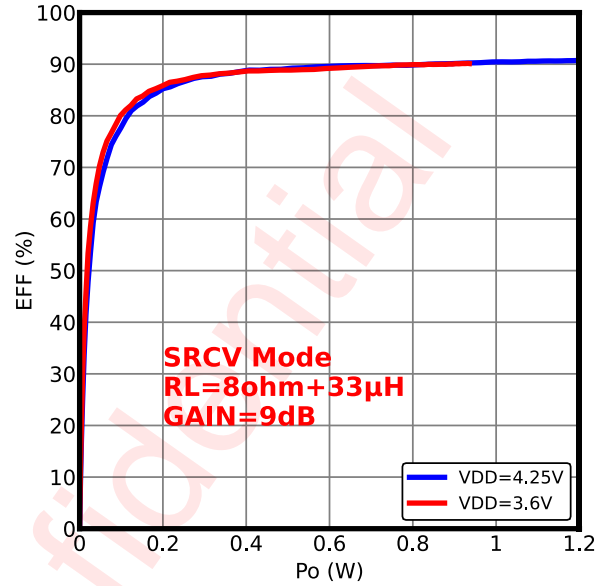
Efficiency VS. Output Power



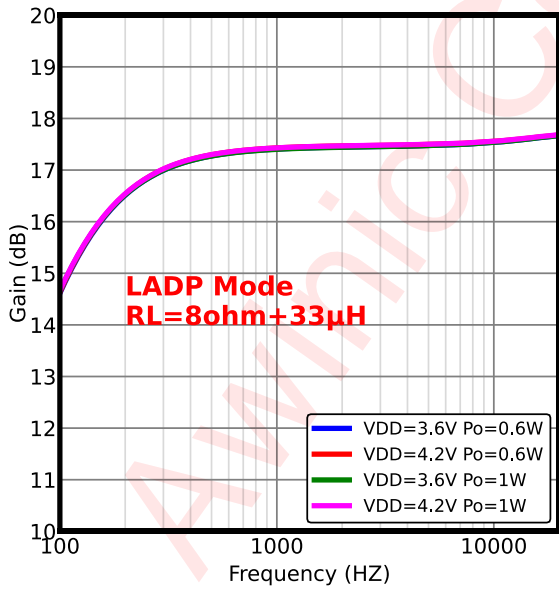
Efficiency VS. Output Power



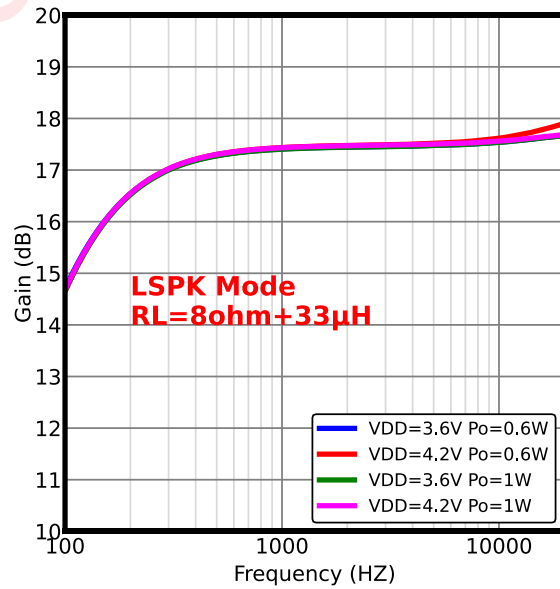
Efficiency VS. Output Power



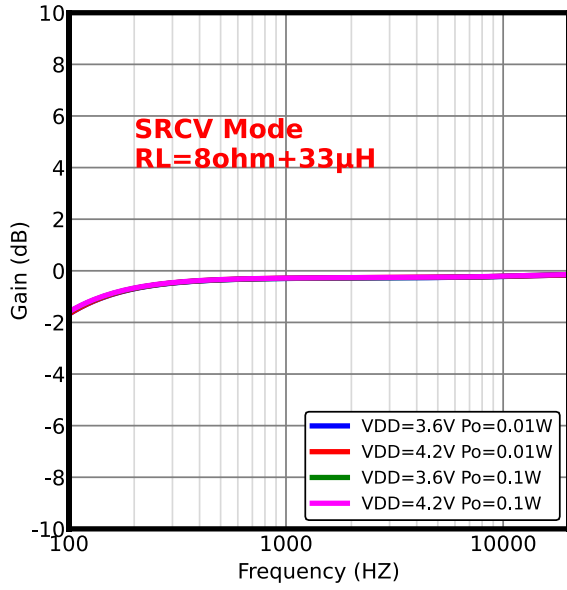
Gain VS. Frequency



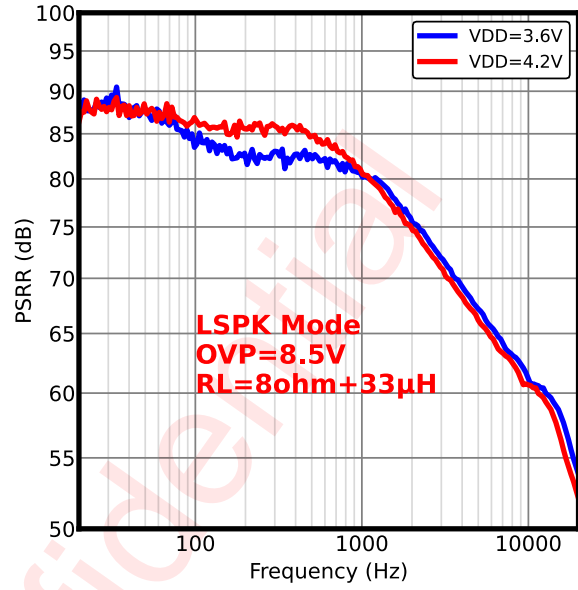
Gain VS. Frequency



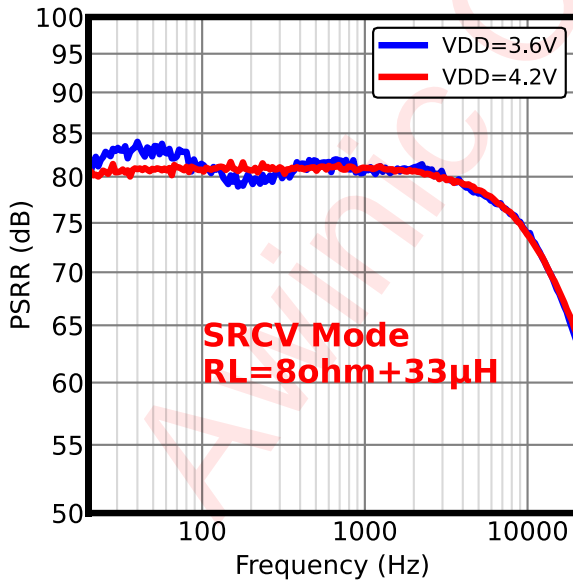
Gain VS. Frequency



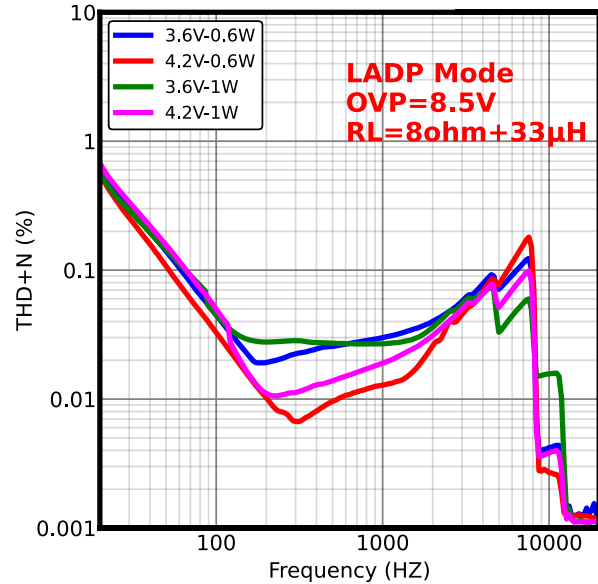
PSRR VS. Frequency



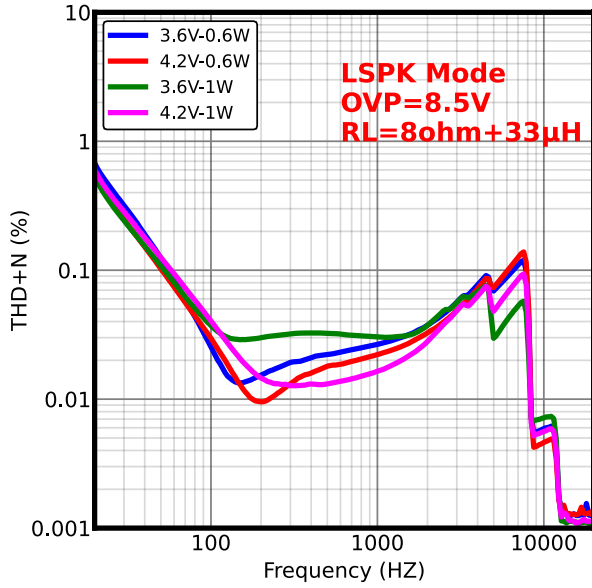
PSRR VS. Frequency



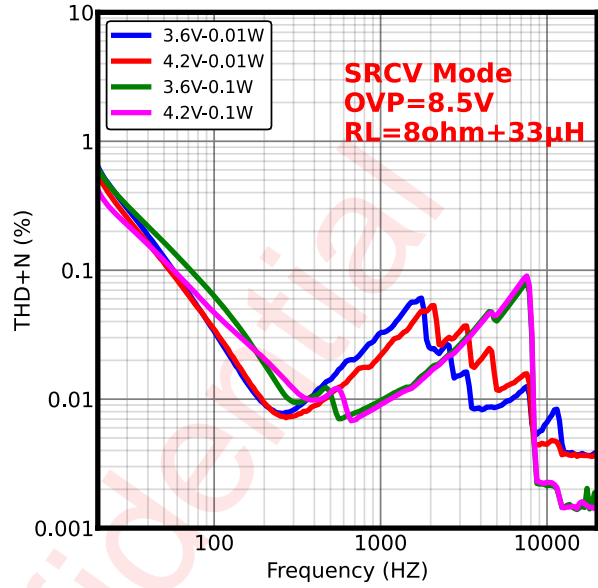
THD+N VS. Frequency



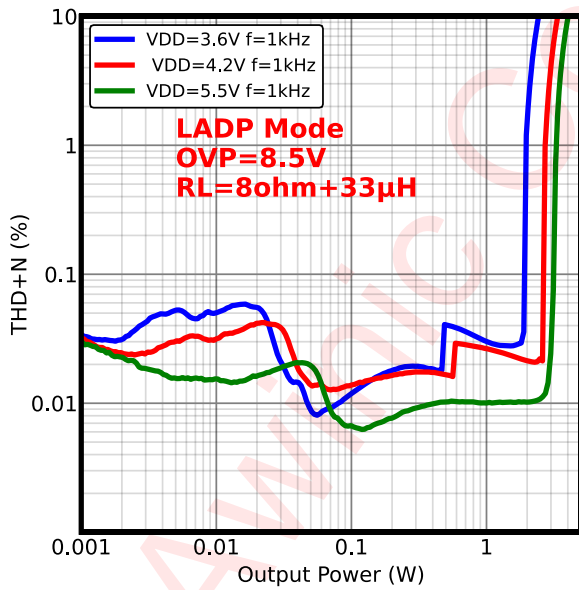
THD+N VS. Frequency



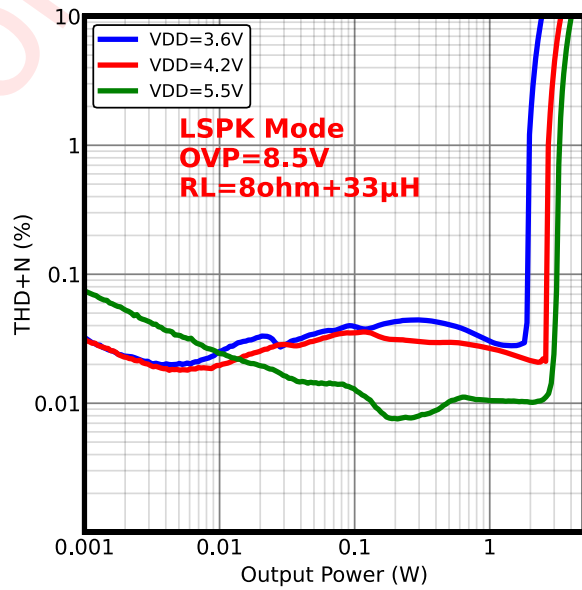
THD+N VS. Frequency



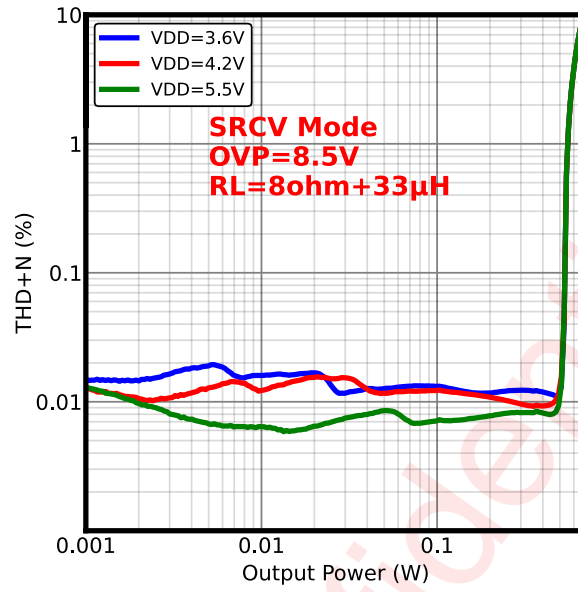
THD+N VS. Output Power



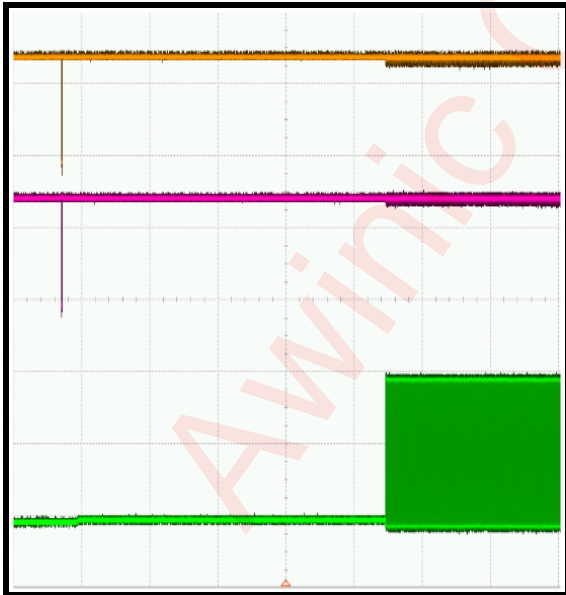
THD+N VS. Output Power



THD+N VS. Output Power



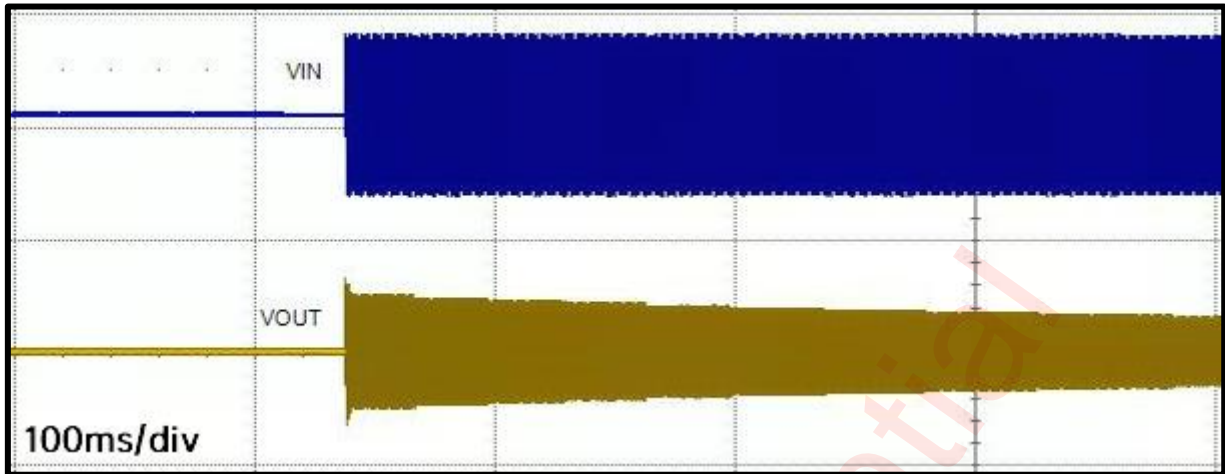
Start-up Sequence



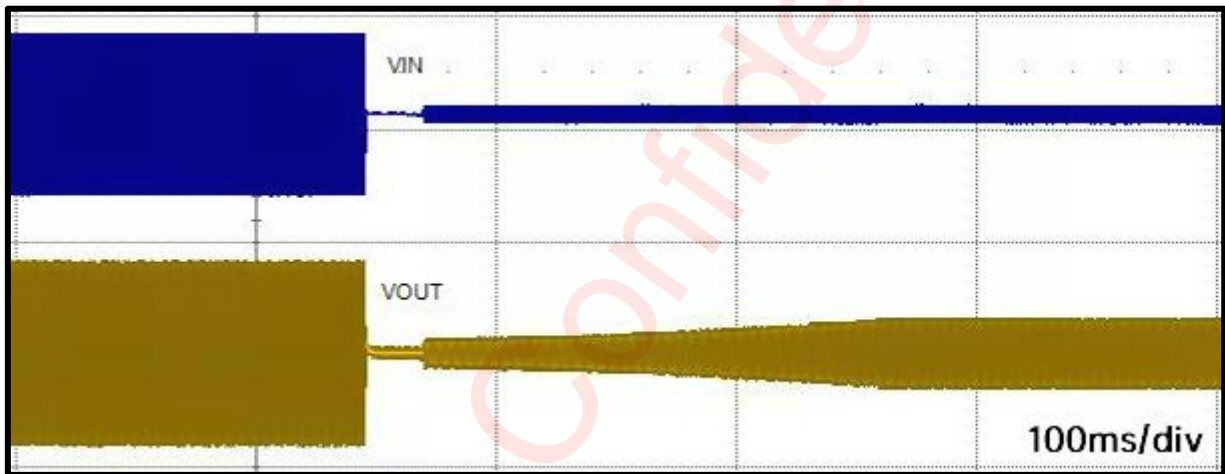
Shutdown Sequence



Multi-Level AGC Attack Timing



Multi-Level AGC Release Timing



## Working Principle

### I<sup>2</sup>C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f <sub>SCL</sub>	SCL Clock frequency			400	kHz
2	t <sub>LOW</sub>	SCL Low level Duration	1.3			μs
3	t <sub>HIGH</sub>	SCL High level Duration	0.6			μs
4	t <sub>RISE</sub>	SCL, SDA rise time			0.3	μs
5	t <sub>FALL</sub>	SCL, SDA fall time			0.3	μs
6	t <sub>SU:STA</sub>	Setup time SCL to START state	0.6			μs
7	t <sub>HD:STA</sub>	(Repeat-start) Start condition hold time	0.6			μs
8	t <sub>SU:STO</sub>	Stop condition setup time	0.6			μs
9	t <sub>BUF</sub>	the Bus idle time START state to STOP state	1.3			μs
10	t <sub>SU:DAT</sub>	SDA setup time	0.1			μs
11	t <sub>HD:DAT</sub>	SDA hold time	10			ns

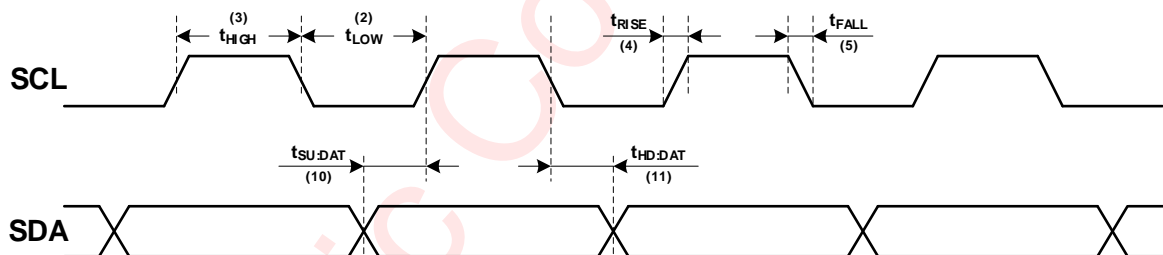


Figure 6 SCL and SDA timing relationships in the data transmission process

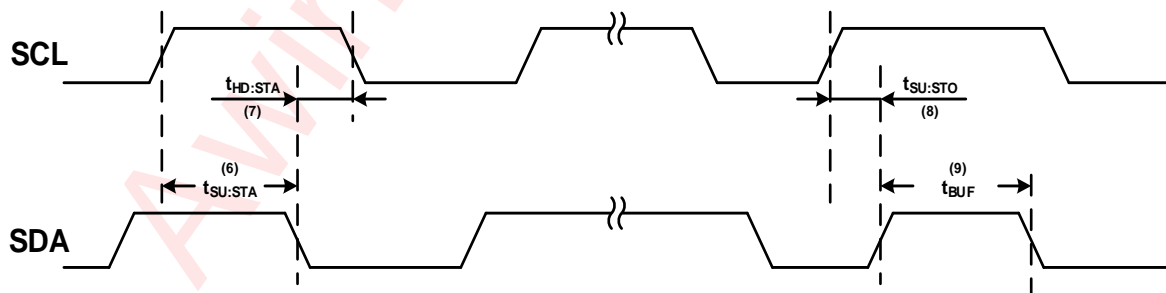


Figure 7 the Timing Relationship between START and STOP State

### General I<sup>2</sup>C Operation

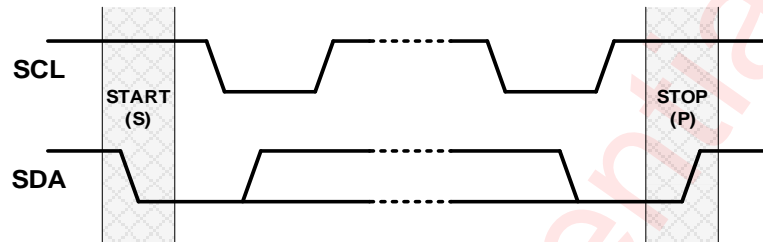
The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. All data to start transmission and end of transmission requires the main device to issue START state and STOP status:

START state: The SCL maintain a high level, SDA from high to low level

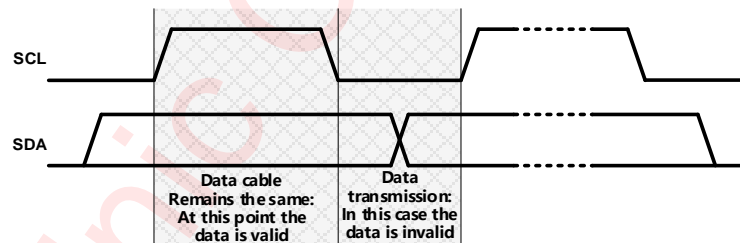
STOP state: The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 8.



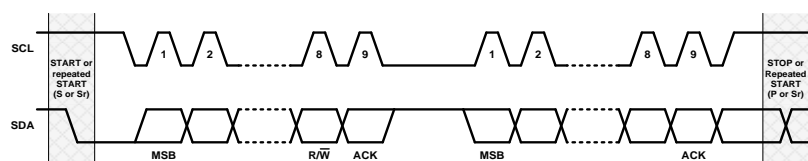
**Figure 8 START and STOP State Generation Process**

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 9. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an acknowledgment bit (Acknowledge, ACK or A), as shown in Figure 10. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.



**Figure 9 The Data Transfer Rules on the I<sup>2</sup>C Bus**

The whole process of actual data transmission is shown in Figure 10. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ( $\overline{R/W}$ ). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.



**Figure 10 Data Transmission on the I<sup>2</sup>C Bus**

## I<sup>2</sup>C Read/Write Processes

The following describes two kinds of ways of the I<sup>2</sup>C bus data transmission:

### Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW87392E as the slave device, the transmission process in accordance with the following steps, as shown in Figure 11:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag  $R/\overline{W} = 0$ );

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW87392E register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW87392E, within AW87392E each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.

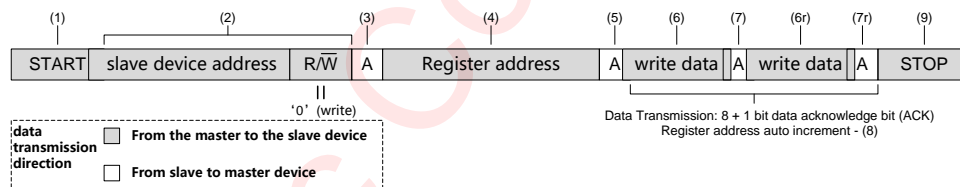


Figure 11 Writing Process (Data Transmission Direction Remains the Same)

### Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW87392E as the slave device, the transmission process carried out by following steps listed in Figure 12:

(1) Master device asserts a start condition;

(2) Master device transmits the 7 bits address of AW87392E, and followed by a "read / write" flag ( $R/\overline{W} = 1$ );

(3) The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

(4) The master device sends the 8bit address that the AW87392E register needs to read the data;

(5) The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

(6) The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

(7) Master sends 7-bits address of the slave device and followed by a read / write flag (flag  $R/\overline{W} = 1$ )

- again;
- (8) The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
  - (9) The slave transmits 8 bits of data to register which needs to be read;
  - (10) The master device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;
  - (11) AW87392E automatically increments register address once after the slave sends each acknowledge bit (ACK);
  - (12) The master device generates the STOP state to end the data transmission;

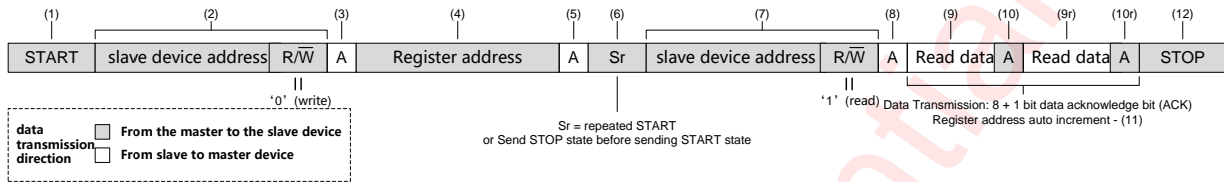
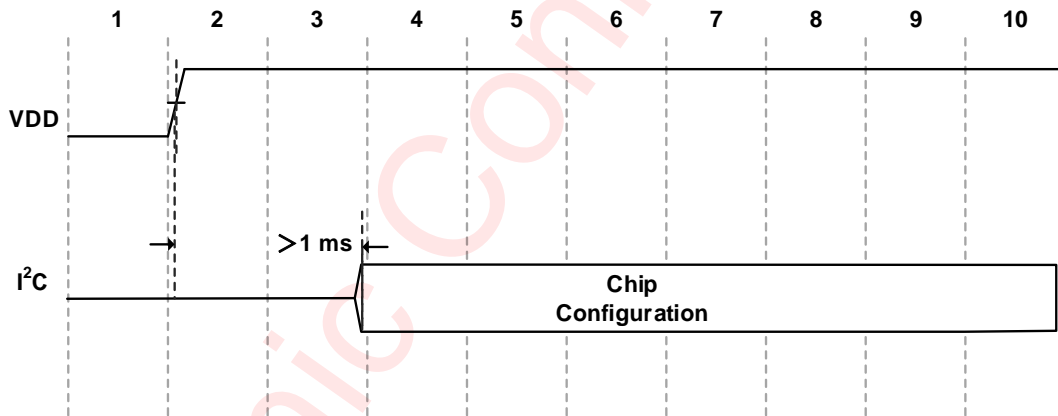


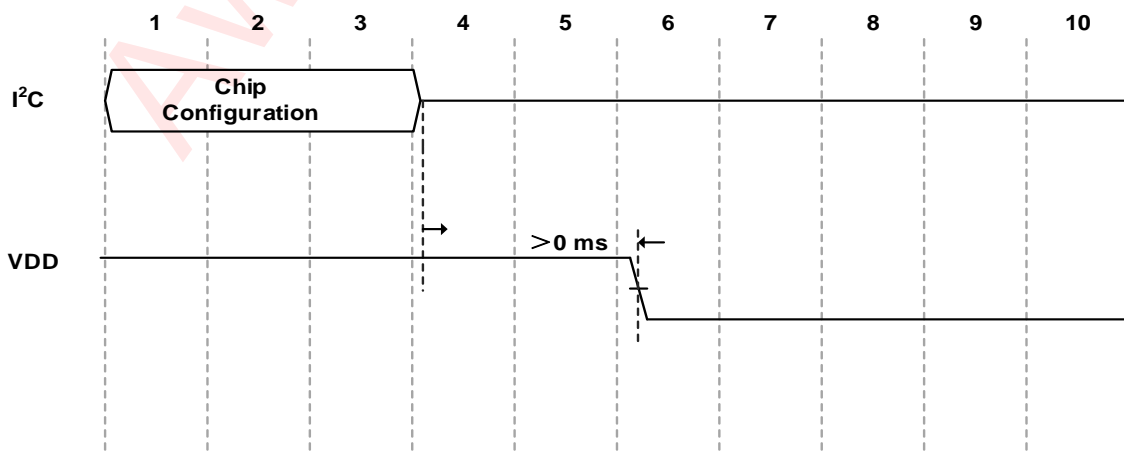
Figure 12 Reading Process (Data Transmission Direction Remains the Same)

Power Up and Power Down Sequence

Power up sequence considering I<sup>2</sup>C timing shows as below:



Power down sequence considering I<sup>2</sup>C timing shows as below:



## Register Configuration

### Register List

Write AA to the 00 register of the AW87392E to reset the register.

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	ID	RO	IDCODE							
0x01	SYSCTRL	RW	REG_VER_SEL	REG_EN_ADAP	REG_EN_2X	EN_SPK	EN_PA	REG_EN_CP	EN_SW	
0x02	CP	RW	REG_CP_OVP							
0x03	PAG	RW	GAIN							
0x04	AGCPO	RW		AK1_S	PD_AGC1	AGC2PO				
0x05	AGC2PA	RW	RK_S			AK2_S			AK2F_S	
0x06	SYSST	RO	UVLO	OTN	OC_FLAG	ADAP_CP	STARTOK	CP_OVP	PORN	
0x07	SYSINT	RC	UVLOI	OTNI	OC_FLAGI	ADAP_CPI	STARTOKI	CP_OVPI	PORNI	

Any register address which is more than 0x05 and all reserved bits are reserved for debugging and testing purposes. Changing their values may affect the normal function of the power amplifier; Reading them will get any possible values. AW87392E's I<sup>2</sup>C address is 10110A2A1, as shown in Table 1, in order to avoid conflict with other I<sup>2</sup>C devices address, you can pull up or pull-down AW87392E of AD2 and AD1 pins to set the value of A2 and A1, respectively. The following lists specific information about all visible registers, including default values and programmable ranges.

AD2/A2	AD1/A1	I <sup>2</sup> C Address
0	0	0x58
0	1	0x59
1	0	0x5A
1	1	0x5B

Table 1 AW87392E Address Byte

### Register Detailed Description

ID: (Address 00h)				
Bit	Symbol	R/W	Description	Default
7:0	IDCODE	RO	Chip ID will be returned after read	0xC1

SYSCTRL: (Address 01h)				
Bit	Symbol	R/W	Description	Default
7:6	REG_VER_SEL	RW	PA Version Select 00: Low noise Version 01: Normal Version (BOM compact) 10: Super RCV Mode (Note: Only EN_SPK=0 valid) 11: turn to 01	0x0
5	REG_EN_ADAP	RW	ADAP Function setting 0:ADP disable 1:ADP enable	0x1

4	REG_EN_2X	RW	2X Charge Pump Mode enable. 0: 2X Charge Pump Mode disable, 1X Direct Through Mode enable 1: 2X Charge Pump Mode enable, 1X Direct Through Mode disable	0x1
3	EN_SPK	RW	SPK Mode or RCV Mode enable. Changing this bit results in reconfiguration of gain scope. 0: SPK Mode disable 1: SPK Mode enable	0x1
2	EN_PA	RW	Power Amplifier enable 0: Power Amplifier disable 1: Power Amplifier enable	0x1
1	REG_EN_CP	RW	Charge Pump enable. 0: Charge Pump disable, PVDD=0 1: Charge Pump enable, the CP working mode depends on EN_2X	0x1
0	EN_SW	RW	Chip software enable. If EN_PA=EN_CP=1, when change EN_CP from 1 to 0, only set EN_SW=0. 0: software disable 1: software enable	0x0

CP: (Address 02h)

Bit	Symbol	R/W	Description	Default
3:0	REG_CP_OVP	RW	Charge Pump OVP Threshold 0000: 6.50V 0001: 6.75V 0010: 7.00V 0011: 7.25V 0100: 7.50V 0101: 7.75V 0110: 8.00V 0111: 8.25V 1000: 8.50V 1001-1111 reserved. If set, turns to default.	0x8

PAG: (Address 03h)

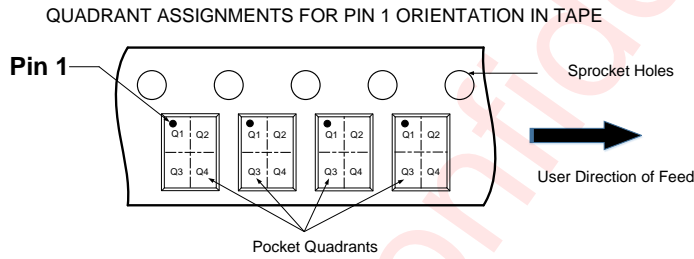
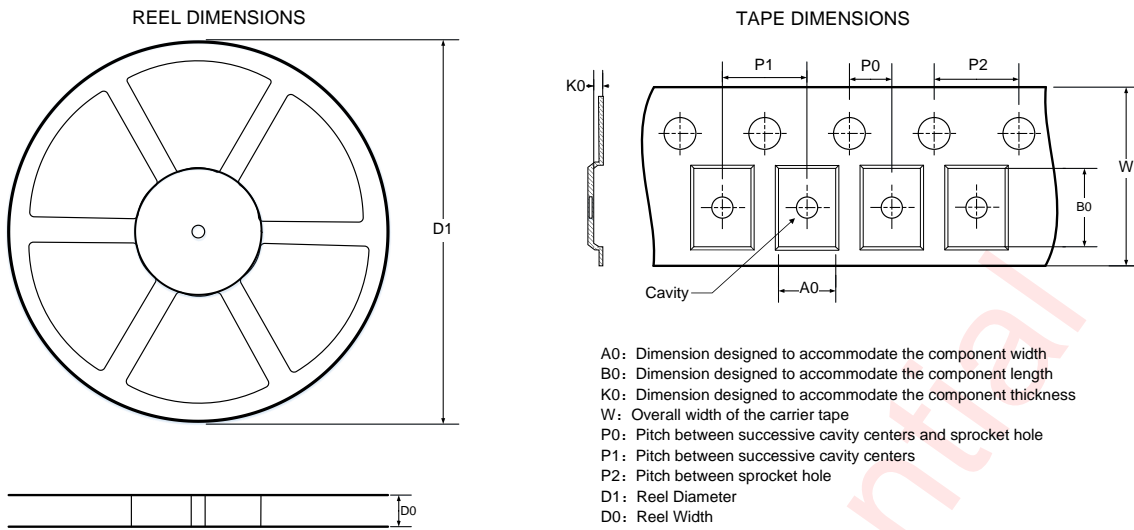
Bit	Symbol	R/W	Description	Default
2:0	GAIN	RW	NSPK: 010: 18.0dB  NRCV/LRCV: 000: 0.0dB  NADP: 010: 18.0dB  LSPK/LADP: 000: 12.0dB 001: 15.0dB 010: 18.0dB 011: 21.0dB 100: 24.0dB 101-111: reserved. If set, turns to default  SRCV: 000: 0.0dB 001: 3.0dB 010: 6.0dB 011: 9.0dB 100-111: reserved. If set, turns to 000	0x2

AGCPO: (Address 04h)				
Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:5	AK1_S	RW	AGC1 Attack Time setting 10: 0.16ms/dB 11: 0.32ms/dB	0x2
4	PD_AGC1	RW	AGC1 function power-down 0: AGC1 function power-up 1: AGC1 function power-down	0x0
3:0	AGC2PO	RW	AGC2 Output Power setting: when EN_SPK=1 & when ADJ AGC2PO enable 0000: 0.5w@8Ω 0001: 0.6w@8Ω 0010: 0.7w@8Ω 0011: 0.8w@8Ω 0100: 0.9W@8Ω VDD>3V   0.5W@8Ω VDD≤3V 0101: 1.0W@8Ω VDD>3V   0.6W@8Ω VDD≤3V 0110: 1.1W@8Ω VDD>3V   0.7W@8Ω VDD≤3V 0111: 1.2W@8Ω VDD>3V   0.8W@8Ω VDD≤3V 1000: 1.3W@8Ω VDD>3V   0.5W@8Ω VDD≤3V 1001: 1.4W@8Ω VDD>3V   0.6W@8Ω VDD≤3V 1010: 1.5W@8Ω VDD>3V   0.7W@8Ω VDD≤3V 1011: 1.6W@8Ω VDD>3V   0.8W@8Ω VDD≤3V 1100-1110: not used, and set to 1011  1111: AGC2 OFF	0x7

AGC2PA: (Address 05h)				
Bit	Symbol	R/W	Description	Default
7:5	RK_S	RW	AGC Release Time setting 000: 5.12ms/dB 001: 10.24ms/dB 010: 20.48ms/dB 011: 41ms/dB 100: 82ms/dB 101: 164ms/dB 110: 328ms/dB 111: 656ms/dB	0x2
4:2	AK2_S	RW	AGC2 Attack Time setting 000: 1.28ms/dB 001: 2.56ms/dB 010: 10.24ms/dB 011: 41ms/dB 100: 82ms/dB 101: 164ms/dB 110: 328ms/dB 111: 656ms/dB	0x3
1:0	AK2F_S	RW	AGC2 First Attack Time setting 00: 10.24ms/dB 01: 20.48ms/dB 10: 41ms/dB 11: 82ms/dB	0x2

SYSST: (Address 06h)				
Bit	Symbol	R/W	Description	Default
7	UVLO	RO	None	0x0
6	OTN	RO	None	0x1
5	OC_FLAG	RO	None	0x0
4	ADAP_CP	RO	None	0x1
3	STARTOK	RO	None	0x0
2	CP_OVP	RO	None	0x0
1	PORN	RO	None	0x0
0	Reserved	RO	Not used	0
SYSINT: (Address 07h)				
Bit	Symbol	R/W	Description	Default
7	UVLOI	RC	None	0x0
6	OTNI	RC	None	0x1
5	OC_FLAGI	RC	None	0x0
4	ADAP_CPI	RC	None	0x1
3	STARTOKI	RC	None	0x0
2	CP_OVPI	RC	None	0x0
1	PORNI	RC	None	0x0
0	Reserved	RC	Not used	0

## TAPE AND REEL INFORMATION



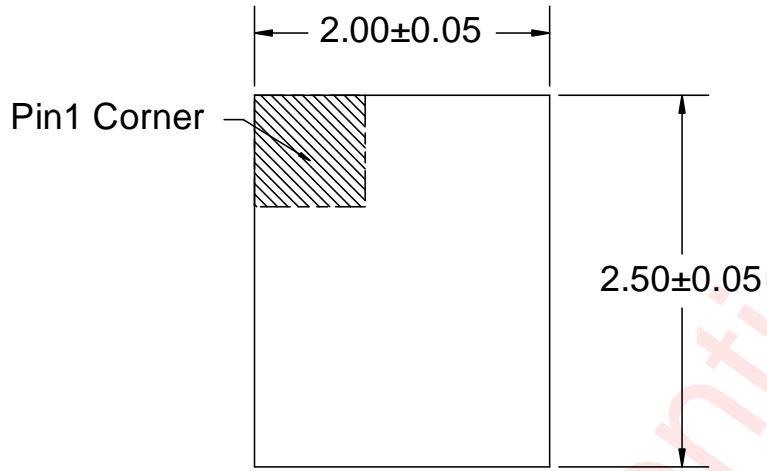
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

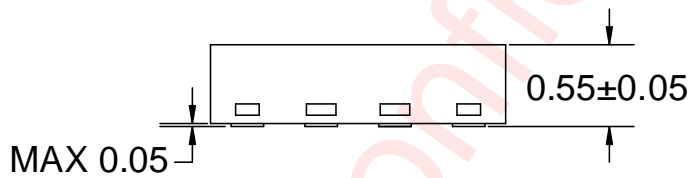
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.60	2.25	2.75	0.75	2.00	8.00	4.00	12.00	Q1

All dimensions are nominal

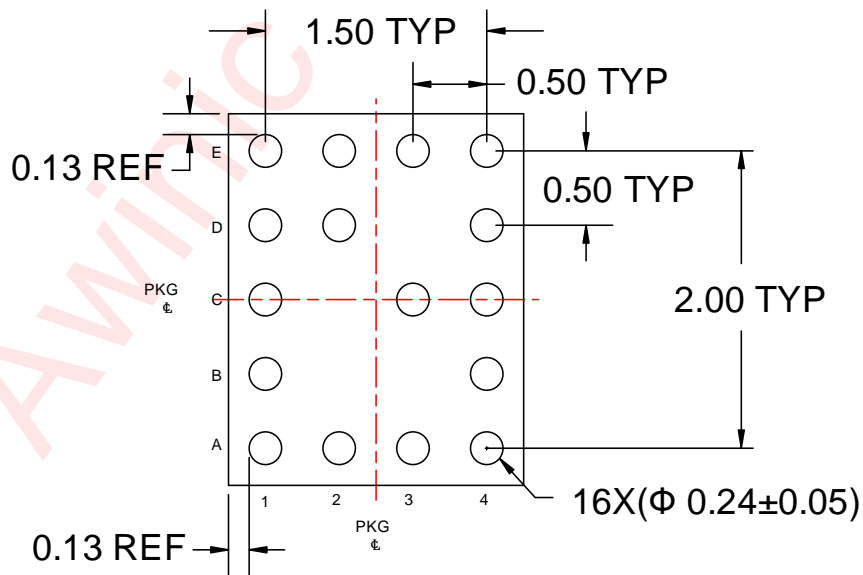
PACKAGE DESCRIPTION



TOP VIEW



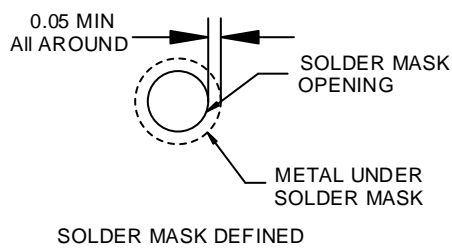
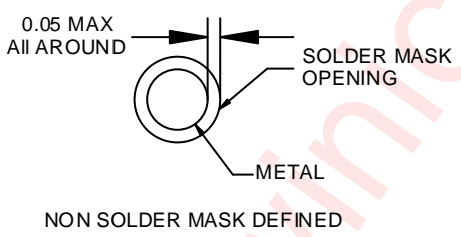
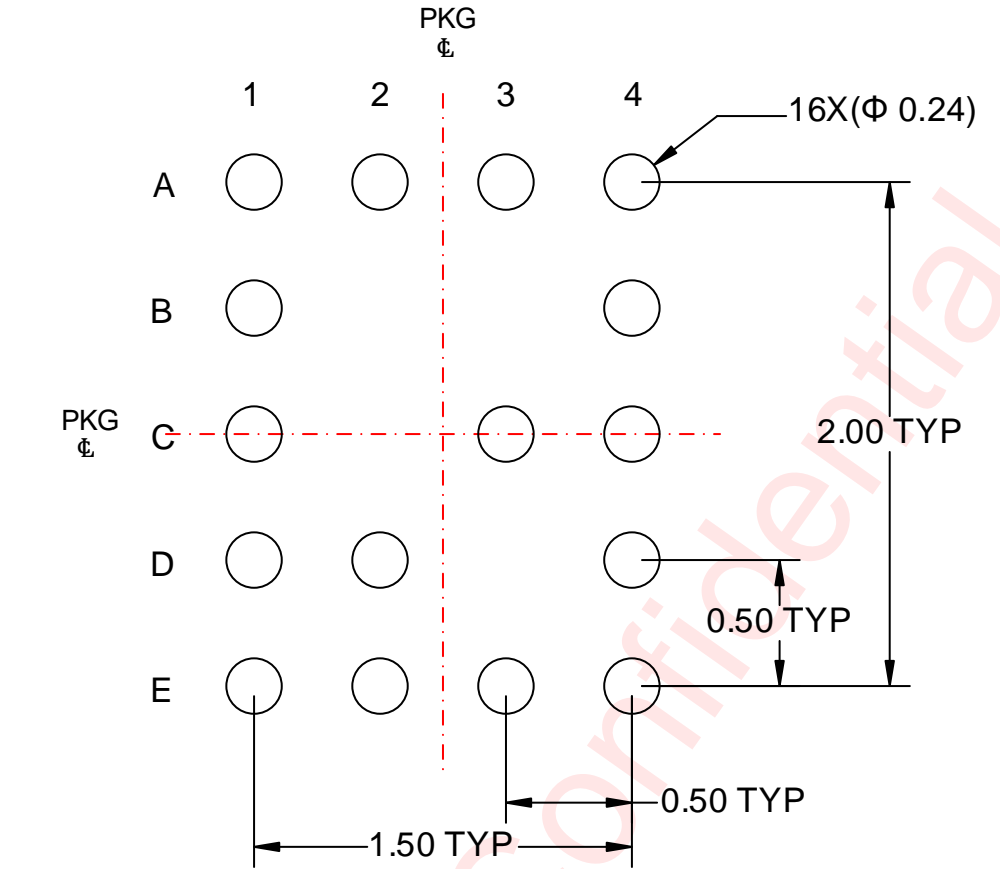
SIDE VIEW



BOTTOM VIEW

Unit: mm

LAND PATTERN DATA



Unit: mm

## REVISION HISTORY

Version	Date	Change Record
V1.0	Sep.2025	Officially Released

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