钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD1176DR/SN75HVD1176DR

PROFIBUS® RS-485 transceiver

网址 www.sztdbdt.com

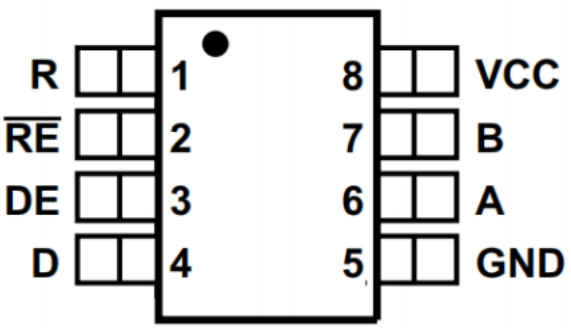
用芯智造 · 卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Optimized for PROFIBUS® networks
  - Signal transmission rate up to 40Mbps
  - Differential output exceeds 2.1 (54Ω load)
  - Low bus capacitance of 10pF (max)
- Complies with TIA/EIA-485-A requirements
- ESD protection exceeds ± 10kV HBM
- Fail-safe receivers for bus open, short, and idle states
- Up to 160 transceivers on a bus
- Low skew during output switching and driver enable/disable
- Common-mode rejection up to 50MHz
- Short-circuit current limiting
- Supports hot-plug
- Thermal shutdown protection



D Package 8-Pin SOIC
Top View

Applications

- Process automation
  - Chemical production
  - Brewing and distillation
  - Paper machines
- Factory automation
  - Automotive production
  - Rolling, embossing, stamping machines
  - Networked sensors
- General RS-485 networks
  - Motor and motion control
  - HVAC and building automation networks
  - Networked security

Description

The SNx5HVD1176 device is a half-duplex differential transceiver whose characteristics are optimized forIBUS (EN 50170) applications. Under a 54Ω load, the driver output differential volt age exceeds the 2.1V required by PROFUS. With a signal transmission rate of up to 40Mbps, it is technically capable of high data transmission speeds. Low bus capacitance provides low signal di stortion.

The SN5HVD1176 and SN75HVD1176 devices meet or exceed the requirements of the ANSI standard TIA/EIA-485A (RS-485), making them suitable for differential data transmission on twisted-pair networks. The driver outputs and receiver inputs are connected together to form a half-du bus port with a one-fifth unit load, thereby supporting up to 160 nodes on a single bus. When the bus is shorted, left open, or no driver active, the receiver output remains at a logic high level. When the supply voltage is below 2.5V, the driver output is in a high-impedance state to prevent interference during power cycling or hot-plugging onto the bus. Internal current limiting restricts the output current to a constant value, thereby protecting the transceiver bus pins under short-circuit conditions. A thermal shutdown circuit protects the device from damage caused by excessive power dissipation due to load and drive conditions.

The SN75HVD1176 device has a operating temperature range of 0 ° C to 70 ° C. The SN65HVD1 176 device has a rated operating temperature range of – 40C to 85 ° C.

For isolated versions of this device, refer to the ISO1176 device with integrated digital isolators (SLLS897).

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output/receiver input (complementary to B)
B	7	Bus input/output	Driver output/receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable low
VCC	8	Supply	3-V to 5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	- 0.5	7	V
	Voltage at any bus I/O terminal	- 9	14	V
	Voltage input, transient pulse, A and B, (through 100 Ω, see 图 7-15)	- 40	40	V
	Voltage input at any D, DE or $\overline{RE}$ terminal	- 0.5	7	V
I_O	Receiver output current	- 10	10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	- 40	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
			Bus terminals and GND	±10000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at either bus I/O terminal	A, B	−7		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IL}	Differential input voltage	A with respect to B	−12		12	V
I_O	Output current	Driver	−70		70	mA
		Receiver	−8		8	mA
T_J	Junction temperature (1)	SN65HVD1176	−40		130	°C
		SN75HVD1176	0		130	°C
R_L	Differential load resistance		54			Ω
$1/t_{U1}$	Signaling rate				40	Mbps

(1) See the 节 6.7 table for more information on maintenance of this requirement.

6.4 Thermal Information

THERMAL METRIC(1)		SN75HVD1176 D (SOIC) 8 PINS	SN65HVD1176 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	104.7	116.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.9	63.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.7	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.2	62.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

(2) The intent of $R_{\theta JA}$ specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

6.8 Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{(CFB)}$	Time from application of short-circuit to current foldback	See 图 7-8		0.5		μs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown	T_A = 25°C, See 图 7-8	100			μs

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER							
V_O	Open-circuit output voltage	A or B	No load	0		V_{CC}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude	R_L = 54 Ω	See 图 7-1	2.1	2.9		V
		With common-mode loading, (V_{TEST} from − 7 V to 12 V) See 图 7-2		2.1	2.7		V
$\Delta\|V_{OD(SS)}\|$	Change in steady-state differential output voltage between logic states	See 图 7-1 and 图 7-6		− 0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 7-5		2	2.5	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See 图 7-5		− 0.2	0	0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See 图 7-5			0.5		V
$V_{OD(RING)}$	Differential output voltage over and under shoot	R_L = 54 Ω, C_L = 50 pF See 图 7-6				10%	$V_{OD(PP)}$
I_I	Input current	D, DE		− 50		50	μA
$I_{OS(P)}$	Peak short-circuit output current	DE at V_{CC}, See 图 7-8	V_{OS} = − 7 V to 12 V	− 250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current	DE at V_{CC}, See 图 7-8	V_{OS} > 4 V, Output driving low	60	90	135	mA
			VOS < 1 V, Output driving high	− 135	− 90	− 60	mA
RECEIVER							
$V_{IT(+)}$	Positive-going differential input voltage threshold	See 图 7-9	V_O = 2.4 V, I_O = − 8 mA		− 80	− 20	mV
$V_{IT(-)}$	Negative-going differential input voltage threshold		V_O = 0.4 V, I_O = 8 mA	− 200	− 120		mV
V_{HYS}	Hysteresis voltage (V_{IT+} − V_{IT-})				40		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = − 8 mA, See 图 7-9		4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = − 200 mV, I_{OL} = 8 mA, See 图 7-9			0.2	0.4	V
I_A, I_B	Bus pin input current	V_I = − 7 V to 12 V, Other input = 0 V	V_{CC} = 4.75 V to 5.25 V	− 160		200	μA
$I_{A(OFF)}$ $I_{B(OFF)}$			V_{CC} = 0 V	− 160		200	
I_I	Receiver enable input current	$\overline{RE}$		− 50		50	μA
I_{OZ}	High-impedance - state output current	$\overline{RE}$ = V_{CC}		− 1		1	μA
R_I	Input resistance			60			kΩ
C_{ID}	Differential input capacitance	Test input signal is a 1.5-MHz sine wave with amplitude 1 V_{PP}, capacitance measured across A and B			7	10	pF
C_{MR}	Common mode rejection	See 图 7-11			4		V

(1) All typical values are at V_{CC} = 5 V and 25°C.

6.6 Supply Current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply Current(1)	Driver and receiver, $\overline{RE}$ at 0 V, DE at V_{CC}, All other inputs open, no load		4	6	mA
		Driver only, $\overline{RE}$ at V_{CC}, DE at V_{CC}, All other inputs open, no load		3.8	6	mA
		Receiver only, $\overline{RE}$ at 0 V, DE at 0 V, All other inputs open, no load		3.6	6	mA
		Standby only, $\overline{RE}$ at V_{CC}, DE at 0 V, All other inputs open		0.2	5	μA

(1) Over recommended operating conditions

6.7 Power Dissipation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
P_D	Device power dissipation		R_L = 54 Ω, C_L = 50 pF, 0 V to 3 V, 15 MHz, 50% duty cycle square wave input, driver and receiver enabled		277	318	mW
T_A	Ambient air temperature	SN65HVD1176	Low-K board, no air flow, P_D = 318 mW	-40		64	°C
			High-K board, no air flow, P_D = 318 mW	-40		89	°C
		SN75HVD1176	Low-K board, no air flow, P_D = 318 mW	0			°C
			High-K board, no air flow, P_D = 318 mW	0			°C
T_{SD}	Thermal shut down junction temperature				150		°C

(1) All typical values are with V_{CC} = 5 V and T_A = 25°C.

6.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER							
t_{PLH}	Propagation delay time low-level-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See 图 7-3		4	7	10	ns
t_{PHL}	Propagation delay time high-level-to-low-level output			4	7	10	ns
$t_{sk(p)}$	Pulse skew | t_{PLH} - t_{PHL} |				0	2	ns
t_r	Differential output rise time			2	3	7.5	ns
t_f	Differential output fall time			2	3	7.5	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew	See 图 7-4			0.2	1	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output	R_L = 110 Ω, C_L = 50 pF See 图 7-7	$\overline{RE}$ at 0 V		10	20	ns
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-to- high-impedance output				10	20	ns
$\lvert t_{p(AZL)} - t_{p(BZH)} \rvert$ $\lvert t_{p(AZH)} - t_{p(BZL)} \rvert$	Enable skew time				0.55	1.5	ns
$\lvert t_{p(ALZ)} - t_{p(BHZ)} \rvert$ $\lvert t_{p(AHZ)} - t_{p(BLZ)} \rvert$	Disable skew time					2.5	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output (from sleep mode)	R_L = 110 Ω, C_L = 50 pF See 图 7-7	$\overline{RE}$ at 5 V		1	4	μs
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-output-to high-impedance (to sleep mode)				30	50	ns

6.8 Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
RECEIVER						
t_{PLH}	Propagation delay time, low-to-high level output	See 图 7-10		20	25	ns
t_{PHL}	Propagation delay time, high-to-low level output			20	25	ns
$t_{sk(p)}$	Pulse skew | t_{PLH} - t_{PHL} |			1	2	ns
t_r	Receiver output voltage rise time			2	4	ns
t_f	Receiver output voltage fall time			2	4	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	DE at V_{CC}, See 图 7-13			20	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	DE at V_{CC}, See 图 7-14			20	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				20	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output (standby to active)	DE at 0 V, See 图 7-12		1	4	μs
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output (active to standby)			13	20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output (standby to active)	DE at 0 V, See 图 7-12		2	4	μs
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output (active to standby)			13	20	ns

(1) All typical values are at V_{CC} = 5 V and 25°C.

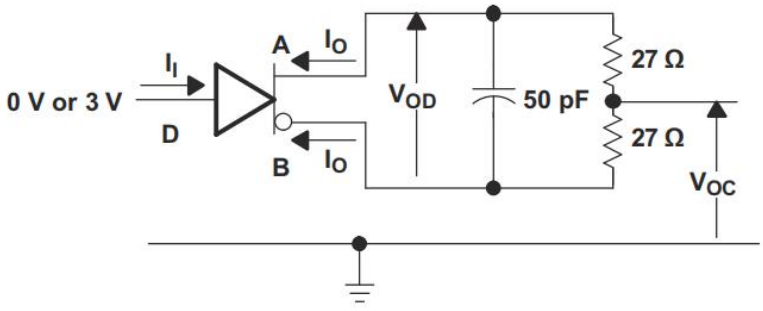


图 7-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

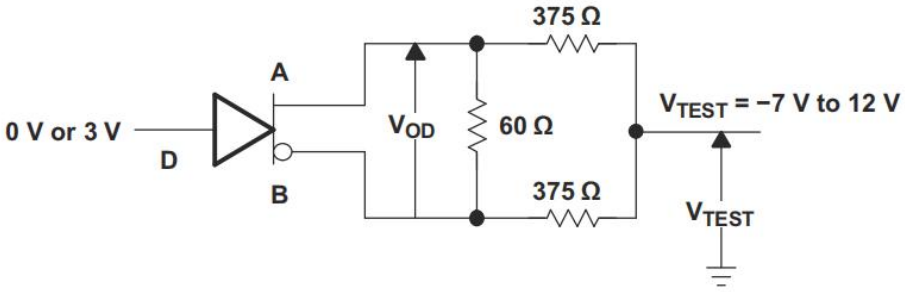


图 7-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

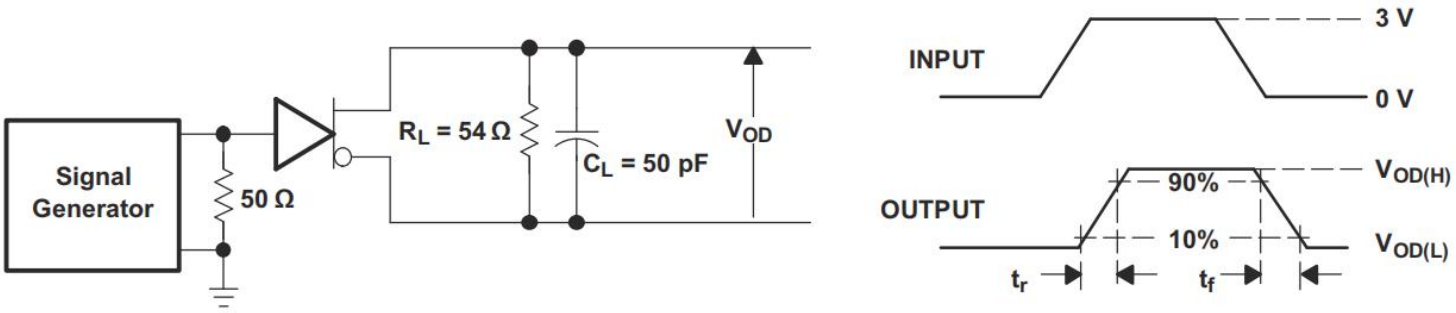


图 7-3. Driver Switching Test Circuit and Rise/Fall Time Measurement

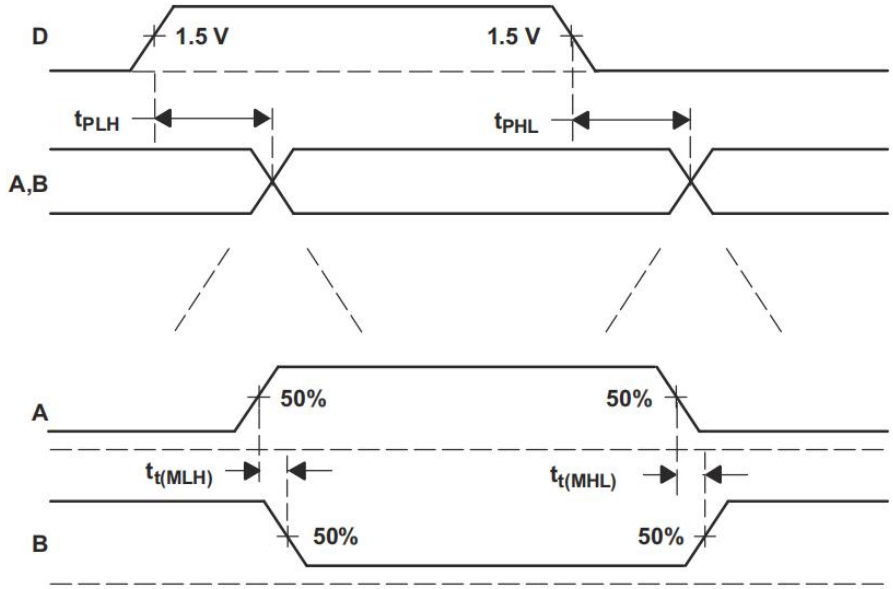


图 7-4. Driver Switching Waveforms for Propagation Delay and Output Midpoint Time Measurements

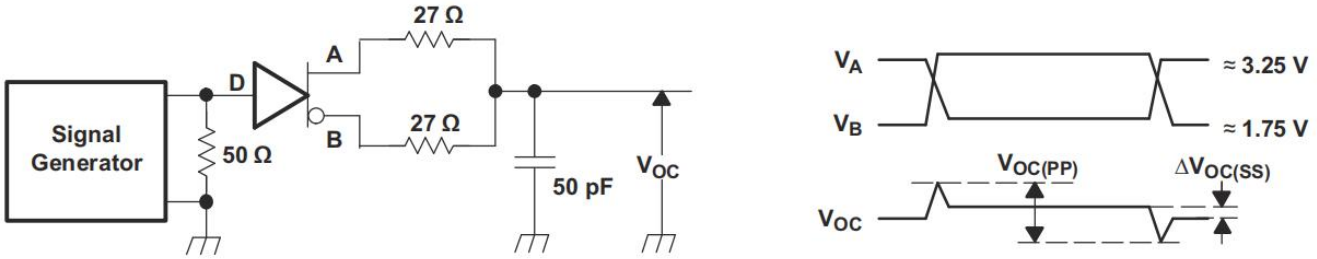
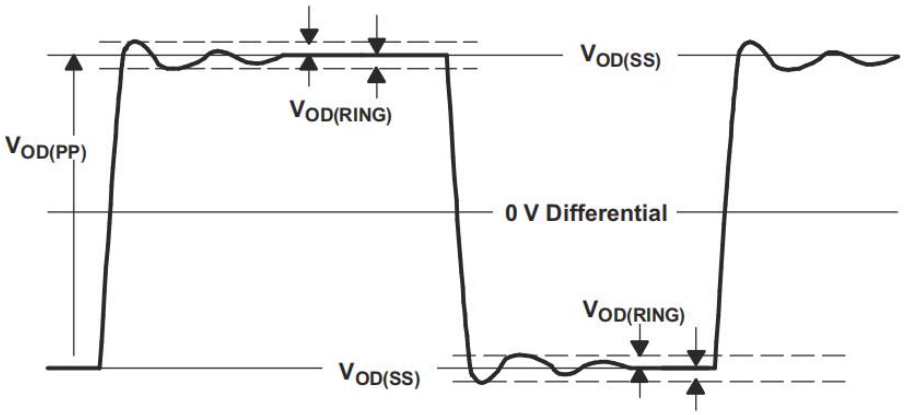
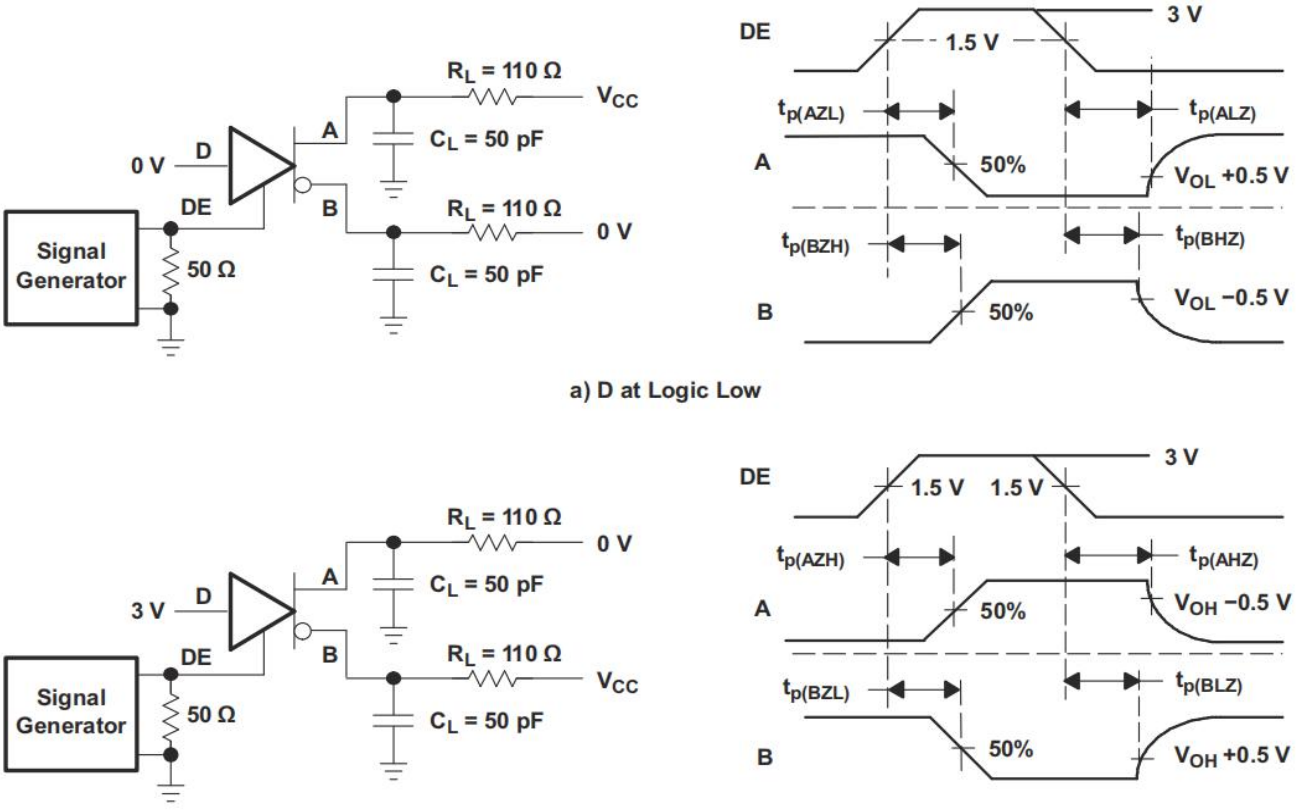


图 7-5. Driver V_{OC} Test Circuit and Waveforms



A. $V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

图 7-6. $V_{OD(RING)}$ Waveform and Definitions



a) D at Logic Low

b) D at Logic High

图 7-7. Driver Enable/Disable Test

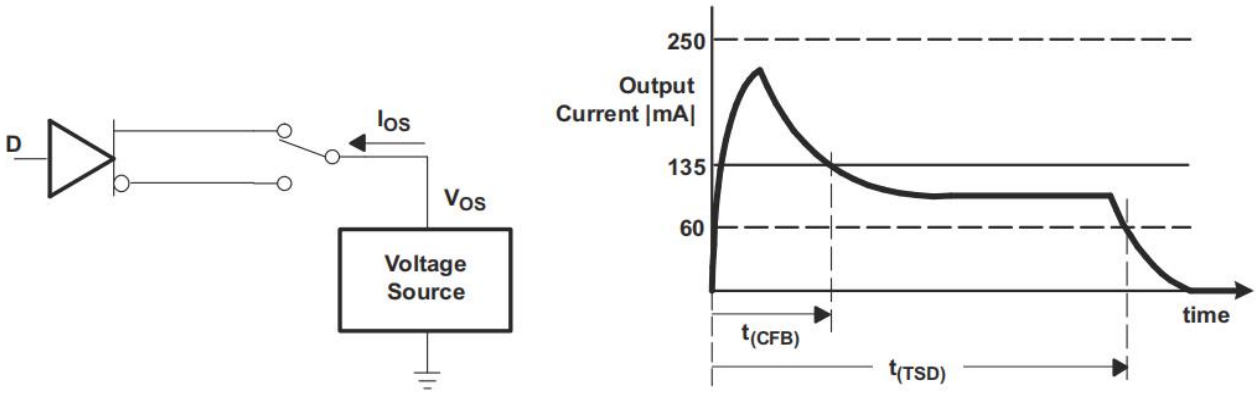


图 7-8. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t = 0)

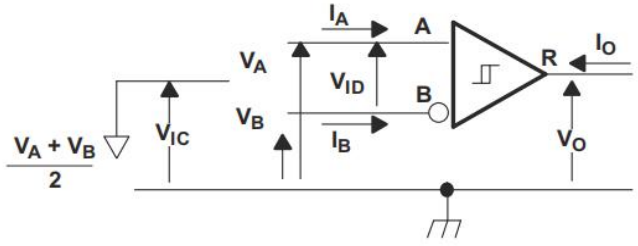


图 7-9. Receiver DC Parameter Definitions

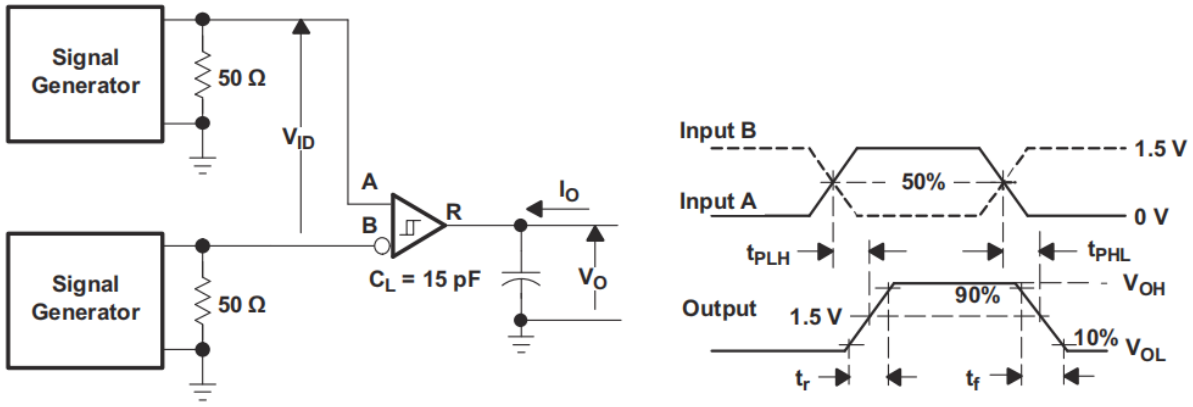


图 7-10. Receiver Switching Test Circuit and Waveforms

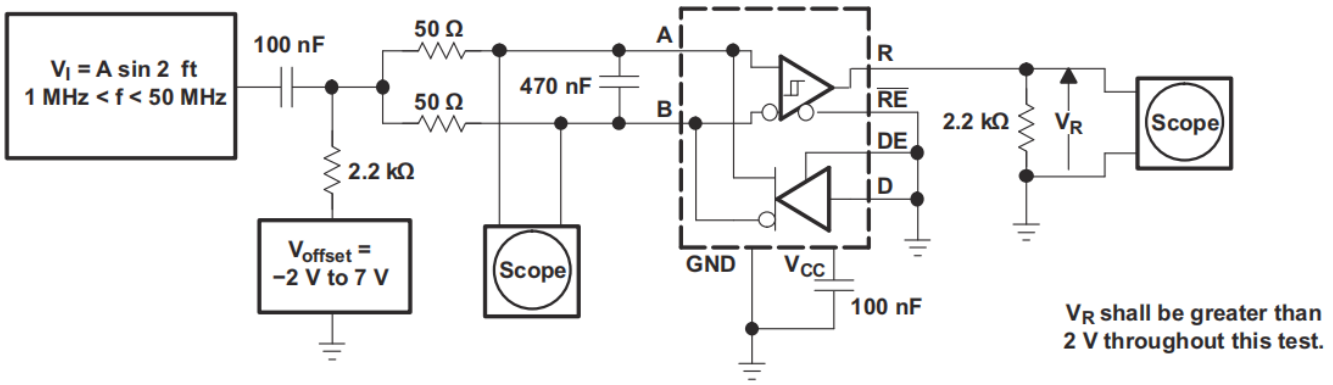


图 7-11. Receiver Common-Mode Rejection Test Circuit

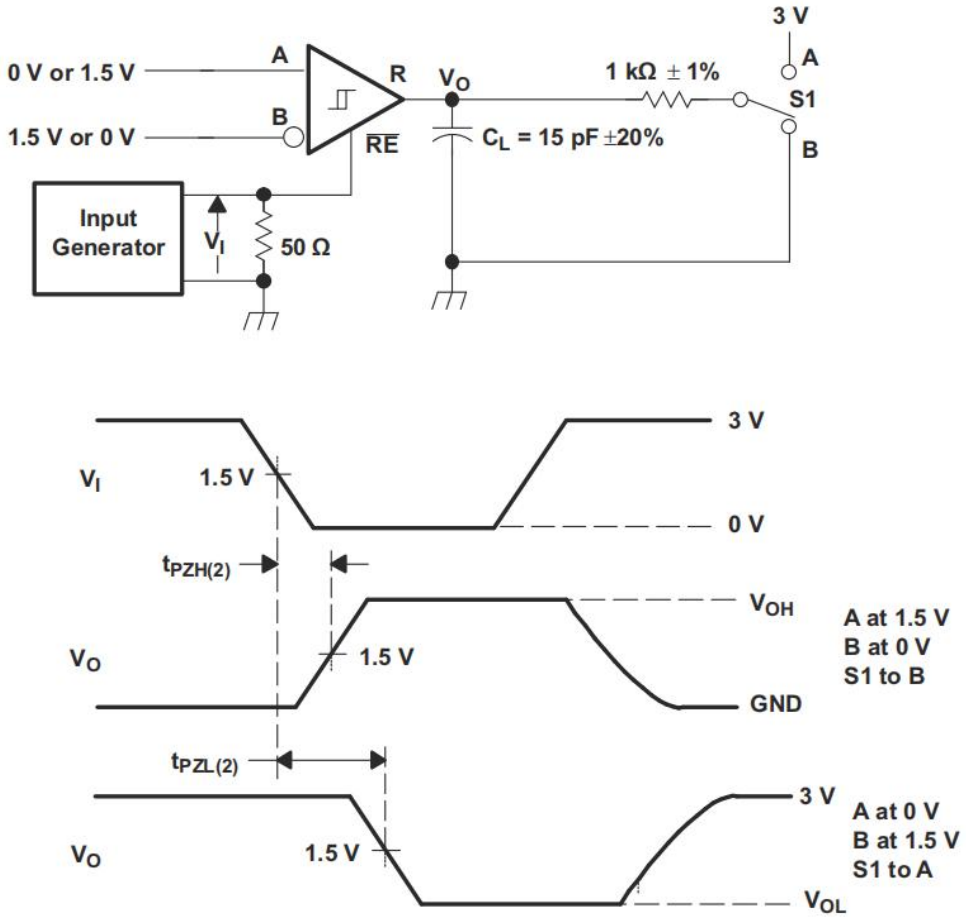


图 7-12. Receiver Enable Time From Standby (Driver Disabled)

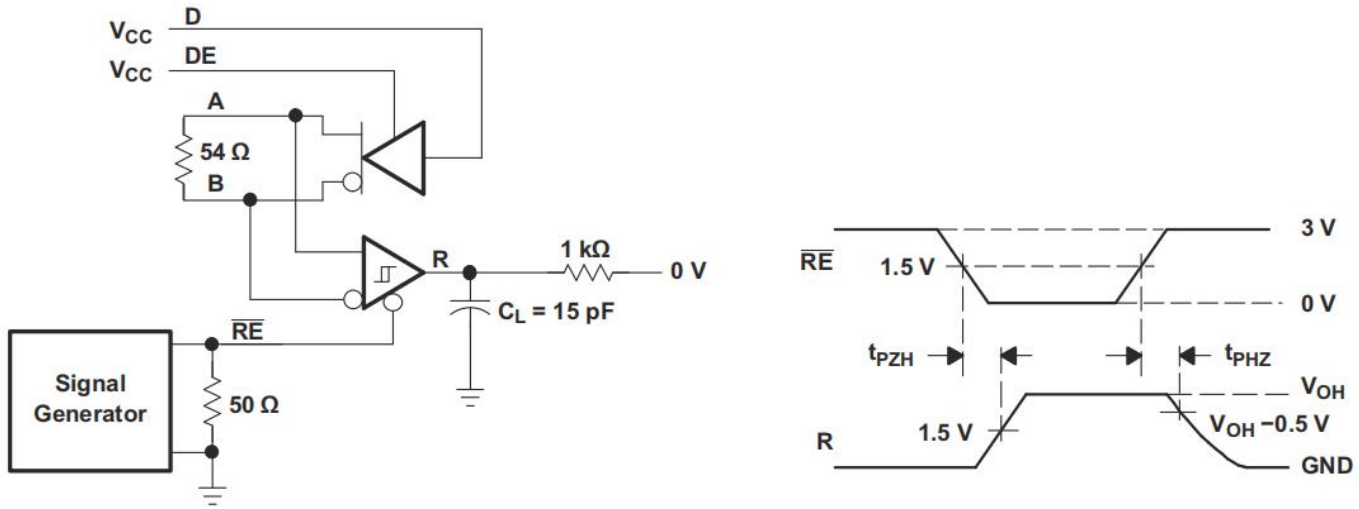


图 7-13. Receiver Enable Test Circuit and Waveforms, Data Output High (Driver Active)

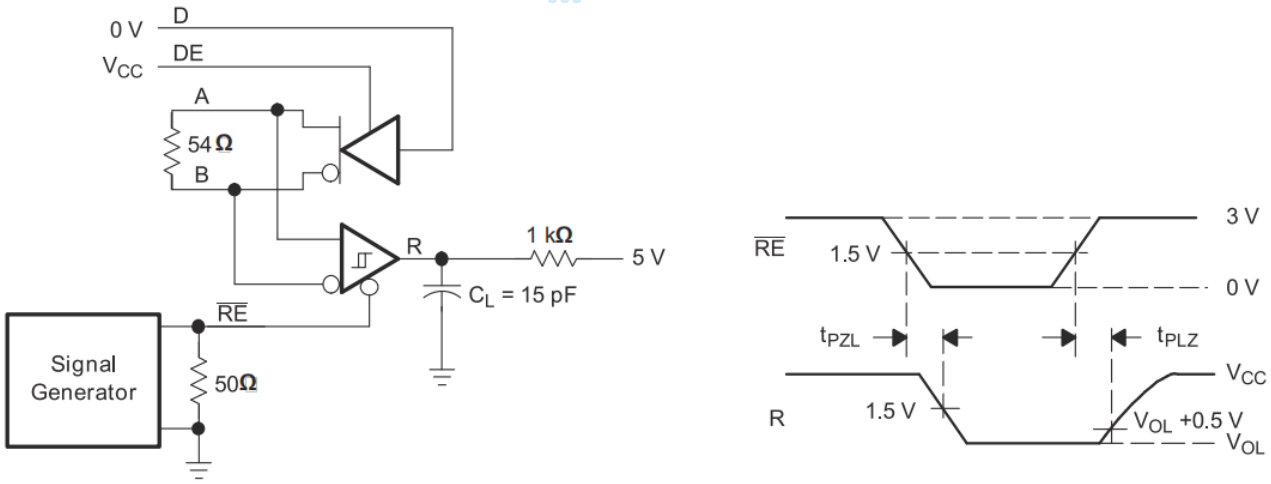


图 7-14. Receiver Enable Test Circuit and Waveforms, Data Output Low (Driver Active)

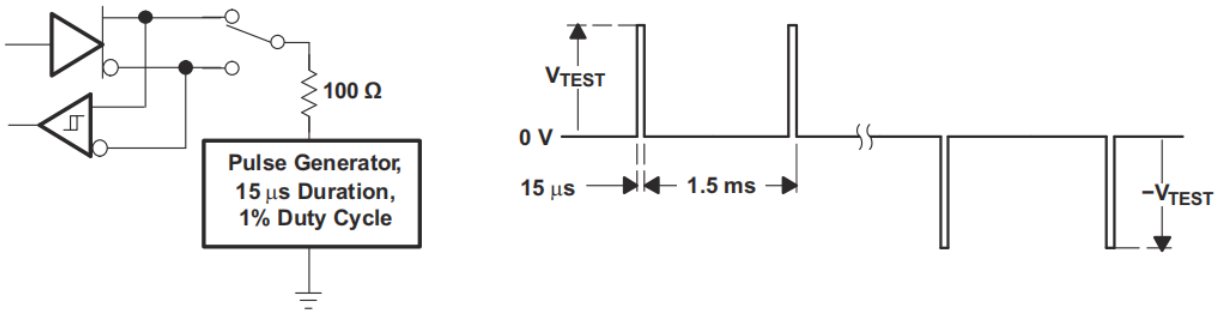


图 7-15. Test Circuit and Waveforms, Transient Overvoltage Test

7 Detailed Description

7.1 Overview

The SNx5HVD1176 device is a 5-V, half-duplex, RS-485 transceiver optimized for use in PROFIBUS (EN50170) applications and suitable for data transmission up to 40 Mbps.

The driver output differential voltage exceeds the PROFIBUS requirement of 2.1 V with a 54-Ω load, and the low transceiver output capacitance of 10 pF supports the PROFIBUS requirements for maximum bus capacitance across various data rates.

This device has an active-high driver enable and an active-low receiver enable. A standby current of less than 5 µA can be achieved by disabling both driver and receiver.

7.2 Functional Block Diagram

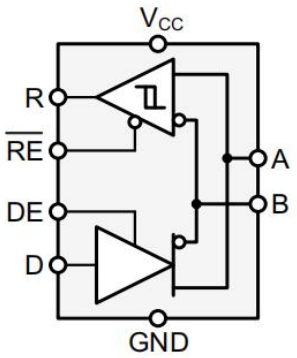


图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±10-kV Human Body Model (HBM) electrostatic discharges and all other pins up to ±4 kV.

The SN65HVD1176 device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions, and a typical receiver hysteresis of 40 mV.

7.4 Device Functional Modes

表 7-1. Driver Function Table(1)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	H	L

(1) H = high level, L = low level, X = don’t care, Z = high impedance (off)

表 7-2. Receiver Function Table(1)

DIFFRENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq -0.02$ V	L	H
-0.2 V < V_{ID} < -0.02 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

表 7-2. Receiver Function Table(1) (continued)

DIFFRENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
X	OPEN	Z
Open Circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = high level, L = low level, X = don't care,
Z = high impedance (off), ? = indeterminate

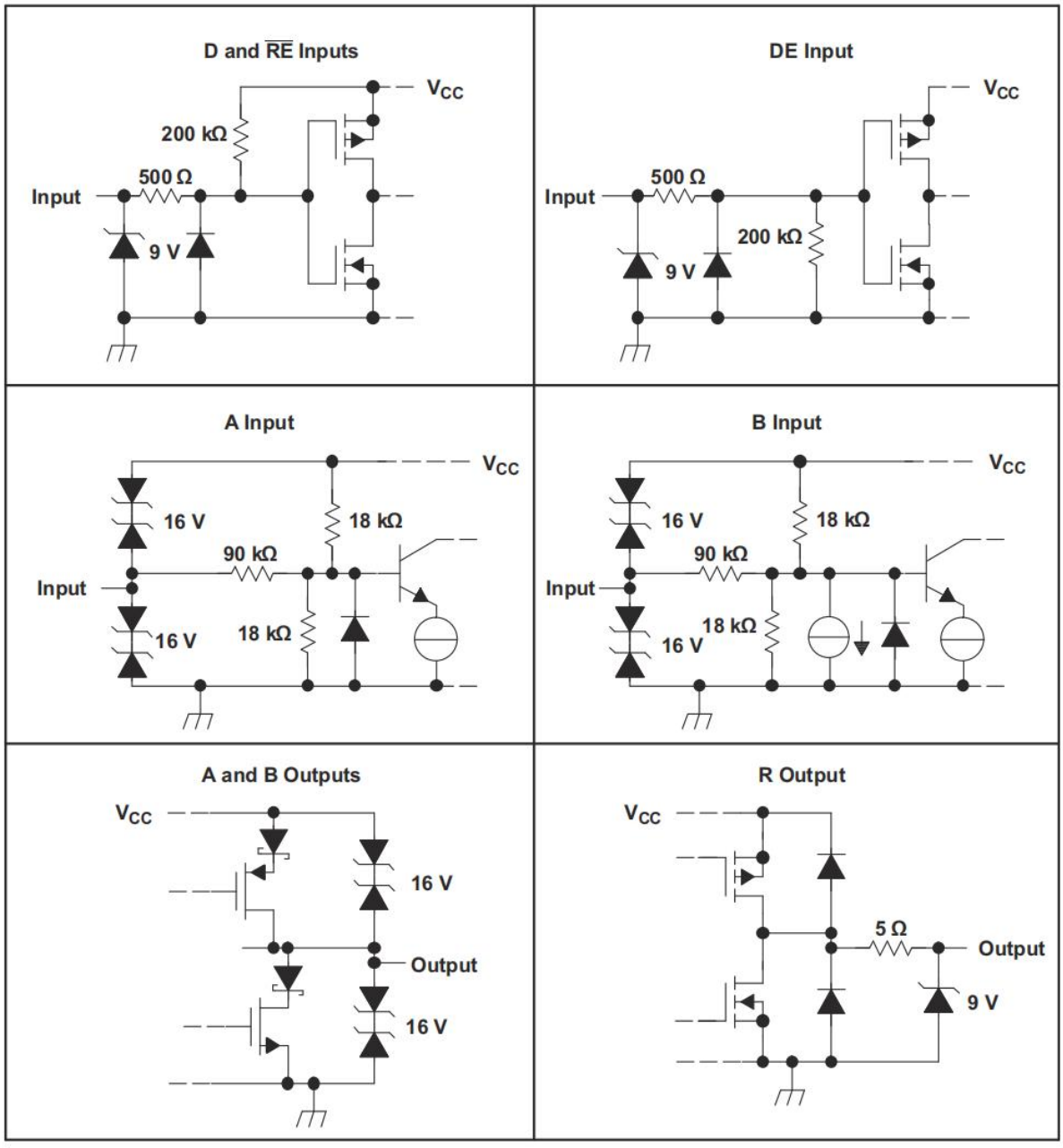
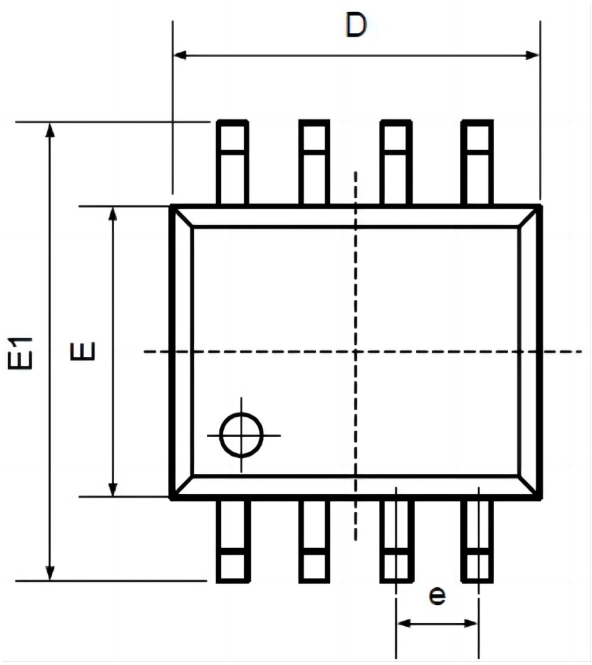


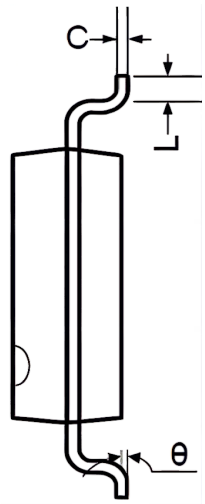
图 7-2. Equivalent Input and Output Schematic Diagrams

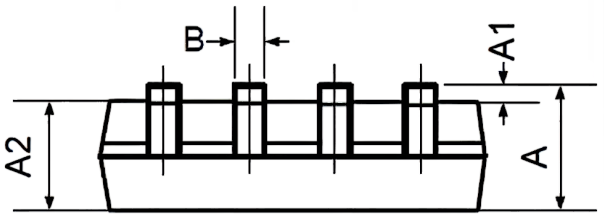
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD1176DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD1176DR
SN75HVD1176DR-TUDI	SOP8	Tape,Reel,2500	SN75HVD1176DR

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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