

16-Channel Multi-function GPIO Controller With I²C Interface

Features

- 16-bit general-purpose I/O expander
- 16 multi-function I/O, each can be configured as GPIO input or output mode independently
- Dual power supply, supporting converting between $V_{DD(P)}$ and $V_{DD(I2C-BUS)}$
- Selectable push-pull or open-drain output
- Interrupt latch function
- Four programmable output drive strengths
- Open-drain active LOW interrupt output (INTN)
- 1MHz I²C interface, 2 selectable addresses
- SCL/SDA inputs supports 1.8V logic input
- Power supply: 1.65V~5.5V
- BGA 3.0mm × 3.0mm × 0.86mm - 24B package

Applications

Cell Phone

Keyboard

PDA/MP3/MP4/CD/Mini display

Smart home appliance

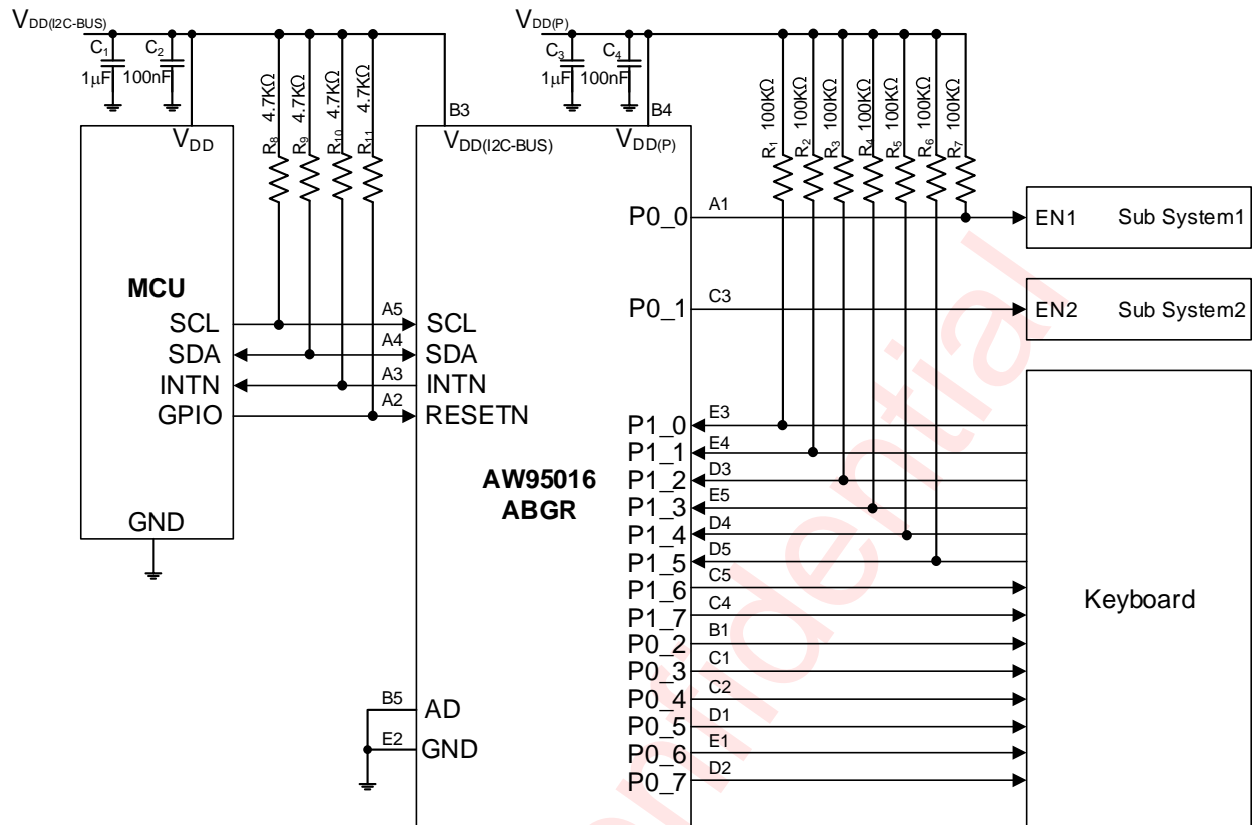
General Description

AW95016ABGR is a 16 channel general purpose I/O (GPIO) expander controller. Each channel can be configured as GPIO input or output separately. There are two supply voltages for AW95016ABGR: $V_{DD(P)}$ and $V_{DD(I2C-BUS)}$. $V_{DD(I2C-BUS)}$ provides the supply voltage for the interface at the master side and the $V_{DD(P)}$ provides the supply for internal circuits and GPIOs. $V_{DD(I2C-BUS)}$ should be connected to the power of the external SCL/SDA lines. The voltage level on Port Px_x of the AW95016ABGR is determined by the $V_{DD(P)}$.

After power-on, all channels are configured as input by default. However, the system master can enable channels as either input or output by writing to configuration bits. In GPIO input mode, when interrupt mask is closed, open-drain interrupt (INTN) is active when any input state differs from its corresponding input port register state and can be used to indicate to the system master that an input state has changed. After reading GPIO state through I²C interface, the interrupt is cleared. In output mode, each channel can be configured as push-pull or open-drain output independently.

AW95016ABGR operates from 1.65V to 5.5V over the temperature range of -40°C to +85°C.

Typical Application Circuit



In this application schematic, P0_0 is configured as GPIO open-drain output to control the sub system1, and external resistors R₇ is needed. P0_1 is configured as GPIO push-pull output to control the sub system2, P1_6~P1_7, P0_2~P0_7 are configured as GPIO push-pull output, P1_0~P1_5 are configured as GPIO input, and external resistors R₁~R₆ are needed when external driver is open-drain output or the input ports are floating.
 If an output in P_x_x port is configured as a push-pull output, there is no need for external pull-up resistor.
 If an output in P_x_x port is configured as an open-drain output, external pull-up resistor is required.
 If an input in P_x_x port is floating, external pull-up resistor may be needed, unless internal pull-up/pull-down resistor is configured.

Figure 1 AW95016ABGR Application Circuit

Pin Configuration And Top Mark

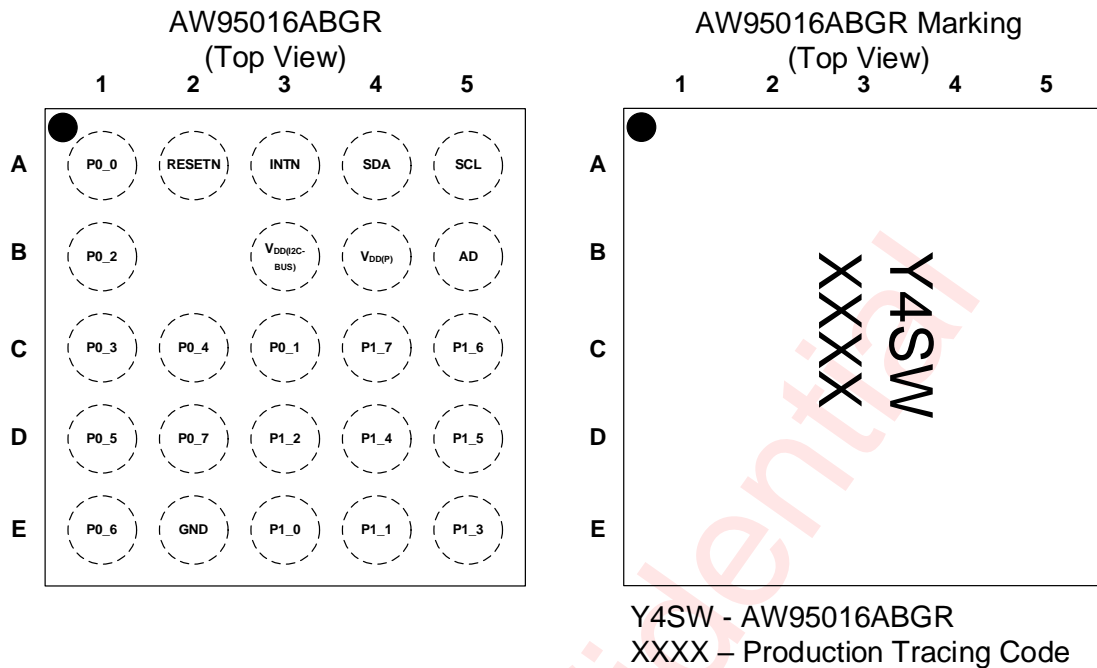


Figure 2 Pin Configuration and Marking

Pin Definition

| No. | NAME | DESCRIPTION |
|-----|--------------------------|--|
| A1 | P0_0 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| A2 | RESETN | Active low hardware reset pin. |
| A3 | INTN | Open-drain active low interrupt output pin, external pull-up resistor is needed. |
| A4 | SDA | Serial data I/O for I ² C interface. |
| A5 | SCL | Serial clock input for I ² C interface. |
| B1 | P0_2 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| B3 | V _{DD(I2C-BUS)} | Power supply for I ² C interface: 1.65V~5.5V. |
| B4 | V _{DD(P)} | Power supply for internal circuit and GPIO interface: 1.65V~5.5V. |
| B5 | AD | I ² C interface device address, connects to GND, V _{DD(P)} for different device address of I ² C. |
| C1 | P0_3 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| C2 | P0_4 | Input/output port, GPIO input mode default. Can be configured as output mode. |

| No. | NAME | DESCRIPTION |
|-----|------|---|
| C3 | P0_1 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| C4 | P1_7 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| C5 | P1_6 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| D1 | P0_5 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| D2 | P0_7 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| D3 | P1_2 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| D4 | P1_4 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| D5 | P1_5 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| E1 | P0_6 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| E2 | GND | Ground. |
| E3 | P1_0 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| E4 | P1_1 | Input/output port, GPIO input mode default. Can be configured as output mode. |
| E5 | P1_3 | Input/output port, GPIO input mode default. Can be configured as output mode. |

Functional Block Diagram

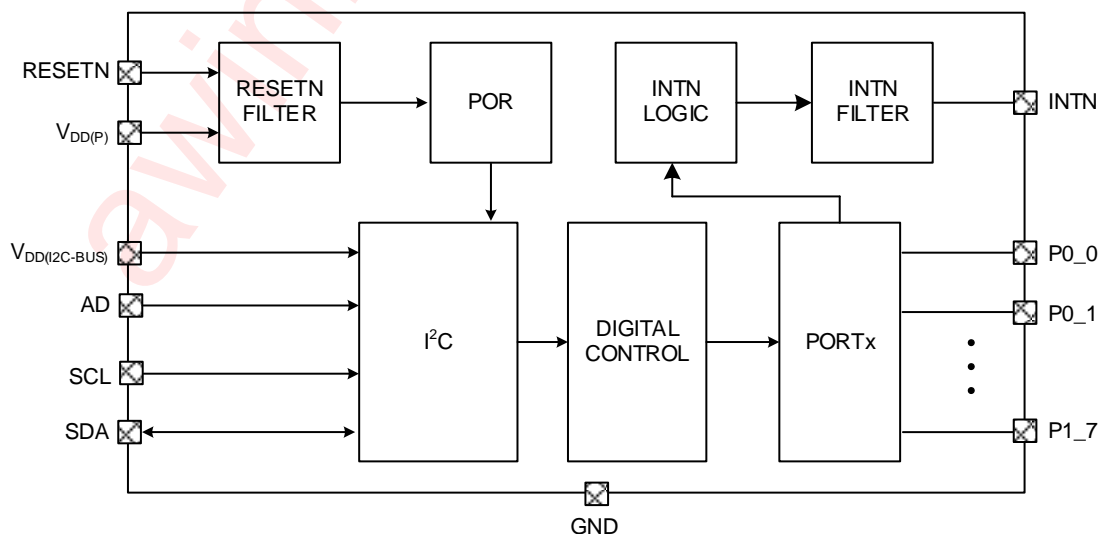


Figure 3 Functional Block Diagram

Ordering Information

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|-------------|-------------|--------------------|---------|----------------------------|---------------------------|------------------------------|
| AW95016ABGR | -40°C~85°C | BGA 3mm×3mm-24B | Y4SW | MSL3 | ROHS+HF | 3000 units/ Tape and Reel |

Absolute Maximum Ratings ^(NOTE 1)

| PARAMETERS | | RANGE |
|--|---------------------|----------------------------|
| Supply voltage range $V_{DD(P)}$, $V_{DD(I2C-BUS)}$ | | -0.3V to 6V |
| Input voltage range | SCL, SDA, RESETN | -0.3V to $V_{DD(I2C-BUS)}$ |
| Output voltage range | AD, INTN, P0_0~P1_7 | -0.3V to $V_{DD(P)}$ |
| Operating free-air temperature range | | -40°C to 85°C |
| Maximum operating junction temperature T_{JMAX} | | 150°C |
| Storage temperature T_{STG} | | -65°C to 150°C |
| Lead temperature (soldering 10 seconds) | | 260°C |
| ESD ^(NOTE 2) | | |
| HBM | | ±2kV |
| CDM | | ±1.5kV |
| Latch-Up | | |
| Test condition: JEDEC STANDARD NO.78E NOVEMBER 2016 | | +IT: 200mA -IT: -200mA |

NOTE 1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE 2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9 EIA/JESD22-C101F(CDM).

Recommended Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------------------------|--------------------------------------|------|------|------|------|
| $V_{DD(P)}$ | Supply voltage | 1.65 | | 5.5 | V |
| $V_{DD(I2C-BUS)}$ | I ² C supply voltage | 1.65 | | 5.5 | V |
| C ₁ , C ₃ | Input capacitance | | 1 | | μF |
| C ₂ , C ₄ | Input capacitance | | 100 | | nF |
| T _A | Operating free-air temperature range | -40 | 25 | 85 | °C |

Electrical Characteristics

$V_{DD(P)}=1.65V$ to $5.5V$, $V_{DD(I2C-BUS)}=1.65V$ to $5.5V$, $T_A=25^\circ C$ for typical values (unless otherwise noted)

| Parameter | Test Condition | Min. | Typ. | Max. | Unit | |
|--|---|--|------|------------------------------|---------|---------|
| Power Supply Voltage and Current | | | | | | |
| $V_{DD(P)}$ | Supply voltage | 1.65 | | 5.5 | V | |
| $V_{DD(I2C-BUS)}$ | I ² C supply voltage | 1.65 | | 5.5 | V | |
| V_{POR} | Power-on reset voltage | 0.9 | 1.2 | 1.5 | V | |
| I_{SD} | Shutdown current | $I_{DD(P)}+I_{DD(I2C-BUS)}$; RESETN=GND | | 1 | μA | |
| I_{STB} ($I_{DD(P)}+I_{DD(I2C-BUS)}$) | Stand-by current | RESETN= $V_{DD(I2C-BUS)}$, SCL, SDA= $V_{DD(I2C-BUS)}$ or GND, AD=GND, GPIO ports=GND or $V_{DD(P)}$ | | 0.5 | 5 | μA |
| | | RESETN= $V_{DD(I2C-BUS)}$, GPIO ports=GND or $V_{DD(P)}$, SDA= $V_{DD(I2C-BUS)}$ or GND, AD=GND, $f_{SCL}=400kHz$ | | 5 | 20 | μA |
| $\Delta I_{DD(I2C-BUS)}$ | Additional quiescent supply current for $V_{DD(I2C-BUS)}$ | SCL, SDA, RESETN; one input at $V_{DD(I2C-BUS)}-0.6V$, other inputs at $V_{DD(I2C-BUS)}$; $V_{DD(P)}=1.65V$ to $5.5V$ | | 20 | μA | |
| $\Delta I_{DD(P)}$ | Additional quiescent supply current for $V_{DD(P)}$ | P port, AD; One input at $V_{DD(P)}-0.6V$, Other inputs at $V_{DD(P)}$; $V_{DD(P)}=1.65V$ to $5.5V$ | | 75 | μA | |
| Digital Pin Input | | | | | | |
| V_{IH} | High-level input voltage | AD, P0_0 to P0_7, P1_0 to P1_7 | | $0.7 \times V_{DD(P)}$ | V | |
| | | SCL, SDA, RESETN | | $0.7 \times V_{DD(I2C-BUS)}$ | | |
| V_{IL} | Low-level input voltage | AD, P0_0 to P0_7, P1_0 to P1_7 | | $0.3 \times V_{DD(P)}$ | V | |
| | | SCL, SDA, RESETN | | $0.3 \times V_{DD(I2C-BUS)}$ | | |

| Parameter | | Test Condition | | Min. | Typ. | Max. | Unit |
|---------------------------|-------------------------------|--|---------------------|------|-------|------|-----------|
| I_{IL} | Input leakage current | P port; $V_I = V_{DD(P)}$ or GND; $V_{DD(P)} = 1.65V$ to $5V$ | | | | 1 | μA |
| R_{PD} | Internal pull-down resistance | RESETN | | | 1 | | $M\Omega$ |
| Digital Pin Output | | | | | | | |
| $V_{OH}^{[1]}$ | High-level output voltage | $I_{SOURCE} = 10mA$ | $V_{DD(P)} = 1.65V$ | | 1.425 | | V |
| | | | $V_{DD(P)} = 3.3V$ | | 3.22 | | |
| | | | $V_{DD(P)} = 5.0V$ | | 4.93 | | |
| | | $I_{SOURCE} = 8mA$ | $V_{DD(P)} = 1.65V$ | | 1.475 | | |
| | | | $V_{DD(P)} = 3.3V$ | | 3.225 | | |
| | | | $V_{DD(P)} = 5.0V$ | | 4.945 | | |
| $V_{OL}^{[1]}$ | Low-level output voltage | $I_{SINK} = 10mA$ | $V_{DD(P)} = 1.65V$ | | 120 | | mV |
| | | | $V_{DD(P)} = 3.3V$ | | 50 | | |
| | | | $V_{DD(P)} = 5.0V$ | | 35 | | |
| | | $I_{SINK} = 8mA$ | $V_{DD(P)} = 1.65V$ | | 95 | | |
| | | | $V_{DD(P)} = 3.3V$ | | 40 | | |
| | | | $V_{DD(P)} = 5.0V$ | | 30 | | |
| $I_{OH}^{[2][3]}$ | High-level output current | $V_{OH} = 0.8 \times V_{DD(P)}$ | $V_{DD(P)} = 1.65V$ | 2.2 | 3.3 | | mA |
| | | | $V_{DD(P)} = 3.3V$ | 12 | 16 | | |
| | | | $V_{DD(P)} = 5.0V$ | 25 | 33 | | |
| | | $V_{OH} = 0.9 \times V_{DD(P)}$ | $V_{DD(P)} = 1.65V$ | 1.2 | 2 | | |
| | | | $V_{DD(P)} = 3.3V$ | 6.5 | 9 | | |
| | | | $V_{DD(P)} = 5.0V$ | 14 | 18 | | |
| $I_{OL}^{[2][4]}$ | Low-level output current | $V_{OL} = 0.2V$ | $V_{DD(P)} = 1.65V$ | 2.5 | 4 | | mA |
| | | | $V_{DD(P)} = 3.3V$ | 8 | 11 | | |
| | | | $V_{DD(P)} = 5.0V$ | 11 | 15 | | |
| | | $V_{OL} = 0.4V$ | $V_{DD(P)} = 1.65V$ | 4.5 | 6 | | |
| | | | $V_{DD(P)} = 3.3V$ | 14 | 20 | | |
| | | | $V_{DD(P)} = 5.0V$ | 21 | 30 | | |

[1]: Register P0DSR1/P0DSR2/P1DSR1/P1DSR2 = 0xFF.

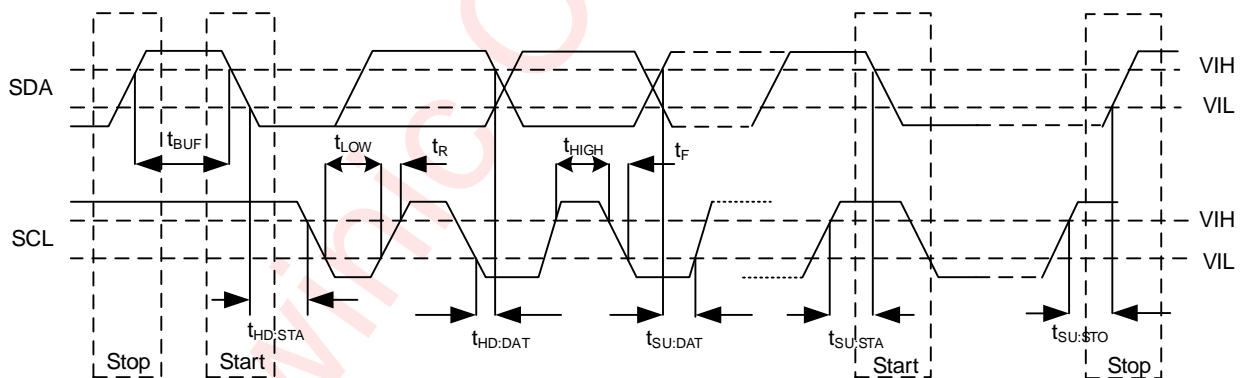
[2]: Register P0DSR1/P0DSR2/P1DSR1/P1DSR2 = 0x00.

[3]: The total current sourced by all I/Os must be limited to 160mA.

[4]: Each I/O must be externally limited to a maximum of 30mA, for a device total of 200mA.

I²C Interface Timing

| PARAMETER | | FAST MODE | | FAST MODE PLUS | | UNIT |
|---------------------|---|-----------|-----|----------------|------|------|
| | | MIN | MAX | MIN | MAX | |
| F _{SCL} | Interface clock frequency | - | 400 | - | 1000 | kHz |
| T _{HD:STA} | (Repeat-start) START condition hold time | 0.6 | - | 0.26 | - | μs |
| T _{LOW} | Low level width of SCL | 1.3 | - | 0.5 | - | μs |
| T _{HIGH} | High level width of SCL | 0.6 | - | 0.26 | - | μs |
| T _{SU:STA} | (Repeat-start) START condition setup time | 0.6 | - | 0.26 | - | μs |
| T _{HD:DAT} | Data hold time | 0 | - | 0 | - | μs |
| T _{SU:DAT} | Data setup time | 0.1 | - | 0.05 | - | μs |
| T _R | Rising time of SDA and SCL | - | 0.3 | - | 0.12 | μs |
| T _F | Falling time of SDA and SCL | - | 0.3 | - | 0.12 | μs |
| T _{SU:STO} | STOP condition setup time | 0.6 | - | 0.26 | - | μs |
| T _{BUF} | Time between start and stop condition | 1.3 | - | 0.5 | - | μs |

Figure 4 I²C Interface Timing

Detailed Functional Description

Overview

AW95016ABGR is a 16 channel GPIO controller with I²C interface. Each I/O port can be configured as output or input independently. After power-on, all channels are configured as inputs.

When configured as input, the user can turn on the interrupt function. At this time, port state changes are indicated by the INTN. The INTN can be cleared by reading GPIO through I²C or enable interrupt mask. When configured as output, push-pull or open-drain modes can be selected.

Operation Mode And Reset

Reset

Power On Reset

Upon initial power-up, the AW95016ABGR is reset by internal power-on-reset, and all registers are reset to default value, and the chip is shut down.

Once the supply voltage $V_{DD(P)}$ drops below the threshold voltage V_{POR} (1.2V), the power-on-reset will reset the chip again. By reading the bit PUST of the register STATE (address 60h), whether the chip has been reset can be detected.

When the $V_{DD(P)}$ and $V_{DD(I2C-BUS)}$ ramps up above the threshold voltage V_{POR} (1.2V) and RESETN is high, POR is pulled high, meanwhile the chip enters into active mode. Only in active mode, registers could be configured. Once $V_{DD(P)}$ is below V_{POR} , POR is triggered and all registers are reset to their default value. The recommended operation timing is shown as bellow.

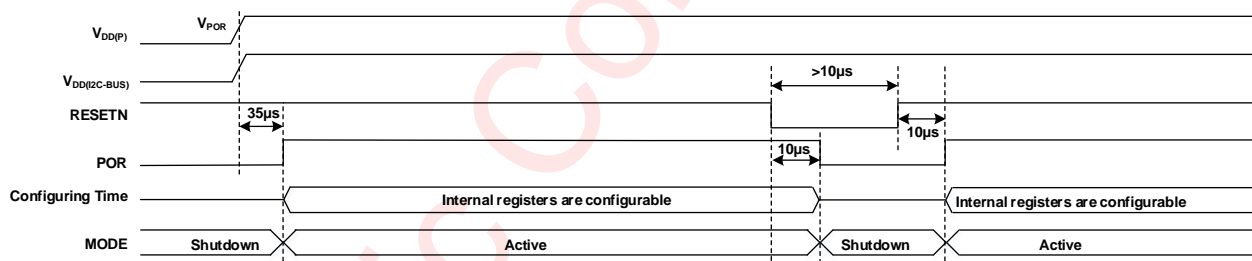


Figure 5 Power on Timing

Software Reset

By writing 00h to register RESET (address 70h), the software reset is triggered. Then all registers will be reset to the default value.

Operating Mode

Shutdown mode

The AW95016ABGR enters into shutdown mode automatically when RESETN is pulled low. In this mode, I²C interface is not accessible, all registers will be reset and can't be configured.

Active mode

If pin RESETN is high, the chip enters into active mode. During this period, all registers are configurable with full function.

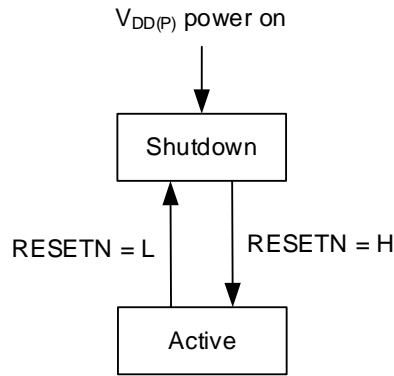


Figure 6 AW95016ABGR Operating Mode Transition

Feature Description

The following figure is the simplified schematic of GPIO. In this figure 'read pulse' is the response signal generated by I²C module during reading data from P0DI/P1DI (address 00h/01h). The letter 'x' in the names of registers in the figure represents '0' or '1'.

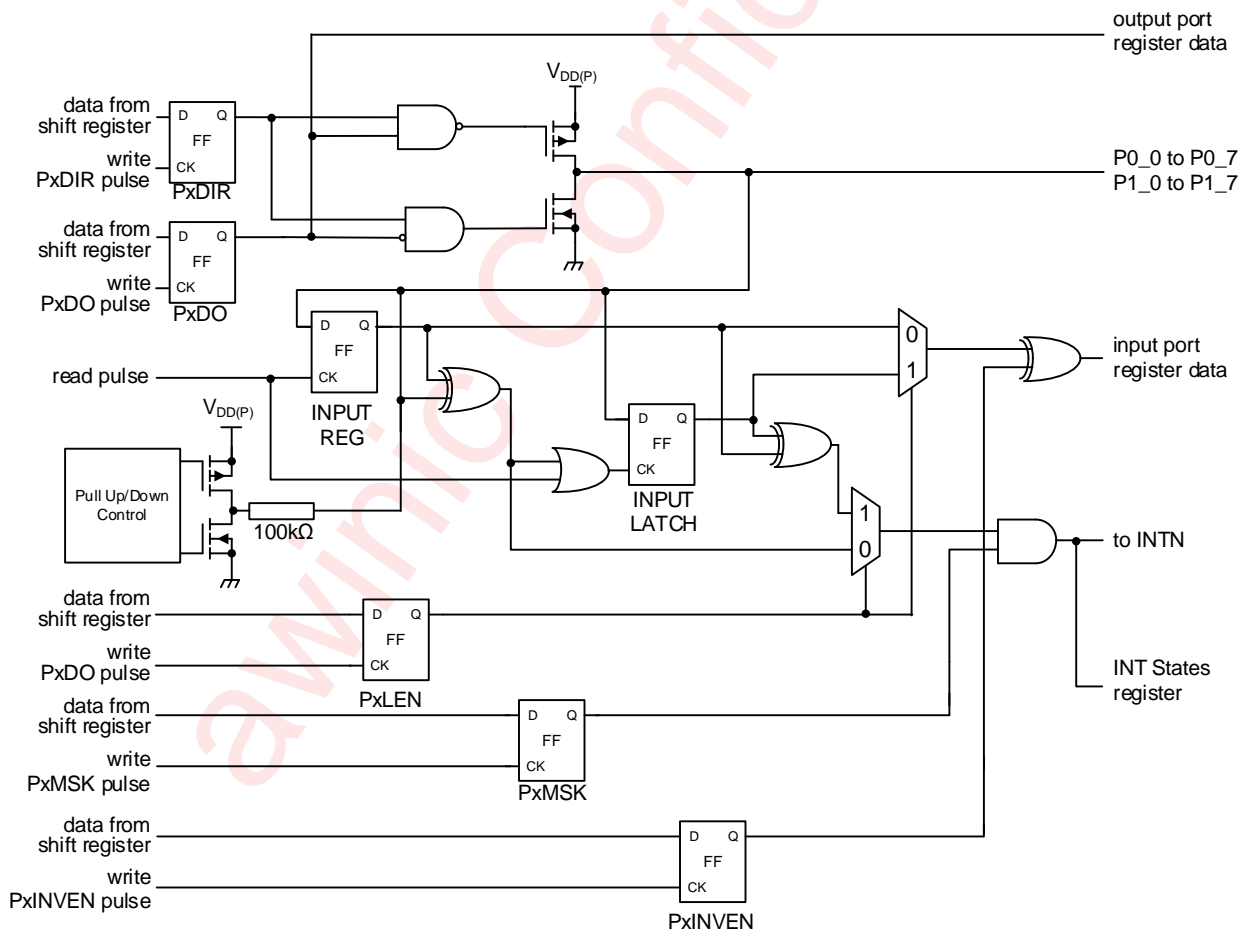


Figure 7 Simplified Schematic of GPIO

GPIO Output

If a bit in registers P0DIR/P1DIR (address 06h/07h) is set to '1', the corresponding port pin is enabled as output. The output data of ports can be configured by P0DO/P1DO (address 02h/03h).

User can choose push-pull or open-drain mode of each port by setting the corresponding bit in P0DOMD/P1DOMD (address 16h/17h) to '0' or '1'. The default value is '0' as push-pull mode.

The output drive strength of GPIO is controlled by registers P0DSR1/P0DSR2/P1DSR1/P1DSR2 (address 08h/09h/0Ah/0Bh). Each port can be configured independently by two bits of those registers. The relationship between two bits and GPIO output drive strength is 00b = 0.25x, 01b = 0.5x, 10b = 0.75x or 11b = 1x.

GPIO Input

If a bit in registers P0DIR/P1DIR (address 06h/07h) is set to '0', the corresponding port pin is enabled as a high-impedance input. Read-only registers P0DI/P1DI (address 00h/01h) reflect the incoming logic levels of the pins and the value can be read by I²C interface. If a bit in registers P0INVEN/P1INVEN (address 04h/05h) is set to '1', the corresponding bit read from P0DI/P1DI will be inverted.

The port level can be configured as '0' or '1' by setting P0PEN/P1PEN (address 0Eh/0Fh) and P0PMD/P1PMD (address 10h/11h) as a fixed port level. User can enable internal pull-up/pull-down resistors for each I/O pins by setting corresponding bit of registers P0PEN/P1PEN (address 0Eh/0Fh) to '1'. Meanwhile, a 100kΩ resistor of pull-up or pull-down for I/O pins can be configured by setting P0PMD/P1PMD (address 10h/11h) to '0' or '1'.

Interrupt

After power on reset, each bit of registers P0MSK/P1MSK (address 12h/13h) is set to '1', which means the interrupt function are disabled. User can set each bit in those registers to '0' to enable the interrupt function of corresponding port.

When one port is configured as input and the interrupt function is enabled, any changes of input data of the port will set the corresponding bit in P0INTST/P1INTST (address 14h/15h) to '1', and at the same time generate an interrupt event. Reading registers P0DI/P1DI by I²C interface will clear the value of registers P0INTST/P1INTST. The sequence diagram is shown as below:

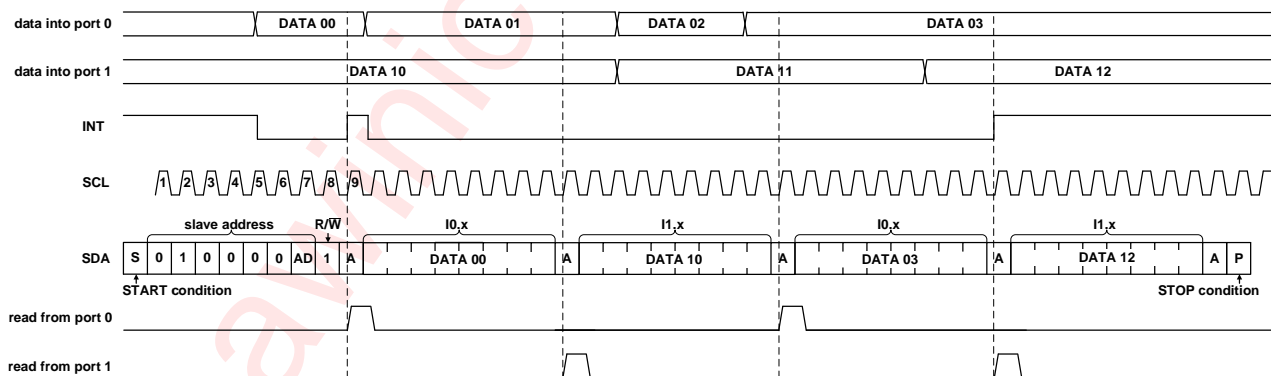


Figure 8 Interrupt Function Is Enabled and Non-latched, Clear by Reading Registers P0DI/P1DI

When interrupt function is enabled and a bit in registers P0LEN/P1LEN (address 0Ch/0Dh) is '0', the corresponding input pin state is not latched (as default). When the input data changes, an interrupt is generated. If the input data recovers, the interrupt is cleared. The sequence diagram is shown as below:

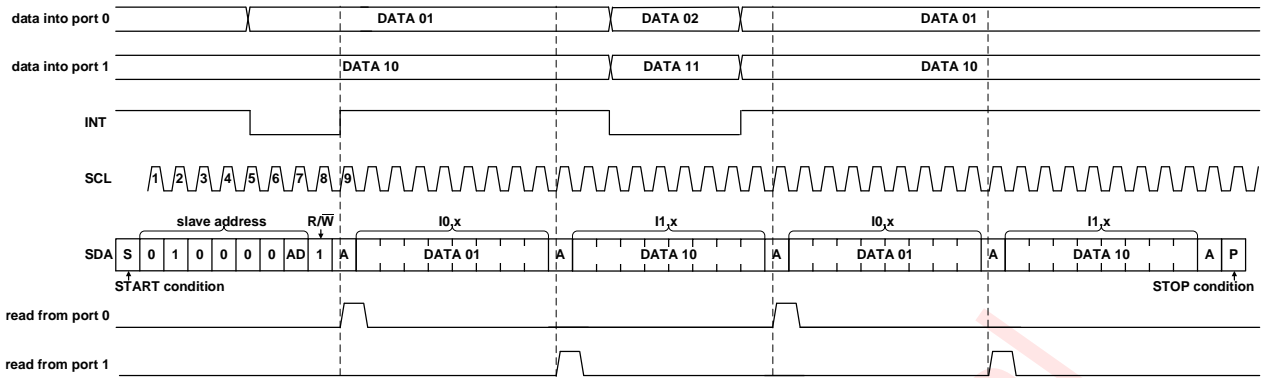


Figure 9 Interrupt Function Is Enabled and Non-latched, Clear by Recovering Input Data

In contrast, when a bit in registers P0LEN/P1LEN is '1', the corresponding input pin state is latched. When the input data of port changes, an interrupt is generated. Even if the input data recovers, the interrupt is not cleared until P0DI/P1DI are read. During the interruption the value read from P0DI/P1DI reflects the value that caused the interrupt. After reading, the interrupt is cleared. If read again, P0DI/P1DI will reflect the current input data of the port. The sequence diagram is shown as below:

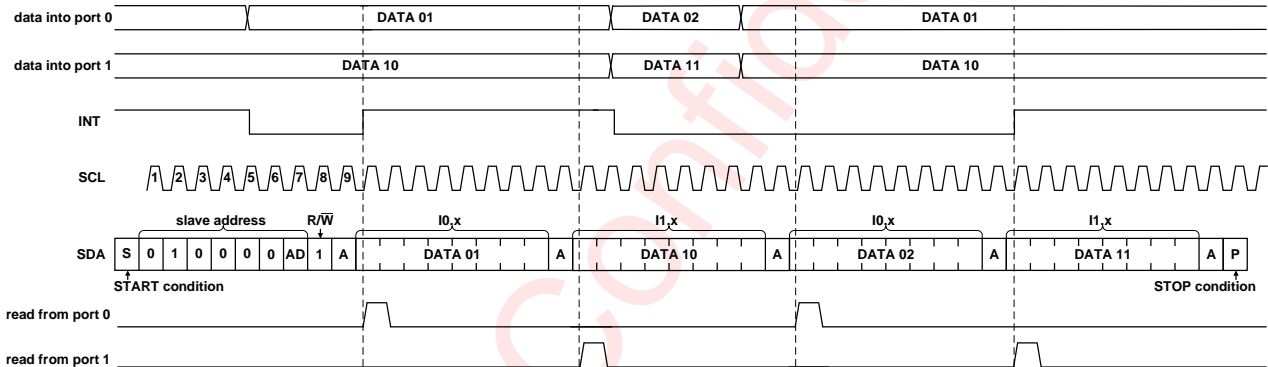


Figure 10 Interrupt Function Is Enabled and Latch Enabled

Note: In addition, when the register address read by the host is 00h or 01h, the address will only jump between 00h and 01h.

I²C Interface

The AW95016ABGR supports the I²C protocol. The maximum frequency supported by the I²C is 1MHz. The pull-up resistor for the SDA and SCL can be selected from 1k to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I²C, 1kΩ is recommended for 1MHz I²C. The voltage from 1.8V to 3.3V is allowed for the I²C interface. Additionally, the I²C chip supports continuous read and write operations. Particularly, if register address is 00h or 01h, the slave chip will poll register address between 00h and 01h.

Device Address

The I²C device address is 7-bit (A7~A1), followed by the bit R/W (A0). Set A0 to "0" for writing and "1" for reading. The values of bit A1 and A2 are depended on the pin AD. There are two options: V_{DD(P)} or GND. The A7 to A3 is "01000" constantly. The chip also supports using a broadcast slave address of 1Ch. All slave addresses as followed.

| AD PIN | A7:A3 | A2:A1 | A0 | Chip Address | Broadcast Address |
|--------------------|-------|-------|-----|--------------|-------------------|
| GND | 01000 | 00 | 0/1 | 20h | 1Ch |
| V _{DD(P)} | | 01 | | 21h | |

I²C Start/Stop

All transactions begin with a START and are terminated by a STOP sent by master to slave. A high-to-low transition on the SDA input/output while the SCL input is high defines a START condition. A low-to-high transition on the SDA input/output while the SCL input is high defines a STOP condition.

In particular, the bus stays busy when a repeated START (Sr) is generated instead of a STOP signal corresponding to the last START (S). Sr and S are usually regarded as equivalent.

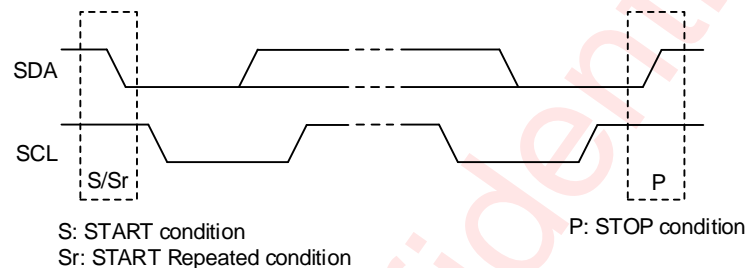


Figure 11 I²C Start/Stop Condition Timing

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level. Each SCL pulse corresponds to one bit data transaction.

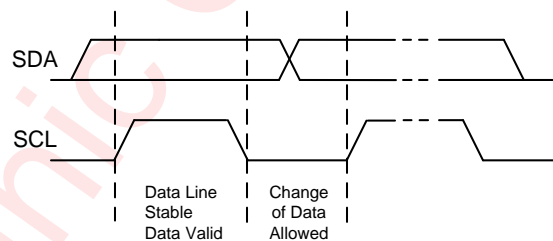
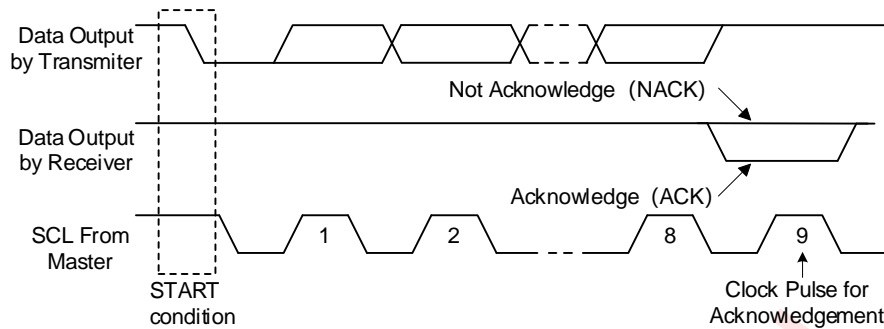


Figure 12 Data Validation Diagram

Acknowledge(ACK)

ACK means the successful transaction of I²C bus data. During writing cycle, after master sends 8-bit data, SDA must be released by master and SDA is pulled down to GND by slave chip when slave sends ACK.

During reading cycle, after slave chip sends 8-bit data, slave releases the SDA and waits for ACK from master. If master sends ACK with STOP condition, slave chip sends the next data. If master sends NACK, slave chip stops sending data and waits for I²C stop.

Figure 13 I²C ACK Timing

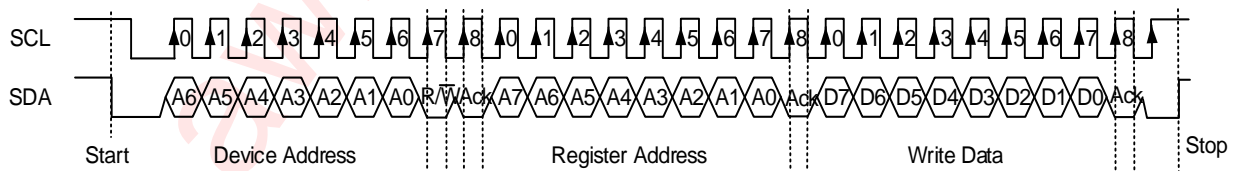
Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line aborts the current transaction during the high state of the SCL. New data should be sent to SDA bus during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits and is transferred with the most significant bit first. After each byte, an ACK signal must follow.

In a write process, the following steps should be followed:

- Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
- Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8-bit).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g).
- Master generates STOP condition to indicate write cycle end.

Figure 14 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

- Master device generates START condition.
- Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
- Slave device sends acknowledge signal if the slave address is correct.

- d) Master sends control register address (8-bit).
- e) Slave sends acknowledge signal.
- f) Master generates STOP condition followed with START condition or REPEAT START condition.
- g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
- h) Slave device sends acknowledge signal if the slave address is correct.
- i) Slave sends data byte from addressed register.
- j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. In particular, if register address is 00h or 01h, the slave chip will poll register address between 00h and 01h.
- k) If the master device generates STOP condition, the read cycle is ended.

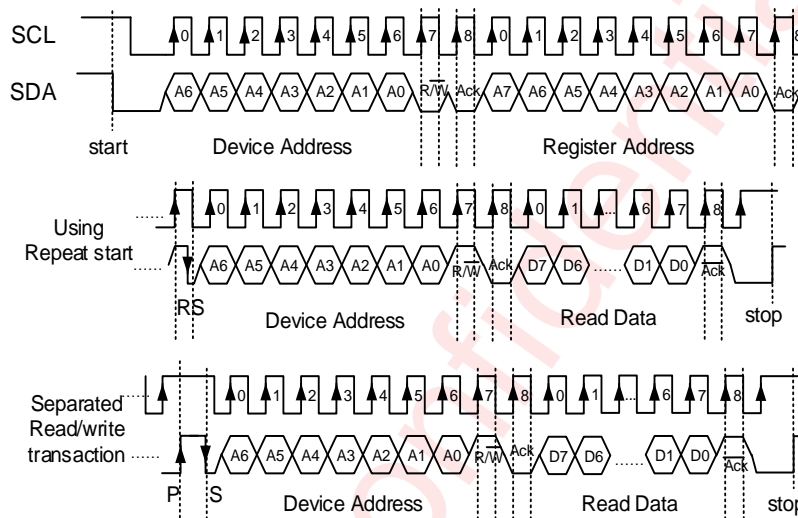


Figure 15 I²C Read Byte Cycle

Register Configuration

Register List

| ADDR | R/W | NAME | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DEF |
|------|-----|---------|---------|-------|----|-------|----|-------|----|-----|-----|
| 00h | R | P0DI | P0DI | | | | | | | | 00h |
| 01h | R | P1DI | P1DI | | | | | | | | 00h |
| 02h | RW | P0DO | P0DO | | | | | | | | 00h |
| 03h | RW | P1DO | P1DO | | | | | | | | 00h |
| 04h | RW | P0INVEN | P0INVEN | | | | | | | | 00h |
| 05h | RW | P1INVEN | P1INVEN | | | | | | | | 00h |
| 06h | RW | P0DIR | P0DIR | | | | | | | | 00h |
| 07h | RW | P1DIR | P1DIR | | | | | | | | 00h |
| 08h | RW | P0DSR1 | P03DS | P02DS | | P01DS | | P00DS | | 00h | |
| 09h | RW | P0DSR2 | P07DS | P06DS | | P05DS | | P04DS | | 00h | |
| 0Ah | RW | P1DSR1 | P13DS | P12DS | | P11DS | | P10DS | | 00h | |
| 0Bh | RW | P1DSR2 | P17DS | P16DS | | P15DS | | P14DS | | 00h | |
| 0Ch | RW | P0LEN | P0LEN | | | | | | | | 00h |
| 0Dh | RW | P1LEN | P1LEN | | | | | | | | 00h |
| 0Eh | RW | P0PEN | P0PEN | | | | | | | | 00h |
| 0Fh | RW | P1PEN | P1PEN | | | | | | | | 00h |

| ADDR | R/W | NAME | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DEF |
|------|-----|---------|----------|----|----|-------|----|----|----|-----|-----|
| 10h | RW | P0PMD | P0PMD | | | | | | | | 00h |
| 11h | RW | P1PMD | P1PMD | | | | | | | | 00h |
| 12h | RW | P0MSK | P0MSK | | | | | | | | FFh |
| 13h | RW | P1MSK | P1MSK | | | | | | | | FFh |
| 14h | R | P0INTST | P0INTST | | | | | | | | 00h |
| 15h | R | P1INTST | P1INTST | | | | | | | | 00h |
| 16h | RW | P0DOMD | P0DOMD | | | | | | | | 00h |
| 17h | RW | P1DOMD | P1DOMD | | | | | | | | 00h |
| 1Ah | RW | GGCR | - | | | | | | | EGC | - |
| 60h | R | STATE | - | | | PUST | - | | | | 00h |
| 61h | RW | GCR2 | - | | | BSDIS | - | | | | 00h |
| 70h | RW | RESET | RESET/ID | | | | | | | | 80h |

Register Detailed Description

P0DI/P1DI: Input State Register (Address 00h/01h)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|--|---------|
| 7:0 | P0DI | R | P0_7~P0_0 input state 0: low level 1: high level | 00h |
| 7:0 | P1DI | R | P1_7~P1_0 input state 0: low level 1: high level | 00h |

P0DO/P1DO: Output State Register (Address 02h/03h)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|---|---------|
| 7:0 | P0DO | RW | P0_7~P0_0 output state 0: low level 1: high level | 00h |
| 7:0 | P1DO | RW | P1_7~P1_0 output state 0: low level 1: high level | 00h |

P0INVEN/P1INVEN: Invert Enable Register (Address 04h/05h)

| Bit | Symbol | R/W | Description | Default |
|-----|---------|-----|--|---------|
| 7:0 | P0INVEN | RW | P0_7~P0_0 input state invert enable 0: disable 1: enable | 00h |
| 7:0 | P1INVEN | RW | P1_7~P1_0 input state invert enable 0: disable 1: enable | 00h |

P0DIR/P1DIR: Direction Register (Address 06h/07h)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|---|---------|
| 7:0 | P0DIR | RW | P0_7~P0_0 input/output direction 0: input 1: output | 00h |
| 7:0 | P1DIR | RW | P1_7~P1_0 input/output direction 0: input 1: output | 00h |

P0DSR1/ P0DSR2/ P1DSR1/P1DSR2: Drive Strength Register (Address 08h~0Bh)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|---|---------|
| 7:6 | P0DSR1 | RW | P0_3 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 5:4 | P0DSR1 | RW | P0_2 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 3:2 | P0DSR1 | RW | P0_1 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 1:0 | P0DSR1 | RW | P0_0 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 7:6 | P0DSR2 | RW | P0_7 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 5:4 | P0DSR2 | RW | P0_6 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 3:2 | P0DSR2 | RW | P0_5 GPIO drive capability of the I/O 00: 0.25x | 00 |

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|---|---------|
| | | | 01: 0.5x 10: 0.75x 11: 1x | |
| 1:0 | P0DSR2 | RW | P0_4 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 7:6 | P1DSR1 | RW | P1_3 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 5:4 | P1DSR1 | RW | P1_2 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 3:2 | P1DSR1 | RW | P1_1 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 1:0 | P1DSR1 | RW | P1_0 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 7:6 | P1DSR2 | RW | P1_7 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 5:4 | P1DSR2 | RW | P1_6 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |
| 3:2 | P1DSR2 | RW | P1_5 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x | 00 |

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|---|---------|
| | | | 11: 1x | |
| 1:0 | P1DSR2 | RW | P1_4 GPIO drive capability of the I/O 00: 0.25x 01: 0.5x 10: 0.75x 11: 1x | 00 |

P0LEN/P1LEN: Latch Enable Register (Address 0Ch/0Dh)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|---|---------|
| 7:0 | P0LEN | RW | P0_7~P0_0 input state latch enable 0: disable 1: enable | 00h |
| 7:0 | P1LEN | RW | P1_7~P1_0 input state latch enable 0: disable 1: enable | 00h |

P0PEN/P1PEN: Pull Up/Down Enable Register (Address 0Eh/0Fh)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|--|---------|
| 7:0 | P0PEN | RW | P0_7~P0_0 pull up/down resistors enable 0: disable 1: enable | 00h |
| 7:0 | P1PEN | RW | P1_7~P1_0 pull up/down resistors enable 0: disable 1: enable | 00h |

P0PMD/P1PMD: Pull Up/Down Mode Register (Address 10h/11h)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|---|---------|
| 7:0 | P0PMD | RW | P0_7~P0_0 pull up/down mode 0: pull down 1: pull up | 00h |
| 7:0 | P1PMD | RW | P1_7~P1_0 pull up/down mode 0: pull down 1: pull up | 00h |

P0MSK/P1MSK: Interrupt Mask Register (Address 12h/13h)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|---|---------|
| 7:0 | P0MSK | RW | P0_7~P0_0 interrupt mask 0: disable 1: enable | FFh |
| 7:0 | P1MSK | RW | P1_7~P1_0 interrupt mask 0: disable 1: enable | FFh |

P0INTST/P1INTST: Interrupt State Register (Address 14h/15h)

| Bit | Symbol | R/W | Description | Default |
|-----|---------|-----|--|---------|
| 7:0 | P0INTST | R | P0_7~P0_0 interrupt state 0: no interrupt occurred 1: interrupt occurred | 00h |
| 7:0 | P1INTST | R | P1_7~P1_0 interrupt state 0: no interrupt occurred 1: interrupt occurred | 00h |

P0DOMD/P1DOMD: Output Mode Register (Address 16h/17h)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|--|---------|
| 7:0 | P0DOMD | RW | P0_7~P0_0 output mode 0: push pull 1: open drain | 00h |
| 7:0 | P1DOMD | RW | P1_7~P1_0 output mode 0: push pull 1: open drain | 00h |

GGCR: GPIO Global Control Register (Address 1Ah)

| Bit | Symbol | R/W | Description | Default |
|-----|----------|-----|--|---------|
| 7:2 | reserved | - | - | 000000 |
| 1:0 | EGC | RW | GPIO output edge control 00: 0.5ns 01: 1ns 10: 4ns 11: 8ns | 00 |

STATE: UVLO Control Register (Address 60h)

| Bit | Symbol | R/W | Description | Default |
|-----|----------|-----|--|---------|
| 7:5 | reserved | - | - | 000 |
| 4 | PUST | R | Power up status 0: no power up occurred 1: Power up occurred | 0 |
| 3:0 | reserved | - | - | 0000 |

GCR2: Global Control Register2 (Address 61h)

| Bit | Symbol | R/W | Description | Default |
|-----|----------|-----|---|---------|
| 7:5 | reserved | - | - | 000 |
| 4 | BSDIS | RW | I ² C broadcast slave address disable 0: I ² C broadcast slave address enable 1: I ² C broadcast slave address disable | 0 |
| 3:0 | reserved | - | - | 0000 |

RESET: Reset Register (Address 70h)

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|--|---------|
| 7:0 | RESET | RW | Software reset/ID Write 00h will reset all registers to their default value. When read, chip ID is read out. | 80h |

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PCB Layout Consideration

AW95016ABGR is a 16 channel general purpose I/O (GPIO) expander controller. Each channel can be configured as GPIO input or output separately. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

1. The C₁, C₂, C₃, C₄ should be placed as close to the chip as possible.
2. The GND pad must be well connected to the ground of the PCB, and add as many thermal vias as possible near the GND on the PCB for the heat conductivity of the device and PCB.

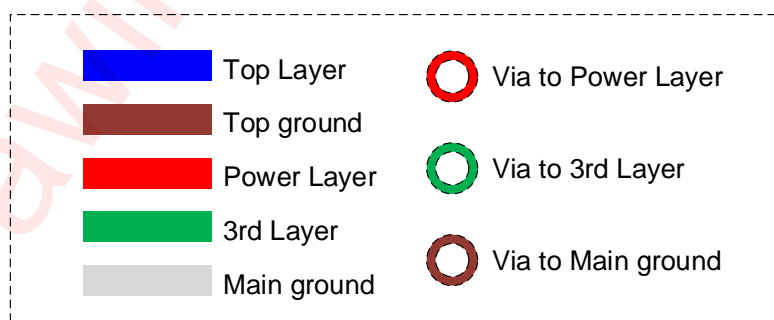
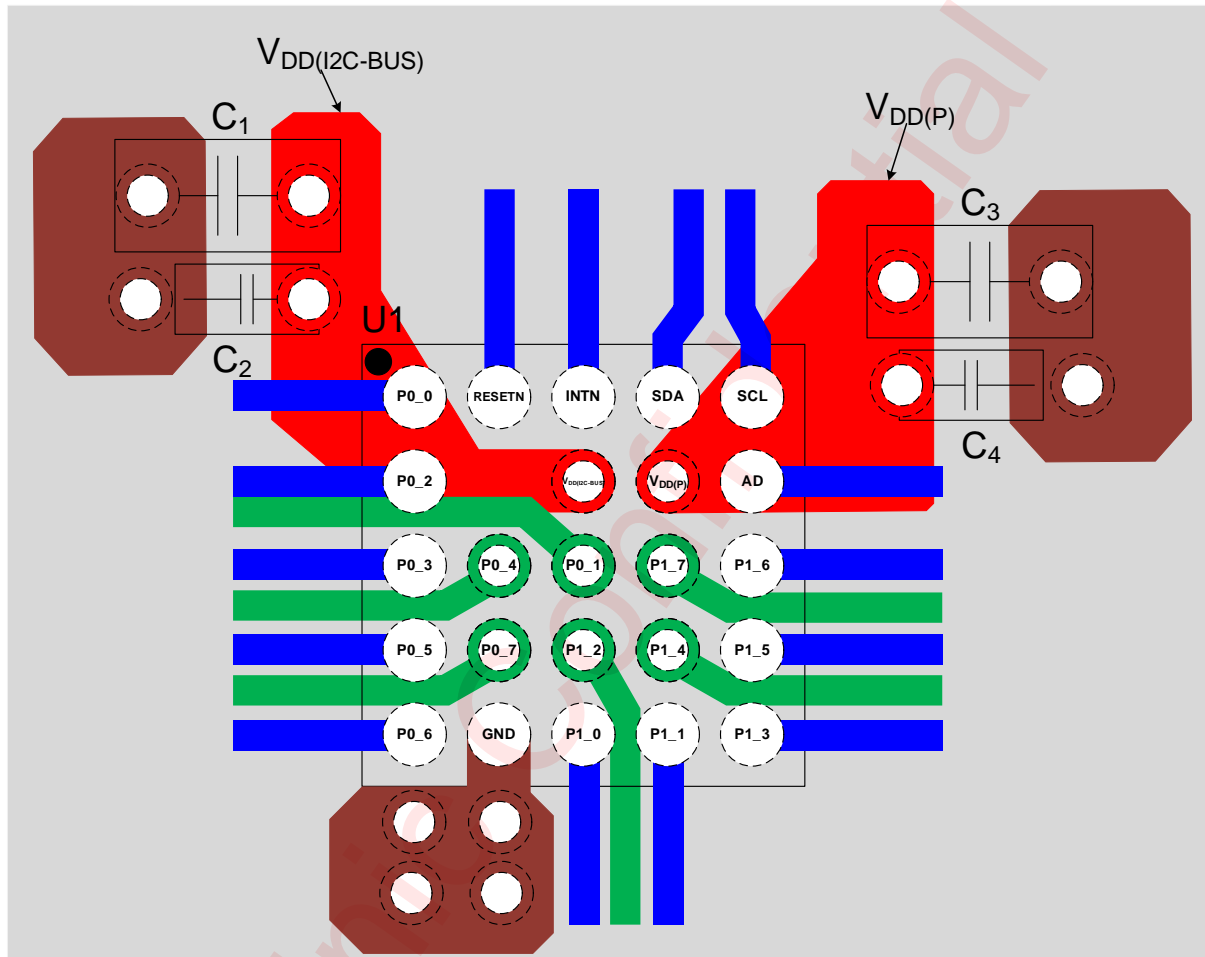
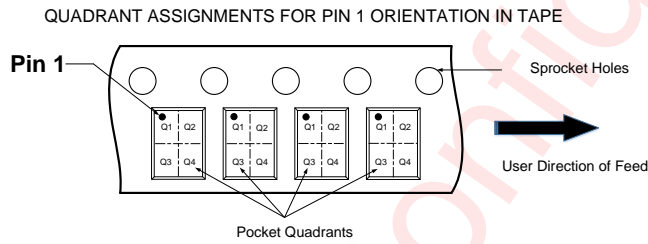
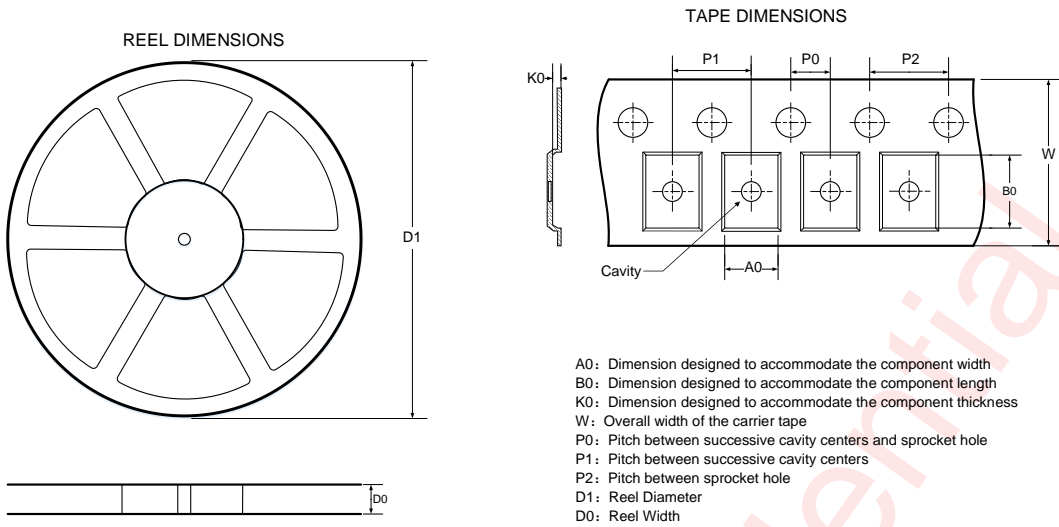


Figure 16 AW95016ABGR Layout Example

Tape And Reel Information

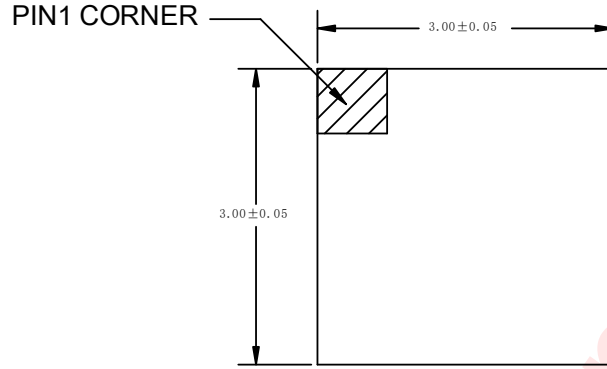


Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

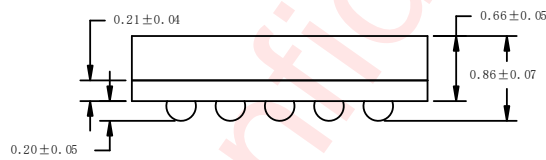
| DIMENSIONS AND PIN1 ORIENTATION | | | | | | | | | |
|---------------------------------|---------|---------|---------|---------|---------|---------|---------|--------|---------------|
| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
| 330 | 12.4 | 3.3 | 3.3 | 1.1 | 2 | 8 | 4 | 12 | Q1 |

All dimensions are nominal

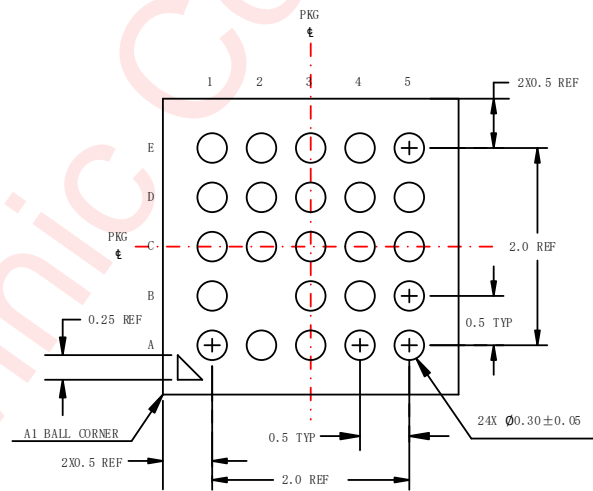
Package Description



Top View



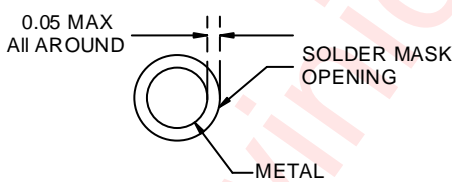
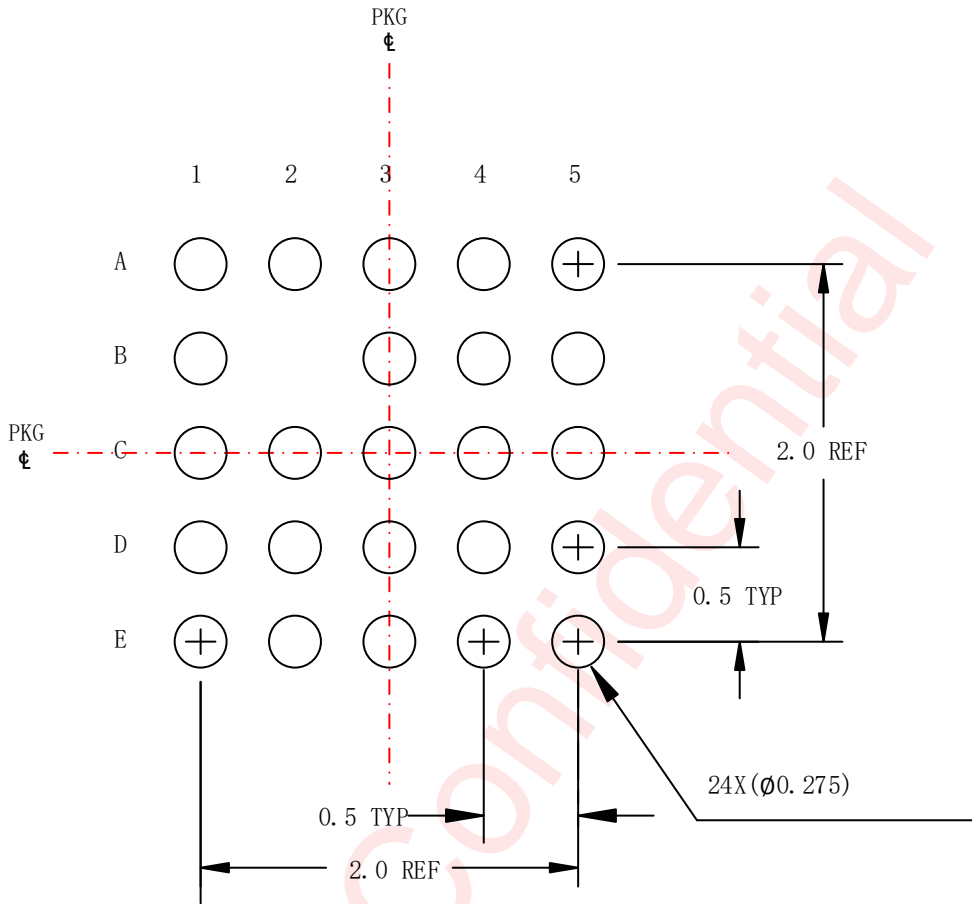
Side View



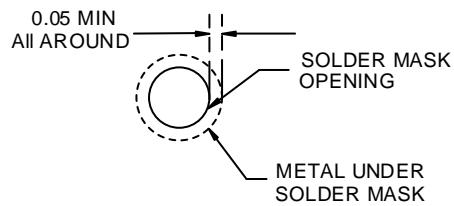
Bottom View

Unit: mm

Land Pattern Data



NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

| Version | Date | Change Record |
|---------|-----------|--|
| V1.0 | Sep. 2020 | Officially released |
| V1.1 | May. 2022 | Add I _{OH} , I _{OL} and I _{IL} , correct default value of register 70h. |
| V1.2 | Mar. 2023 | Update the typical application circuit (P2). Increase the module of Recommended Operating Conditions(P5). Increase the time requirements in the figure of power on timing (P9). Correct the slave address of figure 8, figure 9, figure 10(P11~P12). Modify the description of register 08h~0Bh (P17~P19). Adjust format and related description. |
| V1.3 | Apr. 2023 | Change V _{POR} max from 1.6V to 1.5V in the Electrical Characteristics conditions (P6). |
| V1.4 | May. 2023 | Update the description of the features(P1). Update the test condition of I _{STB} and the description of additional quiescent supply current in the Electrical Characteristics conditions (P6). |
| V1.5 | Jul. 2023 | Update the tolerance for length and width dimensions from 3.00±0.10mm to 3.00±0.05mm in the part of Package Description (P24). |

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