28V, 1.1MHz Step-up Converter with 2A Switch

Features

- Internal 0.4Ω Power MOSFET
- Up to 28V Output Voltage
- 38V Over Voltage Shutdown
- 1.1MHz Switching Frequency
- Built-in Over-current and Over-temperature Protection
- SOT23-5L package

General Description

The AW36201 is a monolithic step up converter integrating a 2A/40V power MOSFET. It uses current mode, fixed frequency architecture to regulate the output voltage，providing fast transient response and cycle by cycle current limit.

The AW36201 integrates under-voltage lockout, over voltage protection, over current protection, Over-temperature Protection.

Applications

APD Bias Generation
Portable Media Players
Handheld Computers and PDAs
Digital Still Cameras

Typical Application Circuit

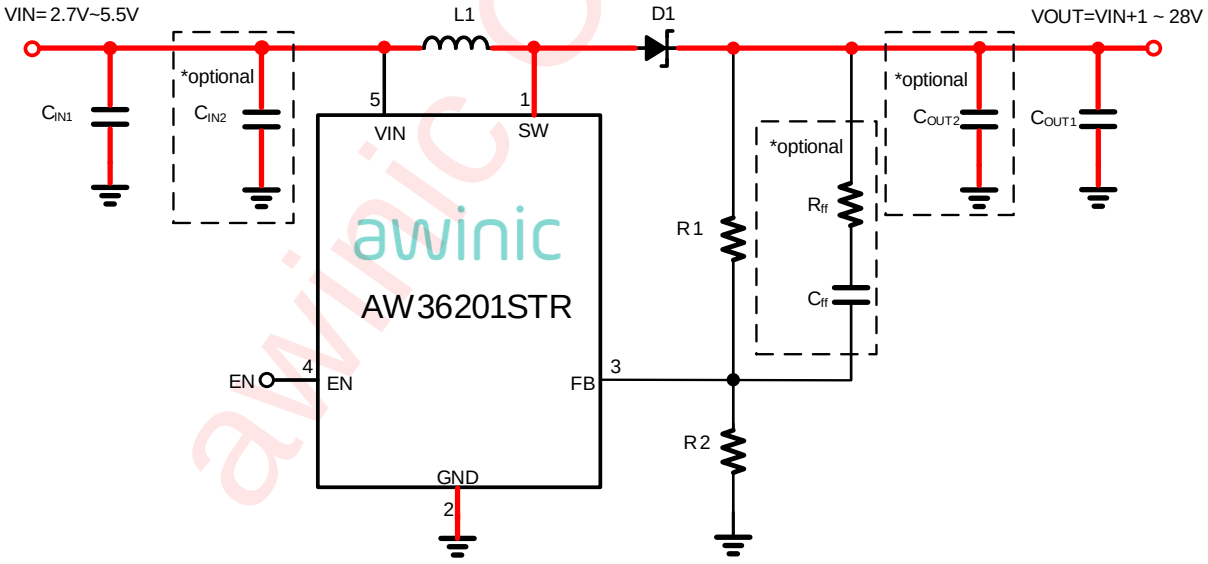


Figure 1 Typical Application Circuit of AW36201

Pin Configuration and Top Mark

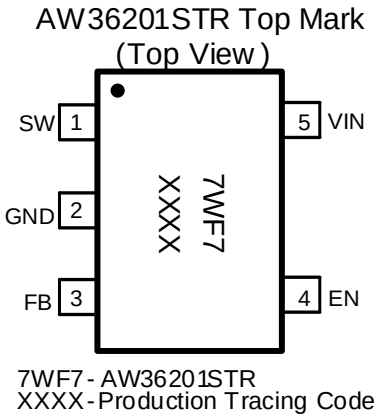


Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	SW	Connect to the drain of the internal NFET. Connect SW to the junction of the inductor and the Schottky diode anode.
2	GND	Ground.
3	FB	Feedback Input. Reference voltage is 0.2V, connect a resistor divider from the output to this pin.
4	EN	ON/OFF Control Input, with an internal 600kΩ pull-down resistor to GND.
5	VIN	Input Supply Pin. Must be locally bypassed.

Functional Block Diagram

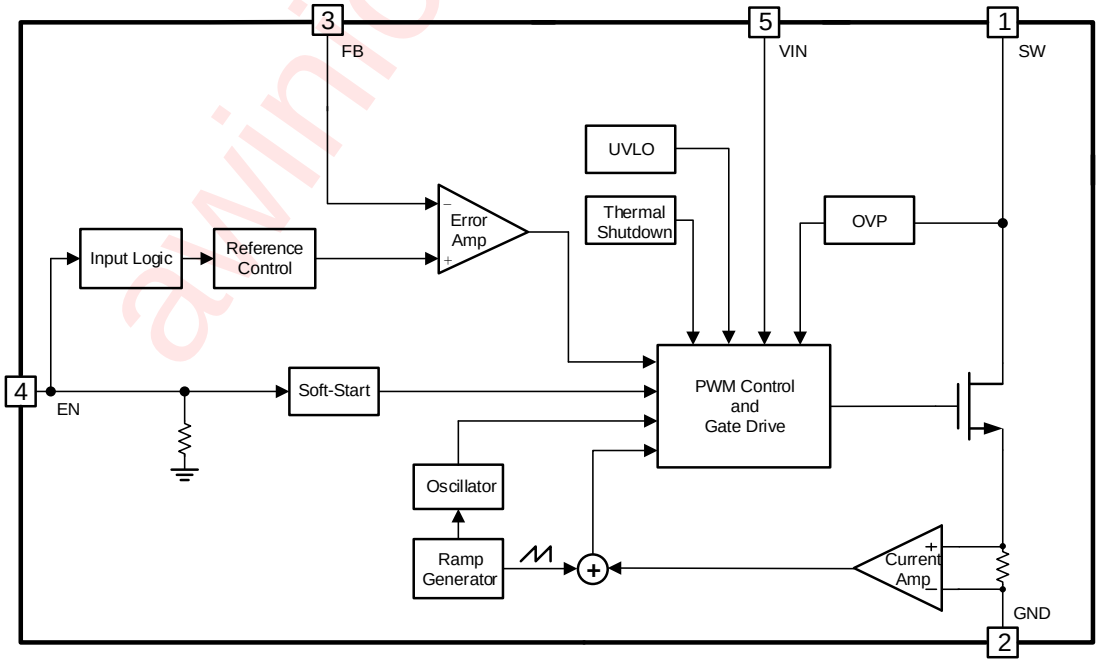


Figure 3 Functional Block Diagram

Typical Application Circuit

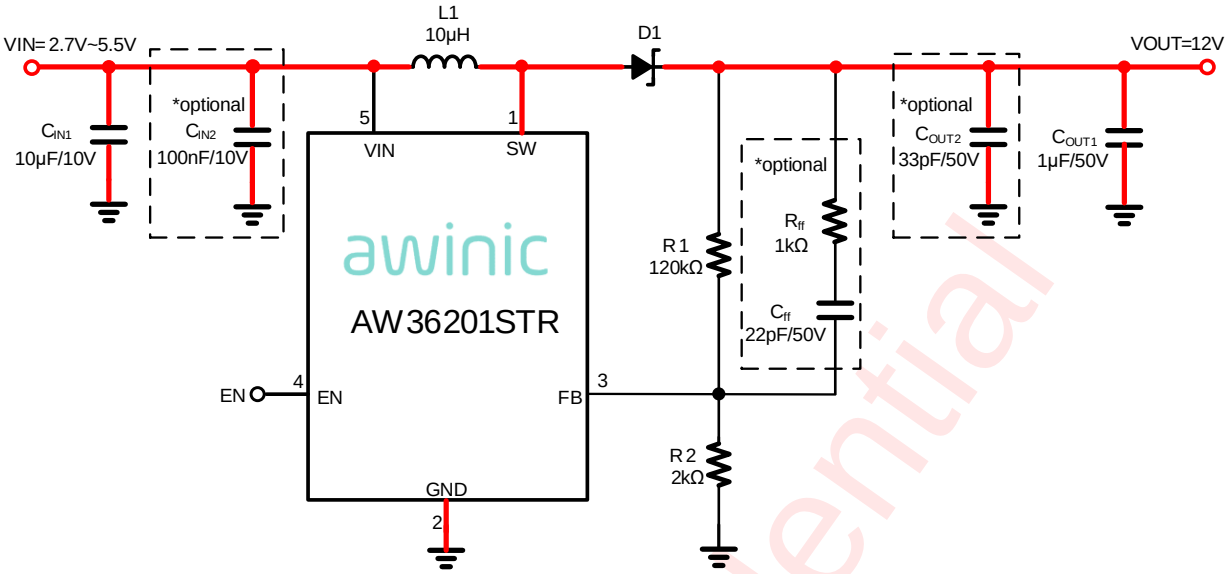


Figure 4 Typical Application Circuit of AW36201

Notice for Typical Application Circuit:

1：Recommended device for AW36201:

L: LQH3NPN100NM0

C_{IN1}: Murata GRM188R61C106MA73

C_{IN2}: Murata GRM155R61C104K

C_{OUT1}: Murata GRM21BR71H105KA

C_{OUT2}: Murata GRM1555C1H330GA

Schottky Diode: ONsemi MBR0540

2：C_{IN2} and C_{OUT2} are recommended to use in parallel with the input capacitor and output capacitor to suppress high frequency noise.

3：Red lines are high current paths, reference to the section Application Information.

4：The capacitors (C_{IN1}, C_{IN2}, C_{OUT1}, C_{OUT2}) should be placed as close to the pins of the IC as possible.

5：Minimize trace lengths between the IC and the inductor, the Schottky diode and the output capacitor, keep these traces short, direct, and wide.

6：Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW36201STR	-40°C～85°C	SOT23-5L	7WF7	MSL3	ROHS+HF	3000 units/ Tape and Reel

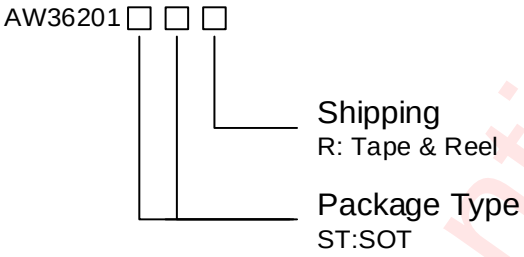


Figure 5 Package Information

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply voltage range VIN(NOTE 2)	-0.3V to 6V
Voltage on EN,FB(NOTE 2)	-0.3V to 6V
Voltage on SW(NOTE 2)	-0.3V to 40V
Junction-to-ambient thermal resistance θ_{JA}	190°C/W
Operating free-air temperature range	-40°C to 85°C
Operating Junction temperature T_J	-40°C to 150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD(NOTE 3)	
ALL PINS HBM (human body model)(NOTE 4)	±2kV
ALL PINS CDM (charge device model)(NOTE 5)	±1.5kV
Latch-up(NOTE 6)	
Latch-up current maximum rating per JEDEC standard	+IT: +200mA -IT: -200mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *All voltage values are with respect to network ground terminal.*

NOTE3: This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. AWINIC recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance

degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE5: Test Condition: ESDA/JEDEC JS-002-2018.

NOTE6: Test Condition: JESD78E.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Input voltage	2.7	3.6	5.5	V
C_{IN1}	Input capacitance	4.7	10	22	μF
C_{OUT1}	Output capacitance	0.47	1	4.7	μF
L1	Inductance	4.7	10	/	μH
R1	Upper resistor of voltage divider			1.4M	Ω
R2	Lower resistor of voltage divider	1k		10k	Ω
T_A	Operating free-air temperature range	-40	25	85	°C

Electrical Characteristics

Test Condition: T_A = 25°C, VIN = 3.6V, V_{EN} = VIN (Unless otherwise specified).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
VIN	Input voltage range		2.7		5.5	V
V_{UVLO}	Under-voltage lockout threshold	VIN falling		2.2	2.39	V
V_{HYS}	Under-voltage lockout hysteresis			100		mV
I_{SD}	Shutdown current	V_{EN} = GND, VIN=4.2V		0.1	1	μA
I_Q	Operating quiescent current	VFB = 1V		250		μA
BOOST CONVERTER						
$R_{DS(on)}$	N-channel MOSFET on-resistance	VIN = 3.6V		0.4	0.7	Ω
		VIN = 3.0V			0.7	Ω
f_S	Oscillator frequency			1100		kHz
D_{MAX}	Maximum duty cycle		90	93		%
V_{REF}	Voltage feedback regulation voltage		194	200	205	mV
OCP AND OVP						
I_{LIM}	N-channel MOSFET current limit		1.5	2	2.5	A
V_{OVP}	Open FB overvoltage protection threshold	Measured on the SW pin	36	38	40	V
t_{REF}	VREF filter time constant			480		μs
EN INTERFACE						
V_{EN_H}	EN logic high voltage	VIN = 2.7V to 5.5V	1.4			V
V_{EN_L}	EN logic low voltage	VIN = 2.7V to 5.5V			0.4	V
R_{EN}	EN pull down resistor			600		kΩ
t_{OFF}	EN pulse width to shutdown	EN high to low	2.5			ms
THERMAL SHUTDOWN						
T_{OTP}	Thermal shutdown threshold			165		°C
T_{HYS}	Thermal shutdown threshold hysteresis			15		°C

Typical Characteristics

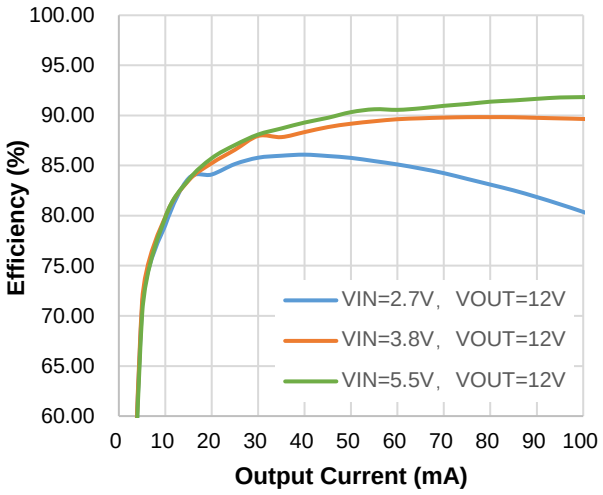


Figure 6 Efficiency vs Output Current

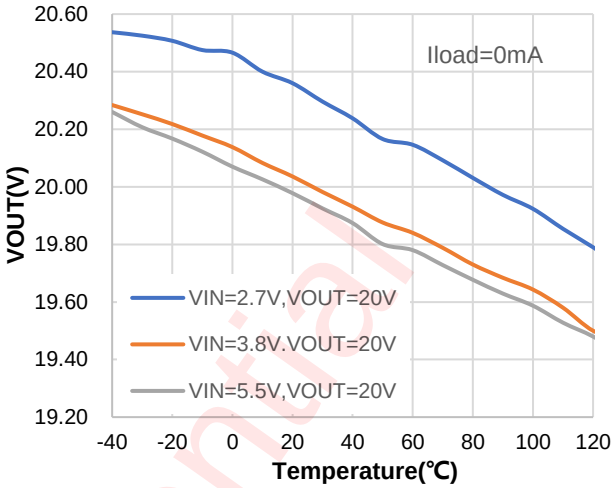


Figure 7 VOUT vs Temperature

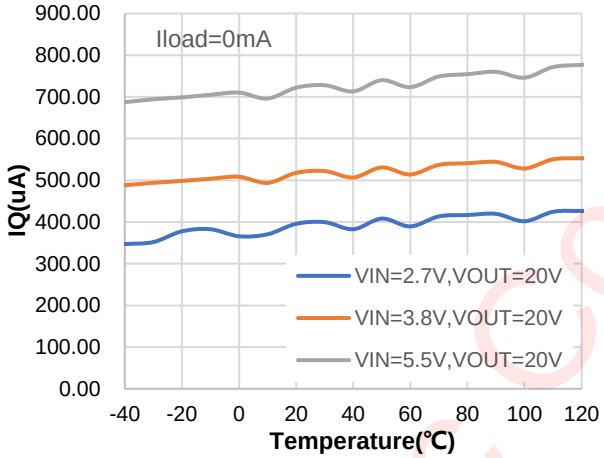


Figure 8 IQ vs Temperature

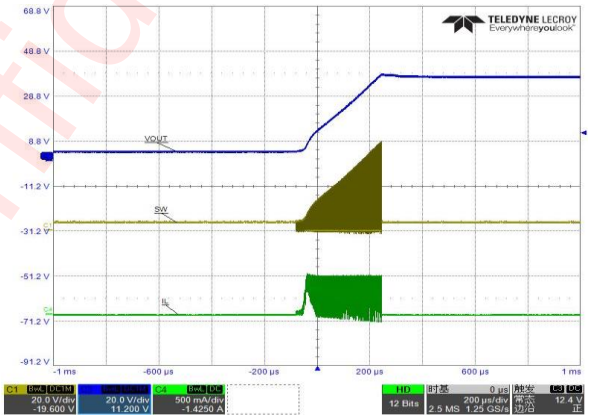


Figure 9 Open FB Protection

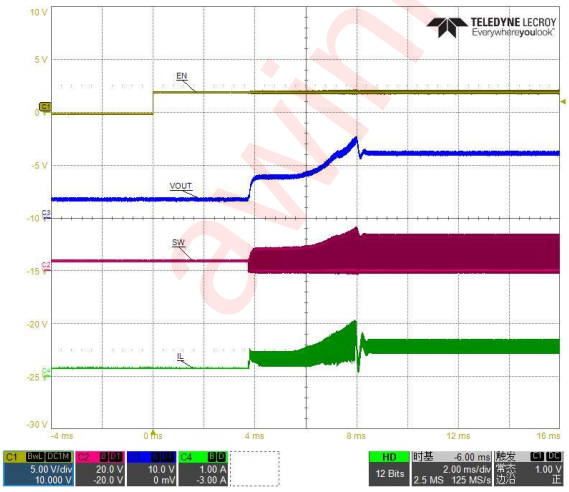


Figure 10 VIN=3.8V,VOUT=12V
Iload=150mA;Start Waveform

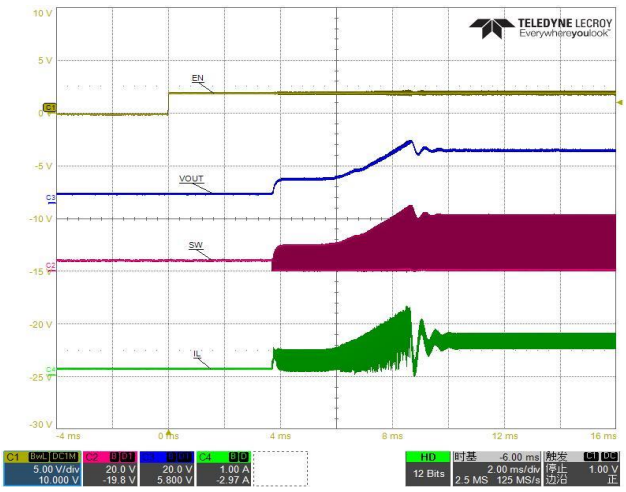


Figure 11 VIN=3.8V,VOUT=20V
Iload=100mA;Start Waveform

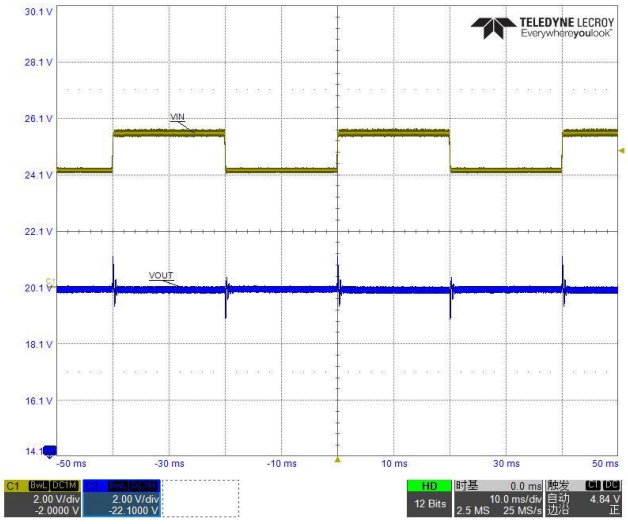


Figure 12 Line Transient Response

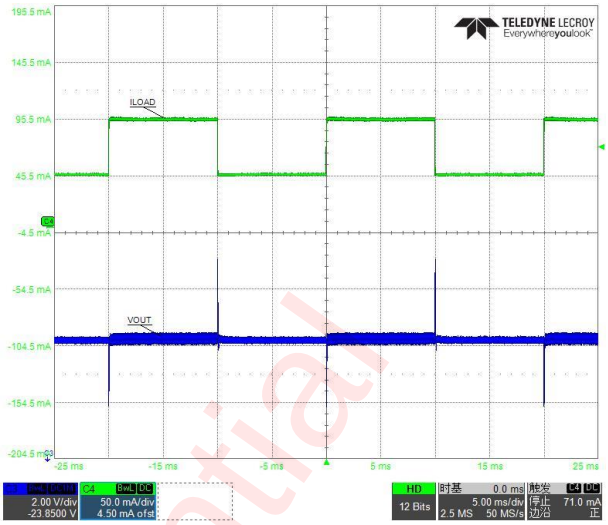


Figure 13 Load Transient Response

Detailed Functional Description

The AW36201 is a high efficiency boost converter, which operates in pulse width modulation (PWM) mode with 1.1MHz constant switching frequency and integrates 2A/40V switch FET. The duty cycle of boost regulator is set by the error amplifier output and the inductor current signal applied to the PWM comparator. When duty cycle exceeds 50%, slope compensation is added to the current signal for current loop stableness .

Soft Start

When the device is enabled, the error amplifier output ramps up to the target voltage in a specific time. This ensures that the output voltage rises slowly to reduce the input inrush current.

Over-Voltage Protection

The over-voltage protection function monitors the output voltage via the SW pin voltage. The OVP threshold voltage is 38V typically. Once the FB is open, the output voltage reaches the OVP threshold, the converter will be shut down. During detect process, output voltage will keep stepping up for 8 clock cycles.

Shutdown

The EN pin is used for enable device. When the EN voltage is logic low for more than 2.5ms, the converter will be shut down.

Under-Voltage Lockout

When the input voltage is lower than the UVLO threshold (2.2V typ.), the converter will turn off. If the input voltage rises by under-voltage lockout hysteresis, the converter restarts.

Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature exceed 165°C. The device will restart when the junction temperature decreases by 15°C.

Application Information

Inductor Selection

Because the selection of inductor affects power supply's steady state operation, transient behavior, loop stability and the boost converter efficiency, the inductor is one of the most important components in switching power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current.

The inductor DC current can be calculated as:

$$I_{IN\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (1)$$

The inductor current peak to peak ripple can be calculated as

$$I_{PP=} \frac{1}{L \times F_S \times (\frac{1}{V_{OUT} + V_F - V_{IN}} + \frac{1}{V_{IN}})} \quad (2)$$

The F_S is the operating frequency，the V_F is the schottky diode's forward voltage.

Therefore, the peak current I_P seen by the inductor is calculated as

$$I_P = I_{IN\_DC} + \frac{I_{PP}}{2} \quad (3)$$

The inductor saturation current rating should be considered to cover the inductor peak current. Smaller size and better efficiency are the major concerns for portable devices. The inductor should have low core loss at 1100kHz and low DCR for better efficiency. For these reasons, a 4.7μH to 10μH inductor value range is recommended. A 10μH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. **Table 1** lists the recommended inductor for the AW36201. When recommending inductor value, the factory has considered –40% and +20% tolerance from its nominal value.

Table1 Recommended Inductors for AW36201

Part Number	L (μH)	DCR Max (Ω)	Saturation Current (mA)	Size (L x W x H mm)	Vendor
MRSC252A10-100M-N	10	0.5	900	2.5 x 2 x 1	Chilisin
LQH3NPN100NM0	10	0.3	750	3 x 3 x 1.5	Murata
CDH3809/SLD	10	0.3	570	4 x 4 x 1.0	Sumida
LPS4018-472ML	4.7	0.125	1900	4 x 4 x 1.8	Coilcraft

Schottky Diode Selection

To optimize the efficiency, a high-speed and low reverse-recovery current Schottky diode are recommended. Make sure the diode's average and peak current ratings exceed the output average current and the peak inductor current. In addition, the diode's break-down voltage rating must exceed the maximum voltage across the diode. Usually, unexpected high-frequency voltage spikes can be seen across the diode when the diode turns off. Therefore, leaving some voltage rating margin is always needed to guarantee normal long-term operation when selecting a diode. The MBR0540 and the NSR05F40 are recommended for AW36201.

Input and Output Capacitors Selection

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming ESR of a capacitor is zero, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}} \quad (4)$$

Where, V_{ripple} represents peak-to-peak output ripple. The additional output ripple caused by ESR can be calculated as:

$$V_{ripple\_ESR} = I_{OUT} \times R_{ESR} \quad (5)$$

V_{ripple_ESR} can be neglected for ceramic capacitors due to its low ESR, but must be considered if tantalum or electrolytic capacitors are used.

Note that the ceramic capacitance is dependent on the voltage rating. With a DC bias voltage, the capacitance can lose as much as 50% of its value at its rated voltage rating. Leave a large enough voltage rating margin when selecting the component. Therefore, leave enough margin on the voltage rating to ensure adequate capacitance at the required output voltage.

An X5R or X7R capacitor of 10μF is recommended for input side. The output requires a X5R or X7R capacitor in the range of 0.47μF to 4.7μF. A 100nF capacitor and a 33 pF capacitor are recommended to use in parallel with the input capacitor and the output capacitor to suppress high frequency noise.

The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

Output Voltage Setting

The output voltage is set through the voltage divider R1 and R2:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (6)$$

Larger value of R1 and R2 can reduce the power loss and improve the efficiency. We suggest 1kΩ≤R2≤10kΩ and R1≤1.4MΩ. Smaller value of R2 could reduce the noise sensitivity of FB pin.

Feedforward Capacitor

A feedforward capacitor C_{ff} connected from the VOUT to the FB pin of the chip can enhance the transient response capability. The feedforward capacitor can improve the loop stability of boost circuit. It can improve the load transient response of the loop.

When the feedforward capacitor is connected to the feedback network of the circuit, a low frequency zero point f_z will be added. C_{ff} can be calculated according to R1 and f_z:

$$C_{ff} = \frac{1}{2\pi \times R1 \times f_z} \quad (7)$$

For AW36201, we recommend to set f_z at 30kHz.

The high frequency noise from VOUT will affect the voltage of FB pin by the path of feedforward capacitor. So it is necessary to connect a 1kΩ resistor in series on the path of the feedforward capacitor to reduce the impact on the voltage of FB pin caused by the high frequency noise.

Power Dissipation

The maximum IC junction temperature should not be exceed 125°C under normal operating conditions. This restriction limits the power dissipation of the AW36201. It is recommended to keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined by using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{\theta_{ja}} \quad (8)$$

Where, T_{Jmax} is the Maximum Junction Temperature, T_A is the maximum ambient temperature for the application. θ_{ja} is the thermal resistance junction-to-ambient given in Power Dissipation Table.

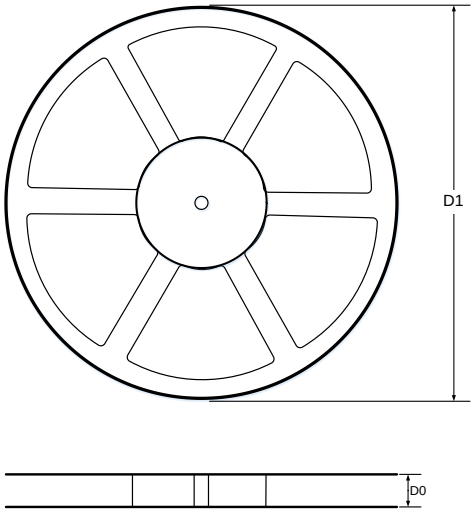
PCB Layout Consideration

PCB layout is an important design step for those high frequency, high current switching power regulators in order to minimize noise and keep loop stable. To reduce switching losses, it is better to make the SW pin rise and fall times as short as possible. Minimizing the length and area of all traces connected to the SW pin and using a ground plane under the switching regulator are strongly recommended to minimize inter-plane coupling. The input capacitor should be very close to the IC to get the best decoupling. The path of the inductor, schottky diode and output capacitor should be kept as short as possible to minimize noise and ringing. FB is a sensitive node and it should be kept separate from the SW pin in the PCB layout.

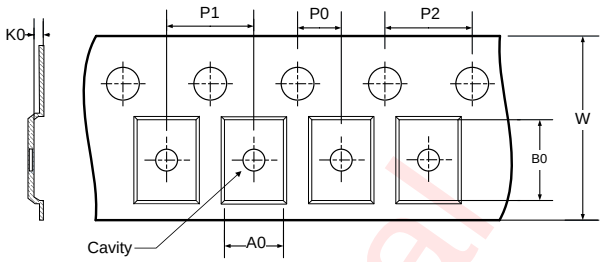
Connect the exposed paddle to the PCB ground plane using at least two vias. The input and the output bypass capacitors should be placed as close to the IC as possible. Minimize trace lengths between the IC and the inductor, the diode and the output capacitor; keep these traces short, direct, and wide.

Tape and Reel Information

REEL DIMENSIONS

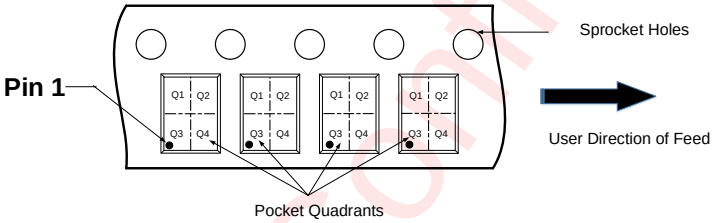


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



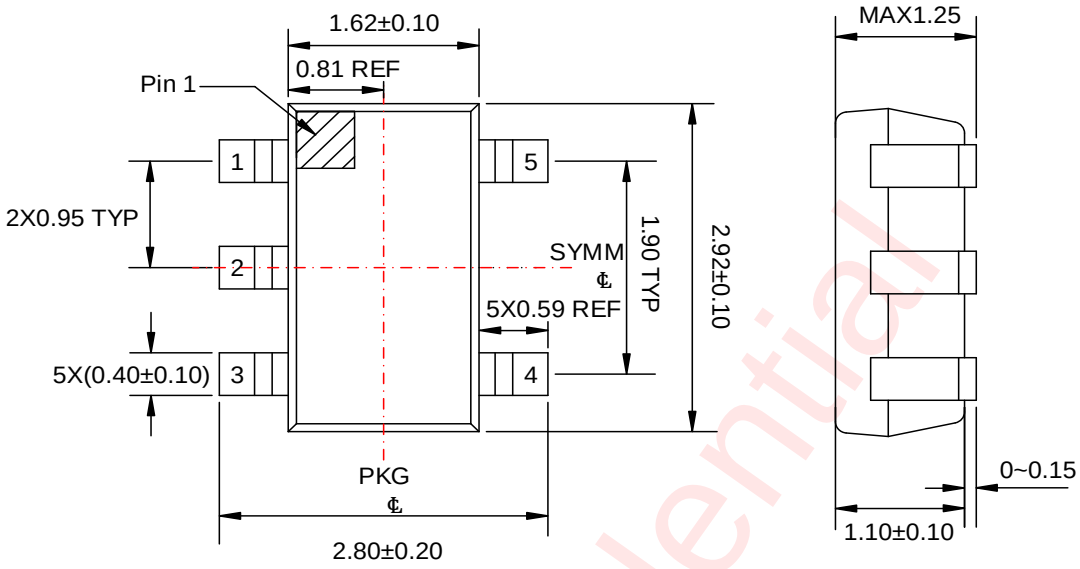
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

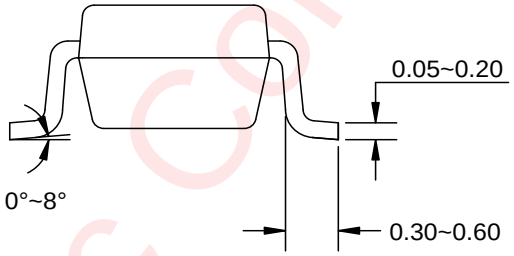
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	3.3	3.2	1.4	2	4	4	8	Q3

All dimensions are nominal

Package Description



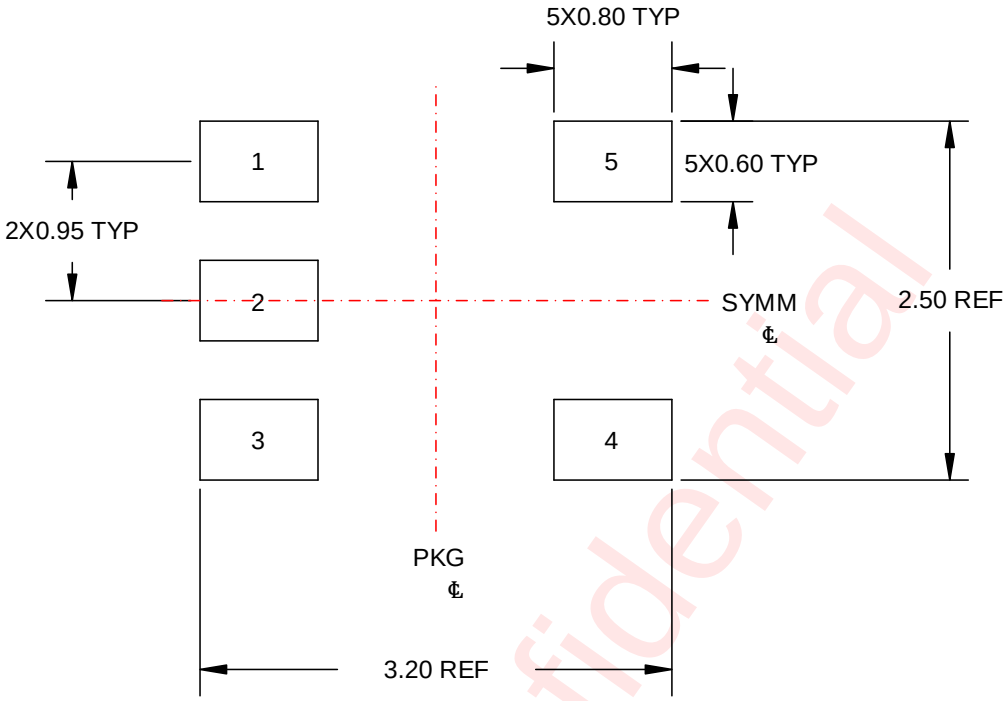
Top View **Side View**

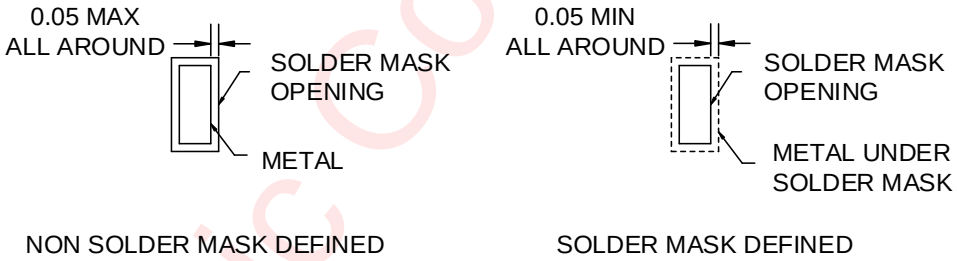


Side View

Unit: mm

Land Pattern Data





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Reversion History

Version	Date	Change Record
V1.0	Jun. 2022	Datasheet V1.0 Released
V1.1	Jan. 2023	Add the range of R1&R2 in Recommended Operating Conditions (page 5); Add Output Voltage and Feedforward Capacitor in Application Information in (page 11).

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