钍地半导体
Tudi Semiconductor

Product Specification

TUDI-MAX13442E/13443E/ 13444E

±15kV ESD-Protected, ±80V Fault-Protected, Fail-Safe RS-485/J1708 Transceivers

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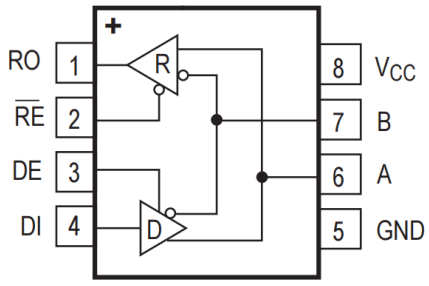
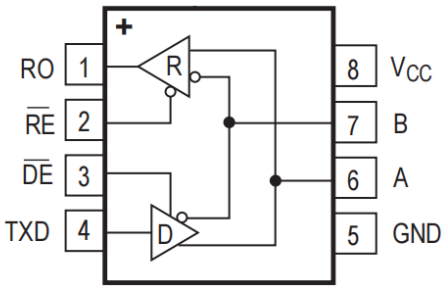
- Design
- research and development
- production
- and sales

Features

- ±15kV ESD Protection
- ±80V Fault Protection (±60V MAX13443E)
- Guaranteed 10Mbps Data Rate (MAX13443E)
- Hot-Swappable for Telecom Applications
- True Fail-Safe Receiver Inputs
- Enhanced Slew-Rate-Limiting Facilitates Error-Free Data Transmission (MAX13442E/MAX13444E)
- Allow Up to 128 Transceivers on the Bus
- -7V to +12V Common-Mode Input Range
- ±6mA FoldBack Current Limit
- Industry-Standard Pinout



MAX13442E MAX13443E



MAX13444E

Applications

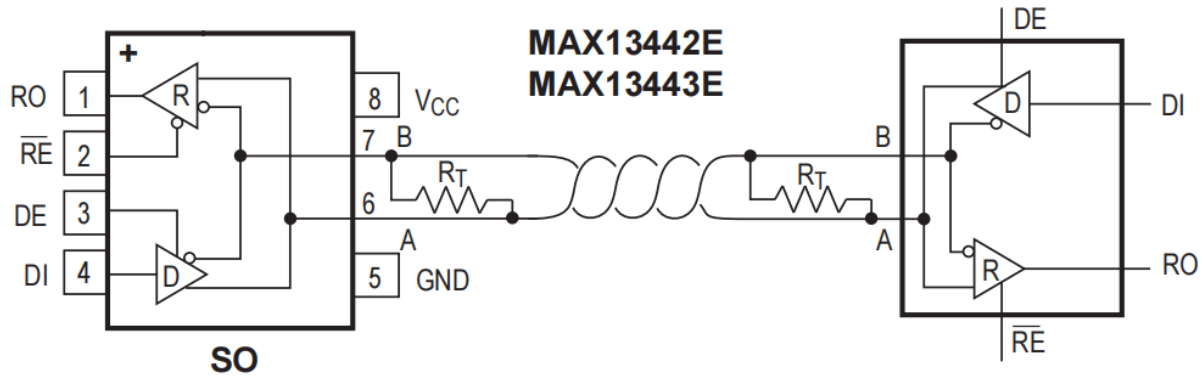
- RS-422/RS-485 Communications
- Truck and Trailer Applications
- Industrial Networks
- Telecommunications Systems
- Automotive Applications
- HVAC Controls

General Description

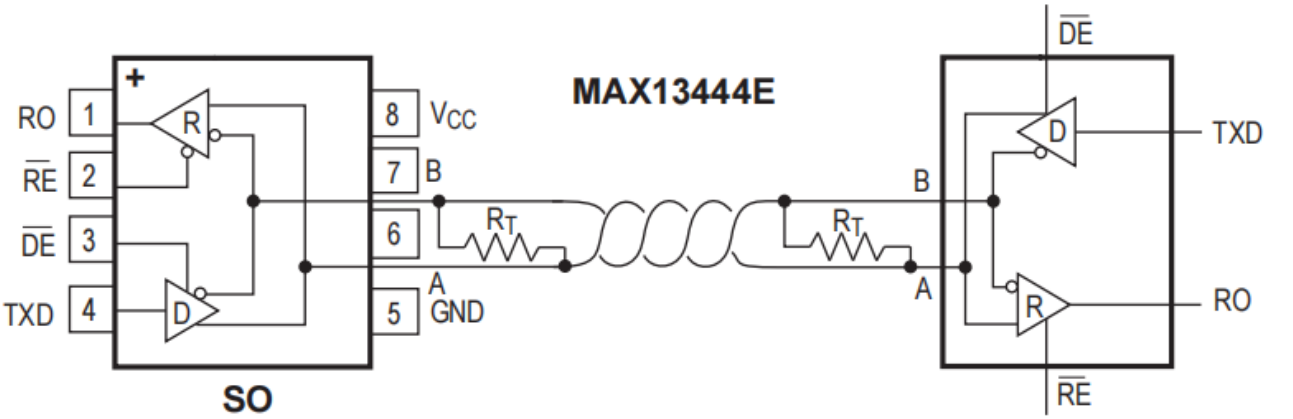
The MAX13442E/MAX13444E are fault-protected RS-485 and J1708 transceivers that feature ±80V protection from signal faults on communication bus lines. The MAX13442E/MAX13444E feature a reduced slew-rate driver that minimizes EMI and reflections, allowing error-free transmission up to 250kbps. The MAX13443E driver can transmit up to 10Mbps. The high-speed MAX13443E RS-485 transceiver features ±60V protection from signal faults on communication bus lines. These transceivers feature foldback current limit. Each device contains one differential line driver with three-state output and one dif-ferential line receiver with three-state input. The 1/4-unit-load receiver input impedance allows up to 128 transceiv-ers on a single bus. The devices operate from a 5V sup-ply. True fail-safe inputs guarantee a logic-high receiver output when the receiver inputs are open, shorted, or connected to an idle data line.

Hot-swap circuitry eliminates false transitions on the data bus during circuit initialization or connection to a live back-plane. Short-circuit current-limiting and thermal-shutdown circuitry protect the driver against excessive power dis-sipation, and on-chip ±15kV ESD protection elimina tes costly external protection devices.

The MAX13442E/MAX13443E/MAX13444E are available in an 8-pin SO package and are specified over the auto-motive temperature range.



Pin Configurations and Typical Operating Circuits continued at end of data sheet.



Absolute Maximum Ratings

(Voltages referenced to GND.)

V_{CC} ..... +7V
RE, DE, DE, DI, TXD ..... -0.3V to (V_{CC} + 0.3V)
A, B (Note 1) (MAX13442E/MAX13444E) ..... ±80V
A, B (Note 1) (MAX13443E) ..... ±60V
RO ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration (RO, A, B) ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
SO (derate 7.6mW/°C above +70°C) 606mW
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: During normal operation, a termination resistor must be connected between A and B in order to guarantee overvoltage protection up to the absolute maximum rating of this device. When not in operation, these devices can withstand fault voltages up to the maximum rating without a termination resistor and will not be damaged.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

SO

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 132°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 38°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations

DC Electrical Characteristics

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Differential Driver Output	V_{OD}	Figure 1, R_L = 100Ω	2		V_{CC}	V
		Figure 1, R_L = 54Ω	1.5		V_{CC}	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	Figure 1, R_L = 100Ω or 54Ω (Note 3)			0.2	V
Driver Common-Mode Output Voltage	V_{OC}	Figure 1, R_L = 100Ω or 54Ω		$V_{CC}/2$	3	V
Change in Magnitude of Common-Mode Voltage	DV_{OC}	Figure 1, R_L = 100Ω or 54Ω (Note 3) (MAX13442E/MAX13443E)			0.2	V
DRIVER LOGIC						
Driver-Input High Voltage	V_{DIH}		2			V
Driver-Input Low Voltage	V_{DIL}				0.8	V
Driver-Input Current	I_{DIN}				±2	µA
Driver Short-Circuit Output Current (Note 4)	I_{OSD}	0V ≤ V_{OUT} ≤ +12V			+350	mA
		-7V ≤ V_{OUT} ≤ V_{CC}	-350			
Driver Short-Circuit Foldback Output Current	I_{OSDF}	(V_{CC} - 1V) ≤ V_{OUT} ≤ +12V (Note 4)	+25			mA
		-7V ≤ V_{OUT} ≤ +1V (Note 4)			-25	
Driver-Limit Short-Circuit Foldback Output Current	I_{OSDL}	V_{OUT} ≥ +20V, R_L = 100Ω	+6			mA
		V_{OUT} ≤ -15V, R_L = 100Ω			-6	

DC Electrical Characteristics (continued)

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER							
Input Current	$I_{A,B}$	A, B receive mode	V_{CC} = GND, $V_{A, B}$ = 12V			250	µA
			$V_{A, B}$ = -7V			-150	
			$V_{A, B}$ = ±80V			±6	mA
Receiver-Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V		-200		-50	mV
Receiver-Input Hysteresis	ΔV_{TH}				25		mV
RECEIVER LOGIC							
Output-High Voltage	V_{OH}	Figure 2, I_{OH} = -1.6mA		V_{CC} - 0.6			V
Output-Low Voltage	V_{OL}	Figure 2, I_{OL} = 1mA				0.4	V
Three-State Output Current at Receiver	I_{OZR}	0V ≤ $V_{A, B}$ ≤ V_{CC}				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V		48			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	0V ≤ V_{RO} ≤ V_{CC}				±95	mA
CONTROL							
Control-Input High Voltage	V_{CIH}	DE, $\overline{DE}$, $\overline{RE}$		2			V
Input-Current Latch During First Rising Edge	I_{IN}	DE, $\overline{RE}$			90		µA
SUPPLY CURRENT							
Normal Operation	I_{CC}	No load, DI = V_{CC} or GND	DE = V_{CC}, $\overline{RE}$ = GND (MAX13442E) ($\overline{DE}$ = $\overline{RE}$ = GND) (MAX13444E)			30	mA
			(DE = V_{CC}, $\overline{RE}$ = GND) (MAX13443E)			10	
Supply Current in Shutdown Mode	I_{SHDN}	DE = GND, $\overline{RE}$ = V_{CC} (MAX13442E/MAX13443E)				20	µA
		DE = GND, $\overline{RE}$ = V_{CC}, T_A = +25°C (MAX13442E/MAX13443E)				10	
		$\overline{DE}$ = $\overline{RE}$ = V_{CC} (MAX13444E)				100	
		$\overline{DE}$ = $\overline{RE}$ = V_{CC}, T_A = +25°C (MAX13444E)				10	
Supply Current with Output Shorted to ±60V	I_{SHRT}	DE = GND, $\overline{RE}$ = GND, no load output in three-state (MAX13443E)				±15	mA

Protection Specifications

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Overvoltage Protection		A, B; R_{SOURCE} = 0Ω, R_L = 54Ω	MAX13442E/ MAX13444E	±80			V
			MAX13443E	±60			
ESD Protection		A, B	Human Body Model		±15		kV

Switching Characteristics (MAX13442E/MAX13444E)

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{PLHA}, t_{PLHB}	Figure 3, R_L = 54Ω, C_L = 50pF (MAX13442E) R_{DIFF} = 60Ω, C_{DIFF} = 100pF (MAX13444E)			2000	ns
Driver Differential Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 4			2000	ns
Driver Differential Output Transition Time	t_{LH},t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 4	200		2000	ns
Driver Output Skew	t_{SKEWAB}, t_{SKEWBA}	R_L = 54Ω, C_L = 50pF, t_{SKEWAB} = $\lvert t_{PLHA} - t_{PHLB} \rvert$, t_{SKEWBA} = $\lvert t_{PLHB} - t_{PHLA} \rvert$			350	ns
Differential Driver Output Skew	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, t_{DSKEW} = $\lvert t_{DPLH} - t_{DPHL} \rvert$			200	ns
Maximum Data Rate	f_{MAX}		250			kbps
Driver Enable Time to Output High	t_{PDZH}	R_L = 500Ω, C_L = 50pF, Figure 5			2000	ns
Driver Disable Time from Output High	t_{PDHZ}	R_L = 500Ω, C_L = 50pF, Figure 5			2000	ns
Driver Enable Time from Shutdown to Output High	t_{PDHS}	R_L = 500Ω, C_L = 50pF, Figure 5			4.2	µs
Driver Enable Time to Output Low	t_{PDZL}	R_L = 500Ω, C_L = 50pF, Figure 6			2000	ns
Driver Disable Time from Output Low	t_{PDLZ}	R_L = 500Ω, C_L = 50pF, Figure 6			2000	ns
Driver Enable Time from Shutdown to Output Low	t_{PDLS}	R_L = 500Ω, C_L = 50pF, Figure 6			4.2	µs
Driver Time to Shutdown	t_{SHDN}	R_L = 500Ω, C_L = 50pF			800	ns
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 20pF, V_{ID} = 2V, V_{CM} = 0V, Figure 7			2000	ns
Receiver Output Skew	t_{RSKEW}	C_L = 20pF, t_{RSKEW} = $\lvert t_{RPLH} - t_{RPHL} \rvert$			200	ns
Receiver Enable Time to Output High	t_{RPZH}	R_L = 1kΩ, C_L = 20pF, Figure 8			2000	ns
Receiver Disable Time from Output High	t_{RPHZ}	R_L = 1kΩ, C_L = 20pF, Figure 8			2000	ns
Receiver Wake Time from Shutdown	t_{RPWAKE}	R_L = 1kΩ, C_L = 20pF, Figure 8			4.2	µs
Receiver Enable Time to Output Low	t_{RPZL}	R_L = 1kΩ, C_L = 20pF, Figure 8			2000	ns
Receiver Disable Time from Output Low	t_{RPLZ}	R_L = 1kΩ, C_L = 20pF, Figure 8			2000	ns
Receiver Time to Shutdown	t_{SHDN}	R_L = 500Ω, C_L = 50pF			800	ns

Switching Characteristics (MAX13443E)

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{PLHA}, t_{PLHB}	R_L = 27Ω, C_L = 50pF, Figure 3			60	ns
Driver Differential Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 4			60	ns
Driver Differential Output Transition Time	t_{LH},t_{HL}	R_L = 54Ω, CL = 50pF, Figure 4			25	ns
Driver Output Skew	t_{SKEWAB}, t_{SKEWBA}	R_L = 54Ω, C_L = 50pF, t_{SKEWAB} = $\|t_{PLHA} - t_{PHLB}\|$, t_{SKEWBA} = $\|t_{PLHB} - t_{PHLA}\|$			10	ns
Differential Driver Output Skew	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, t_{DSKEW} = $\|t_{DPLH} - t_{DPHL}\|$			10	ns
Maximum Data Rate	f_{MAX}		10			Mbps
Driver Enable Time to Output High	t_{PDZH}	R_L = 500Ω, C_L = 50pF, Figure 5			1200	ns
Driver Disable Time from Output High	t_{PDHZ}	R_L = 500Ω, C_L = 50pF, Figure 5			1200	ns
Driver Enable Time from Shutdown to Output High	t_{PDHS}	R_L = 500Ω, C_L = 50pF, Figure 5			4.2	µs
Driver Enable Time to Output Low	t_{PDZL}	R_L = 500Ω, C_L = 50pF, Figure 6			1200	ns
Driver Disable Time from Output Low	t_{PDLZ}	R_L = 500Ω, C_L = 50pF, Figure 6			1200	ns
Driver Enable Time from Shutdown to Output Low	t_{PDLS}	R_L = 500Ω, C_L = 50pF, Figure 6			4.2	Fs
Driver Time to Shutdown	t_{SHDN}	R_L = 500Ω, C_L = 50pF, Figure 6			800	ns
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 20pF, V_{ID} = 2V, V_{CM} = 0V, Figure 7			85	ns
Receiver Output Skew	t_{RSKEW}	C_L = 20pF, t_{RSKEW} = $\|t_{RPLH} - t_{RPHL}\|$			15	ns
Receiver Enable Time to Output High	t_{RPZH}	R_L = 1kΩ, C_L = 20pF, Figure 8			400	ns
Receiver Disable Time from Output High	t_{RPHZ}	R_L = 1kΩ, C_L = 20pF, Figure 8			400	ns
Receiver Wake Time from Shutdown	t_{RPWAKE}	R_L = 1kΩ, C_L = 20pF, Figure 8			4.2	µs
Receiver Enable Wake Time from Shutdown	t_{RPSH}	R_L = 1kΩ, C_L = 20pF, Figure 8			400	ns
Receiver Disable Time from Output Low	t_{RPLZ}	R_L = 1kΩ, C_L = 20pF, Figure 8			400	ns
Receiver Time to Shutdown	t_{SHDN}	R_L = 500Ω, C_L = 50pF			800	ns

Note 3: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 4: The short-circuit output current applies to peak current just before foldback current limiting. The short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

Test Circuits and Waveforms

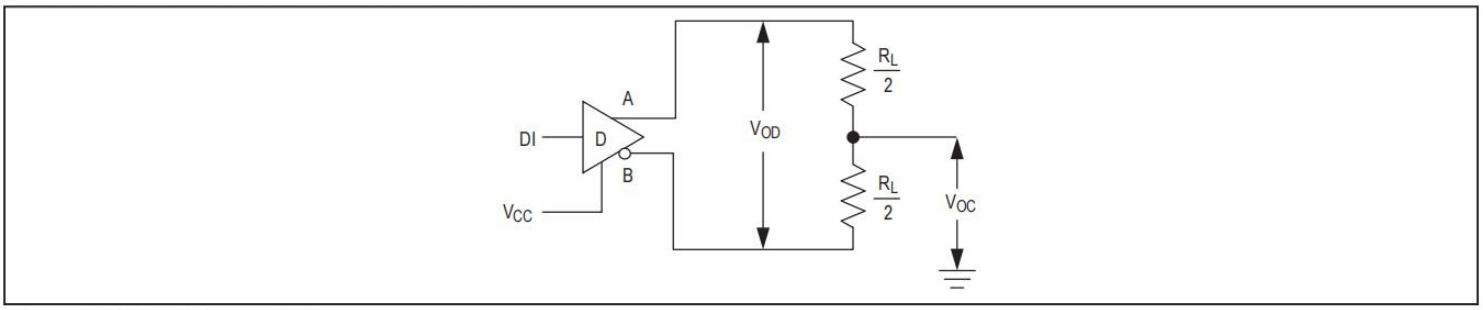


Figure 1. Driver V_{OD} and V_{OC}

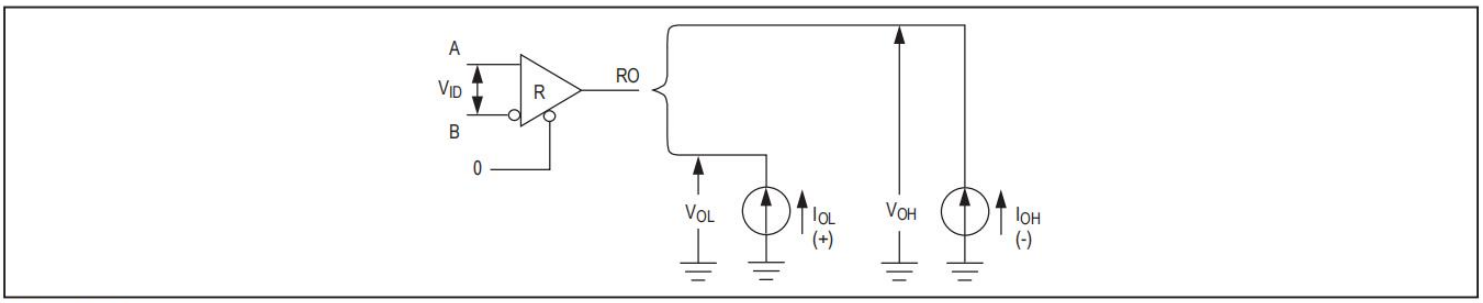


Figure 2. Receiver V_{OH} and V_{OL}

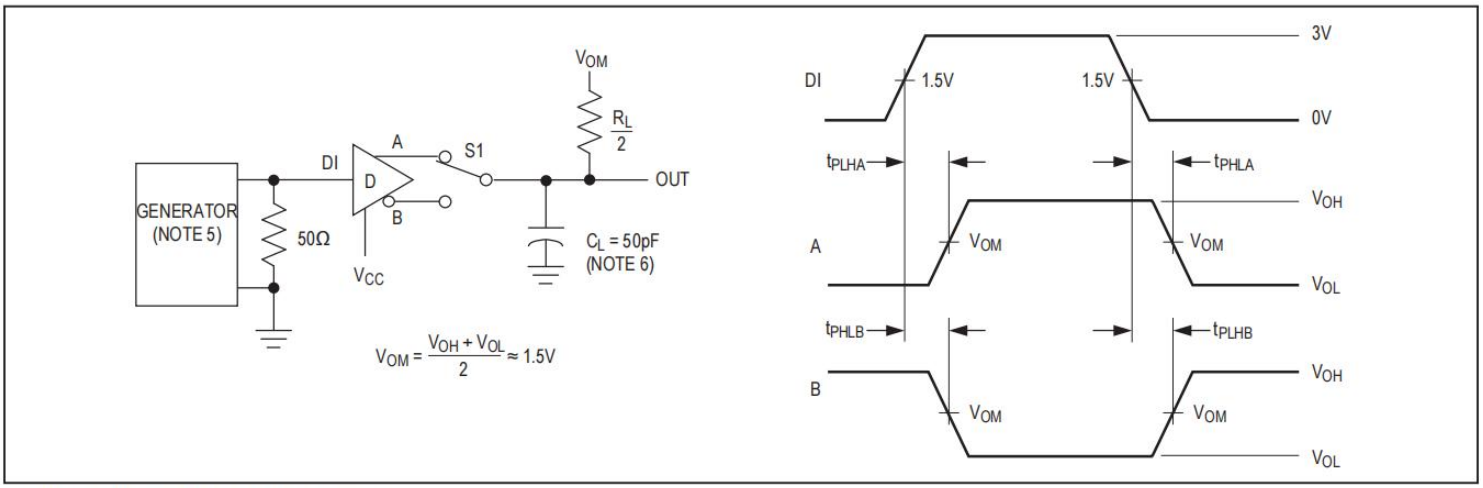


Figure 3. Driver Propagation Times

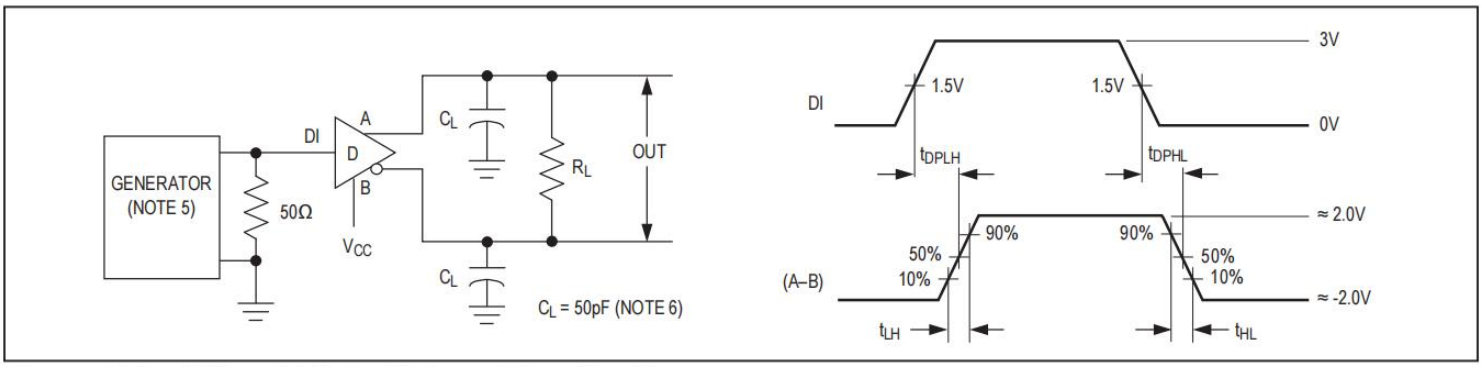


Figure 4. Driver Differential Output Delay and Transition Times

Test Circuits and Waveforms (continued)

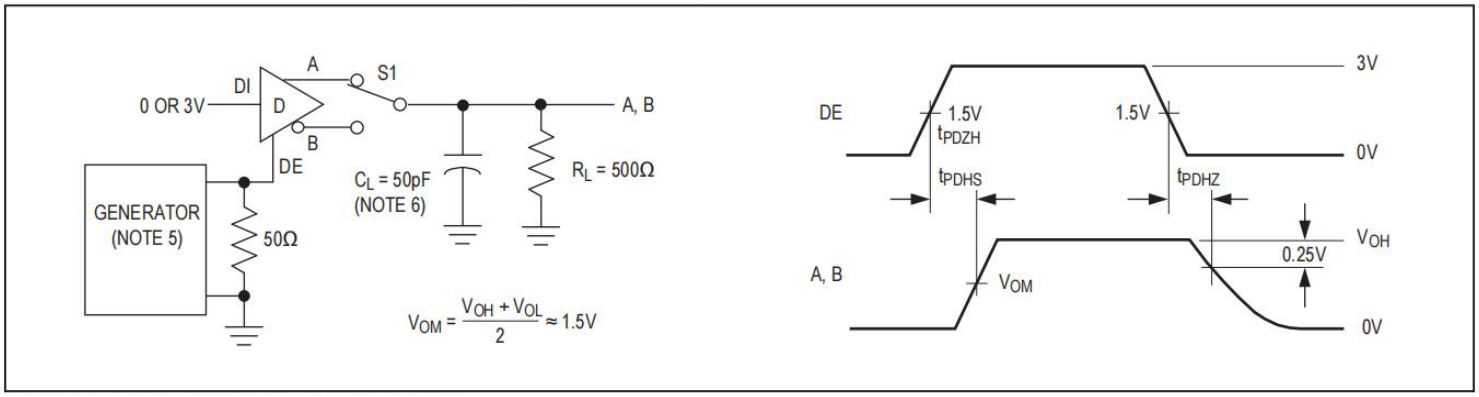


Figure 5. Driver Enable and Disable Times

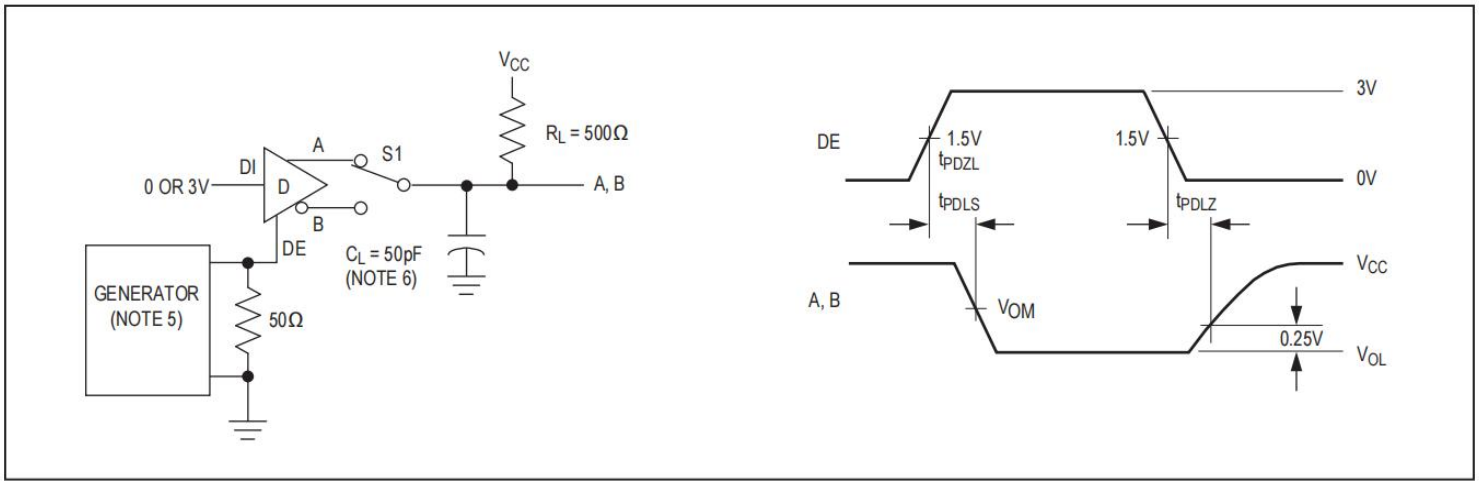


Figure 6. Driver Enable and Disable Times

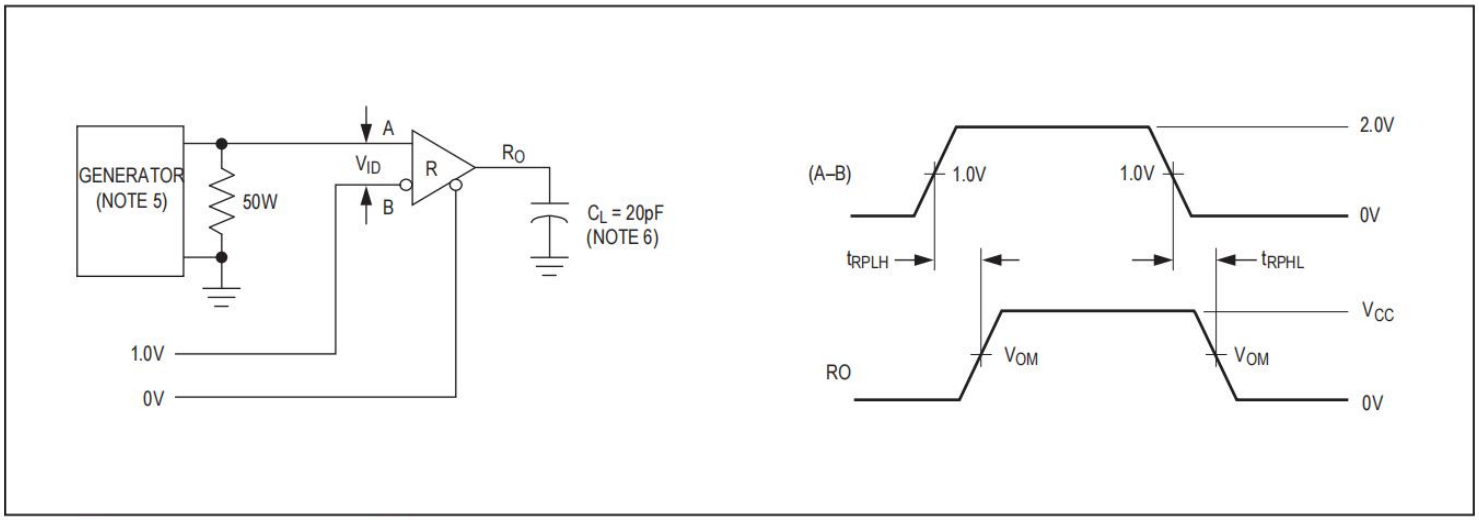


Figure 7. Receiver Propagation Delay

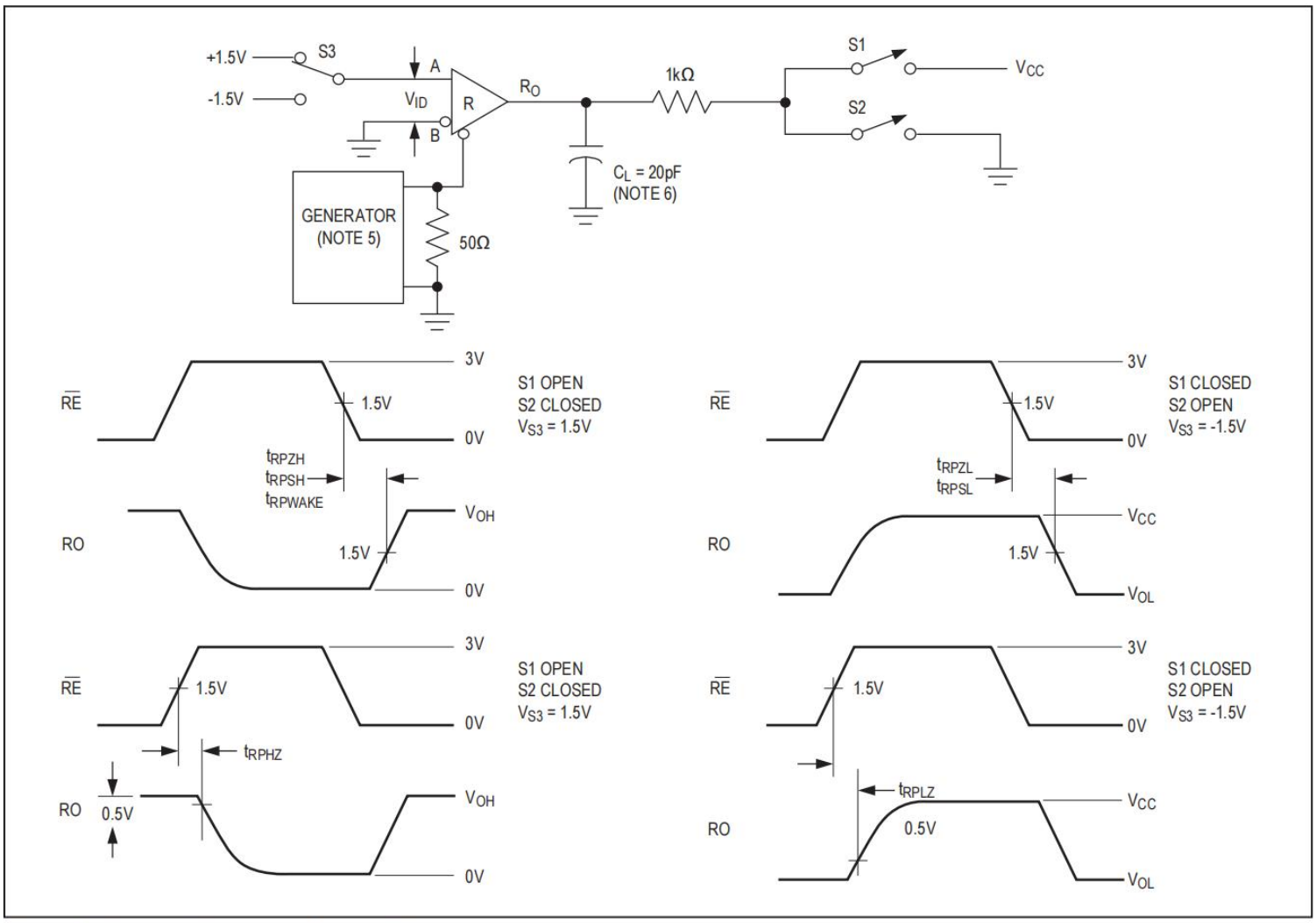


Figure 8. Receiver Enable and Disable Times

Note 5: The input pulse is supplied by a generator with the following characteristics: f = 5MHz, 50% duty cycle; t_r ≤ 6ns; Z_0 = 50Ω.
Note 6: C_L includes probe and stray capacitance.

Pin Description

PIN		NAME	FUNCTION
MAX13442E MAX13443E	MAX13444E		
1	1	RO	Receiver Output. If the receiver is enabled and (V_A- V_B) ≥ -50mV, RO = high; if (V_A - V_B) ≤ -200mV, RO = low.
2	2	$\overline{RE}$	Receiver Output Enable. Pull $\overline{RE}$ low to enable RO.
3	—	DE	Driver Output Enable. Force DE high to enable driver. Pull DE low to three-state the driver output. Drive $\overline{RE}$ high and pull DE low to enter low-power shutdown mode.
4	—	DI	Driver Input. A logic-low on DI forces the noninverting output low and the inverting output high. A logic-high on DI forces the noninverting output high and the inverting output low.
5	5	GND	Ground
6	6	A	Noninverting Receiver Input/Driver Output
7	7	B	Inverting Receiver Input/Driver Output
8	8	V_{CC}	Positive Supply, V_{CC} = +4.75V to +5.25V. For normal operation, bypass V_{CC} to GND with a 0.1µF ceramic capacitor. For full ESD protection, bypass V_{CC} to GND with 1µF ceramic capacitor.
—	3	$\overline{DE}$	Driver Output Enable. Pull $\overline{DE}$ low to enable the outputs. Force $\overline{DE}$ high to three-state the outputs. Drive $\overline{RE}$ and $\overline{DE}$ high to enter low-power shutdown mode.
—	4	TXD	J1708 Input. A logic-low on TXD forces outputs A and B to the dominant state. A logic-high on TXD forces outputs A and B to the recessive state.

Function Tables

Table 1. MAX13442E/MAX13443E (RS-485/RS-422)

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	A	B
0	0	X	High-Z	High-Z
0	1	0	0	1
0	1	1	1	0
1	0	X	Shutdown	Shutdown
1	1	0	0	1
1	1	1	1	0

X = Don't care.

Table 2. MAX13444E (J1708) Application

TRANSMITTING				
INPUTS		OUTPUTS		CONDITIONS
TXD	$\overline{DE}$	A	B	—
0	1	High-Z	High-Z	—
1	1	High-Z	High-Z	—
0	0	0	1	Dominant state
1	0	High-Z	High-Z	Recessive state

Table 3. MAX13442E/MAX13443E (RS-485/RS-422)

RECEIVING			
INPUTS			OUTPUTS
$\overline{RE}$	DE	$(V_A - V_B)$	RO
0	X	≥-0.05V	1
0	X	≤-0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

X = Don't care.

Table 4. MAX13444E (RS-485/RS-422)

RECEIVING			
INPUTS			OUTPUTS
$\overline{RE}$	$\overline{DE}$	$(V_A - V_B)$	RO
0	X	≥-0.05V	1
0	X	≤-0.2V	0
0	X	Open/shorted	1
1	0	X	High-Z
1	1	X	Shutdown

X = Don't care.

Detailed Description

The MAX13442E/MAX13443E/MAX13444E fault-protected transceivers for RS-485/RS-422 and J1708 communication contain one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the *True Fail-Safe* section). All devices have a hot-swap input structure that prevents disturbances on the differential signal lines when a circuit board is plugged into a hot backplane (see the *Hot-Swap Capability* section). The MAX13442E/MAX13444E feature a reduced slew-rate driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps (see the *Reduced EMI and Reflections* section). The MAX13443E driver is not slew-rate limited, allowing transmit speeds up to 10Mbps.

Driver

The driver accepts a single-ended, logic-level input (DI) and transfers it to a differential, RS-485/RS-422 level output (A and B). Deasserting the driver enable places the driver outputs (A and B) into a high-impedance state.

Receiver

The receiver accepts a differential, RS-485/RS-422 level input (A and B), and transfers it to a single-ended logic-level output (RO). Deasserting the receiver enable places the receiver inputs (A and B) into a high-impedance state (see Table 1–Table 4).

Low-Power Shutdown

The MAX13442E/MAX13443E/MAX13444E offer a low-power shutdown mode. Force DE low and $\overline{RE}$ high to shut down the MAX13442E/MAX13443E. Force DE and $\overline{RE}$ high to shut down the MAX13444E. A time delay of 50ns prevents the device from accidentally entering shutdown due to logic skews when switching between transmit and receive modes. Holding DE low and $\overline{RE}$ high for at least 800ns guarantees that the MAX13442E/MAX13443E enter shutdown. In shutdown, the devices consume a maximum 20µA supply current.

±80V Fault Protection

The driver outputs/receiver inputs of RS-485 devices in industrial network applications often experience voltage faults resulting from shorts to the power grid that exceed the -7V to +12V range specified in the EIA/TIA-485 standard. In these applications, ordinary RS-485 devices (typical absolute maximum -8V to +12.5V) require costly external protection devices. To reduce system complexity and eliminate this need for external protection, the driver outputs/receiver inputs of the MAX13442E/MAX13444E withstand voltage faults up to ±80V (±60V for the MAX13443E) with respect to ground without damage. Protection is guaranteed regardless whether the device is active, shut down, or without power.

True Fail-Safe

The MAX13442E/MAX13443E/MAX13444E use a -50mV to -200mV differential input threshold to ensure true fail-safe receiver inputs. This threshold guarantees the receiver outputs a logic-high for shorted, open, or idle data lines. The -50mV to -200mV threshold complies with the ±200mV threshold EIA/TIA-485 standard.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. The MAX13442E/MAX13443E/MAX13444E receiver inputs/driver outputs (A, B) have extra protection against static electricity found in normal operation. Maxim's engineers have developed state-of-the-art structures to protect these pins against ±15kV ESD without damage. After an ESD event, the MAX13442E/MAX13443E/MAX13444E continue working without latchup.

ESD protection can be tested in several ways. The receiver inputs are characterized for protection to ±15kV using the Human Body Model.

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 9a shows the Human Body Model, and Figure 9b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus contention. The first, a foldback current limit on the driver output stage, provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C. Normal operation resumes when the die temperature cools to +140°C, resulting in a pulsed output during continuous short-circuit conditions.

Hot-Swap Capability

Hot-Swap Inputs

Inserting circuit boards into a hot, or powered, backplane may cause voltage transients on DE, $\overline{RE}$, and receiver inputs A and B that can lead to data errors. For example, upon initial circuit board insertion, the processor undergoes a power-up sequence. During this period, the high-impedance state of the output drivers makes them unable to drive the MAX13442E/MAX13443E/MAX13444E enable inputs to a defined logic level. Meanwhile, leakage currents of up to 10µA from the high-impedance output, or capacitively coupled noise from V_{CC} or GND, could cause an input to drift to an incorrect logic state. To prevent such a condition from occurring, the MAX13442E/MAX13443E/MAX13444E feature hot-swap input circuitry on DE, and $\overline{RE}$ to guard against unwanted driver activation during hot-swap situations. The MAX13444E has hot-swap input circuitry only on $\overline{RE}$. When V_{CC} rises, an internal pulldown (or pullup for $\overline{RE}$) circuit holds DE low for at least 10µs, and until the current into DE exceeds 200µA. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Hot-Swap Input Circuitry

At the driver-enable input (DE), there are two NMOS devices, M1 and M2 (Figure 10). When V_{CC} ramps from zero, an internal 15µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 2mA current sink, and M1, a 100µA current sink, pull DE to GND through a 5.6kΩ resistor. M2 pulls DE to the disabled state against an external parasitic capacitance up to 100pF that may drive DE high. After 15µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakage currents that may drive DE high. M1 remains on until an external current source overcomes the required input current. At this time, the SR latch resets M1 and turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the input is reset.

A complementary circuit for $\overline{RE}$ uses two PMOS devices to pull $\overline{RE}$ to V_{CC}.

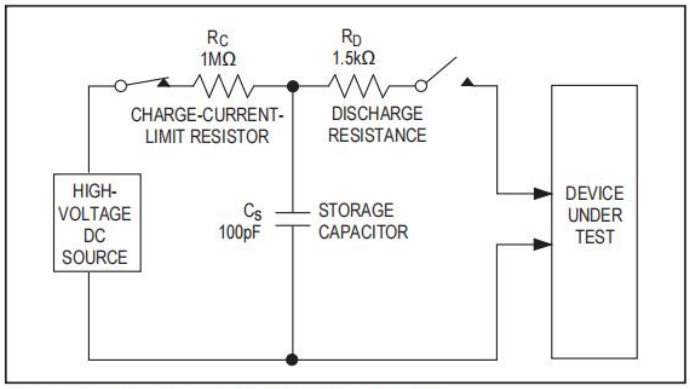


Figure 9a. Human Body ESD Test Model

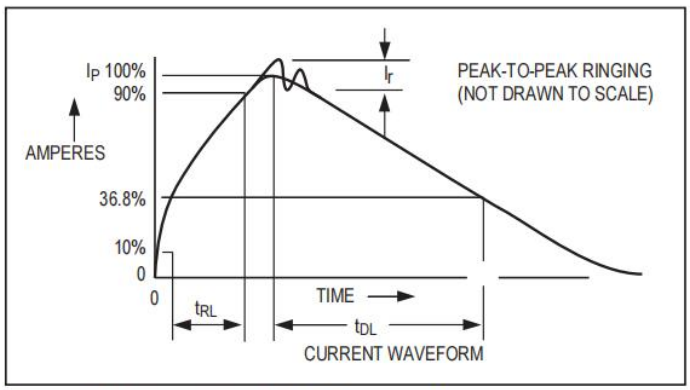


Figure 9b. Human Body Model Current Waveform

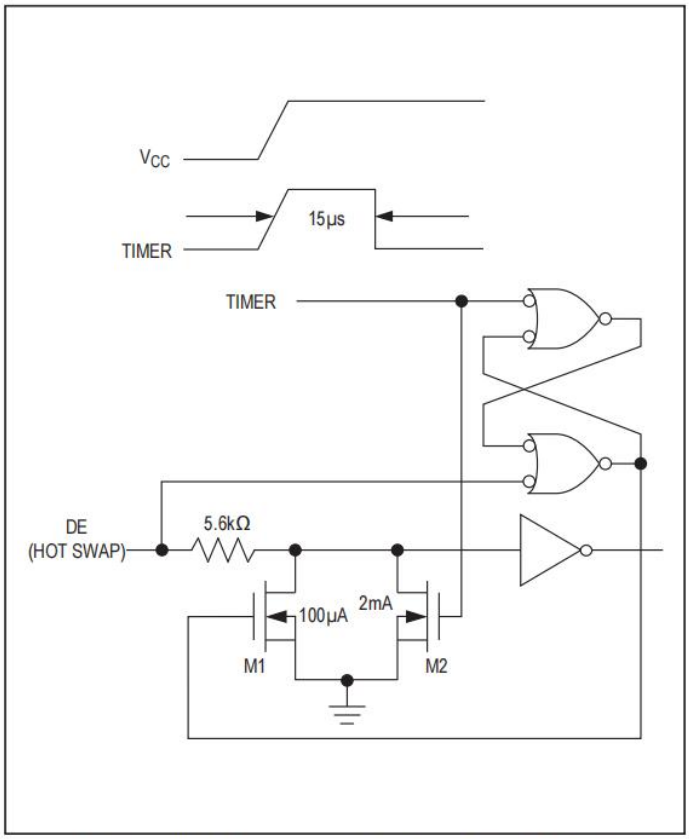
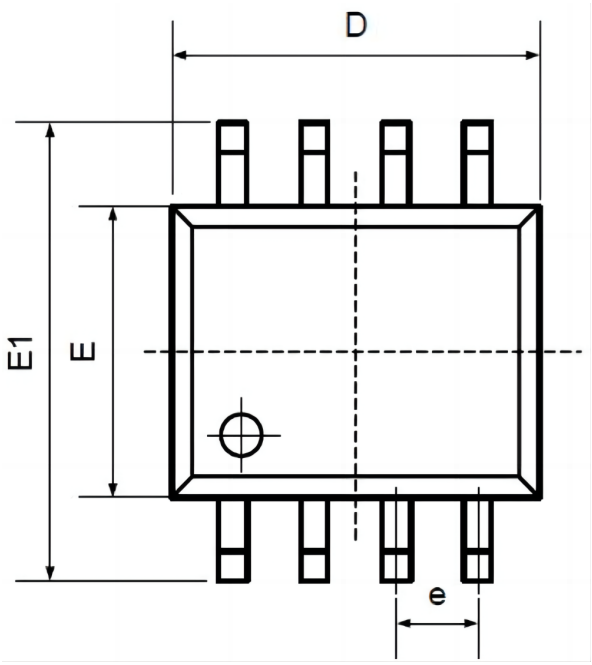


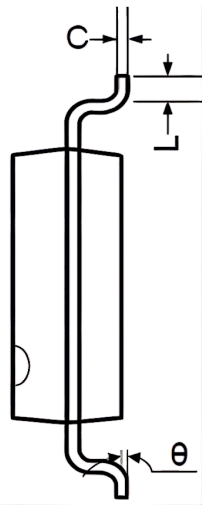
Figure 10. Simplified Structure of the Driver Enable Pin (DE)

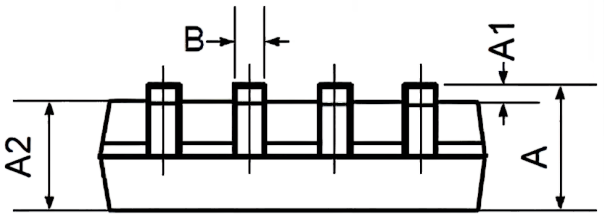
ORDERING INFORMATION

Order Number	Package	Package Quantity	Marking On The park
MAX13442EASA-TUDI	SOP8	Tape,Reel,2500	MAX13442EASA
MAX13442EESA-TUDI	SOP8	Tape,Reel,2500	MAX13442EESA
MAX13443EASA-TUDI	SOP8	Tape,Reel,2500	MAX13443EASA
MAX13443EESA-TUDI	SOP8	Tape,Reel,2500	MAX13443EESA
MAX13444EASA-TUDI	SOP8	Tape,Reel,2500	MAX13444EASA
MAX13444EESA-TUDI	SOP8	Tape,Reel,2500	MAX13444EESA

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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