8.5V Large Volume Ultra Low Bass 2-in-1 TLTR-AGC 2nd Smart K Audio Amplifier

FEATURES

- **Triple-Level Triple-Rate AGC algorithm：**
- **Enhance the bass, improve the dynamic range**
- **Increase volume, eliminate noise, timely and effectively protect the speaker**
- **8.5V Boost**
- **Output Power：4.1W@8Ω 4.6W@6Ω**
- **Low Noise：47μV**
- **Low THD+N：0.015%**
- **Overall efficiency up to 72%**
- **Support speaker, receiver 2-in-1 application**
- **Receiver mode: Noise 20μV, THD+N 0.02%**
- **Support 1.8V I²C Control Interface**
- **Battery tracking AGC, for low-voltage protection**
- **Over current protection, over-temperature protection and short-circuit protection**
- **Super TDD-Noise suppression**
- **Excellent pop-click suppression**
- High PSRR：70dB（217Hz）
- Small 2.76mm*2.36mm CSP-19 package

APPLICATIONS

- **Smart phone**

DESCRIPTION

AW87319 is specifically designed to improve the musical output dynamic range, enhance the overall sound quality, which is a new high efficiency, low noise, constant large volume, 2nd Smart K audio amplifiers. AW87319 integrates the high-voltage synchronous Boost with efficiency up to 84% as the Class D power stage supply. It significantly improves the output dynamic range of music. AW87319 integrates Awinic's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87319 noise floor is as low as to 47uV, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.015% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87319 supports speaker and receiver 2-in-1 applications. In the receiver application, Class D power stage voltage is straightly supplied by battery. AW87319 controls internal registers through the I²C interface. Register parameters include Boost Output Voltage, Boost maximum input peak current, Class D gain, Triple-Level Triple-Rate AGC parameters. AW87319 built-in over current protection, over-temperature protection and short circuit protection function, effectively protect the chip. AW87319 uses small 2.76mm*2.36mm CSP-19 package.

APPLICATION DIAGRAM

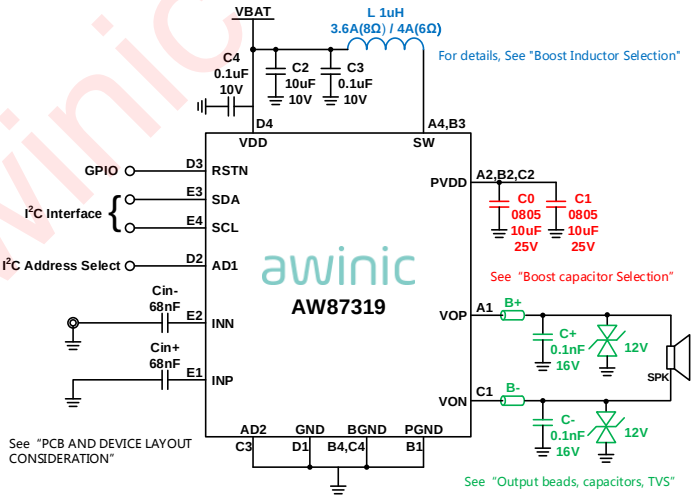

Figure1 AW87319 Single-ended input mode Application Diagram

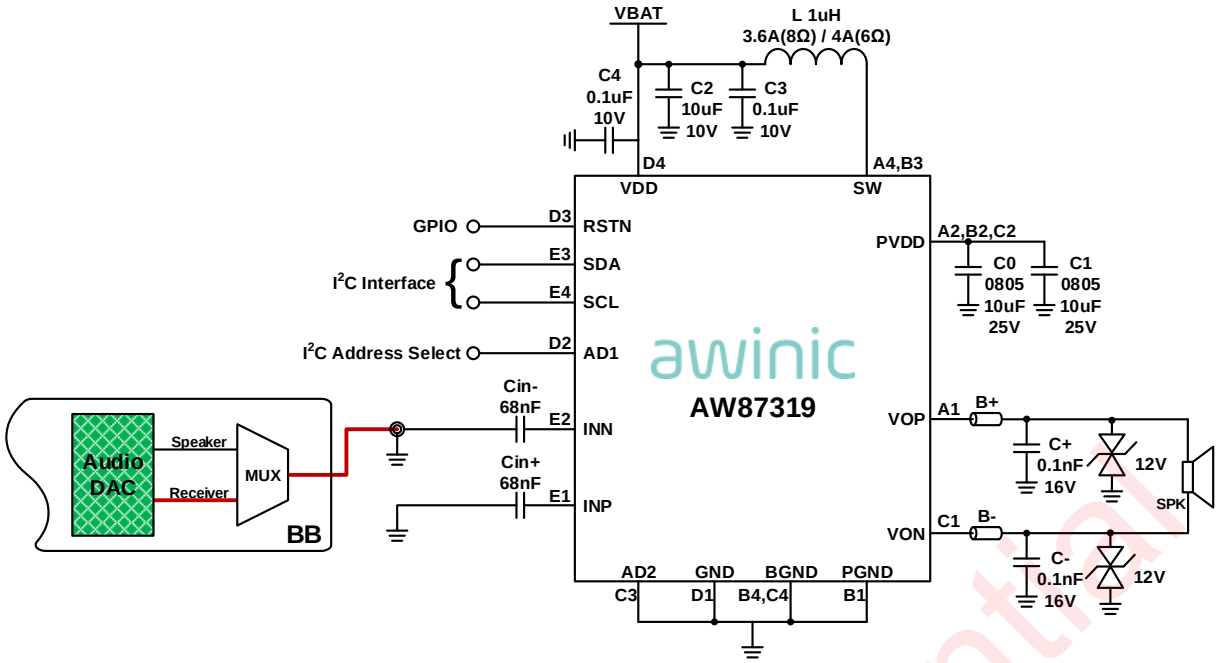

Figure2 AW87319 Receiver Mode Application Diagram

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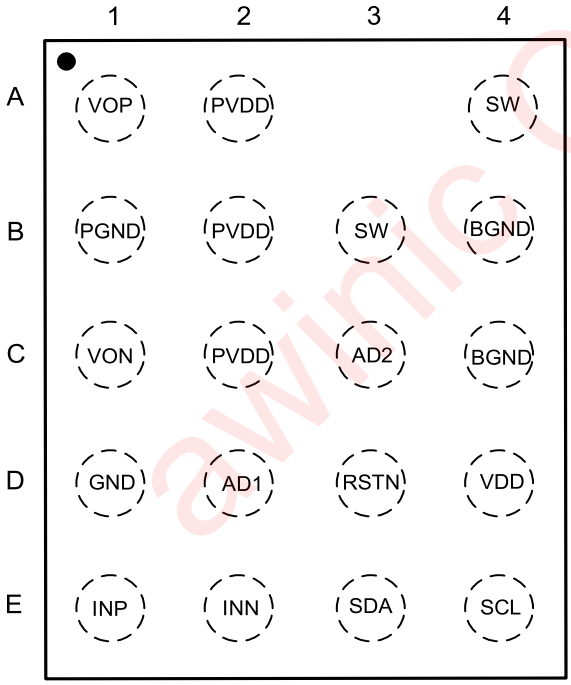
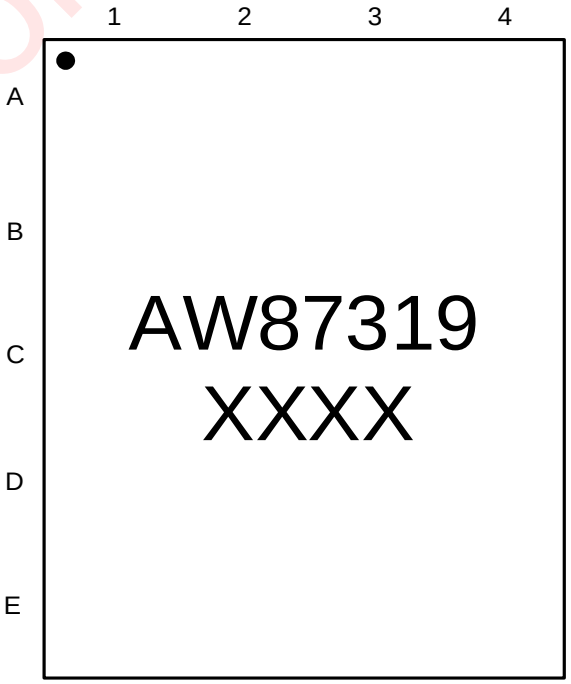
PIN CONFIGURATION AND TOP MARK

AW87319 CSR TOP VIEW



AW87319 CSR MARKING



AW87319 – AW87319 CSR
XXXX – Production tracking code

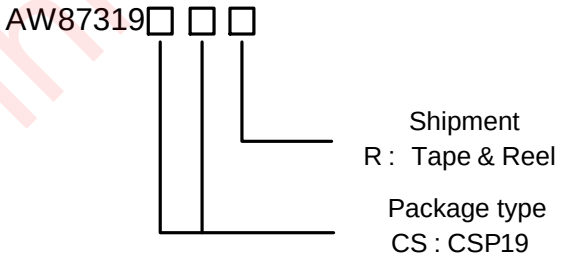
Figure3 AW87319CSR pin diagram top view and device marking

PIN DESCRIPTION

Number	Symbol	Description
A1	VOP	Positive audio output terminal
A2,B2,C2	PVDD	Boost charge pump output voltage
A4,B3	SW	Boost Switch pin
B1	PGND	Amplifier power ground
B4,C4	BGND	Boost power ground
C1	VON	Negative audio output terminal
C3	AD2	I²C address pin2
D1	GND	Ground
D2	AD1	I²C address pin1
D3	RSTN	Reset pin
D4	VDD	Power supply
E1	INP	Positive audio input terminal
E2	INN	Negative audio input terminal
E3	SDA	I²C-bus data input/output
E4	SCL	I²C-bus clock input

ORDERING INFORMATION

Product Type	Operation temperature range	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW87319CSR	-40°C～85°C	CSP-19	AW87319	MSL1	ROHS+HF	Tape and Reel 6000 pcs



FUNCTIONAL DIAGRAM

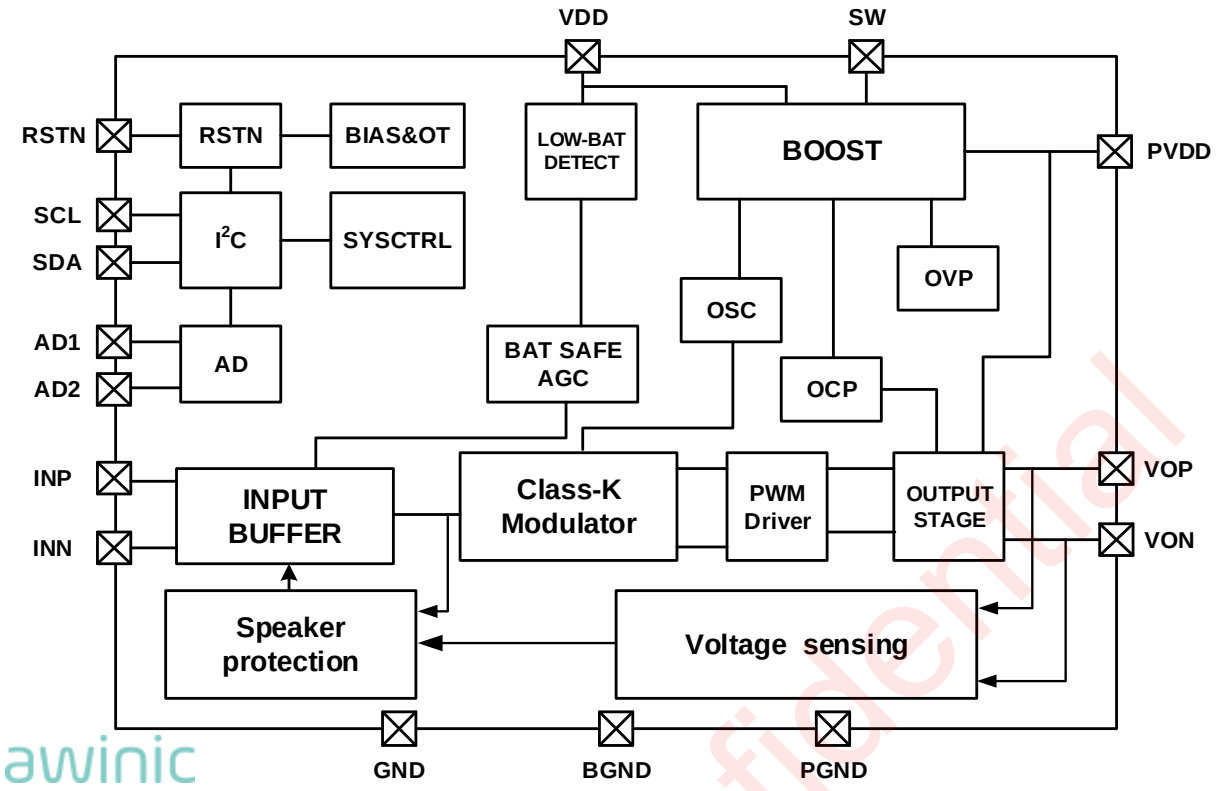


Figure 4 AW87319 functional diagram

ABSOLUTE MAXIMUM RATING(Note1)

Parameter		Range
Supply Voltage V_{DD}		-0.3V to 6V
Input Pin Voltage	INN，INP	-0.3V to VDD+0.3V
Boost output voltage PVDD		-0.3V to 15V
SW		-0.3V to PVDD+2V
VOP, VON		-0.3V to PVDD+0.3V
Minimum load resistance R_L		5Ω
Package Thermal Resistance θ_{JA}		60°C/W
Ambient Temperature Range		-40°C to 85°C
Maximum Junction Temperature T_{JMAX}		125°C
Storage Temperature Range T_{STG}		-65°C to 150°C
Lead Temperature（Soldering 10 Seconds）		260°C
ESD Rating (Note 2)		
HBM（human body model）		±7kV
CDM（charge device mode）		±2kV
Latch-up		

Test Condition：JEDEC STANDARD NO.78B DECEMBER 2008	+IT：450mA -IT：-450mA

Note 1：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7*

ELECTRICAL CHARACTERISTICS

Test condition：T_A=25°C，VDD=3.6V，PVDD=8V，R_L=8Ω+33μH，f=1kHz（unless otherwise noted）

Parameter		Test conditions		Min	Typ	Max	Units
V_{DD}	Power supply voltage			3.3		5.5	V
UVP	Under-voltage protection voltage				2.9		V
	Under-voltage protection hysteresis voltage				150		mV
V_{IH}	RSTN, SCL, SDA, AD1, AD2 high-level input voltage			1.3		V_{DD}	V
V_{IL}	RSTN, SCL, SDA, AD1, AD2 low-level input voltage			0		0.35	V
I_{SD}	Shutdown current	V_{DD}=3.6V，RSTN=0V			0.1	1	μA
T_{SD}	Over temperature protection threshold				160		°C
T_{SDR}	Over temperature protection recovery threshold				130		°C
T_{ON}	Turn-On time				40		ms
T_{OFF}	Turn-Off time			150		500	μs
Boost							
PVDD	The maximum Output voltage	V_{DD}=3.3V to 5.5V			8.5 (Note1)		V
OVP	OVP voltage	V_{DD}=3.3V to 5.5V			1.1*V_{PVDD}		V
	OVP hysteresis voltage				400		mV
F1	Operating Frequency	V_{DD}=3.3V to 5.5V			1.6		MHz
	Soft-start Switching frequency				0.4		MHz
D_{MAX}	The maximum duty cycle				90%		
T_{ST}	Soft-start time	No load，C_{OUT}=22μF			1		ms
η	Boost converter efficiency	V_{DD}=3.6V, R_L=8Ω,P_O=1W			84%		
I_{L_PEAK}	Inductor peak current limit	V_{DD}=3.3V to 5.5V			4 (Note1)		A
I_{SHORT}	Current limit when PVDD short to ground				300		mA
Class D							
V_{OS}	Output offset voltage	Vin=0V，V_{DD}=3.3V to 5.5V		-30	0	30	mV
η	total efficiency（Boost+Class D）	V_{DD}=4.2V, Po=2.5W, R_L=8Ω+33μH, PVDD=8.5V			72		%
I_q	Speaker Quiescent current	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			14		mA
	Receiver Quiescent current	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			6		mA
Fosc	Modulation frequency	V_{DD}=3V to 5.5V			800		kHz
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		70		dB
			1kHz		65		dB
SNR	Signal-to-noise ratio	V_{DD}=4.2V，PVDD=8.5V，Po=4.1W，R_L=8Ω+33μH，Av=18 dB			102		dB
		V_{DD}=4.2V，PVDD=8.5V，Po=0.8W，R_L=8Ω+33μH，Av=18 dB			94		dB

Parameter		Test conditions		Min	Typ	Max	Units
E_N	Speaker Output noise	Av=24 dB	20Hz to 20kHz, input ac grounded, A-weighting		58		μV
		Av=18 dB			47		
	Receiver Output noise	Av=0 dB			20		
Av	Speaker gain				24 (Note1)		dB
	Receiver gain				0 (Note1)		
Rini	Speaker Inner input resistance	Av=24 dB			9		kΩ
	Speaker Inner input resistance	Av=18 dB			18		
	Receiver Inner input resistance	Av=0 dB			95		
Fin	Speaker input Cut-off frequency	Cin=47nF, Av=24 dB			376		Hz
	Speaker input Cut-off frequency	Cin=47nF, Av=18 dB			188		
	Receiver input Cut-off frequency	Cin=47nF, Av=0 dB			36		
	Speaker input Cut-off frequency	Cin=68nF, Av=24 dB			260		
	Speaker input Cut-off frequency	Cin=68nF, Av=18 dB			130		
	Receiver input Cut-off frequency	Cin=68nF, Av=0 dB			25		
	Speaker input Cut-off frequency	Cin=100nF, Av=24 dB			177		
	Speaker input Cut-off frequency	Cin=100nF, Av=18 dB			88		
	Receiver input Cut-off frequency	Cin=100nF, Av=0 dB			17		
THD+N	Total harmonic distortion plus noise	V_{DD}=4.2V, Po=0.6W, R_L=8Ω+33μH, f=1kHz, PVDD=8.5V			0.015		%
Po	Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD=8.5V I_{L_PEAK}=4A			4.1		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD=8.5V I_{L_PEAK}=4A			4.9		W
		THD+N=1%, R_L=6Ω+33μH, V_{DD}=4.2V, PVDD=8.5V I_{L_PEAK}=4A			4.6		W
		THD+N=10%, R_L=6Ω+33μH, V_{DD}=4.2V, PVDD=8.5V I_{L_PEAK}=4A			5.1		W
Battery Tracking AGC							
V_{BSGD}	Battery protection threshold voltage				3.5 (Note1)		V
V_{BSGD_HYS}	Battery protection Hysteresis voltage				100		mV
Triple-Level Triple-Rate AGC							
T_{AT1}	AGC1 Attack Time				0.08 (Note1))		ms/dB
T_{AT2}	AGC2 Attack Time				0.64 (Note1)		ms/dB
T_{AT3}	AGC3 Attack Time				41 (Note1)		ms/dB
T_{RLT}	Release time				21 (Note1)		ms/dB
A_{MAX}	The maximum attenuation gain				-14		dB

Note 1：*Registers are adjustable; Refer to the list of registers.*

MEASUREMENT SETUP

AW87319 features switching digital output, as shown in Figure 5. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

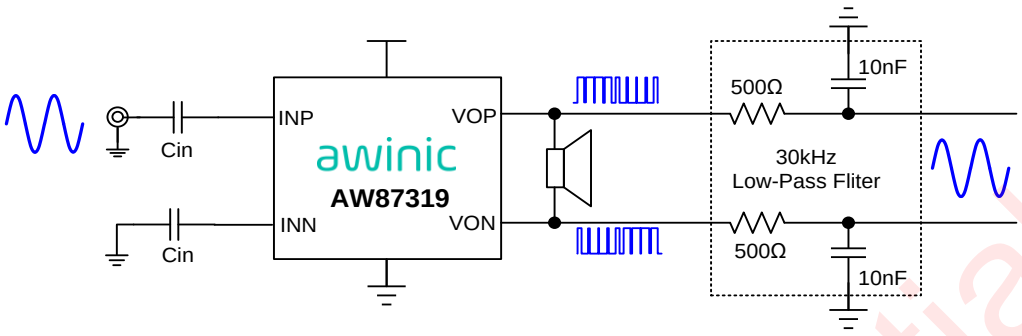


Figure 5 AW87319 test setup

Low pass filter uses resistance and capacitor values listed in Table 1.

R_{filter}	C_{filter}	Low-pass cutoff frequency
500Ω	10nF	32kHz
1kΩ	4.7nF	34kHz

Table 1 AW87319 recommended values for low pass filter

Output Power Calculation

According to the above test methods, the differential analog output signal is obtained at the output of the low pass filter. The valid values Vo_rms of the differential signal as shown below:

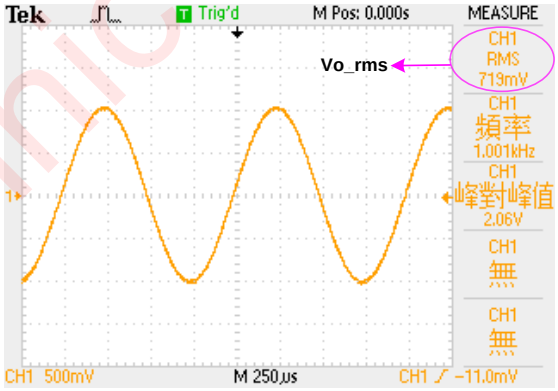


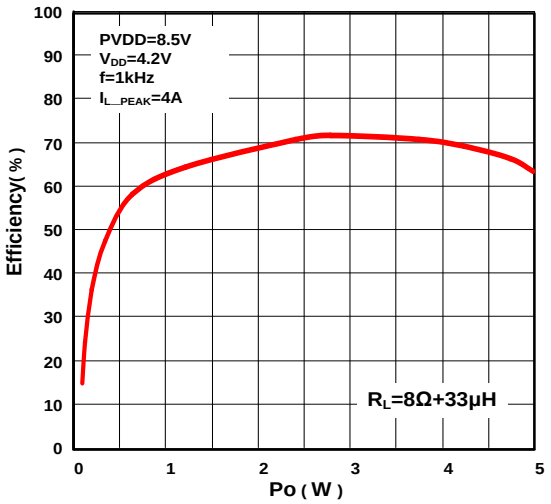
Figure 6 Output RMS value

The power calculation of Speaker is as follows：

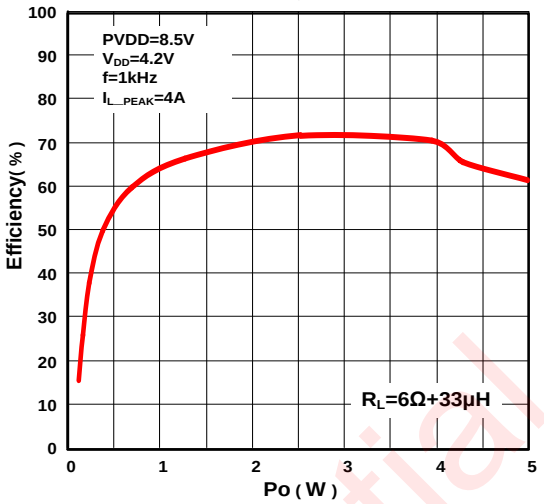
$$P_L = \frac{(Vo\_rms)^2}{R_L} \quad （R_L：\ load\ impedance\ of\ the\ speaker）$$

TYPICAL CHARACTERISTICS

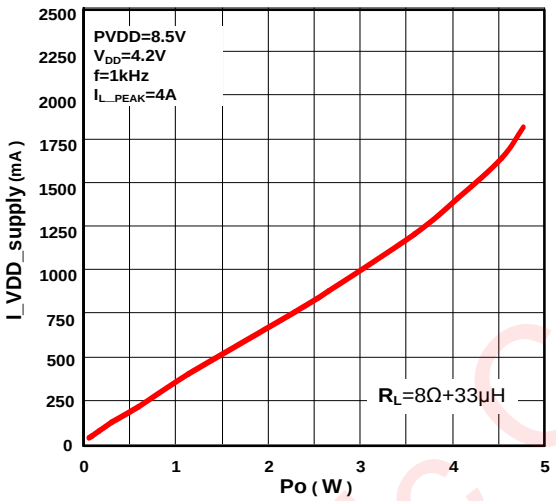
Efficiency vs Po



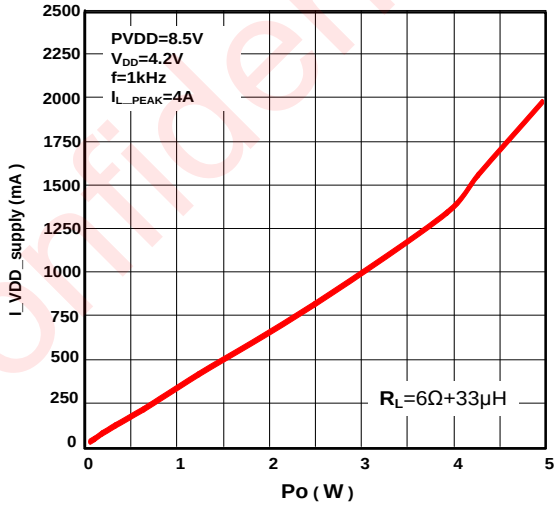
Efficiency vs Po



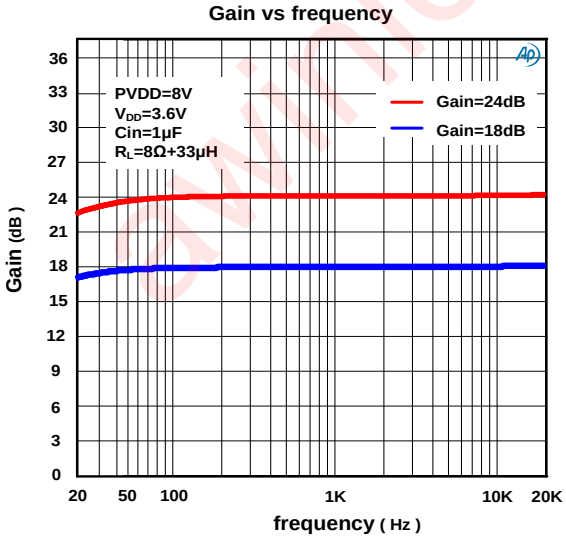
I_VDD_supply vs Po



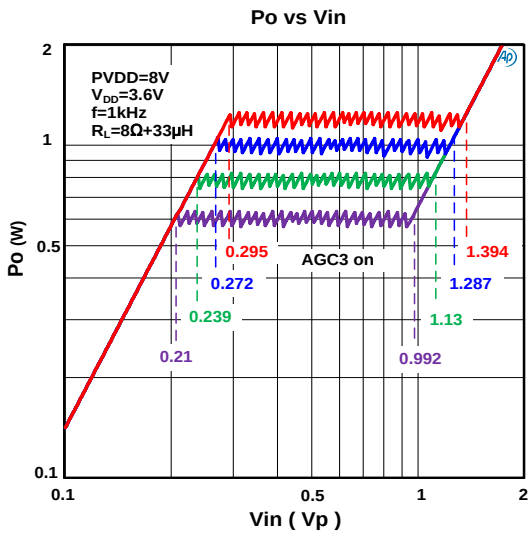
I_VDD_supply vs Po



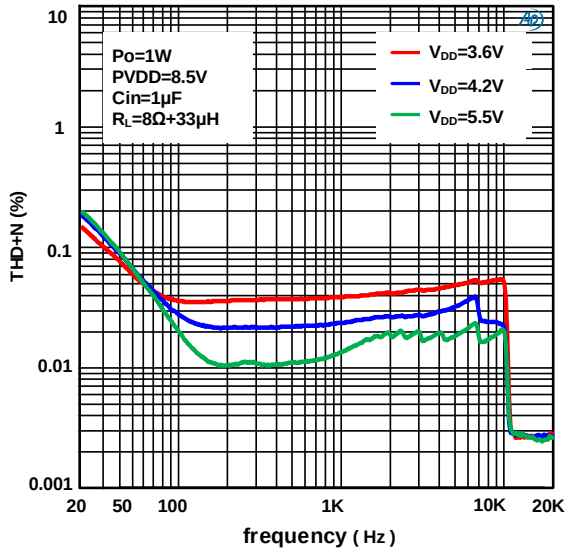
Gain vs frequency



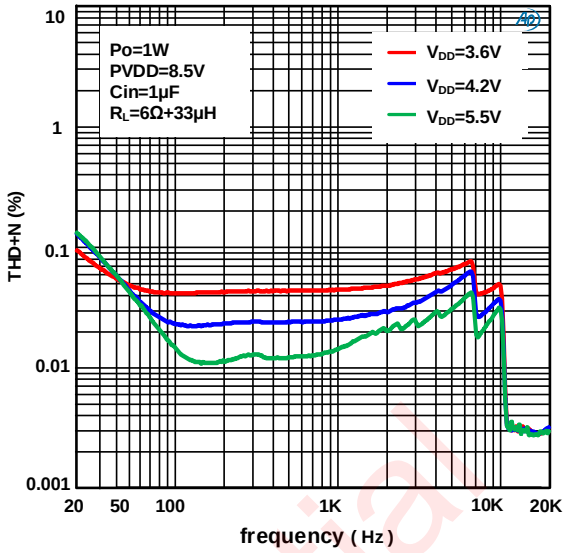
Po vs Vin



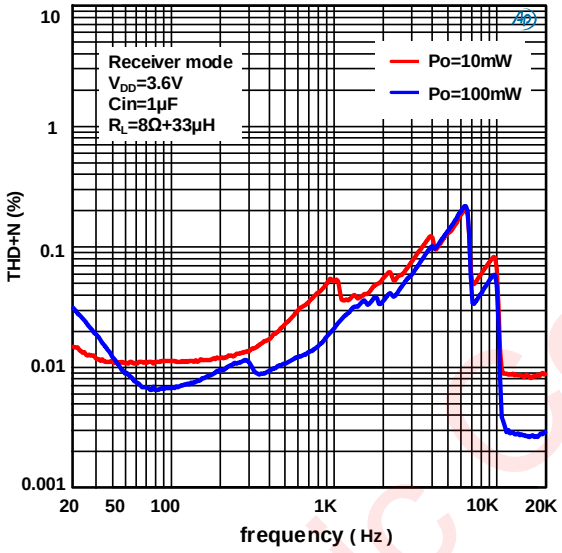
THD+N vs frequency



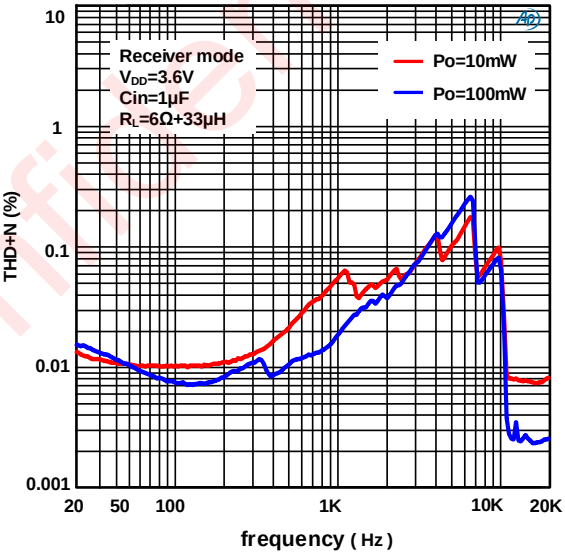
THD+N vs frequency



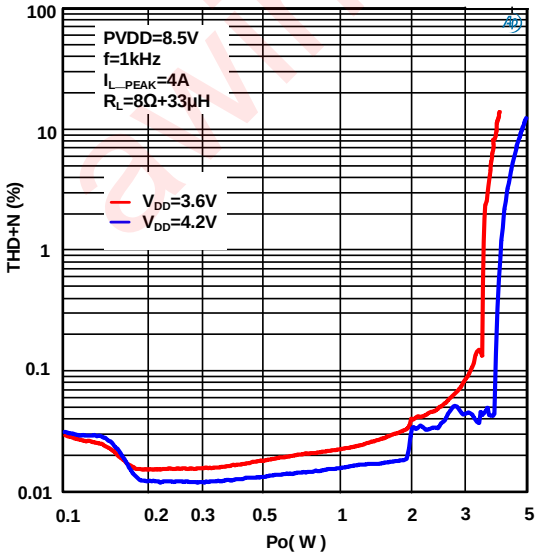
THD+N vs frequency



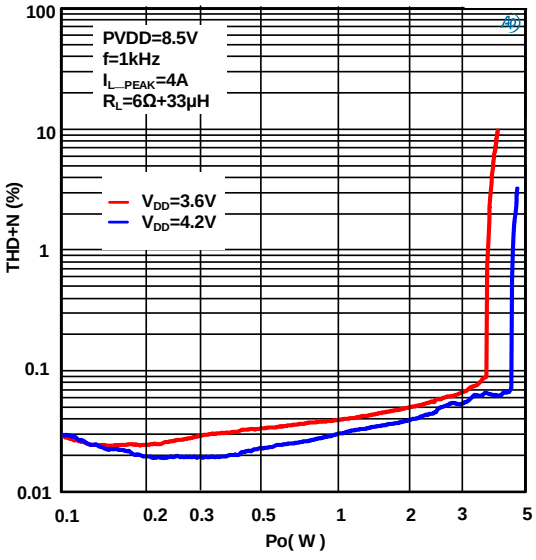
THD+N vs frequency



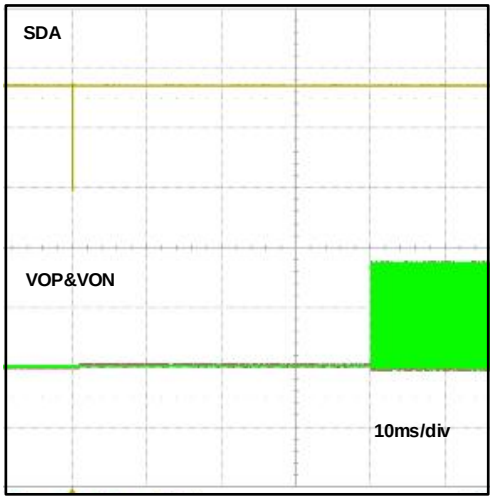
THD+N vs Po



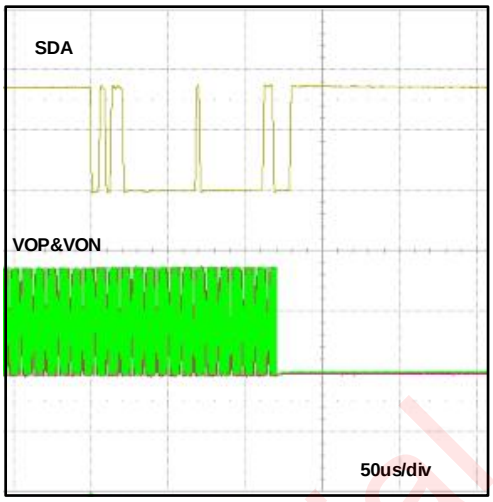
THD+N vs Po



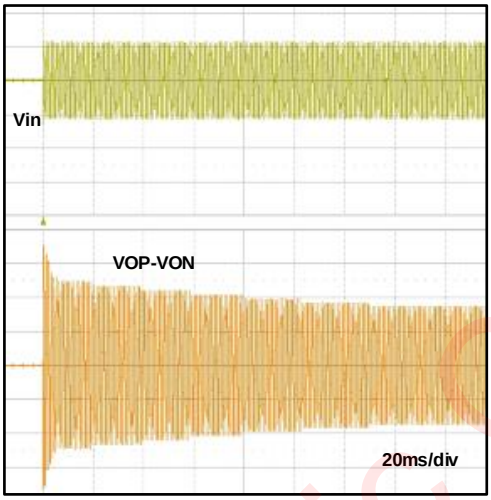
Start-up Sequence



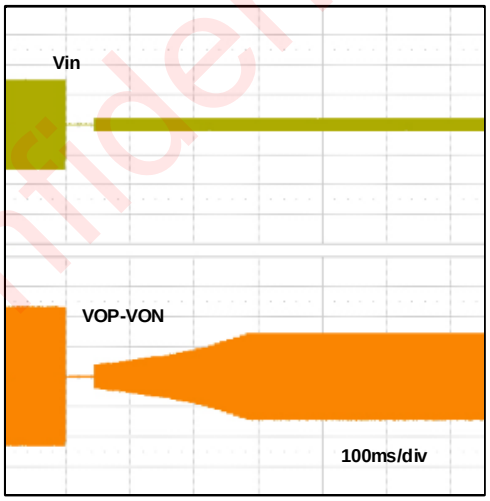
Shuntdown Sequence



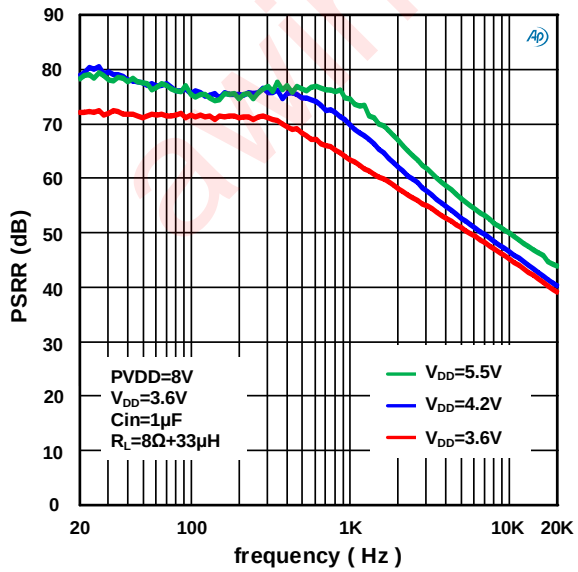
Triple-Level Triple-Rate AGC Attack Timing



Triple-Level Triple-Rate AGC Release Timing



PSRR vs Frequency



DETAILED FUNCTIONAL DESCRIPTION

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AW87319 integrates the high-voltage synchronous Boost with efficiency up to 84% as the Class D power stage supply. It significantly improves the output dynamic range of music. AW87319 integrates Awinic's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87319 noise floor is as low as to 47uV, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.015% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87319 supports speaker and receiver 2-in-1 applications. In the receiver application, Class D power stage voltage is straightly supplied by battery.

AW87319 controls internal registers through the I2C interface. Register parameters include Boost Output Voltage, Boost maximum input peak current, Class D gain, Triple-Level Triple-Rate AGC parameters. AW87319 built-in over current protection, over-temperature protection and short circuit protection function, effectively protect the chip. AW87319 uses small 2.76mm*2.36mm CSP-19 package.

CONSTANT OUTPUT POWER

In the mobile phone audio applications, the AGC function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually. So, it is hard to provide high quality music within the battery voltage range. AW87319 uses unique Triple-Level Triple-Rate technology, within lithium battery voltage range (3.3V~ 4.35V), to guarantee that output power is constant, and the output power will not drop along with the decrease of lithium battery voltage. Even if the battery voltage drops, AW87319 can still provide high quality large volume music enjoyment. The output power of AW87319 can be configured from 0.5W to 1.5W via I^2C, matching general speakers. Unique Triple-Level Triple-Rate AGC technology can bring high-quality music enjoyment.

Triple-Level Triple-Rate AGC technology

Awinic proprietary Triple-Level Triple-Rate AGC technology is designed for the protection of the high voltage power amplifier, which is divided into AGC1, AGC2 and AGC3 power levels, to obtain a large volume while maintaining excellent sound quality.

In practical applications, speaker can continuously work long hours at rated power, and also can work short-term at high power. For example, in the standard reliability of the loudspeaker experiment, the powder of peak power reached around four times of the rated power. For achieving larger volume and better sound quality, speakers need to work at high power for short periods of time, in order to improve the performance of the speaker. AW87319 Triple-Level Triple-Rate AGC technology can fit the speaker better. AGC1 prevents output signal clipping by detecting output voltage in a very short time after clipping, which can effectively restrain the noise clipping; AGC2 can improve the dynamic range of the music in a relatively short period of time; AGC3 can make the speaker work under rated power, which can effectively improve the volume and protect the speaker. Triple-Level Triple-Rate AGC can obtain more excellent overall performance.

Triple-Level Triple-Rate AGC detects the peak output voltage of the power amplifier, when the output peak voltage is higher than the compression threshold voltage, the amplifier gain decreases in 0.5dB step. When the output peak voltage is lower than the release threshold voltage, the amplifier gain is recovery to the initial gain in 0.5dB step. The detailed process can be described as follows:

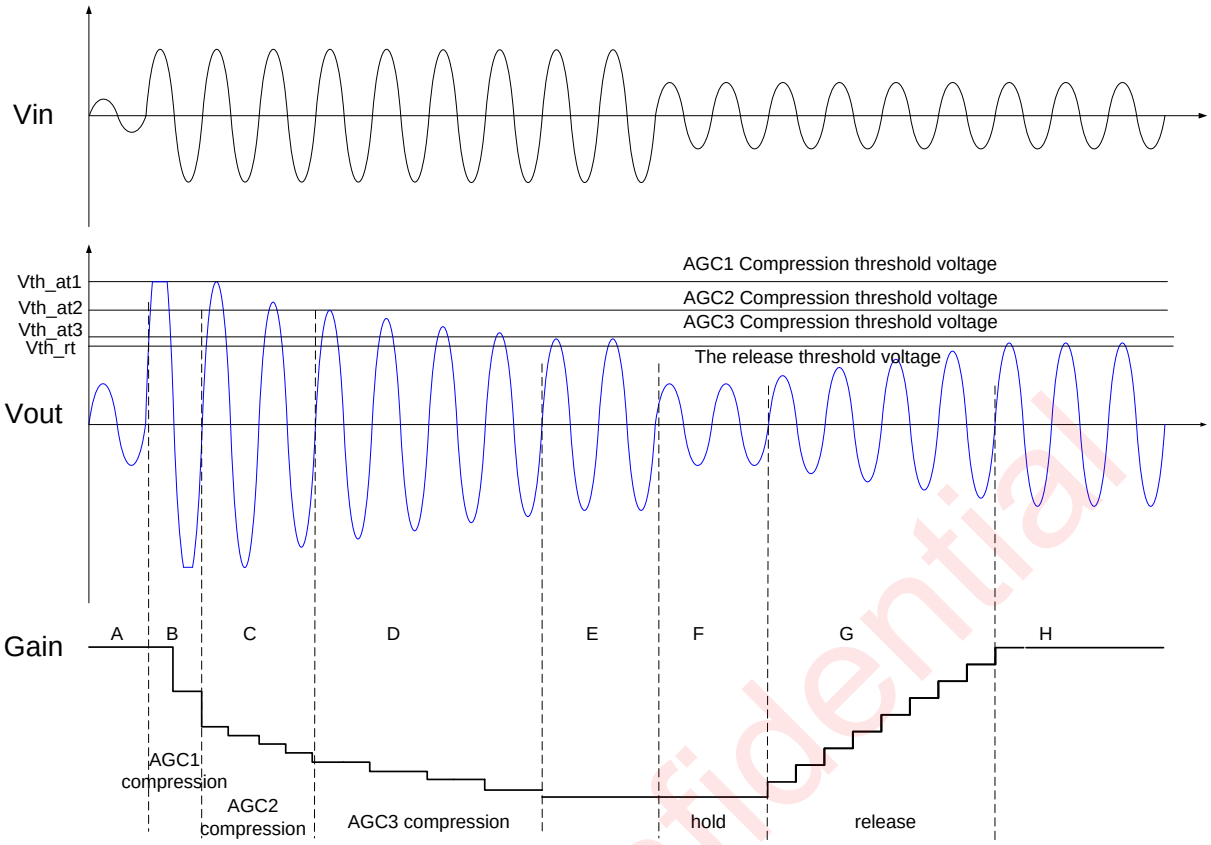


Figure 7 Triple-Level Triple-Rate AGC Operation Principle

A: The output voltage is lower than threshold voltage Vth_at3, AGC don't work.

B: Input voltage becomes large. It leads to the output voltage clipping, AGC1 starts work, the attack time is set through the I²C register 0x09h [2:1], when the output voltage is higher than Vth_at1, and gain register began to decrease. Gain decreases when the output signal passes through the zero. It eliminates the clipping noise as soon as possible.

C: When the output voltage is not clipping and higher than threshold voltage Vth_at2, AGC2 starts work, the attack time is set through the I²C register 0x08h [4:2], gain register begins to decrease at a certain rate. Gain register began to decrease. Gain decreases when the output signal passes through the zero. The output voltage gradually decreases to below the AGC2 attack threshold voltage Vth_at2, which can protect the speaker and enhance the sound.

D: When the output voltage is lower than the AGC2 attack threshold voltage Vth_at2 and higher than the AGC3 attack threshold voltage Vth_at3, AGC3 starts work, the attack time is set through the I²C register 0x07h [4:2], and gain register began to decrease at a certain rate. Gain decreases when the output signal passes through the zero, so the output voltage gradually decreases to below the AGC3 attack threshold voltage Vth_at3.

E: Attack time ends, Amplifier output power is close to the speaker rated power.

F: Input voltage decreases, the output voltage becomes lower than the release threshold voltage Vth_rt, at this point, gain remains the same in the maintain time (10 ms~20 ms).

G: Gain increases When the time of output voltage lower than the release threshold voltage Vth_rt is

longer than the holding time. The release time can be set through I²C register 0x07h [7:5].

H: Stop release when the output signal is larger than the release threshold or the gain is equal to the initial value. The output voltage remains constant.

Triple-Level Triple-Rate AGC can switch independently according to different application requirements. Such as close AGC1 and AGC2, retain only AGC3, this is the single-AGC mode, similar to AW8736(AGC3 attack time is set to 1.28ms/dB; release time is set to 41ms/dB); Close AGC2, open AGC1 and AGC3，this is Multi_level AGC. It can be set similar to AW8738 (AGC1 attack time is set to 80us/dB; AGC3 attack time is set to 0.64ms/dB; release time is set to 10.24ms/dB).

Zero-Crossing Adjustment Technology

Traditional AGC doesn't contain zero adjustment technology; AGC gain changes generally at the peak, the gain variation at the peak would generate a certain transient distortion, such distortions are audibly imperceptible.

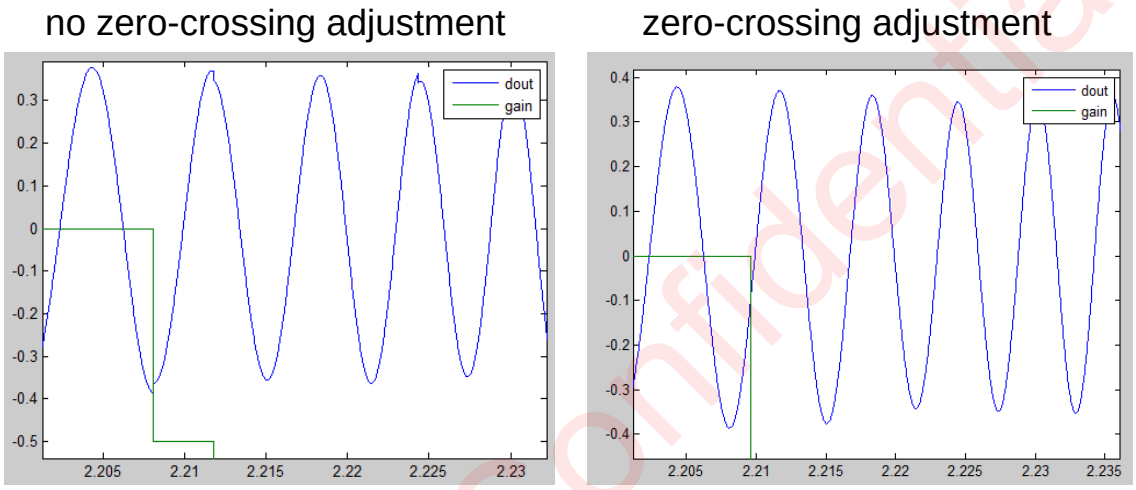


Figure 8 Zero-adjust Comparison

As shown above, when there is no zero-adjustment technology, it can be seen the obvious step change at the peak of large signal, the steps sound slightly perceived in special audio. Gain changes at zero. The steps disappear by using zero-crossing detection technology. Using zero detection technology can make the music pure and natural.

Low-voltage protection AGC technology

Mobile phone battery voltage will decrease in use, but the current will increase. When the battery voltage is low, high current maybe cause the battery protection or mobile phone automatically shut down. Awinic proprietary low voltage protection AGC technology can solve the problems, to prevent high current when the battery voltage is too low.

AW87319 is built-in low voltage protection AGC technology to real-time detection the battery voltage. Gain decreases rapidly when the battery voltage is below the safety threshold, so as to decrease the output voltage and the power supply current, which effectively prevents high current.

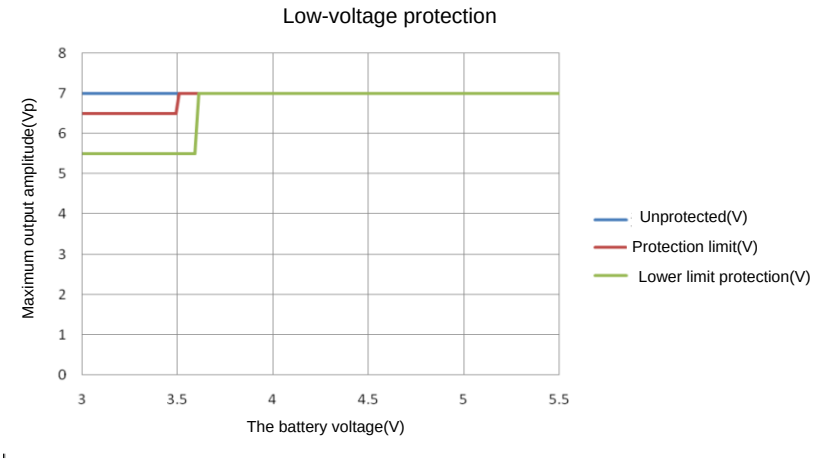


Figure 9 Low voltage protection

The protection safety threshold voltage is set to 3.5 V~3.6 V through the I²C register 0x02h [4:3]. The maximum protection output voltage is set to 5Vp ~ 6.5Vp through I²C register 0x02h [1:0].
Only when the register 0x02h [2] is set to 1, low voltage protection AGC technology is enabled.

Synchronous Boost technology

AW87319 integrated peak current mode synchronous PWM Boost as Class D power stage supply, significantly increase the output voltage dynamic range. Reduces the size of external components and saves PCB space by using 1.6 MHz switching frequency. Boost output voltage can be set through the I²C register 0x03h [2:0]; Boost current limit can be set through register 0x04h [2:0].
AW87319 synchronous Boost with soft-start function to prevent overshoot current at powering-on; integrated the output protection circuit and self-recovery function; integrated Anti-Ring circuit to reduce EMI in DCM mode; built-in substrate switching shutdown circuit, effectively preventing the input and output leakage current anti-irrigation.

2-in-1 application

AW87319 is easy to realize the speaker and receiver 2-in-1 application, better save cost and board space. AW87319 can set the gain through the I²C register 0x05h [3:0].
The typical value of input capacitance is a 68nF, gain is 24dB in default in speaker mode; the cutoff frequency is 376Hz; the gain is 0dB in default in receiver mode; the noise is 20μV; the cutoff frequency is 36Hz. Realize 2-in-1 application without changing any hardware.
Class D power stage voltage is straightly supplied by battery in receiver mode.

RNS (RF TDD Noise Suppression)

GSM radios transmit using time-division multiple access with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers.
In RF applications, improvements to both layout and component selection decrease the AW87319's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Minimizing the trace length prevents them from functioning as antennas and coupling RF signals into the AW87319. Additional RF immunity can also be obtained from relying on the self-resonant frequency of capacitors so as to exhibit the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to

20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors, when placed at the input pins, can effectively shunt the RF noise at the inputs of the AW87319. For these capacitors to be effective, they must have a low-impedance and low-inductance path to the ground plane.
Some RF energy will couple onto audio traces regardless of the effort to prevent this phenomenon from occurring, form audible TDD Noise. The AW87319 features a unique RNS technology, which effectively reduces RF energy, attenuate the RF TDD-noise, an acceptable audible level to the customer.

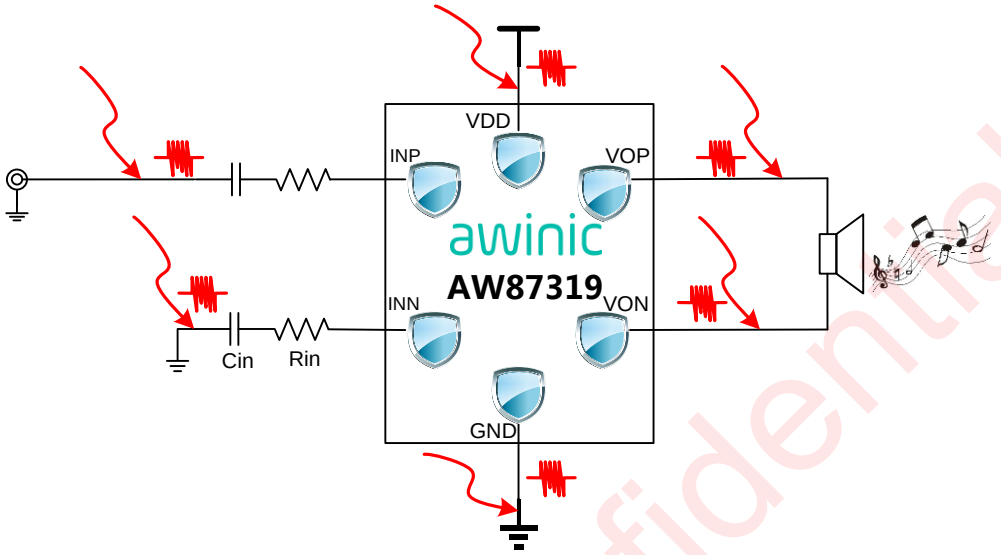


Figure 10 RF Radiation coupling schematic diagram

Filter-Free Modulation Scheme

The AW87319 features a filter-free PWM architecture that reduces the LC filter of the traditional Class-D amplifier, increasing efficiency, reducing board area consumption and system cost.

EEE

The AW87319 features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth.

Pop-Click Suppression

The AW87319 features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

Over temperature protection

AW87319 has automatic temperature detection mechanism. When the chip operates in a fault condition, the chip temperature is too high, up to a preset temperature protection temperature threshold (160°C), the system starts overheating protection, the chip powered off. AW87319 restarts to resume normal work when the chip temperature returns to normal operating range (less than 130°C).

Protection Function

When a short occurs between VOP/VON pin and VDD/GND or VOP and VON, the device will shut down, preventing the device from being damaged. AW87319 can automatically recover when the condition is

removed. The device shuts down when the junction temperature is high. The device returns to normal operation when the temperature decreases to safe levels.

PA Sequence

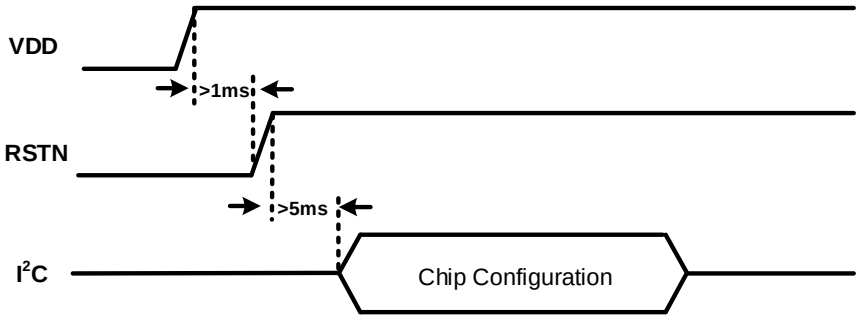


Figure 11 Power-on Sequence

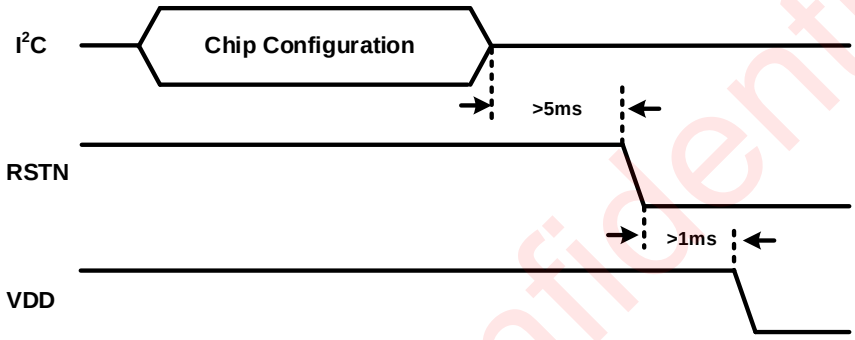


Figure 12 Power-off Sequence

I²C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	0.6			μs
3	t_{HIGH}	SCL High level Duration	1.3			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	START state to STL holding time	0.6			μs
8	$t_{SU:STO}$	Setup time SCL to STOP state	0.6			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA to SCL setup time	0.1			μs
11	$t_{HD:DAT}$	SCL to SDA hold time	10			ns

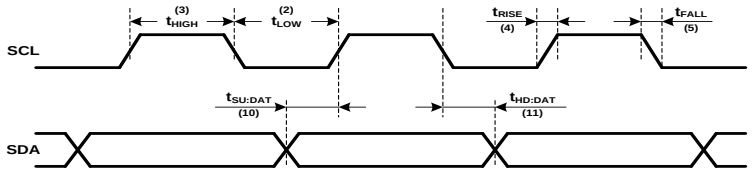


Figure 13 SCL and SDA timing relationships in the data transmission process

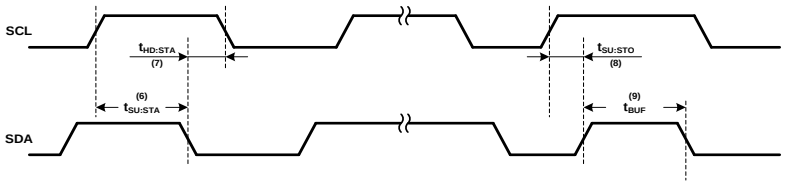


Figure 14 The timing relationship between START and STOP state

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

START state：The SCL maintain a high level, SDA from high to low level

STOP state：The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in figure 15.

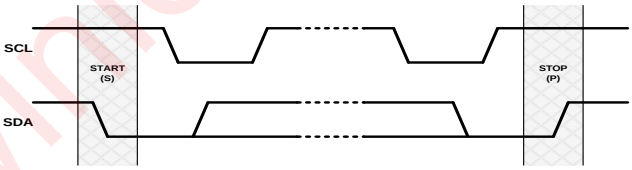


Figure 15 START and STOP state generation process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in figure 16. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in figure 17. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of

data can be transferred between START and STOP state.

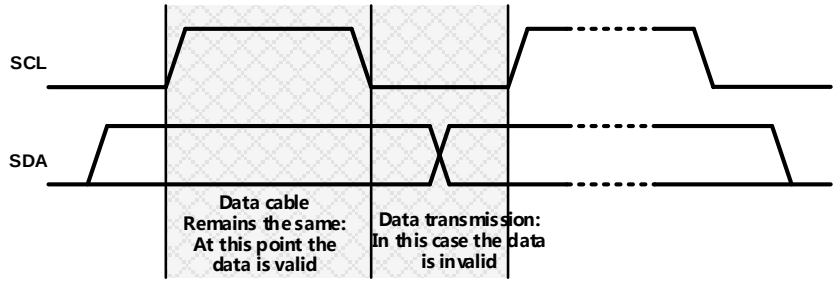


Figure 16 The data transfer rules on the I²C bus

The whole process of actual data transmission is shown in figure 17. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

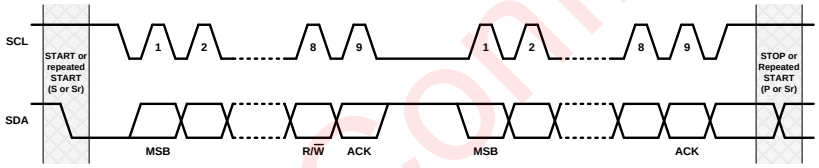


Figure 17 Data transmission on the I²C bus

I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW87319 as the slave device, the transmission process in accordance with the following steps, as shown in figure 18:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW87319 register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;
The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;
If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the AW87319.
The master device generates the STOP state to end the data transmission.

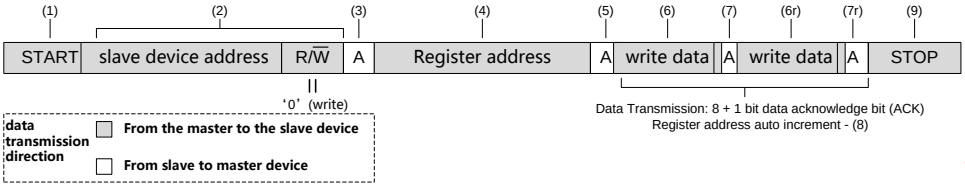


Figure 18 Writing process (data transmission direction remains the same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW87319 as the slave device, the transmission process carried out by following steps listed in figure 19:
Master device asserts a start condition;
Master device transmits the 7 bits address of AW87319, and followed by a "read / write" flag ($R/\overline{W} = 0$);
The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
The master device transmits the AW87319 register address to make sure where the first data byte will read;
The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;
Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W} = 1$) again;
The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
Master transmits 8 bits of data to register which needs to be read;
The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;
AW87319 automatically increment register address once after sent each acknowledge bit (ACK),
The master device generates the STOP state to end the data transmission.

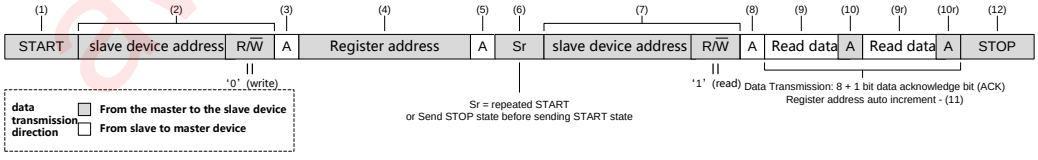


Figure 19 Reading process (data transmission direction remains the same)

Register List

name	address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Chip ID	0x00	1	0	0	1	1	0	1	1
SYSCTRL	0x01	0	0	0	0	0	EN_SW	EN_ClassD	EN_Boost
BATSAFE	0x02	0	0	1	BSTV(1)[1]	BSTV(1)[0]	EN_SS (2)	BSMOL(3)[1]	BSMOL(3)[0]
BOV(4)	0x03	0	0	0	0	0	1	BOV(4)[1]	BOV(4)[0]
BP	0x04	0	0	0	0	0	BMCPC(5)[2]	BMCPC(5)[1]	BMCPC(5)[0]
Gain	0x05	0	0	0	0	Gain[3]	Gain[2]	Gain[1]	Gain[0]
AGC3_Po	0x06	0	0	0	0	AGC3_Po[3]	AGC3_Po[2]	AGC3_Po[1]	AGC3_Po[0]
AGC3	0x07	AGC3_RT[2]	AGC3_RT[1]	AGC3_RT[0]	AGC3_AT[2]	AGC3_AT[1]	AGC3_AT[0]	1	0
AGC2	0x08	AGC2_Po[2]	AGC2_Po[1]	AGC2_Po[0]	AGC2_AT[2]	AGC2_AT[1]	AGC2_AT[0]	0	0
AGC1	0x09	0	0	0	0	0	AGC1_AT[1]	AGC1_AT[0]	PD_AGC1

(1) BSTV: Battery_Safeguard_Threshold_Voltage
(2) EN_SS: EN_Software_Safeguard
(3) BSMOL: Battery_Safeguard_Max_Output_Level
(4) BOV: Boost_Output_Voltage
(5) BMCPC: Boost_Maxim_Coil_Peak_Current

register	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09
Default	0x9B	0x03	0x28	0x05	0x04	0x02 (EN_Boost=0) 0x0D (EN_Boost=1)	0x03	0x52	0x28	0x02

Table 2. AW87319 Register Default value

Any register address which is more than 0x09 and all reserved bits are reserved for debugging and testing purposes. Changing their values may affect the normal function of the power amplifier; Reading them will get any possible values. AW87319's I²C address is 10110A2A1, which, in order to avoid conflict with other I²C devices address, you can pull up or pull-down AW87319 of AD2 and AD1 pins to set the value of A2 and A1, respectively. The following lists specific information about all visible registers, including default values and programmable ranges.

CHIP ID* Register *(address: 0x00)

I²C Bit	Name	R/W	Default	Description
7:0	IDCODE	R	0x9B	Chip ID will be returned after reading. All configuration registers will be reset to default values after 0xAA is written.

SYSTEM CONTROL (SYSCTRL)* Register *(address: 0x01)

I²C Bit	Name	R/W	Default	Description
7:3	--	--	0000 0	Reserved and Unused
2	EN_SW	R/W	0	Chip Software Enable 0: Chip Software Disable: Shutdown the whole chip except BIAS and OSC. 1: Chip Software Enable
1	EN_ClassD	R/W	1	Class D Enable 0: Class D Disable 1: Class D Enable
0	EN_Boost	R/W	1	Boost Enable: This bit must be unchanged when EN_SW=1. 0: Boost Disable 1: Boost Enable

BATTERY SAFEGUARDS (BATSAFE)* Register *(address: 0x02)

I²C Bit	Name	R/W	Default	Description
7:5	--	--	001	Reserved and Unused
4:3	Battery_Safeguard_ Threshold_Voltage	R/W	01	Setting Battery Threshold Voltage for Triggering Battery Safeguard Mode: When EN_Boost=0, these bits are fixed in '00'.
				00: On-Chip Threshold Detect Disable: Use off-chip signal to control mode switch.
				01: Threshold Voltage is 3.50V
				10: Threshold Voltage is 3.55V
				11: Threshold Voltage is 3.60V
2	EN_Software_Safeguard	R/W	0	Battery Safeguard Mode Software Enable
				0: Battery Safeguard Mode Software Disable
				1: Battery Safeguard Mode Software Enable
1:0	Battery_Safeguard_Max_ Output_Level	R/W	00	Setting Maximum Output Level when Battery Safeguard Mode Triggered
				00: 5.5Vp
				01: 5.0Vp
				10: 6.0Vp
				11: 6.5Vp

BOOST OUTPUT VOLTAGE (BOV)* Register *(address: 0x03)

I²C Bit	Name	R/W	Default	Description
7:3	--	--	0000 0	Reserved and Unused
2:0	Boost_Output_Voltage	R/W	101	Setting Boost Output Voltage
				111: 8.5V
				110: 8.25V
				101: 8.0V
				100: 7.75V
				0XX: Unavailable

BOOST PARAMETER (BP)* Register *(address: 0x04)

I²C Bit	Name	R/W	Default	Description
7:3	--	--	0000 0	Reserved and Unused
2:0	Boost_Max_Coil_Peak_Current	R/W	100	Setting Boost Max Inductor Peak Current
				000: 1.50A
				001: 2.00A
				010: 2.50A
				011: 3.00A
				100: 3.25A
				101: 3.50A
				110: 3.75A
				111: 4.00A

CLASS D GAIN (Gain) Register *(address: 0x05)*

For EN_Boost=0 (Receiver Mode):

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	Class_D_Gain	R/W	0010	Setting Class D Amplifying Gain
				0000: -3.0dB R_{ini}=134kΩ
				0001: -1.5dB R_{ini}=113kΩ
				0010: 0.0dB R_{ini}=95kΩ
				0011: 1.5dB R_{ini}=80kΩ
				0100: 3.0dB R_{ini}=67kΩ
				0101: 4.5dB R_{ini}=57kΩ
				0110: 6.0dB R_{ini}=47kΩ
				0111: 7.5dB R_{ini}=40kΩ
				1000: 9.0dB R_{ini}=34kΩ
				1XXX (XXX≠000): Unavailable

For EN_Boost=1 (Boost Mode):

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	Class_D_Gain	R/W	1101	Setting Class D Amplifying Gain
				0XXX: Unavailable
				1000: Unavailable
				1001: 18.0dB R_{ini}=18kΩ
				1010: 19.5dB R_{ini}=15kΩ
				1011: 21.0dB R_{ini}=13kΩ
				1100: 22.5dB R_{ini}=11kΩ
				1101: 24.0dB R_{ini}=9kΩ
				1110: 25.5dB R_{ini}=8kΩ
				1111: 27.0dB R_{ini}=6.5kΩ

CLASS D AGC3 OUTPUT POWER (AGC3_Po) Register *(address: 0x06)*

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC3_Output_Power	R/W	0011	Setting AGC3 Output Power for Protecting Speaker
				0000: 0.5W@8Ω 0.67W@6Ω
				0001: 0.6W@8Ω 0.80W@6Ω
				0010: 0.7W@8Ω 0.93W@6Ω
				0011: 0.8W@8Ω 1.07W@6Ω
				0100: 0.9W@8Ω 1.20W@6Ω
				0101:1.0W@8Ω 1.33W@6Ω
				0110: 1.1W@8Ω 1.47W@6Ω
				0111: 1.2W@8Ω 1.60W@6Ω
				1000: 1.3W@8Ω 1.73W@6Ω
				1001: 1.4W@8Ω 1.87W@6Ω
				1010: 1.5W@8Ω 2.00W@6Ω
				1011: AGC3 Disable
				1100~1111: Unavailable

CLASS D AGC3 PARAMETER (AGC3)* Register *(address: 0x07)

I²C Bit	Name	R/W	Default	Description
7:5	AGC3_Release_Time	R/W	010	Setting Release Time of AGC3: 000: 5.12ms/dB 001: 10.24ms/dB 010: 21 ms/dB 011: 41 ms/dB 100: 82 ms/dB 101: 164 ms/dB 110: 328 ms/dB 111: Unavailable
4:2	AGC3_Attack_Time	R/W	100	Setting Attack Time of AGC3: 000: 0.64ms/dB 001: 1.28ms/dB 010: 2.56ms/dB 011: 10.24ms/dB 100: 41ms/dB 101~111: Unavailable
1:0	-	-	10	Reserved and Unused

CLASS D AGC2 PARAMETER (AGC2)* Register *(address: 0x08)

I²C Bit	Name	R/W	Default	Description
7:5	AGC2_Output_Power	R/W	001	Setting AGC2 Output Power: 000: 1.2W@8Ω 1.6W@6Ω 001: 1.5W@8Ω 2.0W@6Ω 010: 1.8W@8Ω 2.4W@6Ω 011: 2.1W@8Ω 2.8W@6Ω 100: 2.4W@8Ω 3.2W@6Ω 101: AGC2 Disable 110~111: Unavailable
4:2	AGC2_Attack_Time	R/W	010	Setting Attack Time of AGC2: 000: 0.16ms/dB 001: 0.32ms/ dB 010: 0.64ms/dB 011: 2.56ms/dB 100: 10.24ms/dB 101: 41ms/dB 110~111: Unavailable
1:0	--	--	00	Reserved and Unused

CLASS D AGC1 PARAMETER (AGC1)* Register *(address: 0x09)

I²C Bit	Name	R/W	Default	Description
7:3	--	--	0000	Reserved and Unused
2:1	Fastest_Level_AGC_Attack_Time	R/W	01	Setting Fastest Level AGC Attack Time: 00: 0.04ms/dB 01: 0.08ms/dB 10: 0.16ms/dB 11: 0.32ms/dB
0	PD_Fastest_Level_AGC	R/W	0	Fastest Level AGC Disable: 0: Fastest Level AGC Enable 1: Fastest Level AGC Disable

APPLICATION INFORMATION

Boost Inductor Selection

Selecting inductor needs to consider Inductance, size, magnetic shielding, saturation current and temperature current.

a) Inductance

Inductance value is limited by the boost converter's internal loop compensation. In order to ensure phase margin sufficient under all operating conditions, recommended 1μH inductor.

b) Size

For a certain value of inductor, the smaller the size, the greater the parasitic series resistance of the inductor DCR, the higher the loss, corresponds to the lower efficiency.

c) Magnetic shielding

Magnetic shielding can effectively prevent the inductance of the electromagnetic radiation interference. It is much better to choose inductance with magnetic shielding in the application of EMI sensitive environment.

d) Saturation current and temperature rise of current

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, on the one hand, since the magnetic core begins to saturate, inductance value will decline; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. In general, the current value is defined as the saturation current I_{SAT} when the inductance value drops to 70%; the current value is defined as temperature rise current I_{RMS} when inductance temperature rise 40℃.

For particular applications, need to calculate the maximum I_{L_PEAK} and I_{L_RMS}, which is a basis of selecting the inductor. When VDD = 4.2V, PVDD=8.5V, R_L = 8Ω， amplifier R_{DSON} = 250mΩ, when THD = 1% (the maximum power without distortion), the output power is calculated as follows:

$$P_{OUT}=\frac{\left(V_{OUT}\times\frac{R_L}{R_L+2\times R_{DSON}}\right)^2}{2\times R_L\times(1-2.3\%)}=\frac{\left(8.5\times\frac{8}{8+2\times0.25}\right)^2}{2\times8\times0.977}\text{W}=4.1\text{W}$$

Where the coefficients in the denominator of (0.977) is the power ratio of no truncation maximum output (the power at THD = 1%). In such a large output power, the overall efficiency of the power amplifier is typically 68%, in order to calculate the maximum average current $I_{MAX\_AVG\_VDD}$ and maximum peak current $I_{MAX\_PEAK\_VDD}$ drawn from VDD:

$$I_{MAX\_AVG\_VDD}=\frac{P_{OUT}}{V_{DD}\times\eta}=\frac{4.1}{4.2\times0.68}\text{A}=1.436\text{A}$$

$$I_{MAX\_PEAK\_VDD}=2\times I_{MAX\_AVG\_VDD}=2\times1.436\text{A}=2.872\text{A}$$

If inductor DCR is 50mΩ, then when the output power of 4.1W, the inductor power loss is:

$$P_{DCR,LOSS}=1.5\cdot I_{MAX\_AVG\_VDD}^2\cdot DCR=1.5\times1.436^2\times0.05\text{W}=155\text{mW}$$

Wherein the coefficient 1.5 is the square of the ratio of the sine wave current RMS value and average value (there is no consideration of the impact of the inductor ripple, the actual DCR loss will be even greater). If the loss which is resulting from DCR is less than 1% at maximum efficiency (P_{OUT} = 2.5W, η =

72%), then:

$$I_{AVG\_VDD} = \frac{P_{OUT}}{V_{DD} \times \eta} = \frac{2.5}{4.2 \times 0.72} \text{A} = 0.827\text{A}$$

$$DCR = \frac{P_{DCR,LOSS}}{1.5 \cdot I_{AVG\_VDD}^2} \le 0.01 \times \frac{P_{OUT}}{1.5 \cdot I_{AVG\_VDD}^2 \cdot \eta} = \frac{0.01 \times 2.5}{1.5 \times 0.827^2 \times 0.72} \Omega = 34\text{m}\Omega$$

According to the working principle of the Boost, we can calculate the size of the inductor current ripple Δ_{IL}:

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f \times L} = \frac{4.2 \times (8.5 - 4.2)}{8.5 \times 1.6 \times 1} \text{A} = 1.328\text{A}$$

Thus, the maximum peak inductor current I_{L_PEAK} and maximum effective inductor current I_{L_RMS} is:

$$I_{L\_PEAK} = I_{MAX\_PEAK\_VDD} + \frac{\Delta I_L}{2} = 2.872 + \frac{1.328}{2} \text{A} = 3.54\text{A}$$

$$I_{L\_RMS} = \sqrt{I_{MAX\_PEAK\_VDD}^2 + \frac{\Delta I_L^2}{12}} = \sqrt{2.872^2 + \frac{1.328^2}{12}} \text{A} = 2.90\text{A}$$

From the above calculation results:

1) For typical DCR about 50mΩ inductance, the efficiency loss caused by around1.5%;
2) Need to choose AW87319 inductance input current limit value I_{LIMIT} is greater than I_{L_PEAK} = 3.54 A (< I_{LIMIT} = 4A), to guarantee the amplifier output power can be achieved when THD = 1% (= 4.1W) but not limited by value I_{LIMIT};
3) In practice, the maximum output power of the amplifier is likely to reach 4.1W in an instant, so the selected inductor saturation current I_{SAT} requires more than the maximum inductor peak current I_{L_PEAK}, and cannot be less than 3.6A;
4) In some cases, if the I_{L_PEAK} calculated according to the above method is greater than the set of input inductor current limit value I_{LIMIT}, shows the power amplifier is restricted by inductance input current limit, the actual maximum output power is less than the calculated value, the measured value shall prevail, and I_{SAT} need greater than the set current limiting value I_{LIMIT}, and cannot be less than 3.6A;
5) Take PVDD = 8.5V for example, under different conditions, the typical method of selecting I_{SAT} in the following table:

V_{DD} (V)	PVDD (V)	R_L (Ω)	I_{LIMIT} (A)	Efficiency(η) (%)	P_O@THD=1% (W)	I_{L_PEAK} (note2) (A)	Inductor saturation current ISAT minimum value (A)
4.2	8.5	8	4	68	4.1 (4.1) (note1)	3.54	3.6
3.6	8.5	8	4	60	3.6 (4.1) (note1)	4.44	4.0
4.2	8.5	6	4	67	4.7 (5.3) (note1)	4.40	4.0
3.6	8.5	6	4	60	3.7 (5.3) (note1)	5.51	4.0

Note 1: The values in parentheses are calculated PO @ THD = 1% when there is no "inductor input current limit"

Note 2: I_{L_PEAK} is in parentheses in the "note 1" for power and actual efficiency calculated, if its value is greater than I_{LIMIT}, then triggers the inductance input current limit.

6) As the result of the action of TLTR-AGC，amplifier will not work long hours at maximum power without distortion (4.1W), the actual average inductor current is far less than the maximum inductor current effective I_{L_RMS}, so when selecting the inductor, the inductor temperature rise current is not usually a limiting factor;
7) Inductor Selection example: Sunlord WPN252012H1R0MT inductance. The inductor package size is 252012, inductance value is 1μH, DCR Typical value is 48mΩ, the typical saturation current I_{SAT} is 4.2A, the typical temperature rise current I_{RMS} is 3.4A, suitable for VDD=3.6V, PVDD=8.5 V, speaker impedance R_L=8Ω, inductor input current limit I_{LIMIT}= 4A. If you choose I_{SAT} or I_{RMS} of the inductance is too small, it is possible to cause the chip don't work properly, or the temperature of the inductance is too high.

Model	Inductance value	producer	size	DCR（Ω）	I_{SAT}（A）	I_{RMS}（A）
WPN252012H1R0MT	1uH	Sunlord	2.5×2.0×1.2mm	0.054	4.2	3.4

Boost capacitor Selection

Boost output capacitor is usually within the range 0.1uF~47uF. It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically $BaTiO_3$), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

A) temperature stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive; X5R capacitance change within ± 15% in temperature range of 55°C to 85°C, X7R capacitance change within ±15% in temperature range of -55°C~125°C. The Boost output capacitance of AW87319 recommends X5R ceramic capacitors.

B) Voltage Stability

Class II type capacitor has poor voltage stability Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take for TDK C series X5R for example, its pressure voltage value is 16V or 25V; the package size is 0805, 1206 or 0603, the capacitance value is 10uF. The capacitor's voltage stability of different types of capacitor is as shown below:

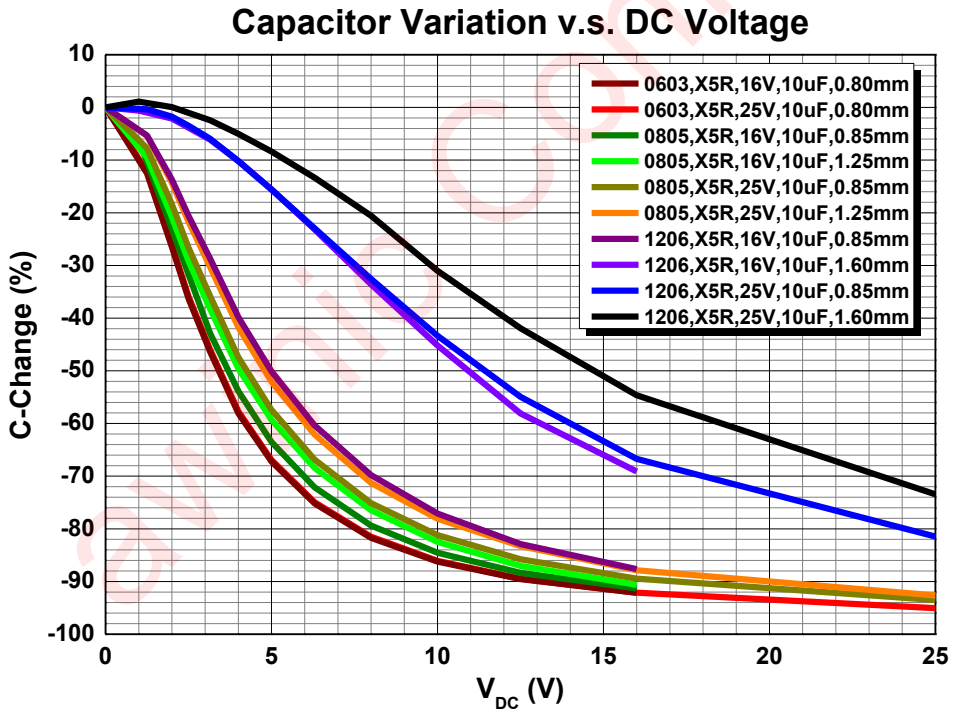


Figure 20 Different types of capacitive voltage stability

Among them, the space remaining value of different types of capacitors at V_{DC} = 8.5 V as shown in the figure 21:

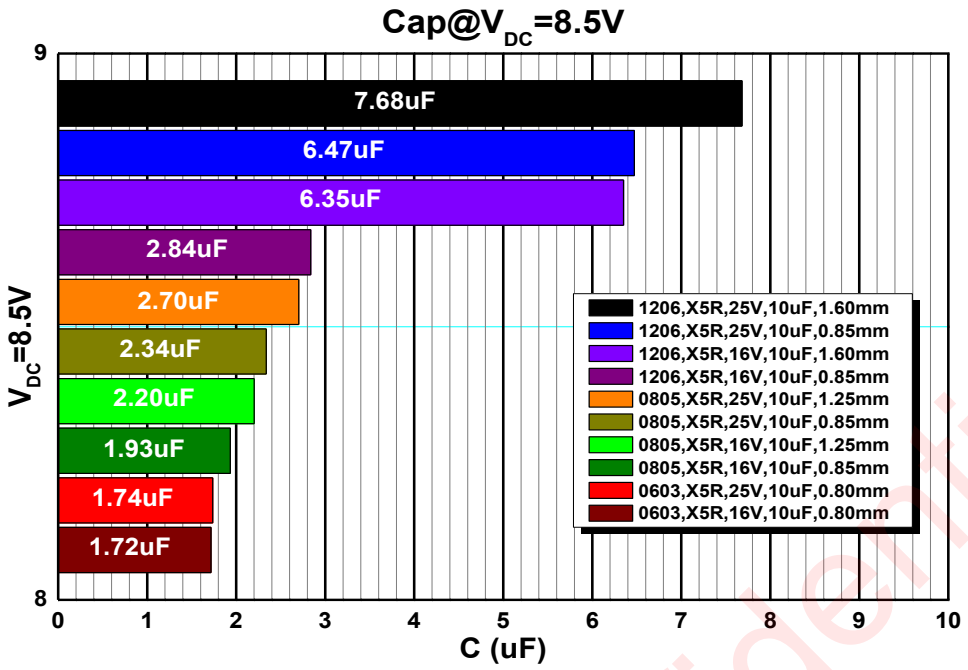


Figure 21 The space remaining value of different types of capacitors at V_{DC} = 8.5 V

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. the higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of smaller package size (0603) capacitor change affected by the pressure value is very small.

In AW87319 typical applications, it is necessary to ensure the output value of the capacitor Boost≥5uF when PVDD=8.5V. Take the above TDK capacitor for example; recommend the following capacitance combination as the Boost of the output capacitor:

model	value	material	size (mm^3)	rated voltage (V)	quantity	value@8.5V
C1608X5R1C106M080AB	10uF	X5R	1.60×0.80×0.80 (0603)	16	3	5.1uF
C1608X5R1E106M080AC	10uF	X5R	1.60×0.80×0.80 (0603)	25	3	5.2uF
C2012X5R1E106M125AB	10uF	X5R	2.00×1.25×1.25 (0805)	25	2	5.4uF
C3216X5R1C106M160AA	10uF	X5R	3.20×1.60×1.60 (1206)	16	1	6.4uF
C3216X5R1E106M085AC	10uF	X5R	3.20×1.60×0.85 (1206)	25	1	6.5uF

Notice that the analysis is only for TDK capacitors, when elected other manufacturers' capacitance, it still need to determine the type and quantity of the capacitors through the capacitor voltage stability data provided by the manufacturer. Different manufacturer's approximate specifications of the capacitor may still have some difference. Construing a different circumstance needs deducting in a different approach.

Input Capacitor-C_{in}（input high-pass cutoff frequency）

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. The input capacitors and input resistors form a high-pass filter with the corner frequency:

$$f_H(-3dB) = \frac{1}{2\pi \times R_{intotal} \times C_{in}}(Hz)$$

Setting the high-pass filter point high can block the 217Hz GSM noise coupled to inputs. Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise. Take typical application as an example, the input high-pass cutoff frequency is calculated as below:

$$f_H(-3dB) = \frac{1}{2\pi \times R_{intotal} \times C_{in}}(Hz) = \frac{1}{2\pi \times 9k\Omega \times 47nF}(Hz) = 376Hz$$

Supply Decoupling Capacitor（C_S）

The AW87319 is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the AW87319 is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

Output beads, capacitors, TVS

The AW87319 passed FCC and CE radiated emissions with no ferrite chip beads and capacitors. Use ferrite chip beads and capacitors if device near the EMI sensitive circuits and/or there are long leads from amplifier to speaker, placed as close as possible to the output pin.
In the class K mode, the output is a square wave signal, which causing switch current at the output capacitor, increasing static power consumption, and therefore output capacitor should not be too large, 0.1nF ceramic capacitors is recommended.

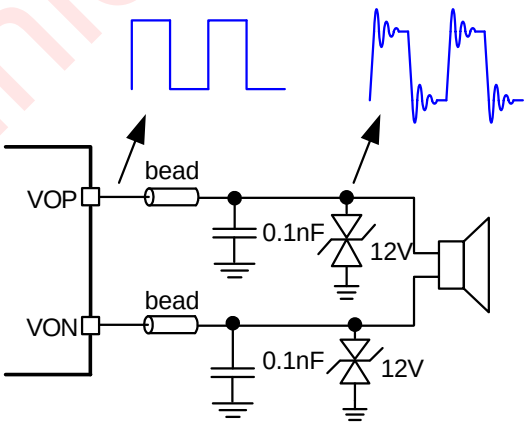


Figure 22 Ferrite Chip Bead and capacitor

Amplifier output is a square wave signal. The voltage across the capacitor will be much larger than the PVDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 16V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 16V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 16V capacitor, but quiescent current will increase.

Power amplifier output PWM signals of high voltage to PVDD voltage, voltage to 8.5 V, will produce some ringing after bead capacitor, resulting in higher peak voltage. Recommended choose the operating voltage of 12V TVS.

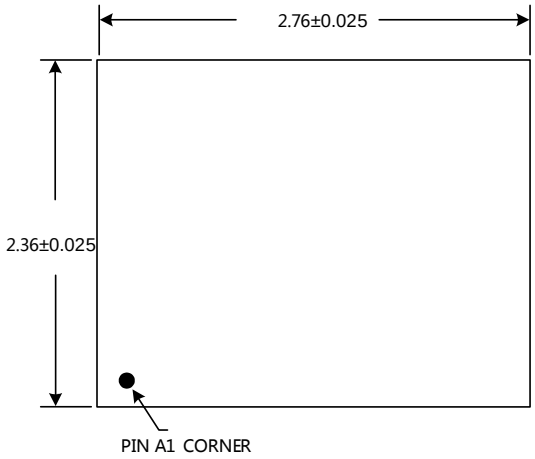
PCB AND DEVICE LAYOUT CONSIDERATION

In order to obtain excellent performance of AW87319, PCB layout must be carefully considered. The design consideration should follow the following principles:

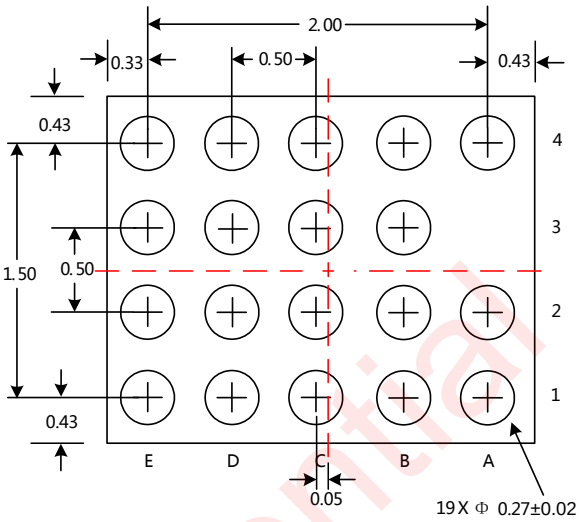
1. In AW87319 peripheral device layout, you first need to guarantee the Boost output capacitance close to PVDD pin.
2. Try to provide a separate short and thick power line to AW87319, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin.
3. The input capacitors and resistors should be close to AW87319 INN and INP input pin, the input line should be parallel to suppress noise coupling.
4. The beads and capacitor should be placed near to AW87319 VON and VOP pin. The output line from AW87319 to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.

PACKAGE DESCRIPTION

TOP VIEW



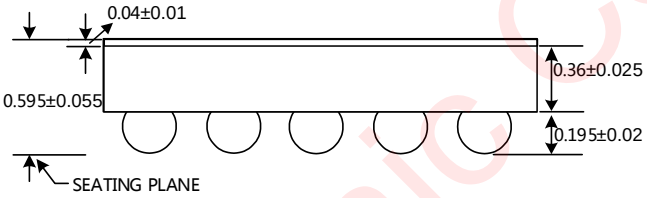
BOTTOM VIEW



CSP 19

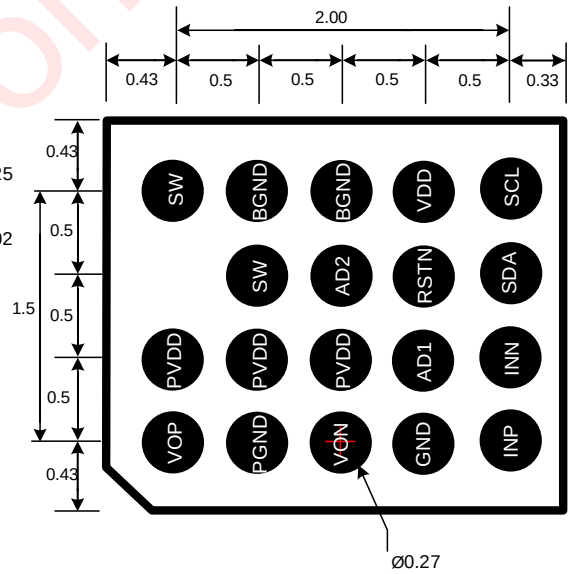
19 - Ball Wafer Level Chip Scale Package

SIDE VIEW



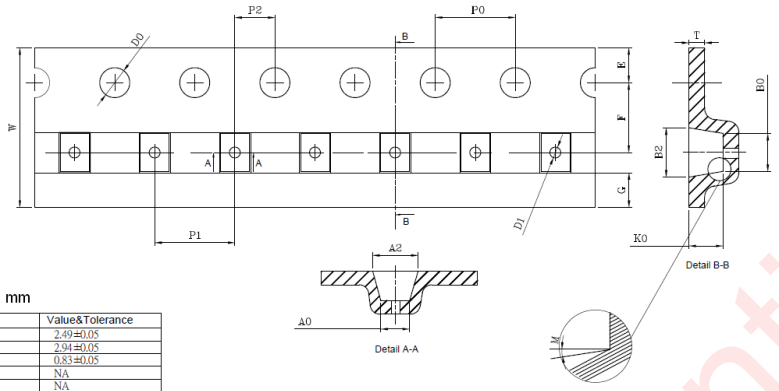
Unit: mm

LAND PATTERN



Tape Description

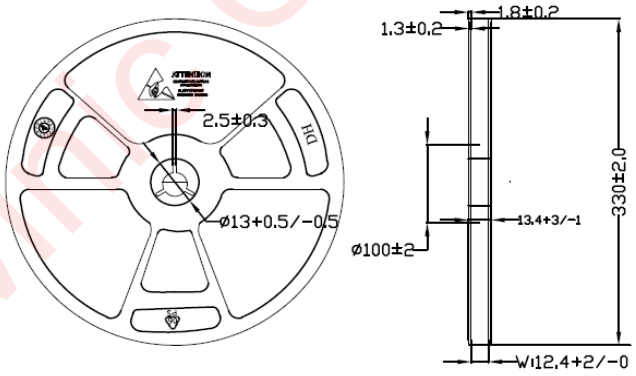
Carrier Tape



Unit: mm

Item	Value&Tolerance
A0	2.49±0.05
B0	2.94±0.05
K0	0.83±0.05
A2	NA
B2	NA
D0	1.50 +0.10/-0.00
D1	1.50 +0.25/-0.00
P0	4.00±0.10
P1	4.00±0.10
P2	2.00±0.05
E	1.75±0.10
F	5.50±0.05
G	NA
T	0.25±0.03
W	12.00 +0.30/-0.10
M	Max 5°

Reel

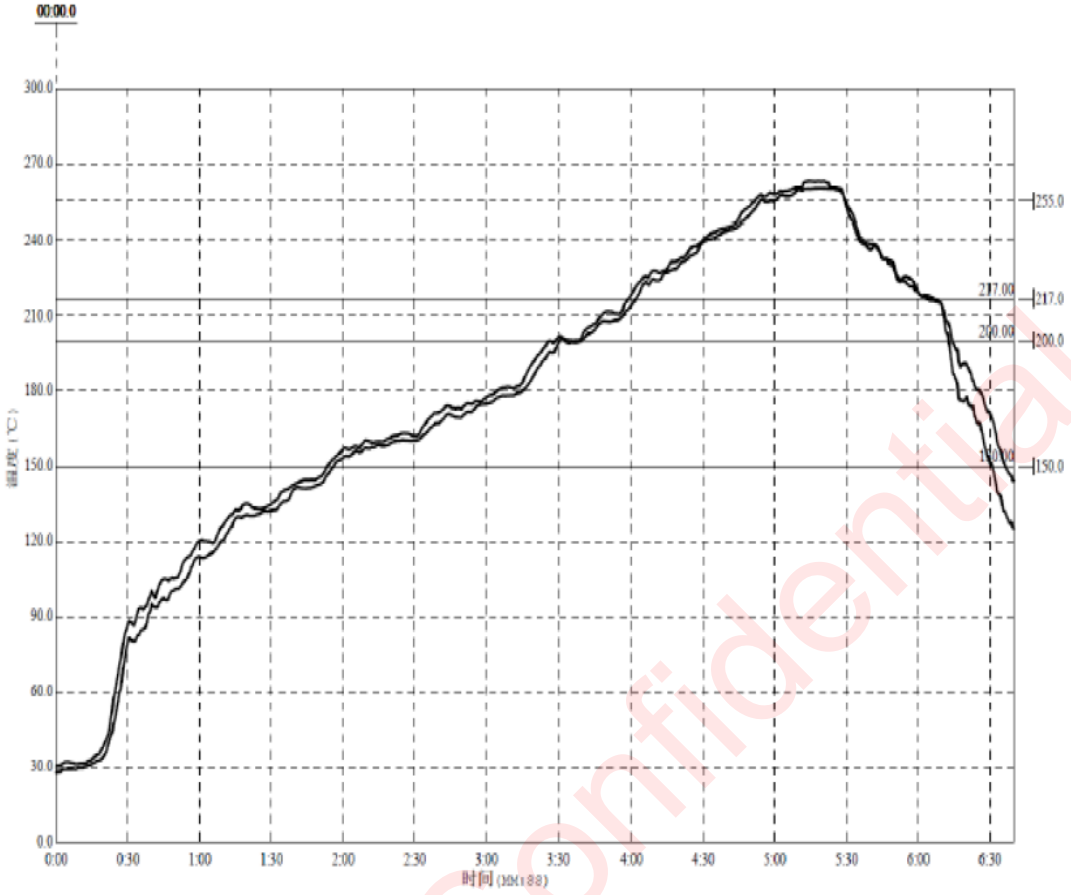


Note:

1. surface resistivity: 10^{5} to 10^{11} ohms/sq.
2. The colour of reel is deep blue.
3. Restriction criterion of hazardous substance for packing material follow GP-M001.

Unit： mm

Reflow Soldering curve



Reflow Note	Spec
Average ramp-up rate (217℃c to Peak)	Max. 3℃/sec
Time of Preheat temp.(from 150℃ to 200℃)	60-120sec
Time to be maintained above 217℃	60-150sec
Peak Temperature	>260℃
Time within 5℃ of actual peak temp	20-40sec.
Ramp-down rate	Max. 6℃/sec
Time from 25℃ to peak temp	Max. 8min.

VERSION INFORMATION

Version	Date	Description
V1.0	2015-11-30	AW87319CSR datasheet V1.0
V1.1	2016-11-10	Boost inductor Selection I_{L_PEAK} cannot be less than 3.5A modified to not less than 3.6A (page 26) Tape description increase the position description of pin1 (page 34) Add Reflow soldering curve (page35) Product information added MSL instructions (page3) “the SDA transmits a high level in ninth clock pulse” modify to “the SDA transmits a low level in ninth clock pulse” (page18) The functional block diagram add feedback loop (page4)
V1.2	2016-12-10	Add PVDD,SW,VON,VOP absolute maximum rating Add information about CDM Add Environmental Information
V1.3	2017-5-12	Update tape information and Add unit
V1.4	2020-4-25	Change negative PSRR to positive PSRR.

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