钍地半导体
Tudi Semiconductor

# Product Specification

## TUDI-SN65HVD3082E/ SN65HVD3085E/ SN65HVD3088E

Low power RS-485 transceiver

网址 www.sztdbdt.com

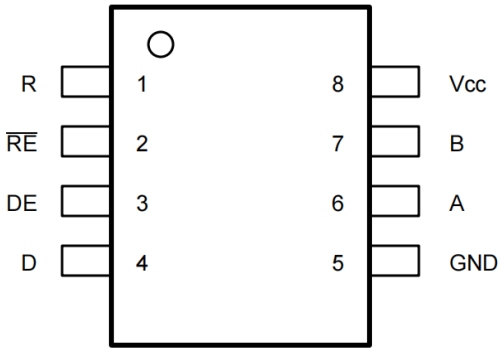
**用芯智造·卓越品质**

**semiconductor device manufacturer**

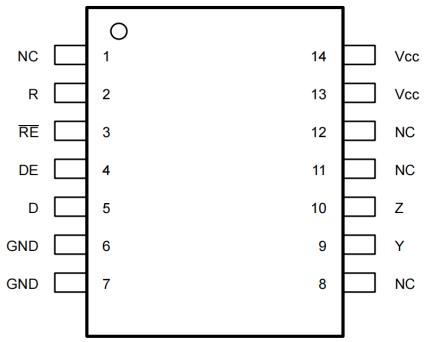
- Design
- research and development
- production
- and sales

## Features

●Complies with or exceeds TIA/EIA-485A standard requirements
●Low static power
– 0.3mA active mode
– 1nA in shutdown mode
● 1/8 unit load, up to 256 nodes on a single bus
●Up to 1kV bus pin ESD protection
● Industry-standard SN75176 package
● Fail-safe receiver (bus open, bus short, bus idle)
●Interference- power-up and power-down bus inputs and outputs




SOIC PDIP and VSSOP Packages, 8-Pin
(Top View)




SN65HVD3088E, NS Package, 14-pin
(Top View)

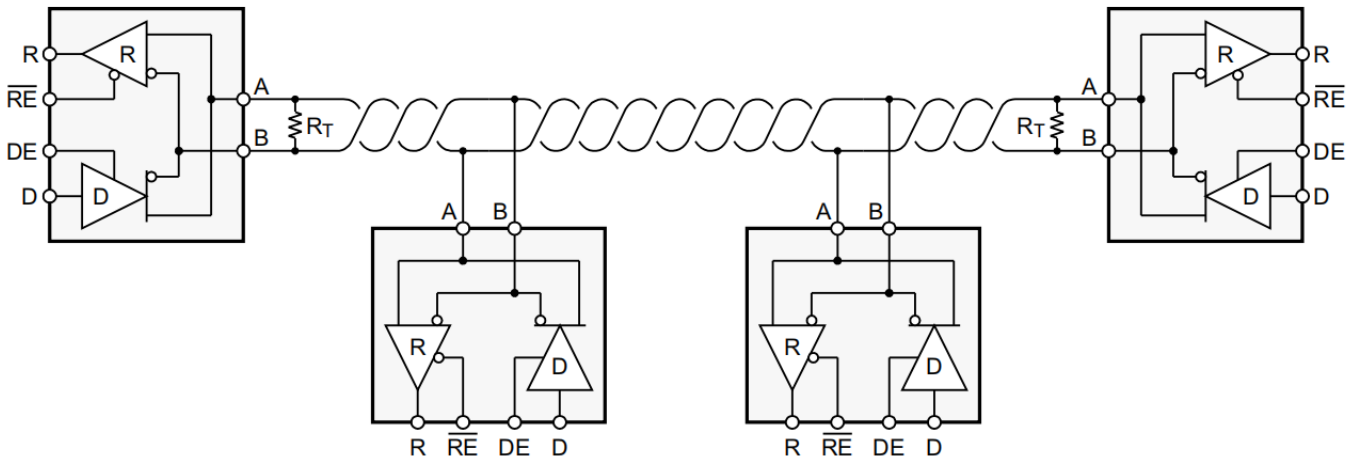
## Applications

●Energy metering networks
●Motor control
●Power inverters
● Industrial automation
● Building automation networks
●Battery-powered applications
● Tele equipment

## Description

The SNx5HVD308xE is a half-duplex transceiver designed specifically for RS-485 data bus networks. These are powered by a 5V supply and are fully compliant with the TIA/EIA-485A standard. By controlling the conversion time, these devices are suitable for transmitting over long twisted-pair cables. The SN65HVD3082E and SN75HVD3082E are optimized to support signal transmission rates up to 00kbps. The SN65HVD3085E is suitable for data transmission up to 1Mbps, while the SN65HVD3088 is suitable for applications requiring signal transmission rates up to 20Mbps.

These devices are designed to operate at very low supply currents (typically 0.3mA, excluding load). In the non-operating shutdown, the supply current can be reduced to a few nanoamps, making these devices an ideal choice for power-sensitive applications.
These devices feature a wide common-mode range and ESD protection levels, making them suitable for demanding applications such as smart meter networks, electrical inverters, status and command signals on telecom racks, wired chassis interconnects, and industrial automation where noise immunity is critical. These devices comply with the industry-standard dimensions of SN75176 devices. The power-on reset circuit keeps the outputs in a highimpedance state until the supply voltage stabilizes. The thermal shutdown function protects the devices from damage caused by system failures.SN75HVD3082E features an temperature range of 0°C to 70°C, while SN65HVD30xE features an operating temperature range of －40°C to 5°C. The D package version of SN65HVD3082E features an operating temperature range of －40°C to 105°.




简化原理图

表 5-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| R | 1 | Digital output | Receive data output |
| $\overline{RE}$ | 2 | Digital input | Receiver enable, active low |
| DE | 3 | Digital input | Driver enable, active high |
| D | 4 | Digital input | Driver data input |
| GND | 5 | Reference potential | Local device ground |
| A | 6 | Bus input/output | Driver output or receiver input (complementary to B) |
| B | 7 | Bus input/output | Driver output or receiver input (complementary to A) |
| $V_{CC}$ | 8 | Supply | 4.5-V to 5.5-V supply |

表 5-2. Pin Functions, NS Package

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| NC | 1, 8 | No Connect | Not Electrically Connected |
| R | 2 | Digital output | Receive data output |
| $\overline{RE}$ | 3 | Digital input | Receiver enable, active low |
| DE | 4 | Digital input | Driver enable, active high |
| D | 5 | Digital input | Driver data input |
| GND | 6, 7 | Reference potential | Local device ground |
| Y | 9 | Bus I/O | Differential transceiver input and output (complementary to Z) |
| Z | 10 | Bus I/O | Differential transceiver input and output (complementary to Y) |
| NC | 12 | No Connect | Not Electrically Connected |
| NC | 11 | No Connect | Not Electrically Connected |
| $V_{CC}$ | 13,14 | Supply | 4.5-V to 5.5-V supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ | –0.5 | 7 | V |
| Voltage at A or B | –9 | 14 | V |
| Voltage at any logic pin | –0.3 | $V_{CC}$ + 0.3 | V |
| Receiver output current | –24 | 24 | mA |
| Voltage input, transient pulse, A and B, through 100 Ω (see 图 7-13) | –50 | 50 | V |
| Junction Temperature, $T_J$ | | 170 | °C |
| Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratingss* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | Bus pins and GND | ±15000 | V |
| | | All pins | ±4000 | |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | | ±1000 | |
| | Electrical Fast Transient/Burst, A, B, and GND(3) | | ±4000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested in accordance with IEC 61000-4-4.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted(1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.5 | | 5.5 | V |
| Voltage at any bus terminal (separately or common mode) , $V_I$ | | –7 | | 12 | V |
| High-level input voltage (D, DE, or $\overline{RE}$ inputs), $V_{IH}$ | | 2 | | $V_{CC}$ | V |
| Low-level input voltage (D, DE, or $\overline{RE}$ inputs), $V_{IL}$ | | 0 | | 0.8 | V |
| Differential input voltage, $V_{ID}$ | | –12 | | 12 | V |
| Output current, $I_O$ | Driver | –60 | | 60 | mA |
| | Receiver | –8 | | 8 | |
| Differential load resistance, $R_L$ | | 54 | 60 | | Ω |
| Signaling rate, $1/t_{UI}$ | SN65HVD3082E, SN75HVD3082E | | | 0.2 | Mbps |
| | SN65HVD3085E | | | 1 | |
| | SN65HVD3088E | | | 20 | |
| Operating free-air temperature, $T_A$ | SN65HVD3082E (D package) | –40 | | 105 | °C |
| | SN65HVD3082E (DGK and P packages), SN65HVD3085E, SN65HVD3088E | –40 | | 85 | |
| | SN75HVD3082E | 0 | | 70 | |
| Junction temperature, $T_J$ | | –40 | | 130 | °C |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## 6.4 Thermal Information, SN65HVD308xE

| THERMAL METRIC(1) | | SN65HVD3085E, SN65HVD3088E | | SN65HVD3088E | SN65HVD3088E | UNIT |
|---|---|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | P (PDIP) | NS (SO) | |
| | | 8 PINS | 8 PINS | 8 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 116.7 | 137.8 | 84.3 | 88.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.3 | 31.2 | 65.4 | 46.13 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 63.4 | 71.7 | 62.1 | 49.12 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.8 | 0.6 | 31.3 | 14.17 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 62.6 | 70.5 | 60.4 | 48.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Thermal Information, SNx5HVD3082E

| THERMAL METRIC(1) | | SN65HVD3082E, SN75HVD3082E | | SN65HVD3082E | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | P (PDIP) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 114.4 | 142.2 | 88.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 55.1 | 35.8 | 65.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 61.6 | 75.6 | 69.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.8 | 0.8 | 35.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 60.8 | 74.8 | 64.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.6 Electrical Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\|V_{OD}\|$ | Differential output voltage | $I_O$ = 0, No Load | 3 | 4.3 | | V |
| | | $R_L$ = 54 Ω (see 图 7-1) | 1.5 | 2.3 | | |
| | | $R_L$ = 100 Ω | 2 | | | |
| | | $V_{TEST}$ = –7 V to 12 V (see 图 7-2) | 1.5 | | | |
| $\Delta\|V_{OD}\|$ | Change in magnitude of differential output voltage | See 图 7-1 and 图 7-2 | –0.2 | 0 | 0.2 | V |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | See 图 7-3 | 1 | 2.6 | 3 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage | | –0.1 | 0 | 0.1 | |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | See 图 7-3 | | 500 | | mV |
| $I_{OZ}$ | High-impedance output current | See receiver input currents in Electrical Characteristics: Receiver | | | | |
| $I_I$ | Input current | D, DE | –100 | | 100 | μA |
| $I_{OS}$ | Short-circuit output current | –7 V ≤ $V_O$ ≤ 12 V (see 图 7-7 ) | –250 | | 250 | mA |

(1) All typical values are at 25°C and with a 5-V supply.

## 6.7 Electrical Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going differential input threshold voltage | $I_O$ = –8 mA | | –85 | –10 | mV |
| $V_{IT-}$ | Negative-going differential input threshold voltage | $I_O$ = 8 mA | –200 | –115 | | mV |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+}$ – $V_{IT-}$) | | | 30 | | mV |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 200 mV, $I_{OH}$ = –8 mA (see 图 7-8) | 4 | 4.6 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –200 mV, $I_O$ = 8 mA (see 图 7-8) | | 0.15 | 0.4 | V |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = 0 or $V_{CC}$, $\overline{RE}$ = $V_{CC}$ | –1 | | 1 | μA |
| $I_I$ | Bus input current | $V_{IH}$ = 12 V, $V_{CC}$ = 5 V | | 0.04 | 0.1 | mA |
| | | $V_{IH}$ = 12 V, $V_{CC}$ = 0 V | | 0.06 | 0.125 | |
| | | $V_{IH}$ = –7 V, $V_{CC}$ = 5 V | –0.1 | –0.04 | | |
| | | $V_{IH}$ = –7 V, $V_{CC}$ = 0 V | –0.05 | –0.03 | | |
| $I_{IH}$ | High-level input current, ( $\overline{RE}$) | $V_{IH}$ = 2 V | –60 | –30 | | μA |
| $I_{IL}$ | Low-level input current, ( $\overline{RE}$) | $V_{IL}$ = 0.8 V | –60 | –30 | | μA |
| $C_{diff}$ | Differential input capacitance | $V_I$ = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V | | 7 | | pF |

(1) All typical values are at 25°C and with a 5-V supply.

## 6.8 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Driver and receiver enabled | D at $V_{CC}$ or open, DE at $V_{CC}$, $\overline{RE}$ at 0 V, No load | | | 425 | 900 | μA |
| | Driver enabled, receiver disabled | D at $V_{CC}$ or open, DE at $V_{CC}$, $\overline{RE}$ at $V_{CC}$, No load | | | 330 | 600 | μA |
| | Receiver enabled, driver disabled | D at $V_{CC}$ or open, DE at 0 V, $\overline{RE}$ at 0 V, No load | | | 300 | 600 | μA |
| | Driver and receiver disabled | D at $V_{CC}$ or open, DE at 0 V, $\overline{RE}$ at $V_{CC}$ | | | 0.001 | 2 | μA |
| $P_{(AVG)}$ | Average power dissipation | Input to D is a 50% duty cycle square wave at max specified signal rate $R_L$ = 54 Ω $V_{CC}$ = 5.5 V, $T_J$ = 130°C | ALL HVD3082E | | | 203 | mW |
| | | | ALL HVD3085E | | | 205 | |
| | | | ALL HVD3088E | | | 276 | |

(1) All typical values are at 25°C and with a 5-V supply.

## 6.9 Switching Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output | $R_L$ = 54 Ω, $C_L$ = 50 pF (see 图 7-4) | HVD3082E | | 700 | 1300 | ns |
| | | | HVD3085E | | 150 | 500 | |
| | | | HVD3088E | | 12 | 20 | |
| $t_r$ $t_f$ | Differential output signal rise time Differential output signal fall time | $R_L$ = 54 Ω, $C_L$ = 50 pF (see 图 7-4) | HVD3082E | 500 | 900 | 1500 | ns |
| | | | HVD3085E | | 200 | 300 | |
| | | | HVD3088E | | 7 | 15 | |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | $R_L$ = 54 Ω, $C_L$ = 50 pF (see 图 7-4) | HVD3082E | | 20 | 200 | ns |
| | | | HVD3085E | | 5 | 50 | |
| | | | HVD3088E | | 1.4 | 2 | |
| $t_{PZH}$ $t_{PZL}$ | Propagation delay time, high-impedance-to-high-level output Propagation delay time, high-impedance-to-low-level output | $R_L$ = 110 Ω, $\overline{RE}$ at 0 V (see 图 7-5 and 图 7-6) | HVD3082E | | 2500 | 7000 | ns |
| | | | HVD3085E | | 1000 | 2500 | |
| | | | HVD3088E | | 13 | 30 | |
| $t_{PHZ}$ $t_{PLZ}$ | Propagation delay time, high-level-to-high-impedance output Propagation delay time, low-level-to-high-impedance output | $R_L$ = 110 Ω, $\overline{RE}$ at 0 V (see 图 7-5 and 图 7-6) | HVD3082E | | 80 | 200 | ns |
| | | | HVD3085E | | 60 | 100 | |
| | | | HVD3088E | | 12 | 30 | |
| $t_{PZH(SHDN)}$ $t_{PZL(SHDN)}$ | Propagation delay time, shutdown-to-high-level output Propagation delay time, shutdown-to-low-level output | $R_L$ = 110 Ω, $\overline{RE}$ at $V_{CC}$ (see 图 7-5) | HVD3082E | | 3500 | 7000 | ns |
| | | | HVD3085E | | 2500 | 4500 | |
| | | | HVD3088E | | 1600 | 2600 | |

## 6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 15 pF (see 图 7-9) | HVD3082E HVD3085E | | 75 | 200 | ns |
| | | | HVD3086E | | | 100 | |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | HVD3082E HVD3085E | | 79 | 200 | ns |
| | | | HVD3088E | | | 100 | |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | | HVD3082E HVD3085E | | 4 | 30 | ns |
| | | | HVD3088E | | | 10 | |
| $t_r$ | Output signal rise time | $V_{ID}$ = –1.5 V to 1.5 V, $C_L$ = 15 pF (see 图 7-9) | | | 1.5 | 3 | ns |
| $t_f$ | Output signal fall time | | | | 1.8 | 3 | |
| $t_{PZH}$ | Output enable time to high level | $C_L$ = 15 pF, DE at 3 V (see 图 7-10 and 图 7-11) | HVD3082E HVD3085E | | 5 | 50 | ns |
| | | | HVD3088E | | | 30 | |
| $t_{PZL}$ | Output enable time to low level | | HVD3082E HVD3085E | | 10 | 50 | ns |
| | | | HVD3088E | | | 30 | |
| $t_{PHZ}$ | Output enable time from high level | | HVD3082E HVD3085E | | 5 | 50 | ns |
| | | | HVD3088E | | | 30 | |
| $t_{PLZ}$ | Output disable time from low level | | HVD3082E HVD3085E | | 8 | 50 | ns |
| | | | HVD3088E | | | 30 | |
| $t_{PZH(SHDN)}$ | Propagation delay time, shutdown-to-high-level output | $C_L$ = 15 pF, DE at 0 V, (see 图 7-12) | | | 1600 | 3500 | ns |
| $t_{PZL(SHDN)}$ | Propagation delay time, shutdown-to-low-level output | | | | 1700 | 3500 | |

## 7 Parameter Measurement Information

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle. $Z_O$ = 50 Ω (unless otherwise specified).

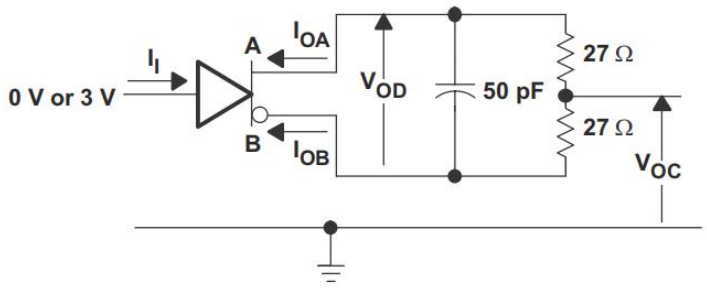



**图 7-1. Driver Test Circuit, $V_{OD}$ and $V_{OC}$ Without Common-Mode Loading**

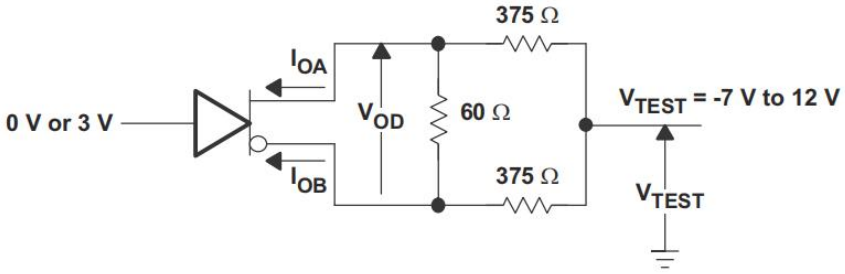



**图 7-2. Driver Test Circuit, $V_{OD}$ With Common-Mode Loading**

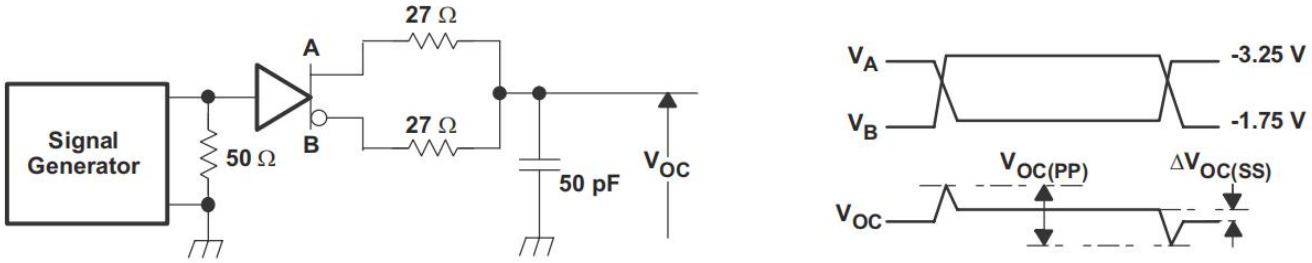



**图 7-3. Driver $V_{OC}$ Test Circuit and Waveforms**

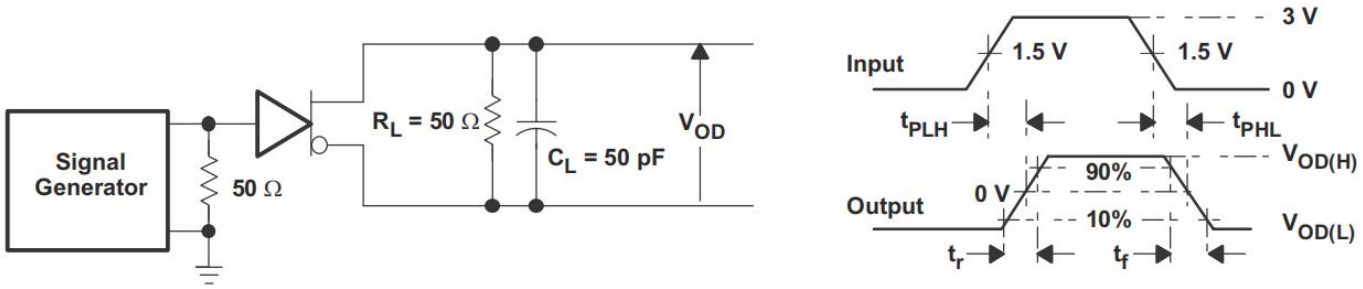



**图 7-4. Driver Switching Test Circuit and Waveforms**

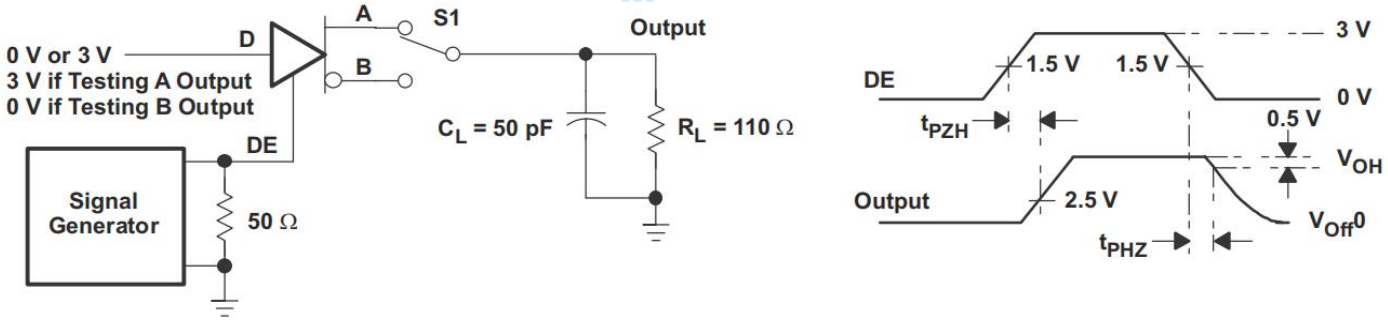



图 7-5. Driver Enable and Disable Test Circuit and Waveforms, High Output

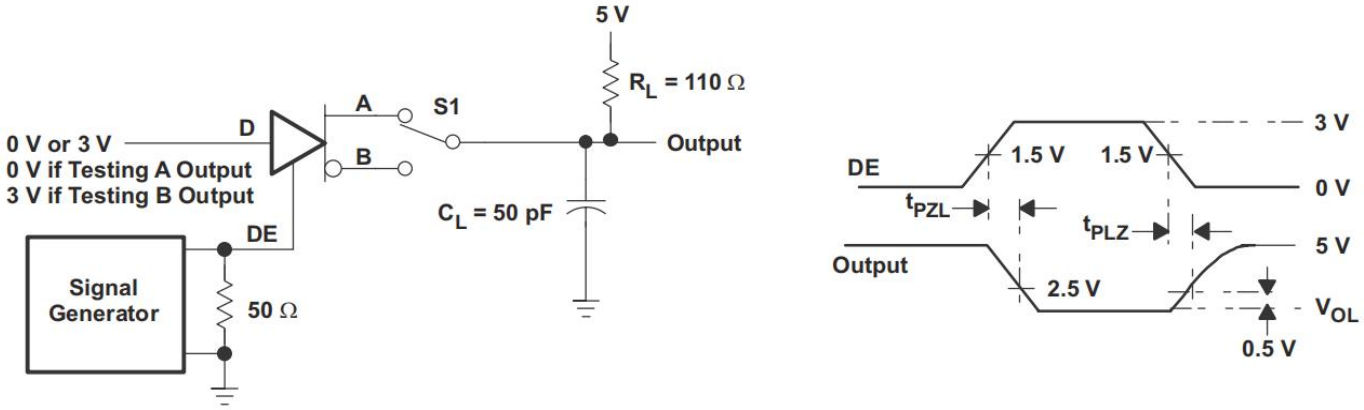



图 7-6. Driver Enable and Disable Test Circuit and Waveforms, Low Output

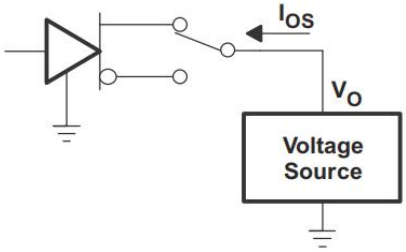



图 7-7. Driver Short-Circuit

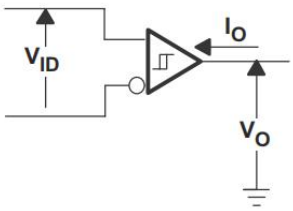
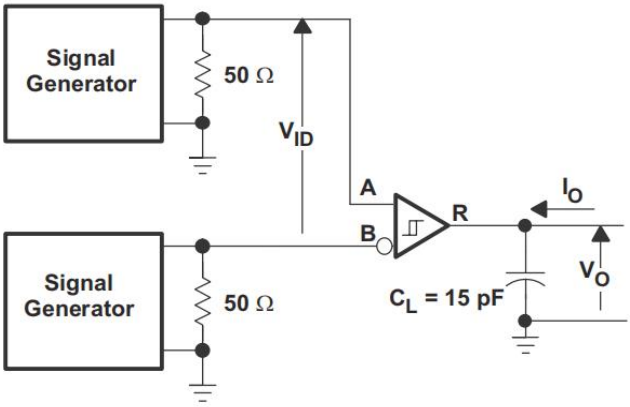



图 7-8. Receiver Switching Test Circuit and Waveforms



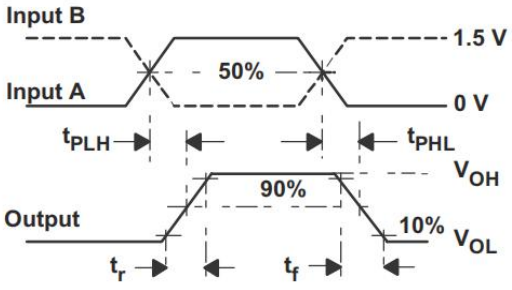




图 7-9. Receiver Switching Test Circuit and Waveforms

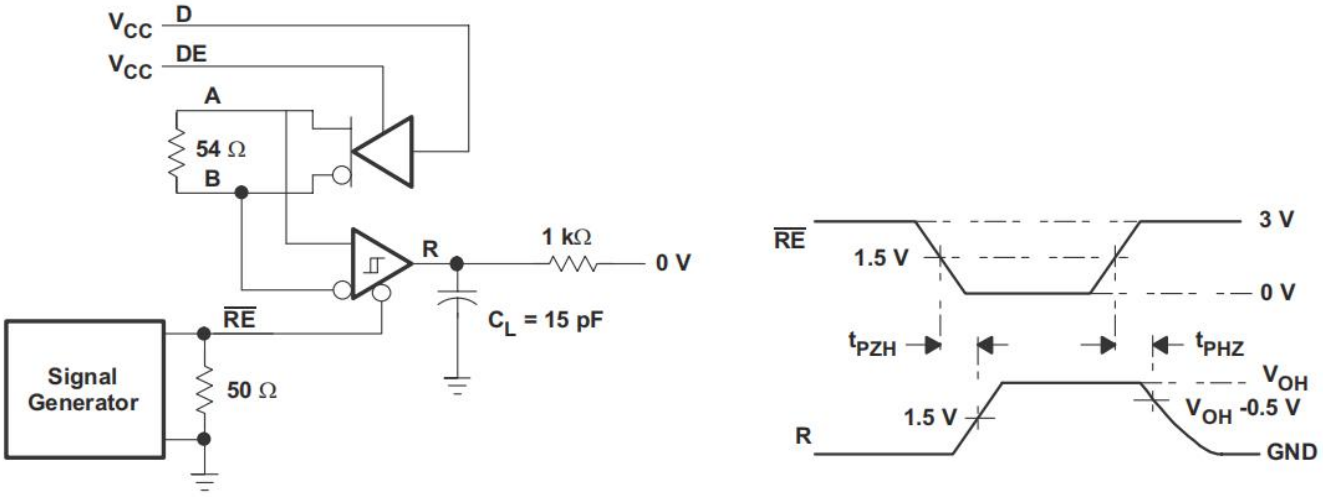



**图 7-10. Receiver Enable and Disable Test Circuit and Waveforms, Data Output High**

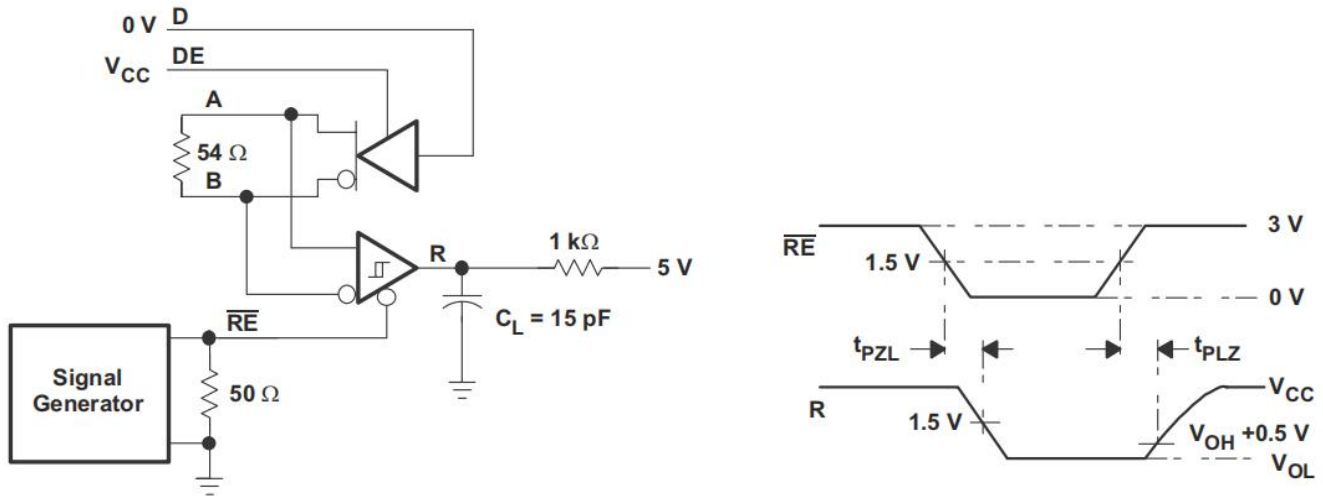



**图 7-11. Receiver Enable and Disable Test Circuit and Waveforms, Data Output Low**

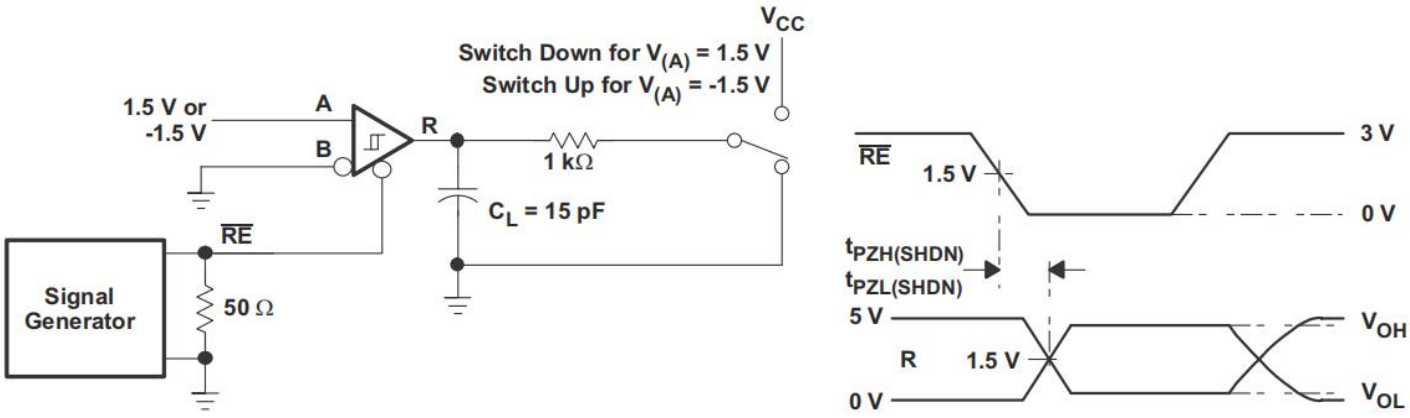



**图 7-12. Receiver Enable From Shutdown Test Circuit and Waveforms**

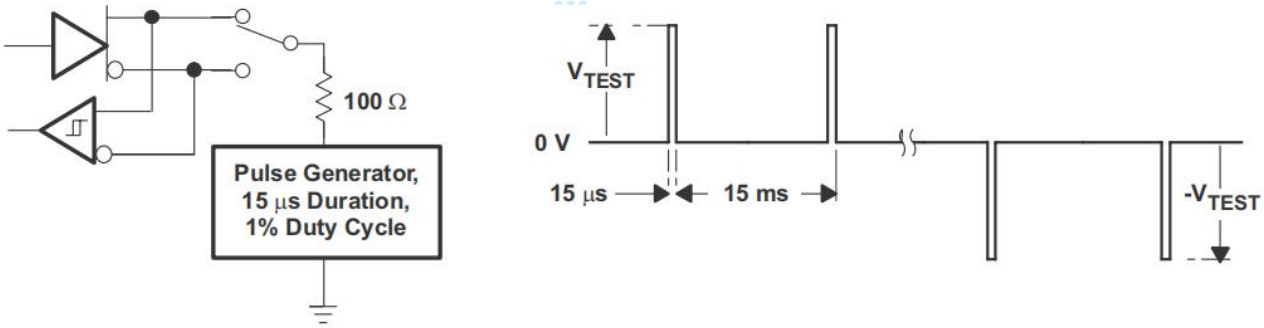



图 7-13. Test Circuit and Waveforms, Transient Overvoltage Test

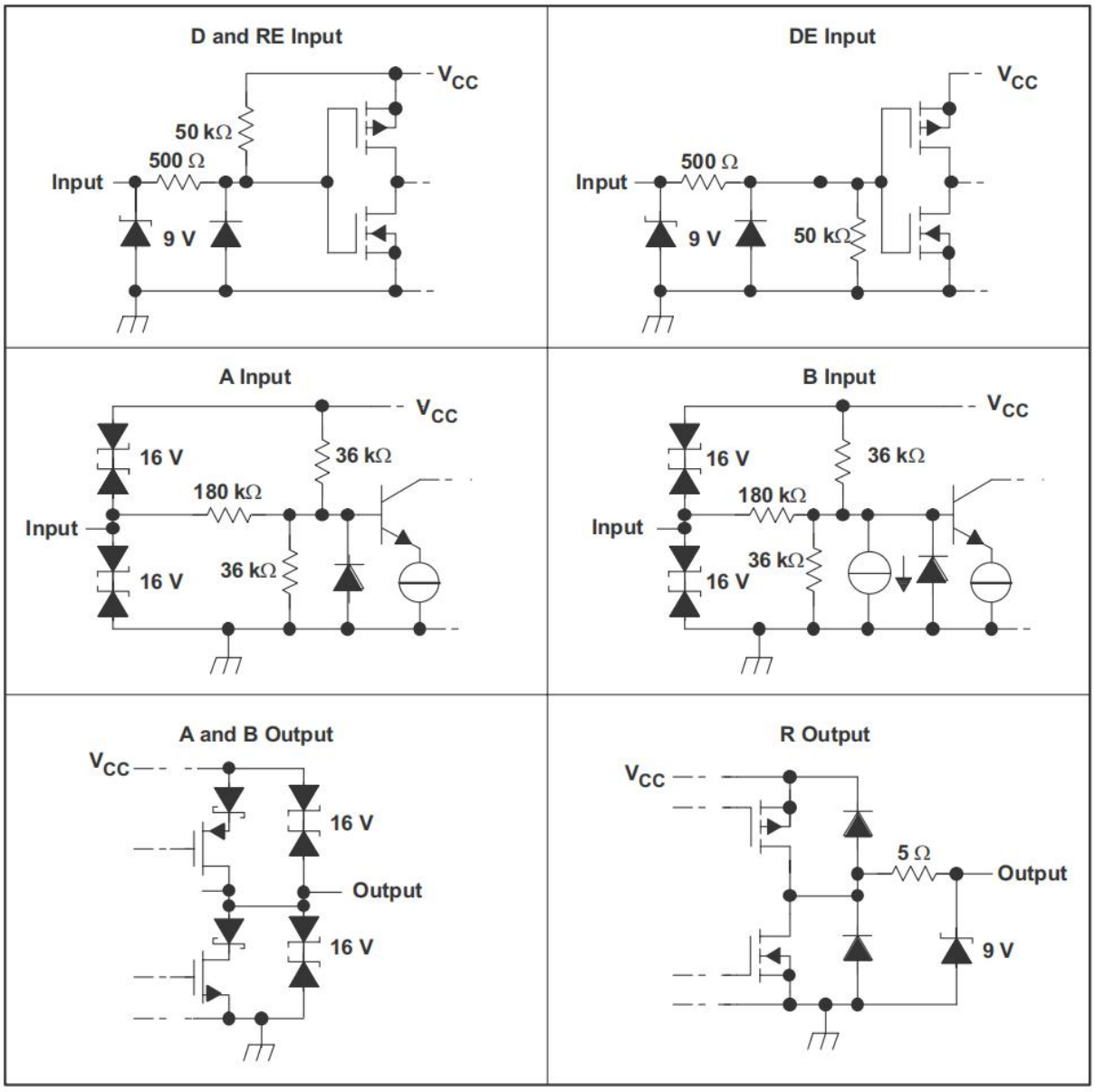


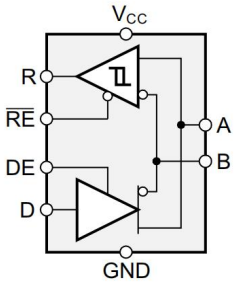

图 7-14. Equivalent Input and Output Schematic Diagrams

# 8 Detailed Description

## 8.1 Overview

The SNx5HVD308xE family of half-duplex RS-485 transceivers is suitable for data transmission at rates up to 200 kbps (for SN65HVD3082E and SN75HVD3082E), 1 Mbps (for SN65HVD3085E), or 20 Mbps (for SN65HVD3088E) over controlled-impedance transmission media (such as twisted-pair cabling). Up to 256 units of SNx5HVD308xE may share a common RS-485 bus due to the family's low bus input currents. The devices also feature a high degree of ESD protection and typical standby current consumption of 1 nA.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

The SNx5HVD308xE provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit fail-safe conditions. It features a typical hysteresis of 30 mV in order to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

The devices protect themselves against damage due to overtemperature conditions, through the use of a thermal shutdown feature. Thermal shutdown is entered at 165°C (nominal) and causes the device to enter a low-power state with high-impedance outputs.

## 8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and $V_{OD}$ is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to $V_{CC}$, thus, when left open while the driver is enabled, output A turns high and B turns low.

**表 8-1. Driver Function Table**

| INPUT | ENABLE(1) | OUTPUTS(1) | | FUNCTION |
|---|---|---|---|---|
| D | DE | A | B | |
| H | H | H | L | Actively drive bus High |
| L | H | L | H | Actively drive bus Low |
| X | L | Z | Z | Driver disabled |
| X | OPEN | Z | Z | Driver disabled by default |
| OPEN | H | H | L | Actively drive bus High by default |

(1) H = high level, L = low level, Z = high impedance, X = irrelevant

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, $V_{IT+}$, the receiver output, R, turns high. When $V_{ID}$ is negative and lower than the negative input threshold, $V_{IT-}$, the receiver output, R, turns low. If $V_{ID}$ is between $V_{IT+}$ and $V_{IT-}$ the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of $V_{ID}$ are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

**表 8-2. Receiver Function Table**

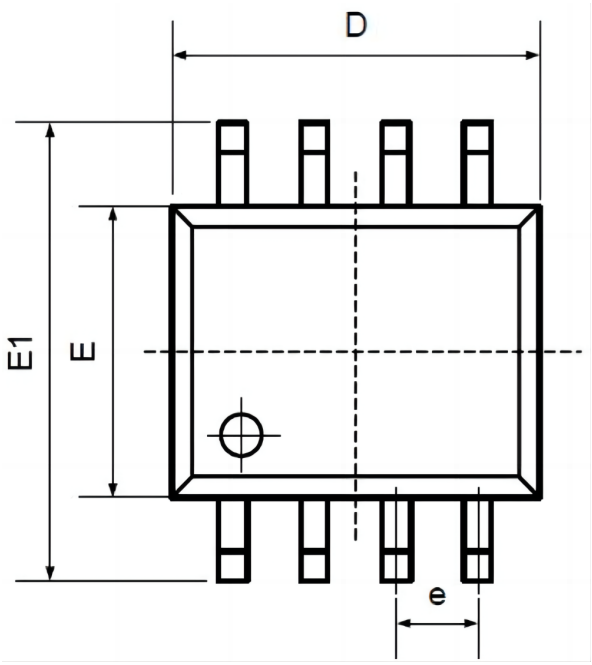
| DIFFERENTIAL INPUT | ENABLE (1) | OUTPUT(1) | FUNCTION |
|---|---|---|---|
| $V_{ID} = V_A - V_B$ | $\overline{RE}$ | R | |
| $V_{IT+} < V_{ID}$ | L | H | Receive valid bus High |
| $V_{IT-} < V_{ID} < V_{IT+}$ | L | ? | Indeterminate bus state |
| $V_{ID} < V_{IT-}$ | L | L | Receive valid bus Low |
| X | H | Z | Receiver disabled |
| X | OPEN | Z | Receiver disabled by default |
| Open-circuit bus | L | H | Fail-safe high output |
| Short-circuit bus | L | H | Fail-safe high output |
| Idle (terminated) bus | L | H | Fail-safe high output |

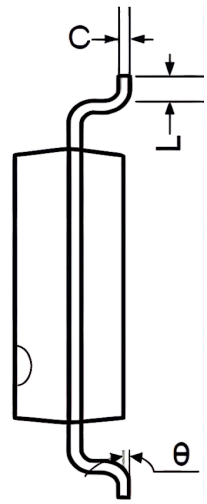
(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

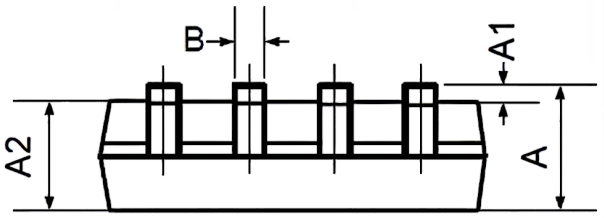
# Order information

| Order Number | Package | Package Quantity | Marking On The park |
|---|---|---|---|
| SN65HVD3082EDGKR-TUDI | MSOP8 | Tape,Reel,2500 | SN65HVD3082EDGKR |
| SN65HVD3082EDR-TUDI | SOP8 | Tape,Reel,2500 | SN65HVD3082EDR |
| SN65HVD3085EDR-TUDI | SOP8 | Tape,Reel,2500 | SN65HVD3085EDR |
| SN65HVD3088EDR-TUDI | SOP8 | Tape,Reel,2500 | SN65HVD3088EDR |

# Package SOP8

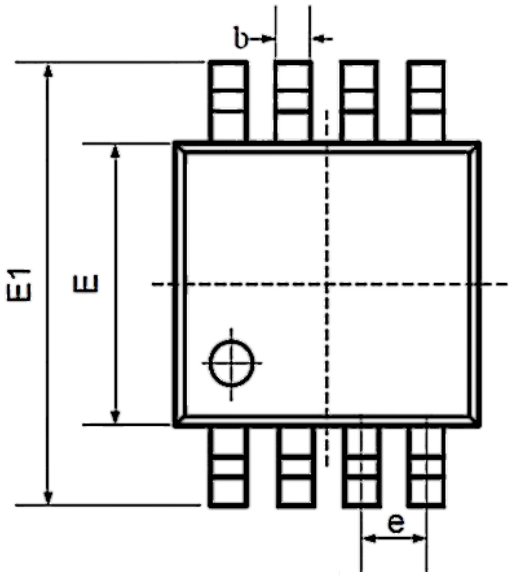


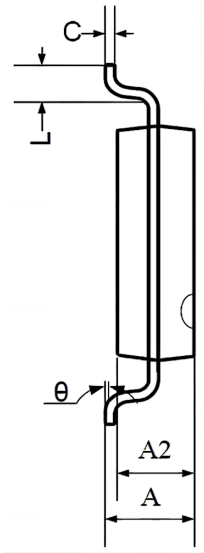



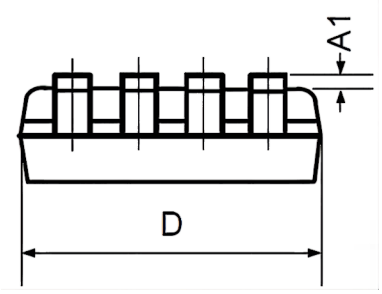




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| B | 0.330 | 0.510 | 0.013 | 0.020 |
| C | 0.190 | 0.250 | 0.007 | 0.010 |
| D | 4.780 | 5.000 | 0.188 | 0.197 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.300 | 0.228 | 0.248 |
| e | 1.270TYP | | 0.050TYP | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

# Package MSOP8




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.800 | 1.200 | 0.031 | 0.047 |
| A1 | 0.000 | 0.200 | 0.000 | 0.008 |
| A2 | 0.760 | 0.970 | 0.030 | 0.038 |
| b | 0.30 TYP | | 0.012 TYP | |
| C | 0.15 TYP | | 0.006 TYP | |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| e | 0.65 TYP | | 0.026 TYP | |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 4.700 | 5.100 | 0.185 | 0.201 |
| L | 0.410 | 0.650 | 0.016 | 0.026 |
| θ | 0° | 6° | 0° | 6° |

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