PI3HDX511F

Utra-Low Power HDMI1.4b 3.4Gbps Redriver for Sink/Source Application

General Features

- **Ultra-low power Low-jitter HDMI 1.4b compliant Redriver**
- **Dual-mode DisplayPort Level Shifter/Redriver with pin stripping option**
- **Operation up to 3.4 Gbps per lane (340MHz pixel clock)**
- **Sink-side application support with TMDS Data & Clock pin swap and high EQ configuration options**
- **4K Ultra-HD, 3D Video formats (1080p, 1080i, 720p), 48-bit per pixel Deep Color support**
- **Ultra-low standby current 2uA with DDC passive switch mode**
- **Flexible 6 steps input equalization control steps: 2.5dB, 5dB, 7.5 dB for short cable range or 5dB, 10dB, 15 dB for long cable application.**
- **Pre-emphasis output driving with 3-step setting: 0dB, 1.5dB, 2.5 dB**
- **Automatic output squelch and/or HPD modes for low power management with no signal input condition**
- **Selectable Active DDC buffer mode for long cable application**
- **Single(3.3V) or Dual(3.3/1.5V) power supply with built-in LDO bypass function.**
- **Integrated ESD protection on I/O pins for 8kV contact per IEC61000-4-2, level 4 and 8kV HBM**
- **40-pin TQFN(ZL40) 3x6mm package**

Description

PI3HDX511F is a ultra-low power HDMI 1.4b redriver and dual-mode DisplayPort level shifter upto 3.4Gbps data rate with 48-bpp Deep Color support.

In the mobile platforms, extending battery hours have been one of the most challenges for system designers. PI3HDX511F has rich power saving features to extend battery life including 2uA Stand-by current, LDO disable pins, Active/Passive DDC switch, Output squelch, HPD (Hot plug Detect) detection.

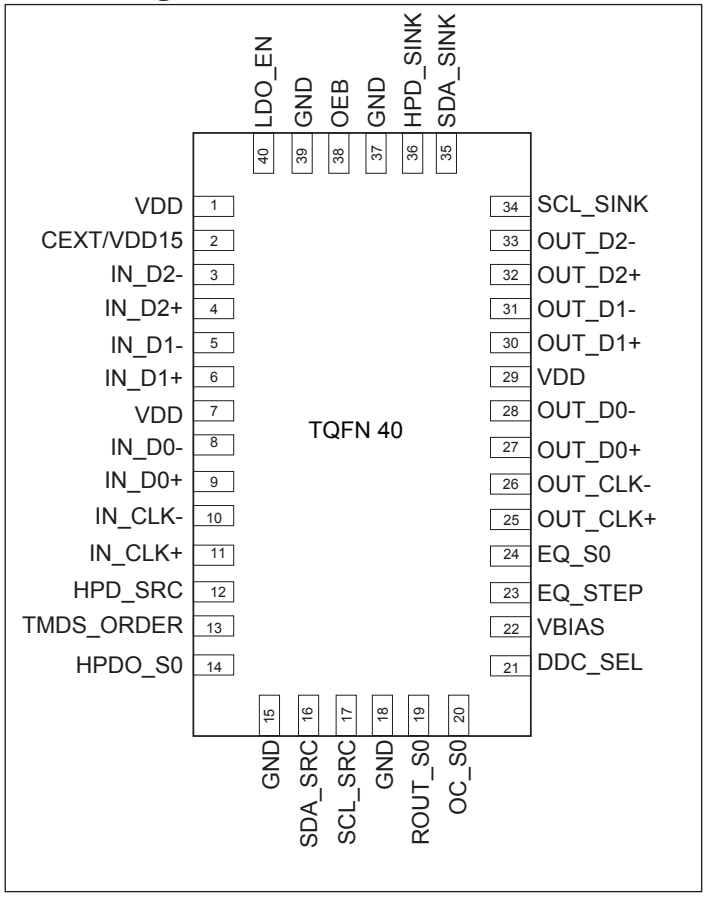
PI3HDX511F can support both source and sink side system application. For Sink side (Recepticle) application, it supports 6-step input EQ adjustment, Data/Clock pin order swap, Double termination / Open-drain outputs.

Main applications are Personal computers, Display monitors, Docking and related PC/Video devices.

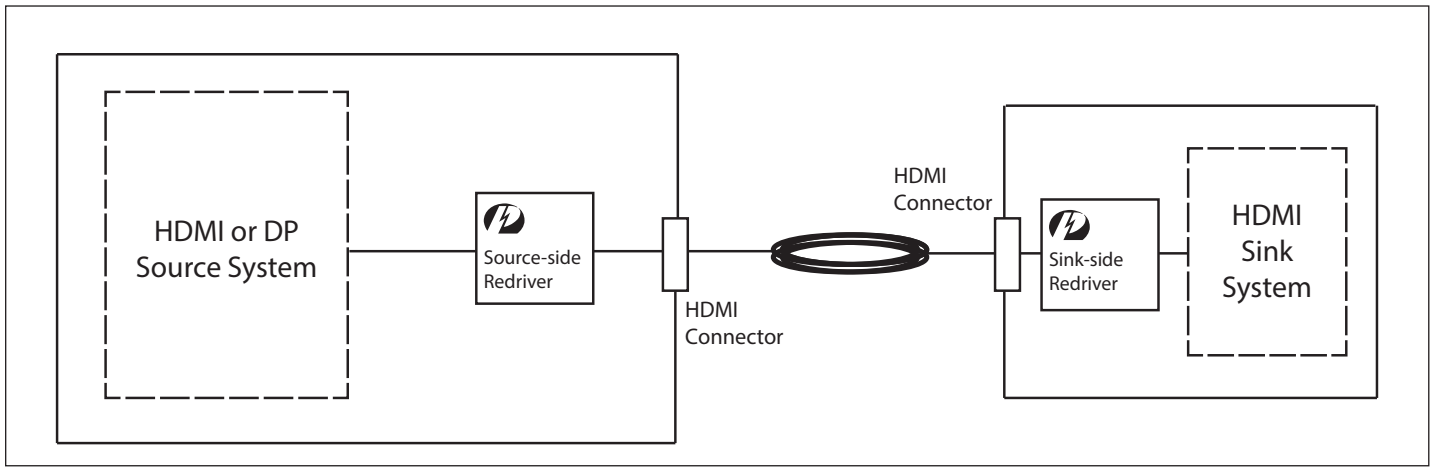
Application

- Notebook/Desktop computers
- Displays, Monitor
- A/V receivers, Set Top Box, Video Players
- Dongles, Repeaters and Switch boxes
- Embedded systems

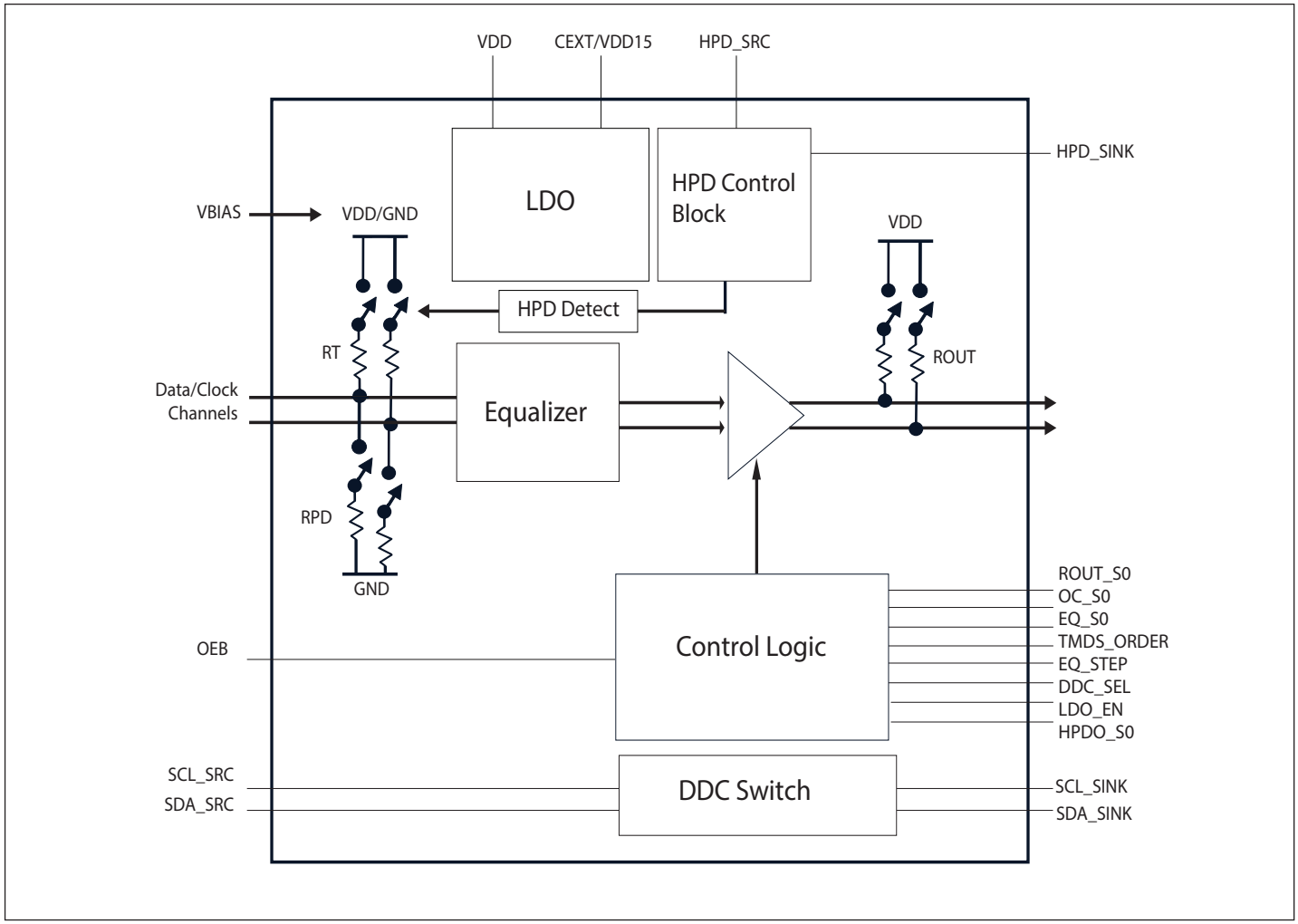
Pin Configuration



Application Diagram



Block Diagram



Pin Description

Pin #	Pin Name	Type	Description
1, 7	VDD	PWR	3.3V power supply. Add external 0.1uF decoupling capacitor to GND.
2	CEXT/VDD15	PWR	LDO output for internal core power supplier. LDO_EN = "0": 3.3V single power supply mode. Add external capacitor (2.2uF-4.7uF) to GND LDO_EN = "1": Dual power supply mode. Apply 1.5V power
15, 18, 37, 39	GND	GND	Ground
36	HPD_SINK	I	Sink side HPD (Hot Plug Detect) input; internal pull-down at 120 Kohm.
12	HPD_SRC	O	HPD output to source side
3, 4, 5, 6, 8, 9, 10, 11	IN_D2- IN_D2+ IN_D1- IN_D1+ IN_D0- IN_D0- IN_CLK- IN_CLK+	I	TMDS inputs. RT=50 Ohm; RPD=200 Kohm.
33, 32, 31, 30, 28, 27, 26, 25	OUT_D2- OUT_D2+ OUT_D1- OUT_D1+ OUT_D0- OUT_D0+ OUT_CLK- OUT_CLK+	O	TMDS outputs. ROUT=50 Ohm is active when ROUT_S0= "1"
17	SCL_SRC	IO	Source side DDC Clock
16	SDA_SRC	IO	Source side DDC Data
34	SCL_SINK	IO	Sink side DDC Clock for connector
35	SDA_SINK	IO	Sink side DDC Data for connector
19	ROUT_S0	I	TMDS output double termination selection. Internal pull high to VDD.
20	OC_S0	I	TMDS output three-level pre-emphasis selection. Internal 50% of VDD.
24	EQ_S0	I	TMDS input three-level equalization selection. Internal 50% of VDD.
38	OEB	I	Output Enable control. Active low. Internal pull-down at 100 kohm.
13	TMDS_ORDER	I	TMDS order selectable control with default pull high.

Pin #	Pin Name	Type	Description
14	HPDO_S0	I	HPD_SRC output control with default pull high.
21	DDC_SEL	I	DDC buffer or passive switch control with default pull high.
22	VBIAS	I	TMDS input termination voltage control with default pull high.
23	EQ_STEP	I	EQ_step selection control with default pull high.
40	LDO_EN	I	1.5/3.3V or 3.3V power supply control pin. Default is pull high (3.3V single power).

Functional Description

Squelch Mode

Automatic output squelch function disables TMDS output when no Input signal presents. Output Disable (Squelch) Mode uses TMDS Clock signal detection. When low voltage levels on the TMDS input clock are detected, Squelch state enables and TMDS outputs shall be disabled. When the TMDS clock inputs are above the pre-determined threshold voltage, TMDS outputs shall return to the normal swing voltage levels.

HPD_SINK Shut Down

When HPD_SINK pin floats or ties to GND, TMDS outputs shall shut down to sleep mode; HPD_SINK does not control DDC channel.

TMDS Pin Order Configuration Table

TMDS_ORDER	Functional Description	Note
"0"	D2/D1/D0/CLK pin order	
"1" or "NC"	CLK/D0/D1/D2 pin order	Default

DDC mode selection DDC_SEL Configuration Table

DDC_SEL	Functional Description	Note
"0"	Passive Switch	
"1" OR "NC"	Active DDC Buffer	Default

LDO Enable Configuration Table

LDO_EN	Functional Description		Note
	Pin 1	Pin 2	
"0"	3.3V	External capacitor	Recommend 2.2~4.7uF pull down capacitor
"1"	3.3V	1.5V	Dual power supply mode. Default

Pre-emphasis Truth Table

Output pre-emphasis setting		Functional Description		Notes
ROUT_S0	OC_S0	Single-end Vswing	Pre-emphasis	
"0"	"0"	500 mV	0 dB	Open drain output.
	"NC" or VDD/2	500 mV	1.5 dB	Open drain output. Default
	"1"	500 mV	2.5 dB	Open drain output
"1"	"0"	500 mV	0 dB	Double termination
	"NC" or VDD/2	500 mV	1.5 dB	Double termination. Default
	"1"	500 mV	2.5 dB	Double termination

TMDS Input Termination Voltage Control VBIAS Truth Table

VBIAS	Functional Description
"1", "NC"	HDMI input. VBIAS ties to VDD.
"0"	DosplayPort input. VBIAS ties to GND.

EQ Step Selection Control EQ_STEP Truth Table

EQ_STEP	Functional Description
"1", "NC"	2.5, 5, 7.5dB EQ setting with EQ_S0 control pin
"0"	5, 10, 15dB EQ setting with EQ_S0 conrol pin

Output Data Signals EQ_S0 Configuration Truth Table

EQ_S0	Functional Description		Note
	EQ_STEP = "1"	EQ_Step = "0"	
"0"	2.5 dB	5 dB	TMDS Clock(CLK) channel EQ is always fixed as 3dB without pre-emphasis.
"NC" , "VDD/2"	5 dB	10 dB	
"1"	7.5 dB	15 dB	

Sink side Hot Plug Detect HPD_SINK Truth Table

HPD_SINK	Functional Description
"1"	Normal mode
"0"	Disable output signal for power saving mode

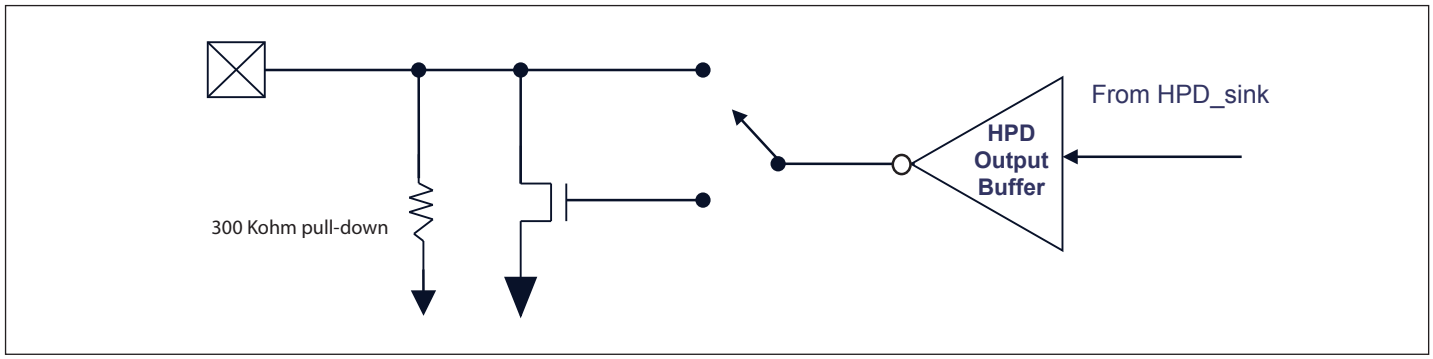
Source side Hot Plug Detect Output Control HPDO_S0 Truth Table

HPDO_S0	Functional Description
"1" or "NC"	Open drain output
"0"	Inverted Buffer output of HPD_SINK signal

Output Enable Conrol Truth Table

OEB	Functional Description
"0"	Active Low. Normal mode
"1"	Disable output signal for power saving mode

Source-side Output Block Diagram



Note:
1.) Open drain buffer is recommended with external pull-up resistor to < 4.5V power supply.

Absolute Maximum Ratings

Item	Absolute Rating*1
Supply Voltage to Ground Potential	4.5V
All Inputs and Outputs	-0.5V to 4.5V
5V Tolerance I/O Pins (SDA_SINK, SCL_SINK, HPD_SINK)	-0.5v to 5.5V
Ambient Operating Temperature	-40 to 85°C
Storage Temperature	-65 to 150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Note *1) Stress beyond those lists under "Absolute Maximum Ratings" may cause permanent damage to the device

Recommended Operation Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
TA	Ambient Operating Temperature	-20		85	°C
VDD	Power Supply Voltage	2.89	3.3	3.6	V

DC Characteristics (VDD = 3.3V ±10%)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
IDD	VDD Supply Current	Open drain 500mV single-end, 0dB pre-emphasis, Exclude 40mA current pass-through from source devices		80	100	mA
ISTB	Standby mode	DDC passive switch, VDD=3.6V, HPD_SINK="0" or OEB = "1"		30		µA
		DDC active buffer VDD=3.6V, , HPD_SINK = "0" or OEB = "1"		1.5		mA
ISQLH	Squelch mode current	DDC passive switch VDD=3.6V, HPD_SINK=3.6V		2.2		mA
		DDC active buffer VDD=3.6V, HPD_SINK=3.6V		3.2		mA

HPD Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HPD_SRC						
VOL	Buffer Output Low Voltage	IOL = 4 mA			0.4	V
	Open Drain Output Low Voltage	IOL = 4 mA	0		0.4	V
VOH	Buffer Output High Voltage	IOH = 0.1 mA	VDD-1.55			V
IOFF	Off leakage current	VDD=0, VIN=3.6V			25	uA
IOZ	Open drain Output leakage current	VDD=3.6V, VIN=3.6V			25	
HPD_SINK						
IIH	High level digital input current	VIH =5.5V	-10		80	µA
IIL	Low level digital input current	VIL = GND	-10		10	µA
VIH	High level digital input voltage	VDD=3.3V	2.0			V
VIL	Low level digital input voltage		0		0.8	V

Control pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OEB with 100k pull to GND						
IIH	High level digital input current	VIH = 3.3V, VDD=3.3V	-10		80	µA
IIL	Low level digital input current	VIL = GND	-10		10	µA
VIH	High level digital input voltage		2.0			V
VIL	Low level digital input voltage		0		0.8	V
EQ_S0, OC_S0 with 100k pull high and 100k pull low when TMDS is active						
IIH	High level digital input current	VIH =3.3V, VDD=3.3V	-10		40	µA
IIL	Low level digital input current	VIL = GND, VDD=3.3V	-40		10	µA
ROUT_S0, TMDS_ORDER, EQ_STEP, VBIAS, LDO_EN, DDC_SEL, HPDO_S0						
IIH	High level digital input current	VIH =VDD	-10		10	µA
IIL	Low level digital input current	VIL = GND	-20		10	µA
VIH	High level digital input voltage		2.0			V
VIL	Low level digital input voltage		0		0.8	V

DDC Channel Switch

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ILK	Input leakage current	DDC switch is off, Vin = 5.5V	-10		30	µA
CIO	Input/Output capacitance when passive switch on	VIpp(peak-peak) = 1V, 100 kHz		10		pF
RON	Passive Switch resistance	IO = 3mA, VO = 0.4V		30	50	Ω
VPASS	Switch Output voltage	VI=3.3V, II=100uA VDD=3.3V	1.5	2.0	2.5	V

DDC Channel Buffers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH_SRC	Source Side DDC Buffer Input High Voltage		2.0			V
VIL_SRC	Source Side DDC Buffer Input Low Voltage				0.4	V
VOL_SRC	Source Side DDC Buffer Output Low Voltage	External pull-up to VDD from 1.5kΩ to 10kΩ	0.47	0.52	0.6	V
VOL_SINK	Sink Side DDC Buffer Output Low Voltage				0.2	V
VIH_SINK	Sink Side DDC Buffer Input High Voltage		2.0			V
VIL_SINK	Sink Side DDC Buffer Input Low Voltage				0.8	V
CI_SRC	Source side DDC capacitance when active switch is on, or passive switch off	VIpp(peak-peak)=1V, 100 KHz		5		pF
CI_SINK	Sink side DDC capacitance when active switch is on, or passive switch off			5		pF

TMDS Differential Pins

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VOH	Single-ended high level output voltage	VDD = 3.3V, ROUT=50Ω	VDD-10		VDD+10	mV
VOL	Single-ended low level output voltage		VDD-600		VDD–400	mV
VSWING	Single-ended output swing voltage		400		600	mV
VOD(O)*1	Overshoot of output differential voltage				180*1	mV
VOD(U)*2	Undershoot of output differential voltage				200*2	mV
VOC(SS)	Change in steady-state common- mode output voltage between logic states				5	mV
IOS	Short Circuit output current at open drain mode	Short to VDD	-12		12	mA
	Short Circuit output current at double termination mode	Short to VDD	-24		24	mA
VI(open)	Single-ended input voltage under high impedance or open case	II = 10uA	VDD-10		VDD+10	mV
RT	Input termination resistance	VIN = 2.9V	45	50	55	Ω
IOZ	Leakage current with Hi-Z I/O	VDD = 3.6V			30	µA

Note:

*1) Overshoot of output differential voltage VOD(O) = (VSWING(MAX) * 2) * 15%

*2) Undershoot of output differential voltage VOD(O) = (VSWING(MIN) * 2) * 25%

AC Characteristics (Over recommended operating conditions unless otherwise noted)

TMDS differential pins

Symbol	Parameter	Test	Min.	Typ.	Max.	Units
t_{pd}	Propagation delay	VDD = 3.3V, ROUT = 50Ω			2000	ps
t_r/t_f	Differential output signal rise/fall time (20% - 80%), open drain, 0dB pre-emphasis			120		
	Differential output signal rise/fall time (20% - 80%), open drain, 2.5dB pre-emphasis			100		
$t_{sk}(p)$	Pulse skew			10	50	
$t_{sk}(D)$	Intra-pair differential skew			23	50	
$t_{sk}(o)$	Inter-pair differential skew				100	
$t_{jit}(pp)$	Peak-to-peak output jitter CLK residual jitter	Data Input = 3.4 Gbps		30	60	
$t_{jit}(pp)$	Peak-to-peak output jitter DATA Residual Jitter			40	70	
t_{en}	Enable time				50	µs
t_{dis}	Disable time				0.01	

DDC I/O pins (Passive switch mode)

Symbol	Parameter	Test	Min.	Typ.	Max.	Units
t_{pd}(DDC)	Propagation delay from SCL_SINK/SDA_SINK to SCL/SDA, or SCL/ SDA to SCL_SINK/SDA_SINK in passive switch.	CL = 10pF in passive switch			5	ns

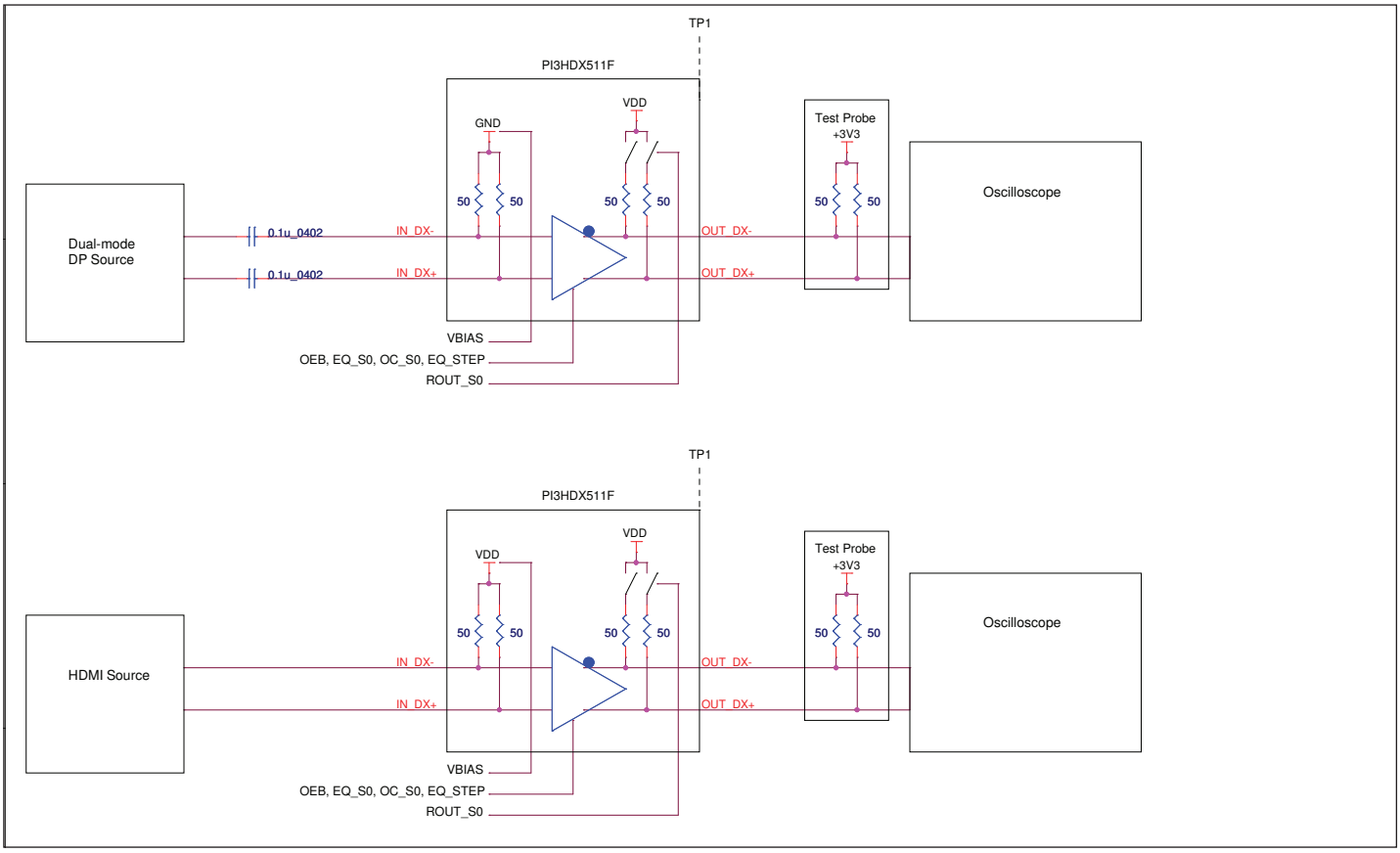
DDC I/O pins (Active buffer mode)

Symbol	Parameter	Test	Min.	Typ.	Max.	Units
t_{PLH}	LOW-to-HIGH propagation delay	SCL/SDA to SCL/SDA_SINK		169	255	ns
t_{PHL}	HIGH-to-LOW propagation delay	SCL/SDA to SCL/SDA_SINK	10	103	300	ns
t_{PLH}	LOW-to-HIGH propagation delay	SCL/SDA_SINK to SCL/SDA	25	67	110	ns
t_{PHL}	HIGH-to-LOW propagation delay	SCL/SDA_SINK to SCL/SDA		118	230	ns

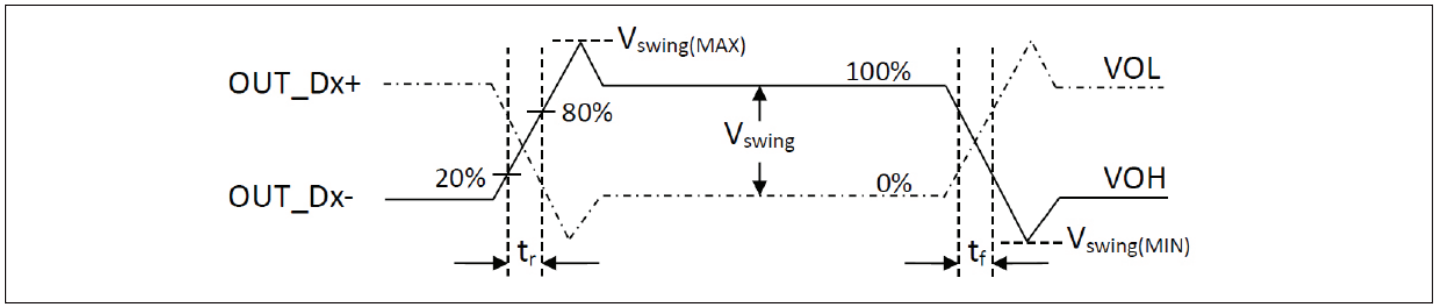
Control and Status pins (HPD_SINK, HPD)

Symbol	Parameter	Test	Min.	Typ.	Max.	Units
$t_{pd(HPD)}$	Propagation delay from HPD_SINK to the active port of HPD, high to low	CL = 10pF, pull high resistor=1kΩ		10		ns

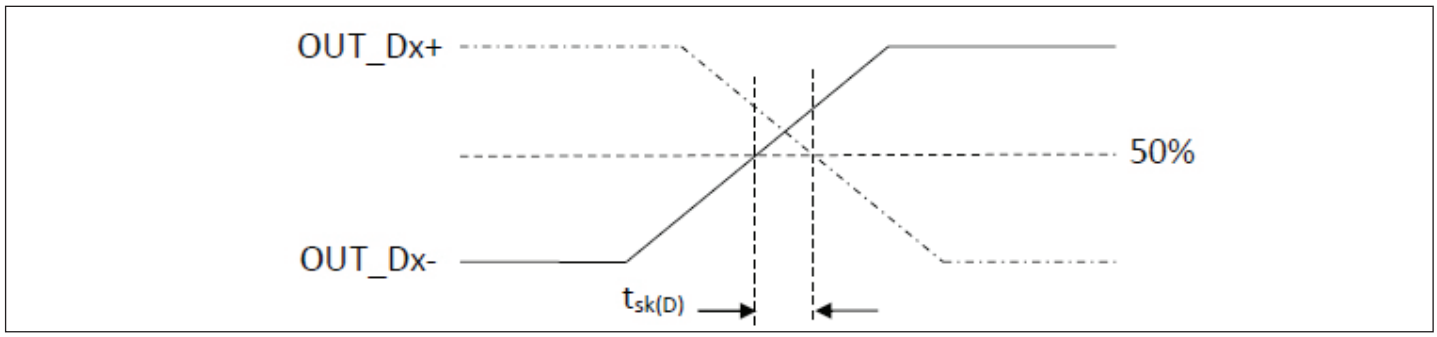
Input Measurement Test Setup



Vswing, t_r/t_f Definition

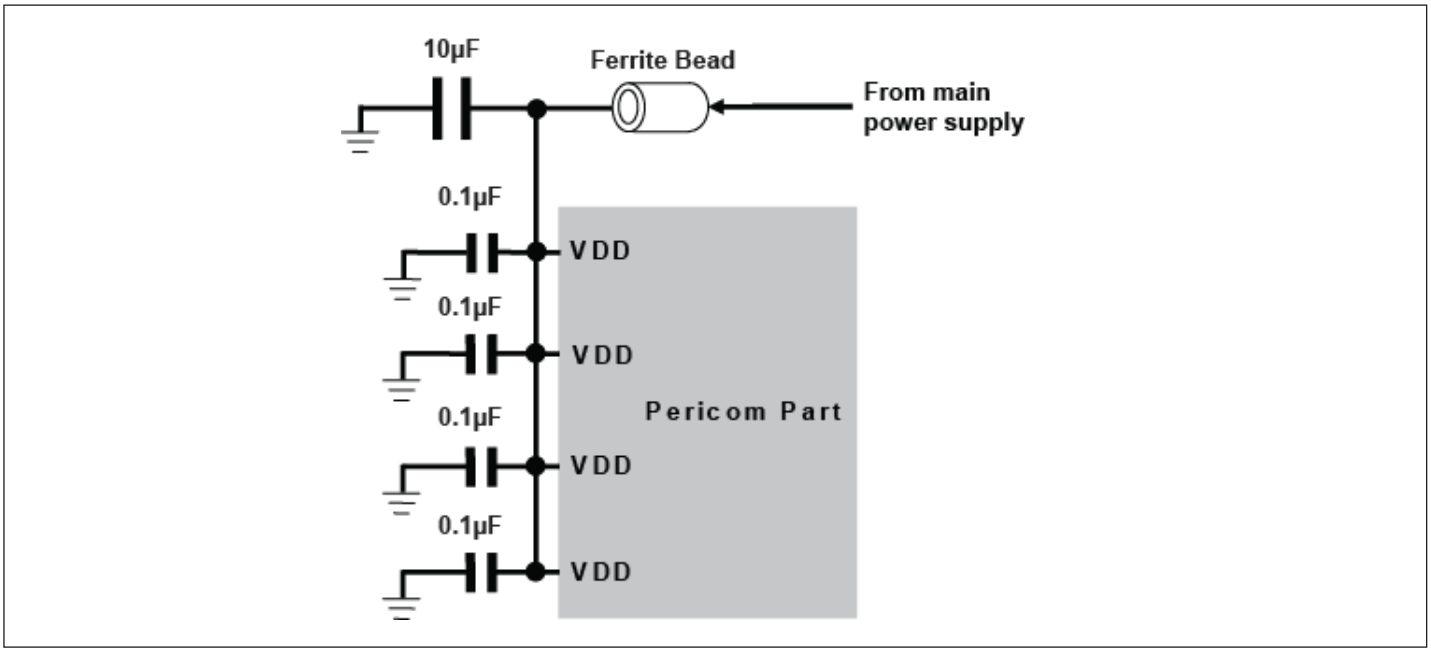


Intra-pair Skew($t_{sk(D)}$) Definition



Power Supply Decoupling Circuit

It is recommended to put 0.1 µF decoupling capacitors on each VDD pins of our part, there are four 0.1 µF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericom parts, the number of 0.1 µF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1 µF decoupling capacitors on each VDD pins, it is recommended to put a 10 µF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.



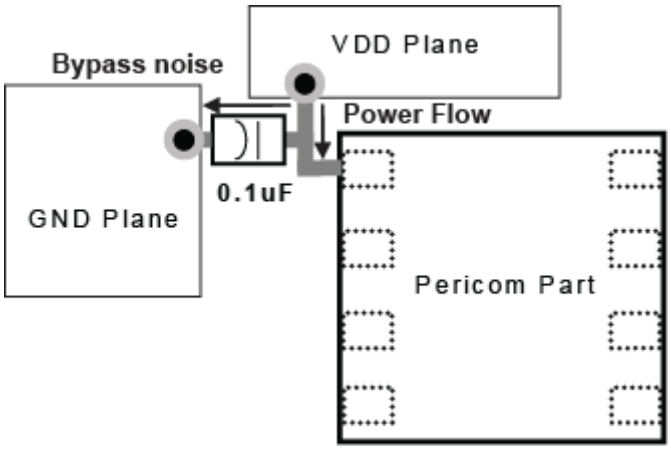
Recommended Power Supply Decoupling Capacitor Diagram

Requirements on the De-coupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

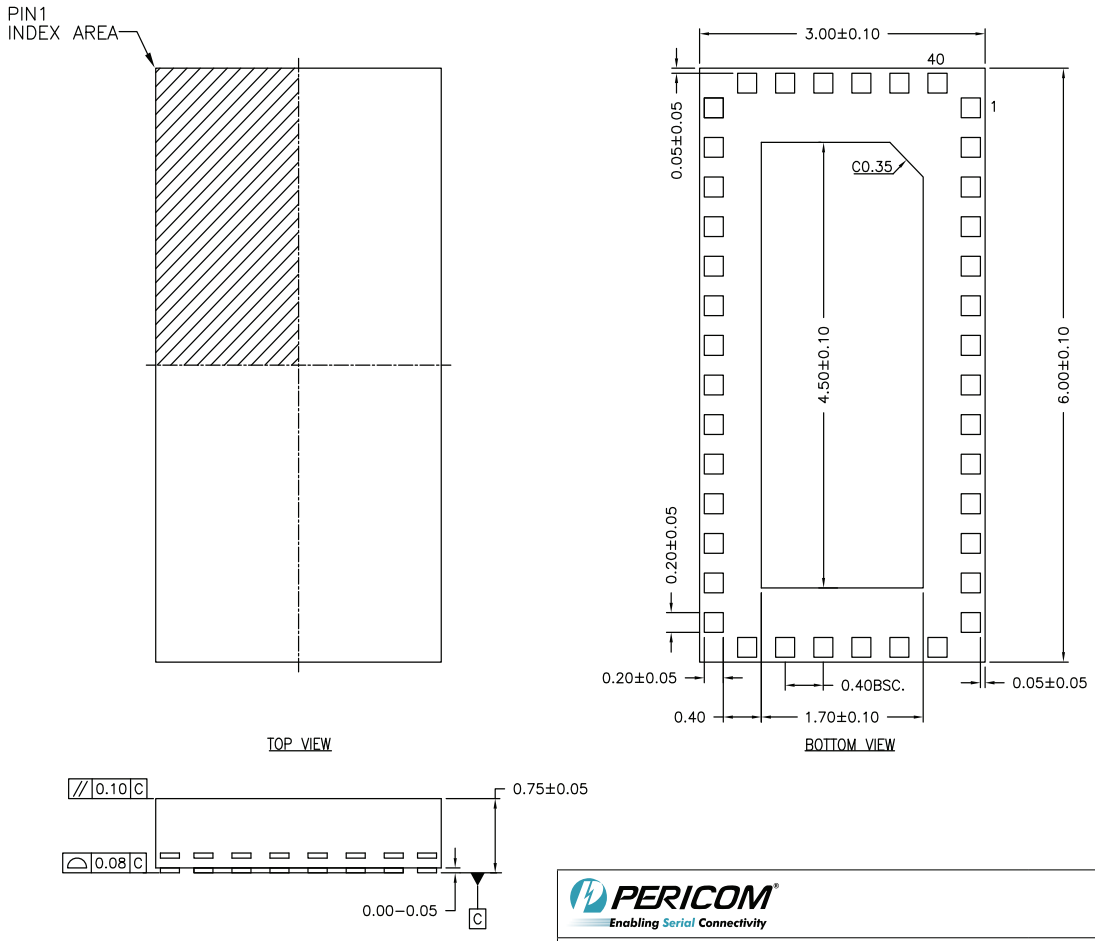
Layout Placement Consideration

- ➔ Each 0.1 µF decoupling capacitor should be placed as close as possible to each VDD pin.
- ➔ VDD and GND planes should be used to provide a low impedance path for power and ground.
- ➔ Via holes should be placed to connect to VDD and GND planes directly.
- ➔ Trace should be as wide as possible
- ➔ Trace should be as short as possible.
- ➔ The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- ➔ 10 µF Capacitor should also be placed closed to our part and should be placed in the middle location of 0.1 µF capacitors.
- ➔ Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.



Decoupling Capacitor Placement Diagram

Packaging Mechanical: 40-Contact TQFN (ZL)



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220

PERICOM Enabling Serial Connectivity

DATE: 07/11/13

DESCRIPTION: 40-contact, Thin Fine Pitch Quad Flat No-Lead, TQFN

PACKAGE CODE: ZL (ZL40)

DOCUMENT CONTROL #: PD-2165 REVISION: --

Please check for the latest package information on the Pericom web site at www.pericom.com/support/packaging.

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX511FZLEX	ZL	40-Contact, Thin Fine Pitch Quad Flat No Lead Package (TQFN)
PI3HDX511FZLIEX	ZL	I-temp grade. 40-Contact, Thin Fine Pitch Quad Flat No Lead Package (TQFN)

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
• E = Pb-free and Green
• X suffix = Tape/Reel

Related Products

Part Number	Product Description
PI3WVR12612	Wide Voltage Range DisplayPort™ & HDMI Video Switch
PI3HDX1204-B	HDMI2.0 Redriver and Displayport Level Shifter for 6Gbps Application
PI3EQXDP1201	Displayport 1.2 redriver with built-in auto test mode
PI3HDX414	1:4 Active 3.4Gbps HDMI1.4b Splitter/DeMux with Signal Conditioning
PI3HDX412BD	1:2 Active 3.4Gbps HDMI1.4b Splitter/DeMux with Signal Conditioning
PI3HDX621	2:1 Active 3.4Gbps HDMI 1.4b Switch
PI3HDMI336	3:1 Active 2.5Gbps HDMI Switch with I2C control and ARC Transmitter

Reference Information

Document	Description
HDMI 1.4	High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC