

## TSM110NB04LCV RGG-VB Datasheet

### N-Channel 40V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>f</sup>	Q <sub>g</sub> (TYP.)
40	0.013 at V <sub>GS</sub> = 10 V	28	6.8 nC
	0.015 at V <sub>GS</sub> = 4.5 V	25	

#### FEATURES

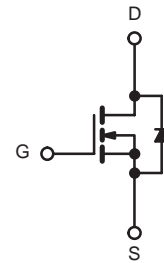
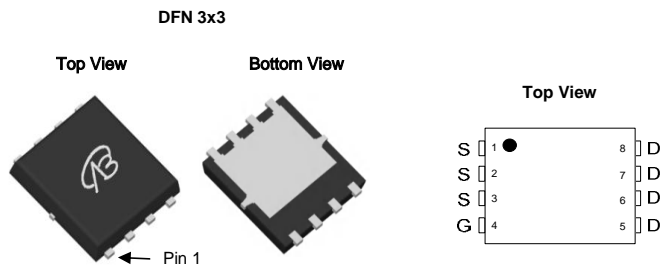
- Trench Gen IV power MOSFET
- Tuned for the lowest R<sub>DS</sub> - Q<sub>oss</sub> FOM
- 100 % R<sub>g</sub> and UIS tested
- Q<sub>gd</sub> / Q<sub>gs</sub> ratio < 1 optimizes switching characteristics



RoHS  
COMPLIANT  
HALOGEN  
FREE

#### APPLICATIONS

- Synchronous rectification
- DC/DC converters
- Motor drive switch
- Battery and load switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V <sub>DS</sub>	40	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	30	A
	T <sub>C</sub> = 70 °C		25.3	
	T <sub>A</sub> = 25 °C		11.4 <sup>a, b</sup>	
	T <sub>A</sub> = 70 °C		9.2 <sup>a, b</sup>	
Pulsed Drain Current (t = 100 μs)		I <sub>DM</sub>	70	A
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	19	
	T <sub>A</sub> = 25 °C		2.2 <sup>a, b</sup>	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	11	mJ
Single Pulse Avalanche Energy		E <sub>AS</sub>	6	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	23	W
	T <sub>C</sub> = 70 °C		14.8	
	T <sub>A</sub> = 25 °C		2.6 <sup>a, b</sup>	
	T <sub>A</sub> = 70 °C		1.7 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering Recommendations (Peak temperature) <sup>c, d</sup>			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient <sup>a, e</sup>	t ≤ 10 s	R <sub>thJA</sub>	38	48	°C/W
Maximum Junction-to-Case (Drain)	Steady state	R <sub>thJC</sub>	4.3	5.4	

#### Notes

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- The DFN 3 x 3 EP is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 94 °C/W.
- Based on T<sub>C</sub> = 25 °C.

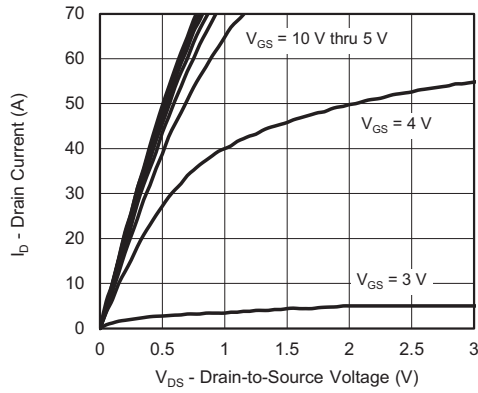
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	22.1	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.1	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V} / -16\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	10	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	-	0.013	-	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	-	0.015	-	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 5\text{ A}$	-	52	-	S
<b>Dynamic <sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1800	-	pF
Output Capacitance	$C_{oss}$		-	155	-	
Reverse Transfer Capacitance	$C_{rss}$		-	20	-	
$C_{rss}/C_{iss}$ Ratio			-	0.018	0.036	
Total Gate Charge	$Q_g$	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	-	14.2	22	nC
		$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	-	6.8	11	
Gate-Source Charge	$Q_{gs}$		-	3	-	
Gate-Drain Charge	$Q_{gd}$		-	1.5	-	
Output Charge	$Q_{oss}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	-	6.5	-	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.4	2	4	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	16	30	ns
Rise Time	$t_r$		-	56	110	
Turn-Off Delay Time	$t_{d(off)}$		-	13	25	
Fall Time	$t_f$		-	27	55	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	7	15	
Rise Time	$t_r$		-	22	45	
Turn-Off Delay Time	$t_{d(off)}$		-	13	25	
Fall Time	$t_f$		-	8	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	19	A
Pulse Diode Forward Current	$I_{SM}$		-	-	3.0	
Body Diode Voltage	$V_{SD}$	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	20	40	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	10	20	nC
Reverse Recovery Fall Time	$t_a$		-	10.5	-	ns
Reverse Recovery Rise Time	$t_b$		-	9.5	-	

### Notes

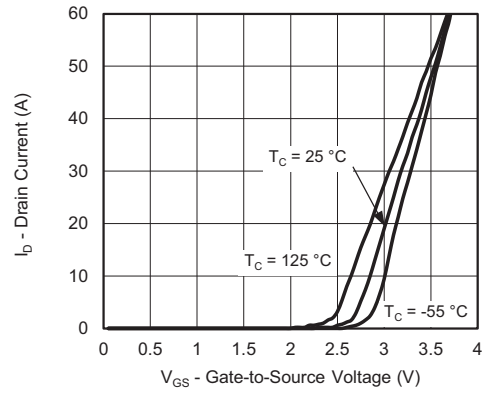
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

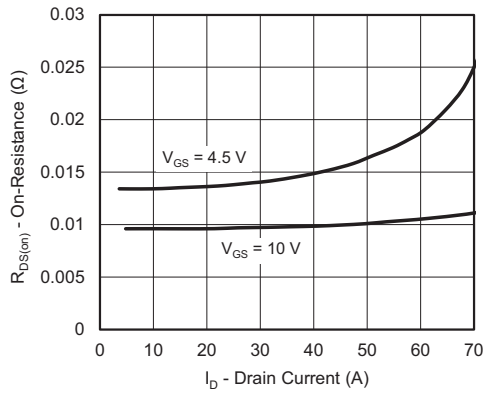
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



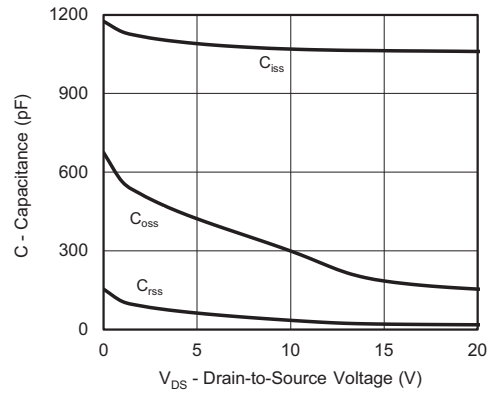
**Output Characteristics**



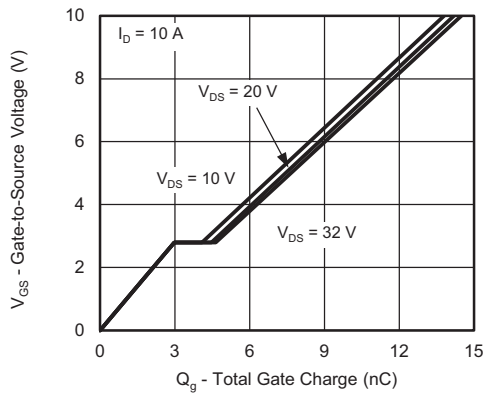
**Transfer Characteristics**



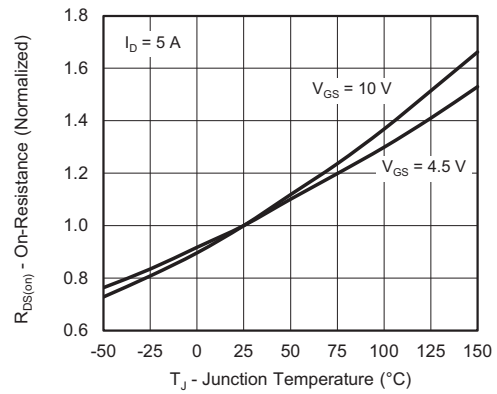
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

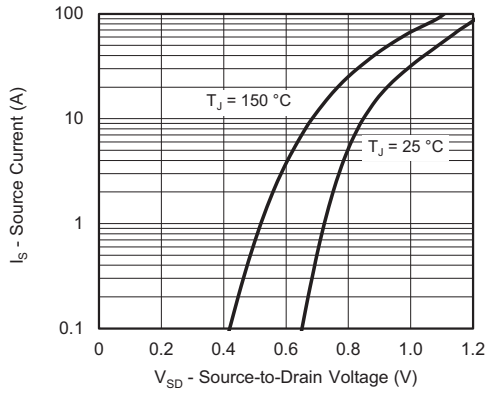


**Gate Charge**

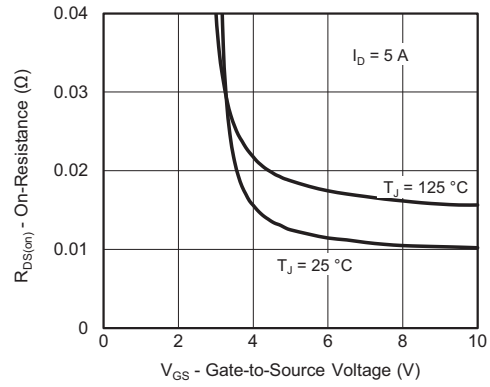


**On-Resistance vs. Junction Temperature**

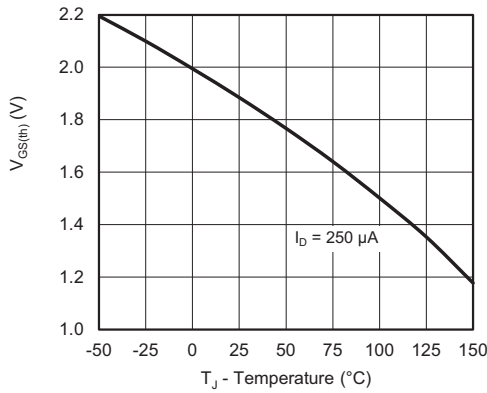
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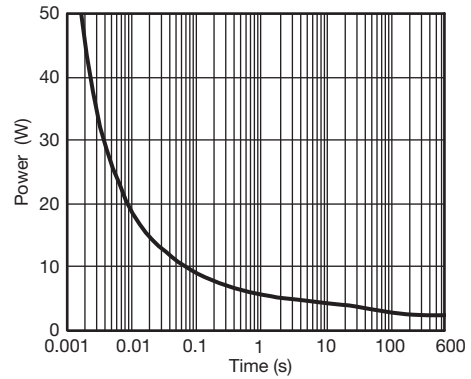
Source-Drain Diode Forward Voltage



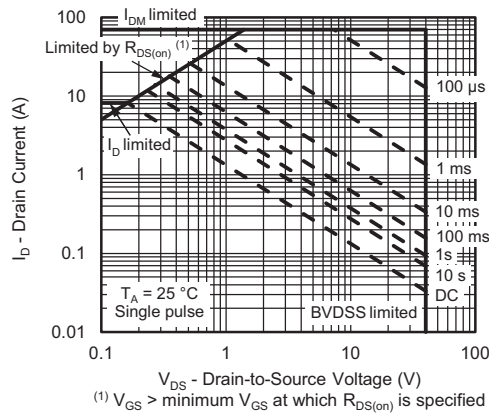
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

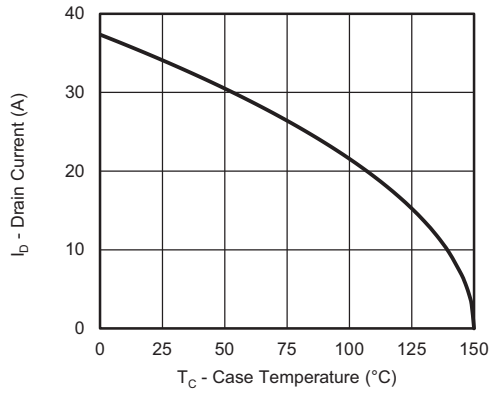


Single Pulse Power, Junction-to-Ambient

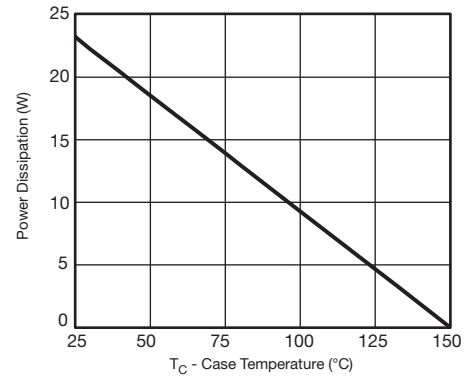


Safe Operating Area, Junction-to-Ambient

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**

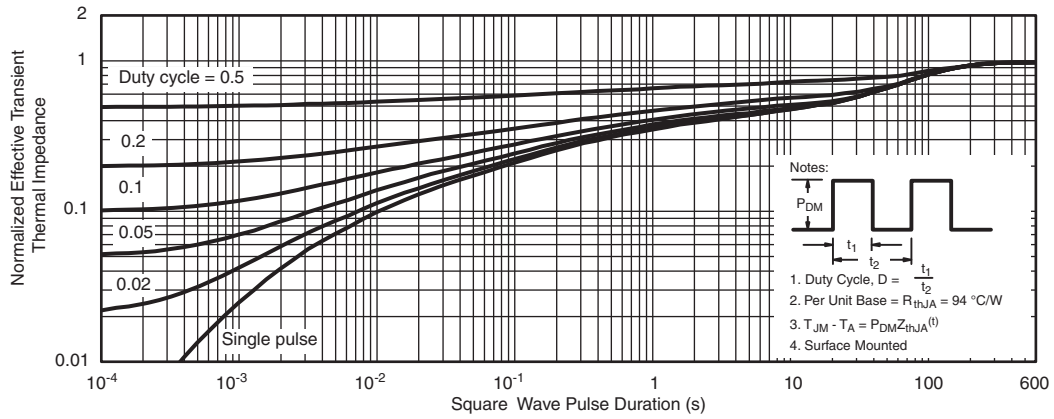


**Power Derating**

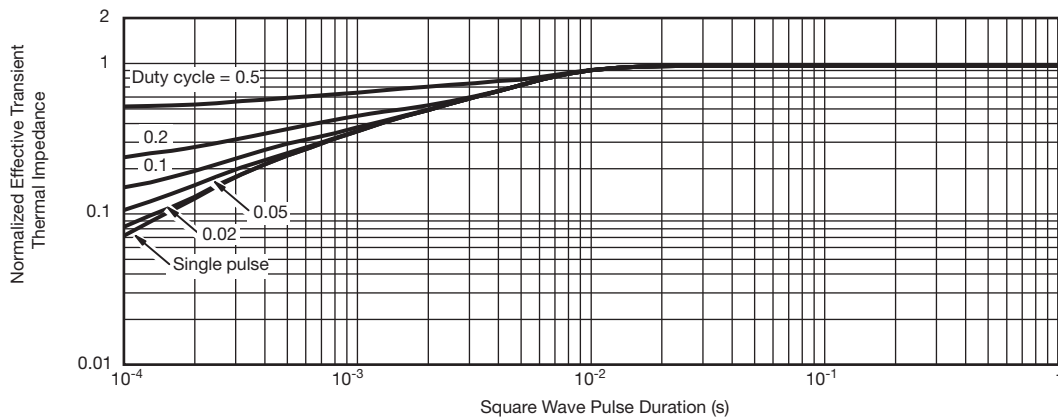
### Note

- The power dissipation  $P_D$  is based on  $T_J$  (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

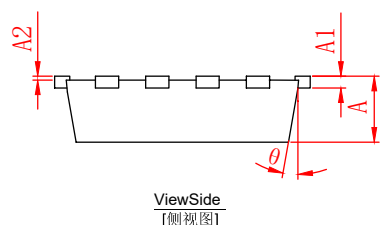
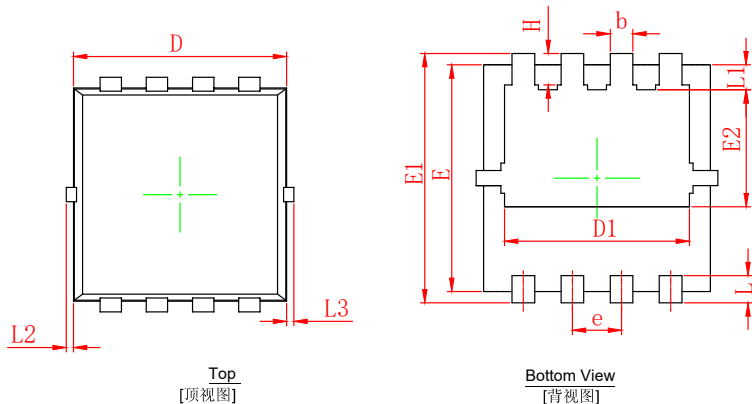


Normalized Thermal Transient Impedance, Junction-to-Ambient



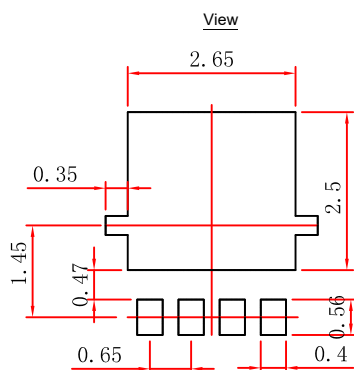
Normalized Thermal Transient Impedance, Junction-to-Case

## PDFNWB3×3-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
φ	9°	13°	9°	13°

## Suggested Pad Layout



### Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.05\text{mm}$ .
3. The pad layout is for reference purposes only.

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