4 x 65W, 2.1 MHz Digital Input 4 channel Automotive H-Driver Amplifier with Advanced Diagnostics and Low Latency Path

Features

- AEC-Q100 Qualified for Automotive Applications
  – Temperature Grade 2: –40°C to +105°C, T_A
- Wide Supply Voltage Range: 4.5V – 25V
- Input interface
  – Support I^2S, 4/8/16 slots TDM
  – Input Sample Rates: 44.1/48/96/192kHz
- Low latency signal path: 100μs (48kHz)
- Output capability
  – Up to 2.1MHz Output Switching Frequency
  – Output Power:
    ·4X23W@4Ω, 14.4V
    ·4X50W@2Ω, 14.4V
    ·4X65W@4Ω, 25V
  – Support 4Ω, 2Ω Load
  – High Resolution Bandwidth Up to 80kHz(I^2S 192kHz)
- Integrated Self Protection：
  – Over Voltage and Under Voltage Protection
  – Over Temperature Protection
  – Temperature Warning Protection
  – DC Offset Protection
  – Short Circuit Protection
  – Over Current Protection
  – Load Dump Protection(40V)
- AC and DC Load Diagnostic Functions：
  – Output Short to Power or GND
  – Shorted Output or Open Output Load
  – Selectable Internal or External Generated waveform for AC Load Diagnostic
- Real Time Current Sense
- Legacy Mode without I^2C Control
- LQFP 10X10-64L package(exposed pad up)

General Description

AWD8904 is a digital input 4 channel automotive H-driver amplifier with I^2C control that delivers up to 65W output at 25V power supply with 4Ω load, designed for high-performance LC feedback architecture for automotive motor products. The output noise of the amplifier is as low as 11μV to achieve extremely high signal-to-noise ratio, and the full power range output distortion is not affected by the nonlinearity of LC devices, achieving an excellent level. The output switching frequency can reach up to 2.1MHz, and the extremely high working frequency can eliminate the AM-band interference and reduces output filter size and cost. AWD8904 supports spread spectrum to enhance EMI performance.

AWD8904 supports all AC and DC diagnostic requirements for all diagnostic scenarios. The device uses a compact and lightweight LQFP 10X10-64L package(exposed pad up) for better use by customers in multi-channel power amplifier design.

Applications

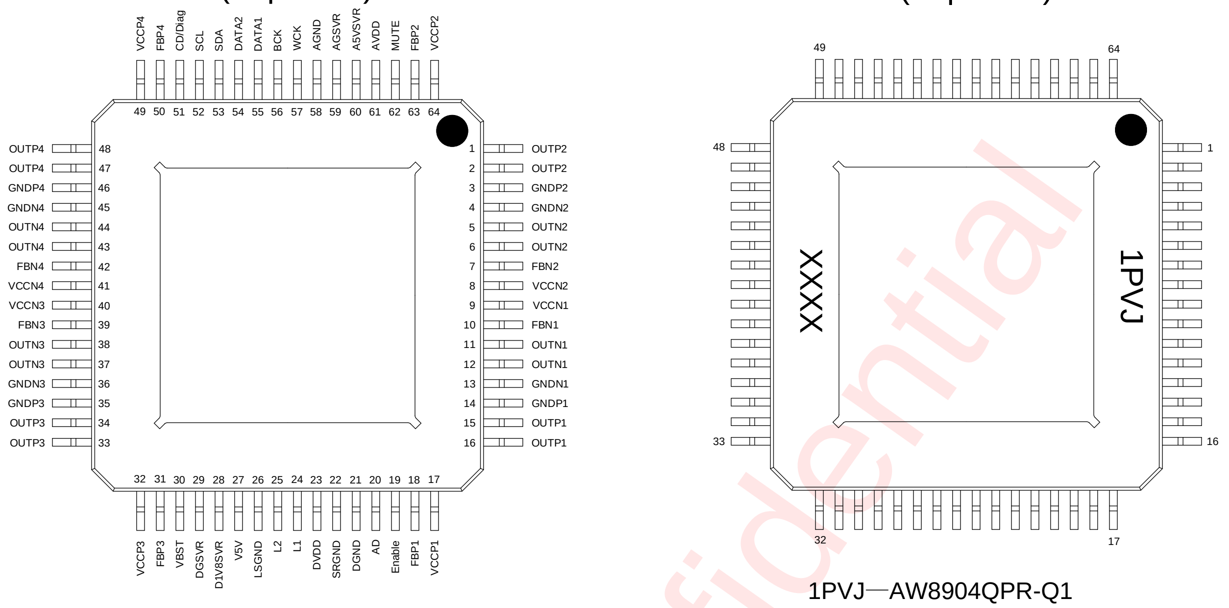
Automotive Head Units

Automotive External Amplifier Modules

Pin Configuration And Top Mark

AWD8904QPR-Q1 (Top View)

AWD8904QPR-Q1 Marking (Top View)



1PVJ—AW8904QPR-Q1
XXXX—Production Tracing Code

Figure 1 AWD8904 pin diagram top view and device marking

Pin Definition

No.	NAME	DESCRIPTION
1	OUTP2	Positive output for channel 2
2	OUTP2	Positive output for channel 2
3	GNDP2	Power Ground for positive side FET of channel 2
4	GNDN2	Power Ground for negative side FET of channel 2
5	OUTN2	Negative output for channel 2
6	OUTN2	Negative output for channel 2
7	FBN2	Feedback for negative side FET of channel 2
8	VCCN2	Power supply for negative side FET of channel 2
9	VCCN1	Power supply for negative side FET of channel 1
10	FBN1	Feedback for negative side FET of channel 1
11	OUTN1	Negative output for channel 1
12	OUTN1	Negative output for channel 1
13	GNDN1	Power Ground for negative side FET of channel 1
14	GNDP1	Power Ground for positive side FET of channel 1
15	OUTP1	Positive output for channel 1
16	OUTP1	Positive output for channel 1
17	VCCP1	Power supply for positive side FET of channel 1

18	FBP1	Feedback for positive side FET of channel 1
19	Enable	Enable pin
20	AD	I^2C address pin
21	DGND	Digital ground
22	SRGND	Power management ground
23	DVDD	Digital Power Supply
24	L1	Power management inductor side 1
25	L2	Power management inductor side 2
26	LSGND	Power management ground
27	V5V	Internal 5V supply
28	D1V8SVR	Internal positive digital supply (V(SVR) +0.9 V)
29	DGSVR	Internal negative digital supply (V(SVR) -0.9 V)
30	VBST	Power supply for internal boost
31	FBP3	Feedback for positive side FET of channel 3
32	VCCP3	Power supply for positive side FET of channel 3
33	OUTP3	Positive output for channel 3
34	OUTP3	Positive output for channel 3
35	GNDP3	Power Ground for positive side FET of channel 3
36	GNDN3	Power Ground for negative side FET of channel 3
37	OUTN3	Negative output for channel 3
38	OUTN3	Negative output for channel 3
39	FBN3	Feedback for negative side FET of channel 3
40	VCCN3	Power supply for negative side FET of channel 3
41	VCCN4	Power supply for negative side FET of channel 4
42	FBN4	Feedback for negative side FET of channel 4
43	OUTN4	Negative output for channel 4
44	OUTN4	Negative output for channel 4
45	GNDN4	Power Ground
46	GNDP4	Power Ground for positive side FET of channel 4
47	OUTP4	Positive output for channel 4
48	OUTP4	Positive output for channel 4
49	VCCP4	Power supply for positive side FET of channel 4
50	FBP4	Feedback for positive side FET of channel 4
51	CD/Diag	Reports clip and diagnostic information
52	SCL	I^2C clock input
53	SDA	I^2C data I/O
54	DATA2	I^2S data input 2 / TDM Data output
55	DATA1	I^2S/TDM data input
56	BCK	I^2S/TDM bit clock input
57	WCK	I^2S word select input / TDM frame sync signal
58	AGND	Analog ground
59	AGSVR	Internal negative analog supply V(SVR) -2.5 V

60	A5VSVR	Internal positive analog supply V(SVR) +2.5 V
61	AVDD	Analog Power Supply
62	MUTE	Mutes the device outputs
63	FBP2	Feedback for positive side FET of channel 2
64	VCCP2	Power supply for positive side FET of channel 2

Block Diagram

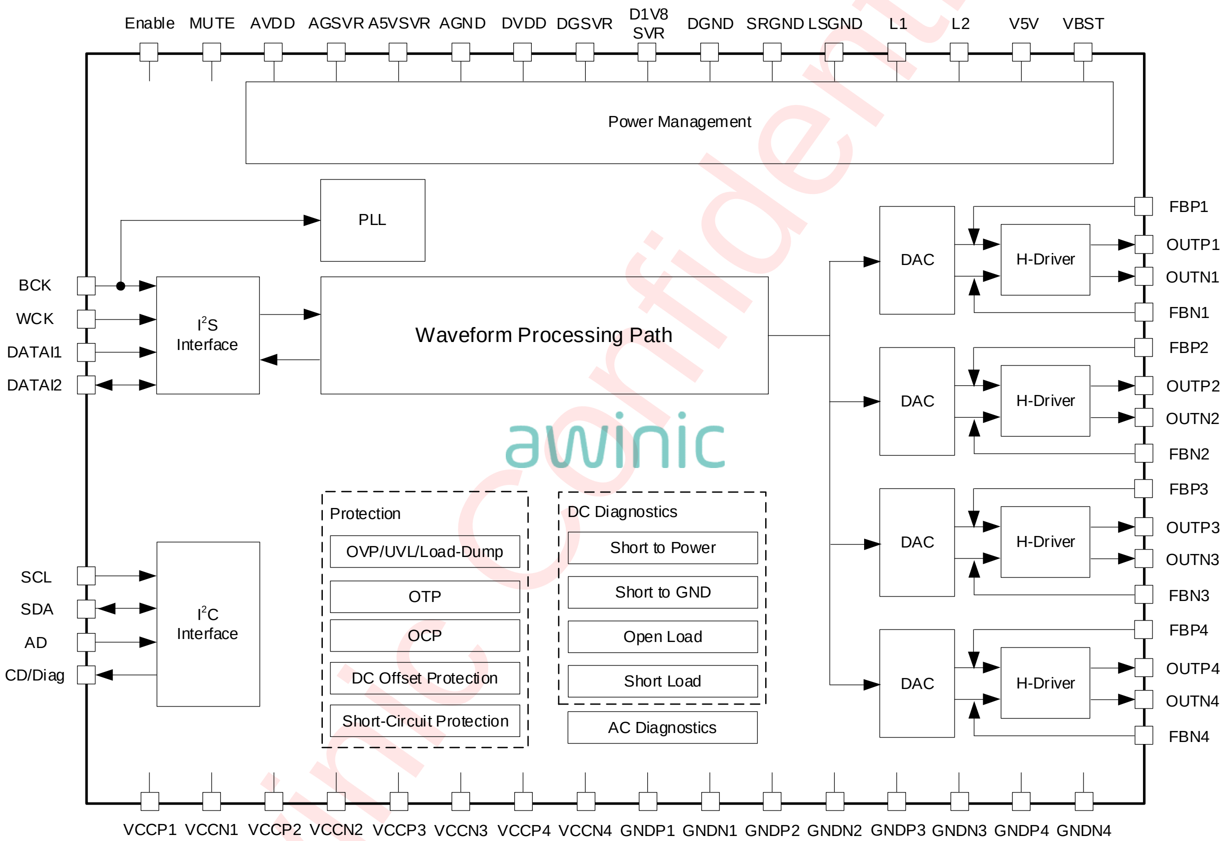


Figure 2 Functional Block Diagram

Typical Application Circuit

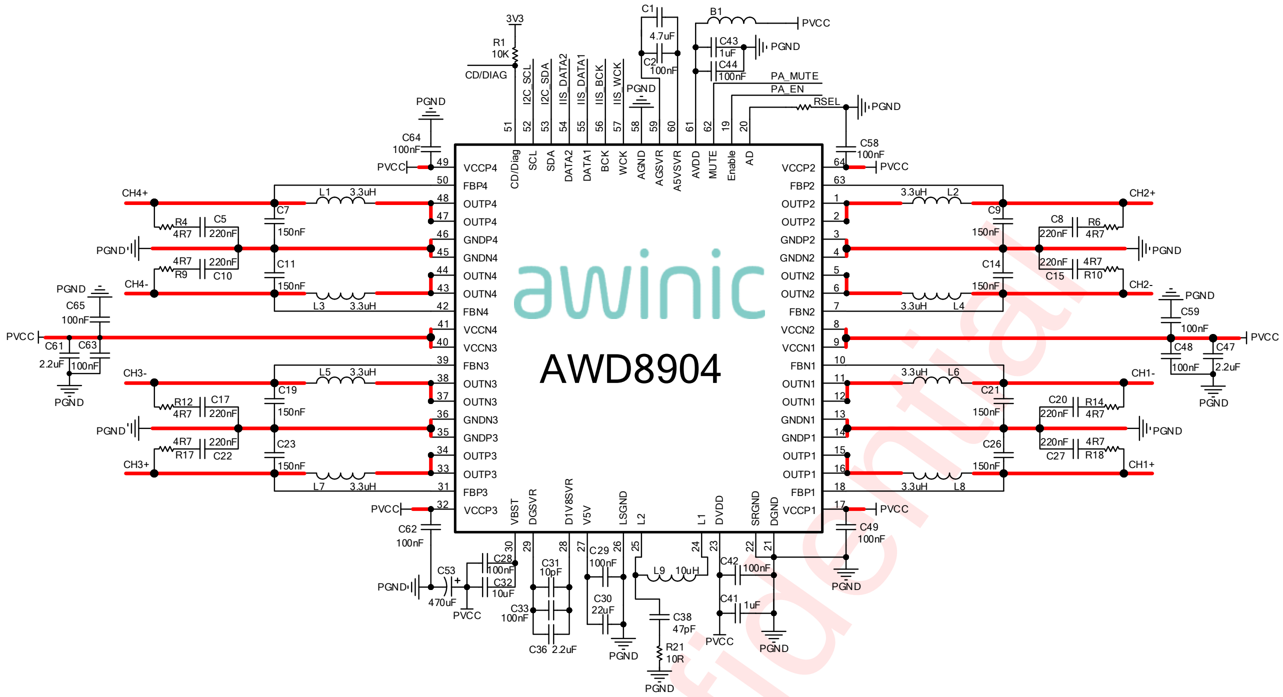


Figure 3 AWD8904 Application Circuit (PVCC = 18 V application)

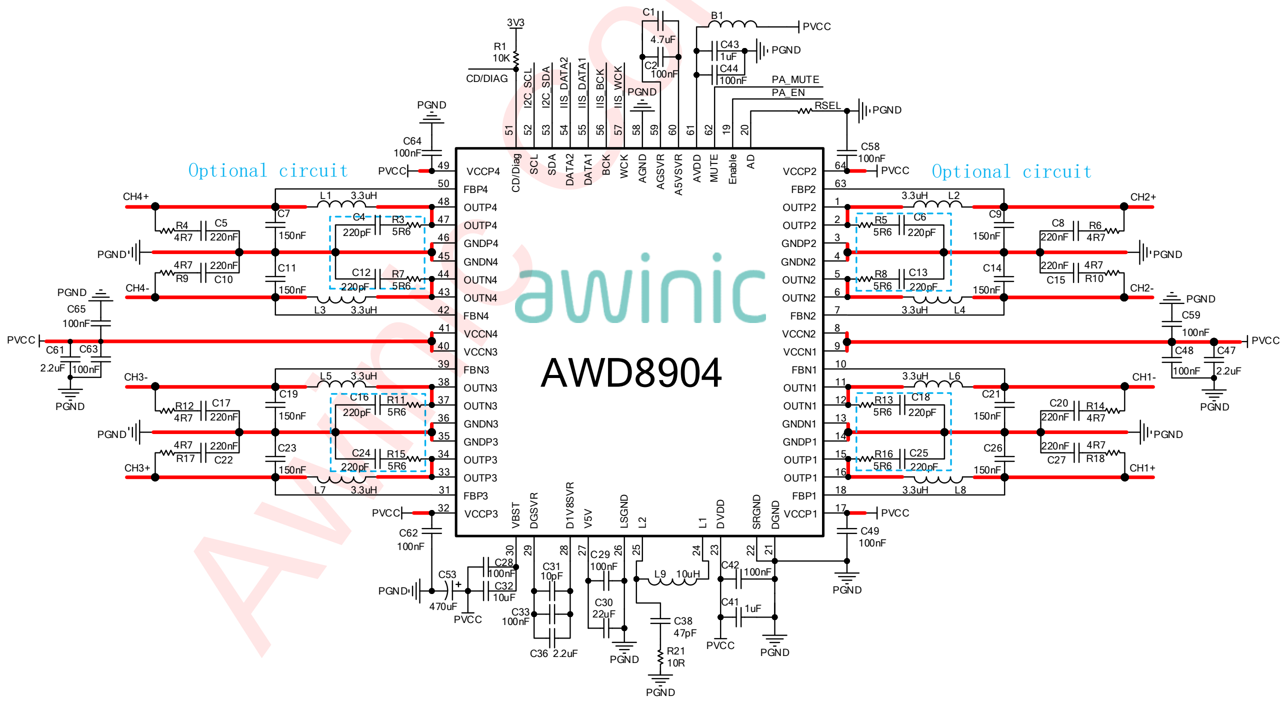


Figure 4 AWD8904 Application Circuit (PVCC = 25 V application)

Note1: Traces carrying high current are marked in red in the above figure.

The output RLC component is optional based on the EMI test result.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWD8904QPR-Q1	-40°C～105°C	LQFP 10X10-64L	1PVJ	MSL3	ROHS+HF	1000 units/ Tape and Reel

Absolute Maximum Rating

Symbol	Param	Range	Unit
VCC [VCCP(x), VCCN(x), AVDD, DVDD]	DC supply voltage	-0.3 to 32	V
GNDmax [GNDP(x), GNDN(x), AGND, DGND, SRGND, LSGND]	Ground pin voltage difference	-0.3 to 0.3	V
FBP(x), FBN(x)	Feedback pin	-0.3 to 32	V
OUTP(x), OUTN(x)	Output pin	-0.3 to 32	V
L1	Internal Regulator pin	-0.3 to 32	V
L2	Internal Regulator pin	-0.3 to 40	V
SDA, SCL	I^2C bus pins voltage	-0.3 to 5.5	V
BCK, WCK, DATA1, DATA2	I^2S bus pins voltage	-0.3 to 5.5	V
Enable	Enable pin voltage	-0.3 to 5.5	V
CD/Diag	CD/DIAG pin	-0.3 to 5.5	V
MUTE	Hardware Mute	-0.3 to 5.5	V
Tamb	Ambient operating temperature	-40 to 105	°C
Tstg,Tj	Storage and junction temperature	-55 to 150	°C
θ_{JA}	Junction-to-ambient thermal resistance	35.25	°C/W
θ_{JB}	Junction-to-board thermal resistance	35.4	°C/W
θ_{JC}	Junction-to-case thermal resistance	0.9	°C/W
ESD Rating			
HBM (Human Body Model)	ESD protection HBM	2000[Note2]	V
CDM (Charge Device Model)	ESD protection CDM	500[Note2]	V

Note2: Definition according to the international standard.

Electrical Characteristics

Test condition：T_A=25°C, VCC =14.4V, R_L=4Ω , f=1kHz(unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ	Max	Units
V_{VCC}	Power Supply	R_L = 4 Ω	4.5		25	V
		R_L = 2 Ω	4.5		18	V
I_{VCC}	Quiescent current	Device in Power Down			2	μA
		Device ON		220		mA
		Device in Eco-mode		65		mA
OVP	VCC overvoltage shutdown		28	29	30	V
UVLO				4	4.2	V
I^2C_resth	I^2C reset threshold(VCC)			2.7		V
VCC low supply mute	during start stop crank, attenuation>=60dB （digital mute disable）			4.2	4.4	V
Tsh	Thermal shutdown		175	185	195	°C
Tph	Thermal Mute	Attenuation=60dB	165	175	185	°C
Tpl		Attenuation=0.5dB	155	165	175	°C
TW1	Thermal Warning		145	155	165	°C
TW2			135	145	155	°C
TW3			122	132	142	°C
TW4			105	115	125	°C
OCP	Overcurrent protection (REG0x0C[Bit4-Bit5])	Bit4-5=00		11.7		A
		Bit4-5=01		8.4		A
		Bit4-5=10		6.2		A
		Bit4-5=11		3.7		A
Output Performance						
PO	Output Power	VCC=14.4V	22	23		W
		VCC=25V	65	67		W
Gv1	Voltage gain 1	Measured at -10 dB Fs	7.5	8.3	9.1	Vp
Gv2	Voltage gain 2		5.5	6.1	6.7	Vp
Gv3	Voltage gain 3		3.15	3.5	3.85	Vp
Gv4	Voltage gain 4		2.3	2.5	2.8	Vp
VOS	Output DC offset		-3		3	mV
CT	Cross talk	f = 1 kHz		105		dB

PSRR	Power supply rejection ratio	f = 1 kHz; Vp-p_sin=1V		95		dB
Efficiency	4x25 W, sine 1 kHz			85.5		%
Current Sense	THD+N	Full scale=4A, Vout=8V_{PEAK}		0.5		%
PWM	Base Frequency			2.1		MHz
Diagnostic thresholds						
Load diagnostic	I_{S2G}	No short to GND detected			4	mA
		Short to GND detected	35			mA
	I_{S2P}	No short to Supply detected			-4	mA
		Short to Supply detected	-35			mA
	R_{SL}	DC diagnostic, short load, 0x0B-Bit7=0		0.6		Ω
		DC diagnostic, short load, 0x0B-Bit7=1		0.5		Ω
	R_{OL}	DC diagnostic, open load, 0x0B-Bit6=0		25		Ω
		DC diagnostic, open load, 0x0B-Bit6=1		16		Ω
		AC diagnostic, open load		25		Ω
Voffout	Output offset detector threshold			1.5		V
Voffin	Input DC offset detection threshold			-18		dB
Digital Logical Interface						
I^2S	Clock frequency				24.57	MHz
	Duty cycle		40		60	%
	I^2S pins low voltage				0.7	V
	I^2S pins high voltage		1.3			V
	Input logic current				500	nA
I^2C	Clock frequency				400	kHz
	I^2C pins low voltage				0.7	V
	I^2C pins high voltage		1.3			V
	Max input leakage current				500	nA
Control Pins						
ADDSEL	V_ADDSEL @ R=∞ （pin open）			1.5		V

	I_ADDSEL @ R=0 (pin shorted to GND)			30		μA
	R_ADDSEL0				18	KΩ
	R_ADDSEL1		33		38	KΩ
	R_ADDSEL2		49		57	KΩ
	R_ADDSEL3		72		81	KΩ
	R_LEGACY		108			KΩ
V_{MUTE}	Mute pin voltage threshold, Attenuation <0.5 dB	Play Mode	2.6			V
	Mute pin voltage threshold, Attenuation ≥60 dB	Mute Mode			1.4	V
V_{Enable}	Enable pin low voltage threshold	Power-Down			0.9	V
	Enable pin high voltage threshold		2.4			V
Internal Supply						
A5VSVR-AGSVR	Delta voltage level		4.3	4.5	4.7	V
D1V8SVR-DGSVR	Delta voltage level			1.8		V
VBOOST	Boosted voltage level above VCC		6.8	7.3	7.8	V
V5V	Internal supply			4.6		V
I_{L1L2}	Inductor current				2	A

I²C INTERFACE TIMING

Parameter			Min	Typ.	Max	Min	Units
No.	Sym	Name					
1	f_{SCL}	SCL Clock frequency			400k		Hz
2	t_{LOW}	SCL Low level Duration	1.3			0.5	μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26	μs
4	t_{RISE}	SCL, SDA rise time			0.3		μs
5	t_{FALL}	SCL, SDA fall time			0.3		μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.26	μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			0.26	μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26	μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			0.5	μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05	μs
11	$t_{HD:DAT}$	SDA hold time	10			10	ns

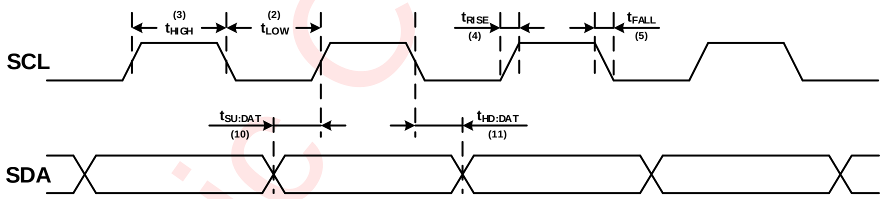


Figure 5 SCL and SDA timing relationships in the data transmission process

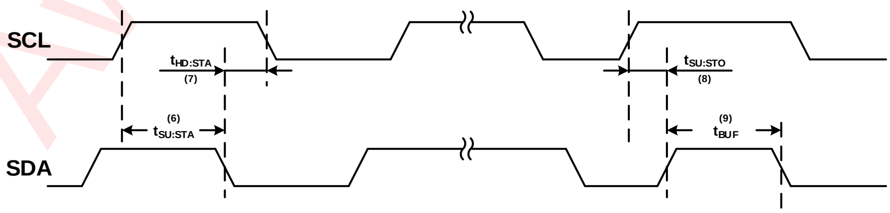


Figure 6 The timing relationship between START and STOP state

DIGITAL INTERFACE TIMING

Parameter Name		Min	Typ.	Max	Units
f_s	Sampling frequency, on pin WCK	8		192Note3	kHz
f_{bck}	Bit clock frequency, on pin BCK	32*fs		24.57MNote3	Hz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns
t_d	DATAO output delay time to BCK			50	ns

Note3：The BCK frequency f_{bck} is determined by sampling frequency, slot number and slot length, please make sure f_{bck} is less than 24.57MHz.

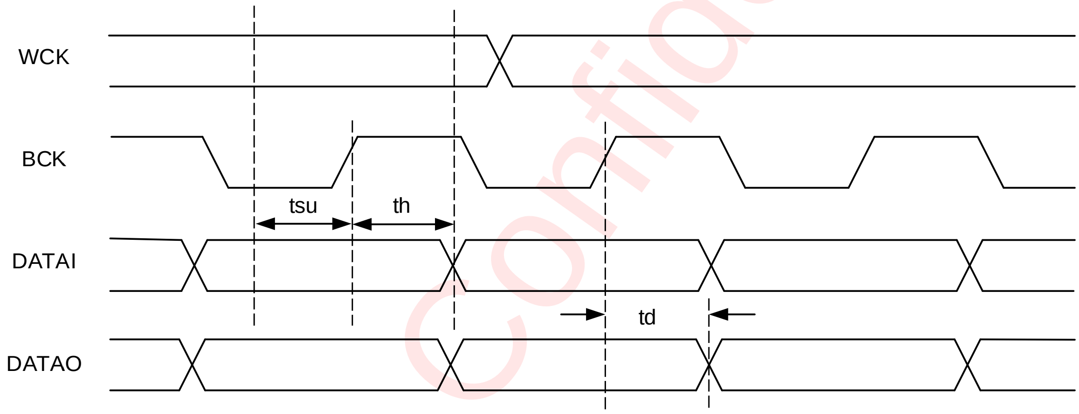


Figure 7 Digital Interface Timing

TYPICAL CHARACTERISTIC CURVES

Figure 8 THD VS. Frequency(VCC=14.4V, P=1W)

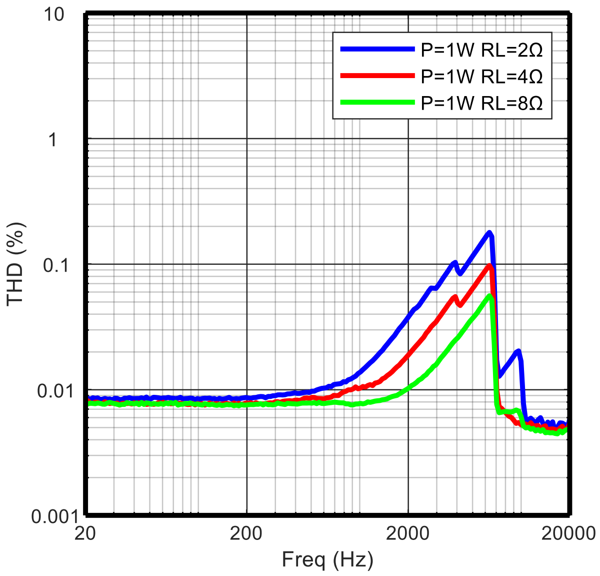


Figure 9 THD+N VS. Input Amplitude(VCC=14.4V)

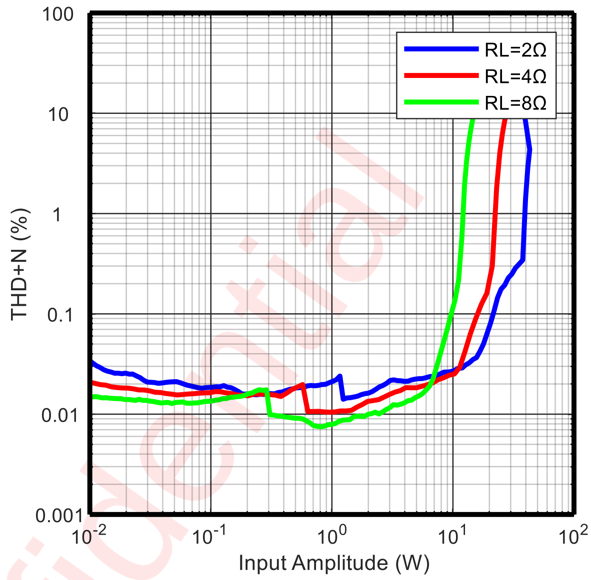


Figure 10 Crosstalk VS. Frequency (VCC=14.4V, 4Vrms, RL=4Ω)

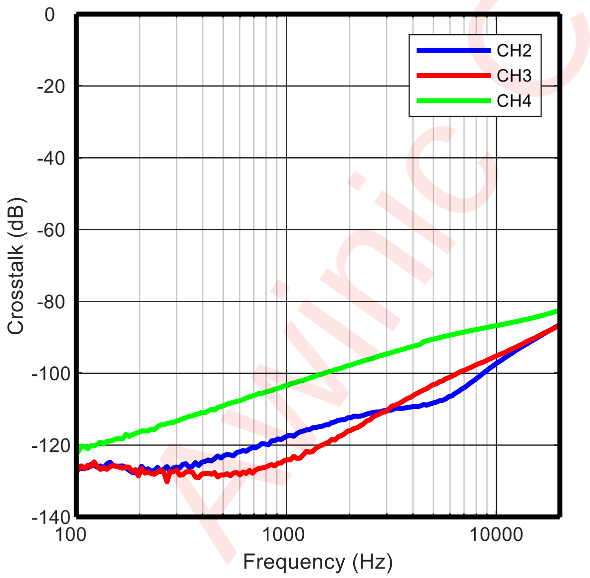


Figure 11 GAIN VS. Frequency (VCC=14.4V)

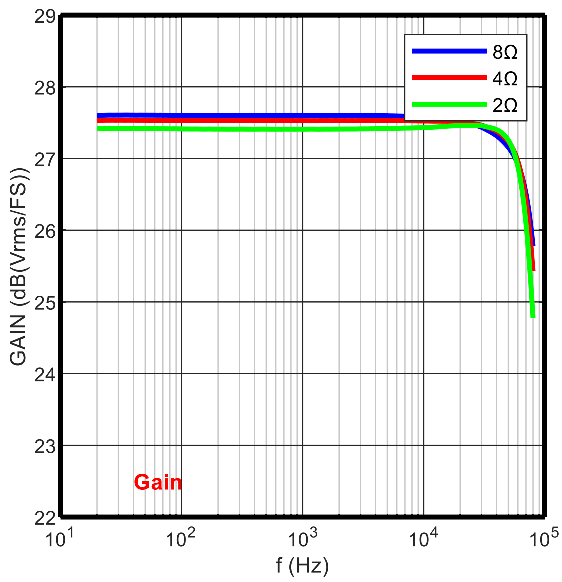


Figure 12 EFF VS. Po (VCC=25V, RL=4Ω, f=1kHz, BTL)

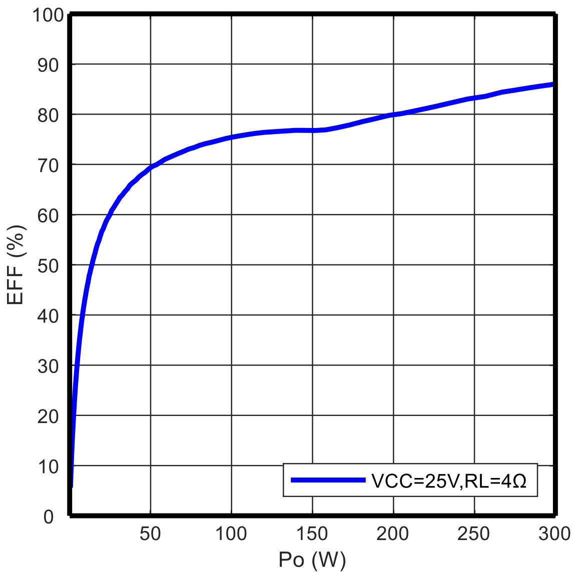


Figure 13 EFF VS. Po (VCC=25V, RL=2Ω, f=1kHz, PBTL)

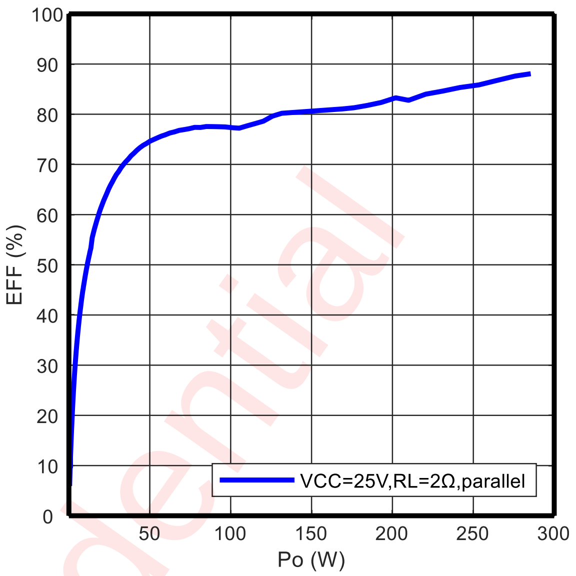


Figure 14 EFF VS. Po (VCC=25V, RL=8Ω, f=1kHz, BTL)

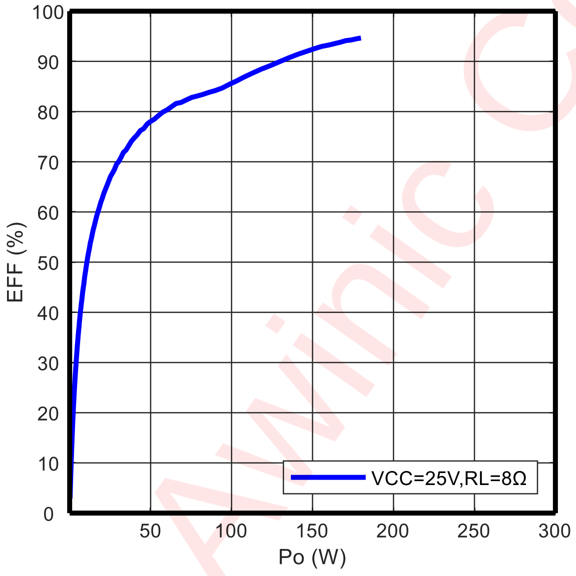


Figure 15 EFF VS. Po (VCC=14.4V, RL=4Ω, f=1kHz, BTL)

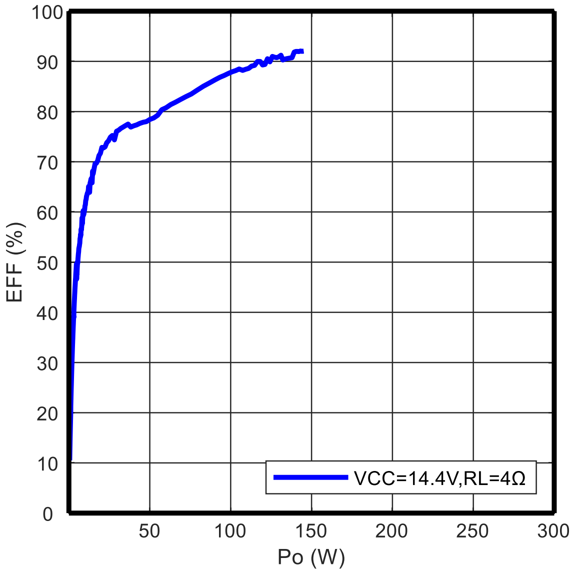


Figure 16 EFF VS. Po (VCC=14.4V, RL=2Ω, f=1kHz, BTL)

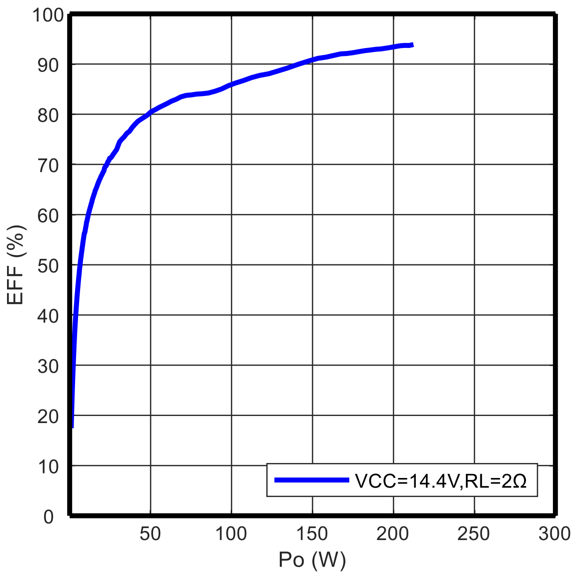


Figure 17 EFF VS. Po (VCC=14.4V, RL=8Ω, f=1kHz, BTL)

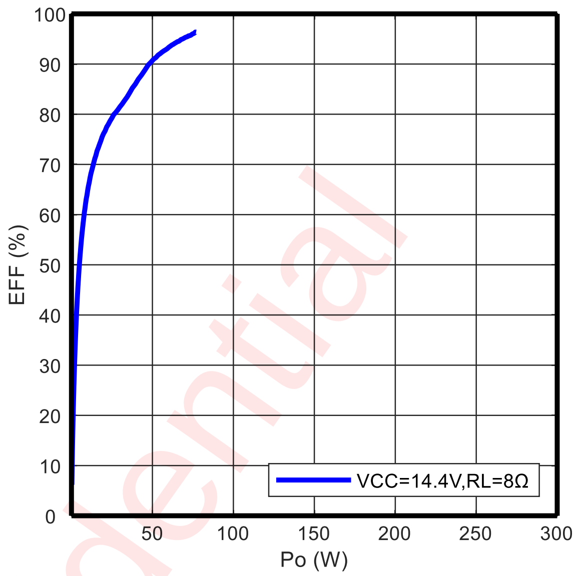


Figure 18 EFF VS. Po (VCC=18V, RL=2Ω, f=1kHz, BTL)

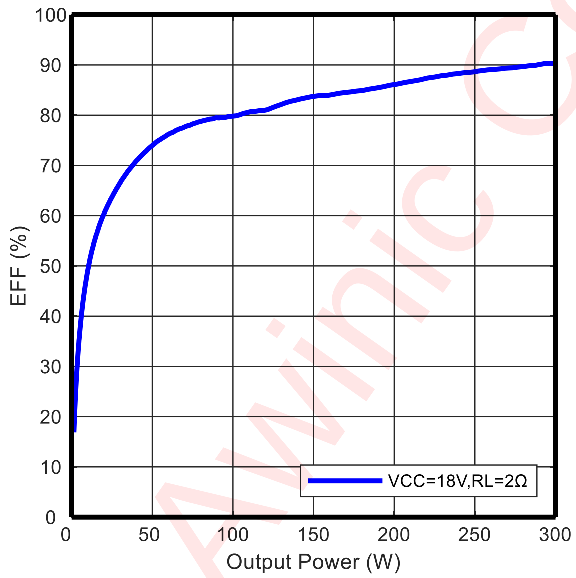


Figure 19 Po VS. VCC(RL=4Ω, f=1kHz, BTL)

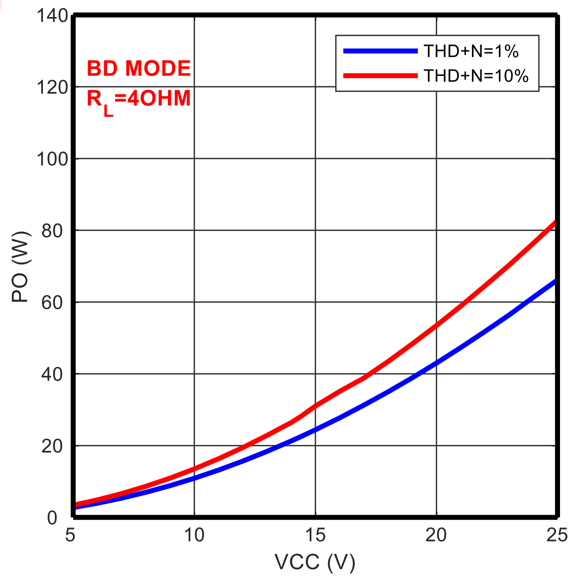


Figure 20 Po VS. VCC(RL=2Ω, f=1kHz, BTL)

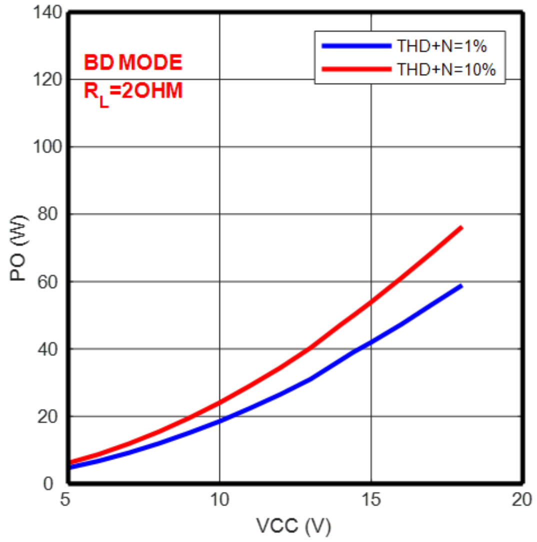


Figure 21 Po VS. VCC(RL=8Ω, f=1kHz, BTL)

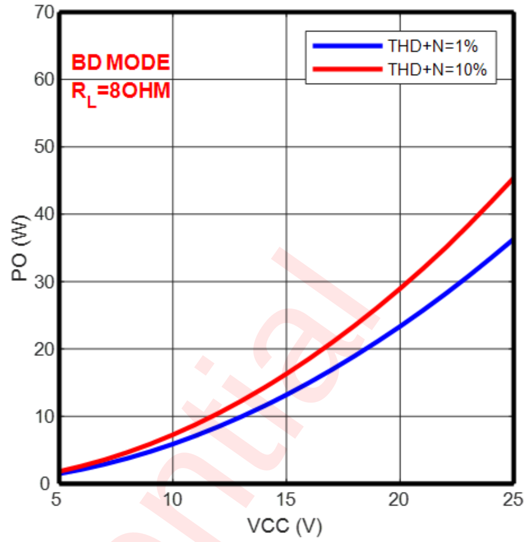


Figure 22 Real Time Current Monitor THD VS. Current (VCC=14.4V, f=100Hz)

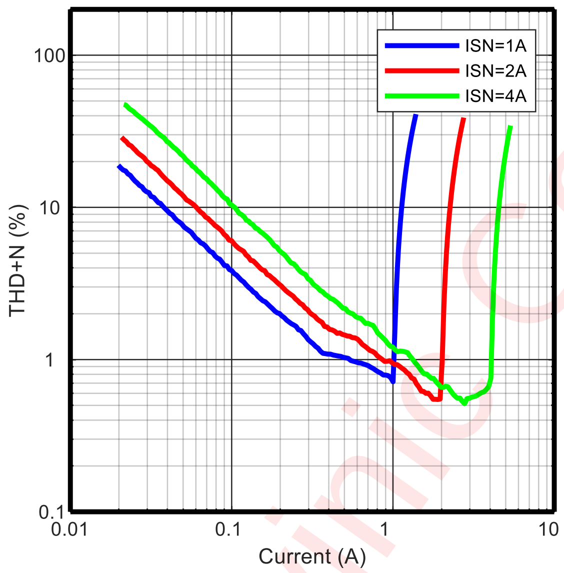
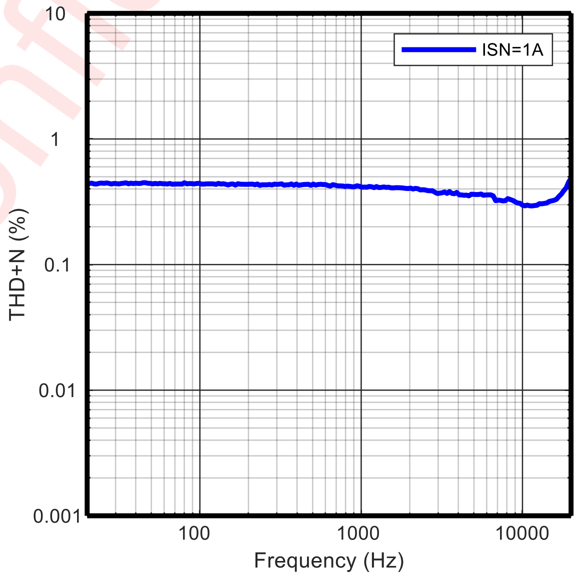


Figure 23 Real Time Current Monitor THD VS. Frequency (VCC=14.4V, ISN=1A)



Functional Description

OPERATION COMPATIBILITY VS BATTERY

The device compatibility vs battery is as below[Note4]:

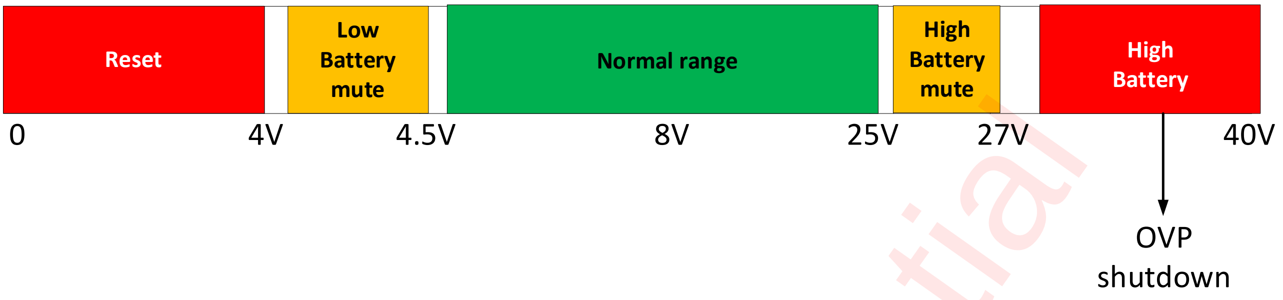


Figure 24 Operation vs battery

Note4: For diagnostic DC or AC voltage in the range of 4.5 V to 8 V, the validity of VCC/GND diagnostic results is not guaranteed. Users can verify data validity after each diagnostic cycle via the diagnostic data validity bits over I^2C.

MUTE PIN

When the MUTE pin is low, the device is muted. Internally, a pull-up current is connected to this pin to keep the device operational when the pin is floating externally. To drive the MUTE pin low (low/high thresholds are specified in the electrical characteristics table), an external pull-down open drain is required, and R_{mute} must be < 100 kΩ.

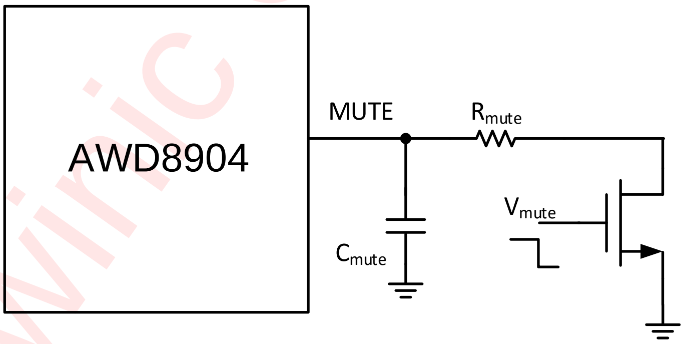


Figure 25 MUTE pin schematic

OPERATION MODE

The device supports 5 operation modes.

Mode	Condition	Description
Power-Down	VCC < 3V V_{Enable} < 1.2V	Power supply is not ready, chipset is power down.
Stand-By	VCC > V_{UVL} V_{Enable} > 1.2V	Power supply is ready, most parts of the device are power down for low power consumption except I²C interface.
Power-Up	Enable Pin = 1 PGM_OK = 1	Device is biased while boost and Class-D output is floating. System configuration carried out in this mode.
ECO		Amplifier is operating except the power stage.
Play-Mute	Mute：PWM_ON=1 Play：PLAY_ON=1	The device is fully operational in this mode.

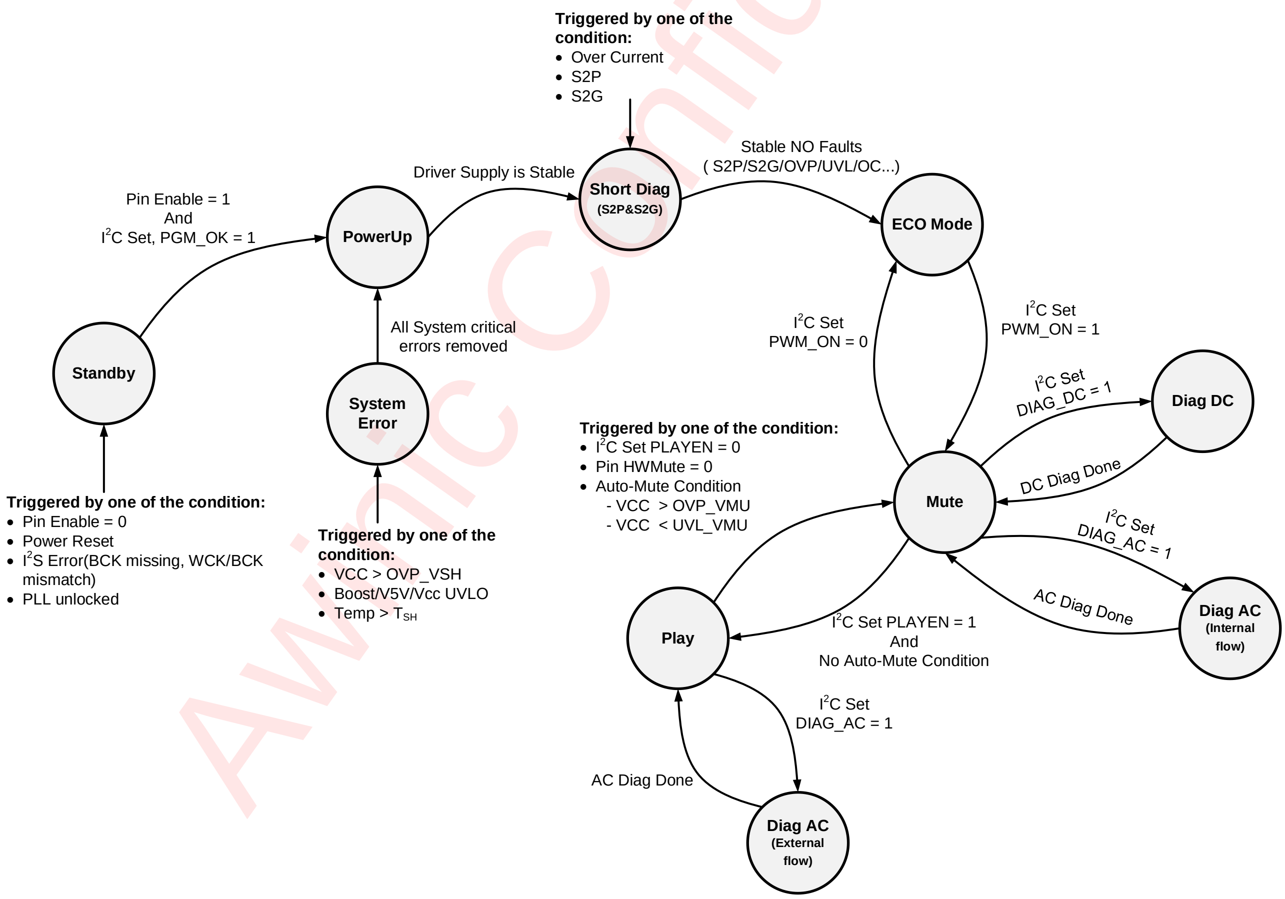


Figure 26 Device operating modes transition

POWER-DOWN MODE

The device enters power-down mode when any of the following events occurs:

- VCC < 2.65 V
- V_{Enable} < 1.2 V

In this mode, all internal circuits of the device are shut down except for the power-on reset circuit. The I²C interface is not accessible, and all internal configurable registers are reset to their default values.

The device will automatically exit power-down mode when all supply voltages are within valid ranges:

VCC > V_{UVL} and Enable goes HIGH.

STANDBY MODE

The device enters standby mode when the power supply voltages are within the valid range and the Enable pin is low. During this mode, the I²C interface remains accessible, while other modules remain powered down. Users can set the device to Standby mode when it is not needed to operate.

POWER-UP MODE

The device switches to Configuring mode when:

- Enable Pin = 1;
- PGM_OK = 1;

In this mode the internal bias, OSC, PLL will start to work.

ECO MODE

The device is operational in this mode except the power stage. Internal power, amplifier loop circuits will start to work. After the driver supply is stable, the device enters diagnostic mode. Once the device is stable and detects no faults(S2P/S2G/OVP/UVL/OC…), it transitions to ECO mode.

Detail description for each step is listed in the following table.

PLAY-MUTE MODE

The amplifier can switch from ECO mode to Mute state by selecting the "PWM_ON" command via the I²C bus (0x0E, Bit4; 0x0F, Bit4; 0x10, Bit4; 0x11, Bit4). This operation activates the PWM signal at the output. When in mute state, the amplifier can transition to play state by sending the "PLAY_ON" I²C command, and return to mute state from play state by manipulating the same data bit. The transition duration between mute and play states can be configured via the I²C bus (0x05 Bit6-Bit7).

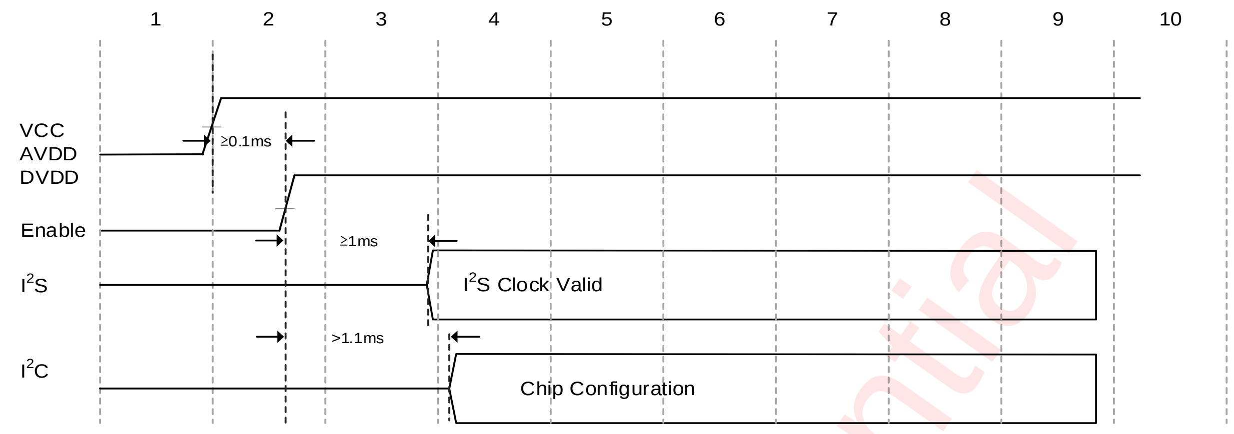
Some external conditions may automatically trigger the amplifier's mute function:

• Low battery mute
• High battery mute
• Thermal mute
• Hardware pin mute

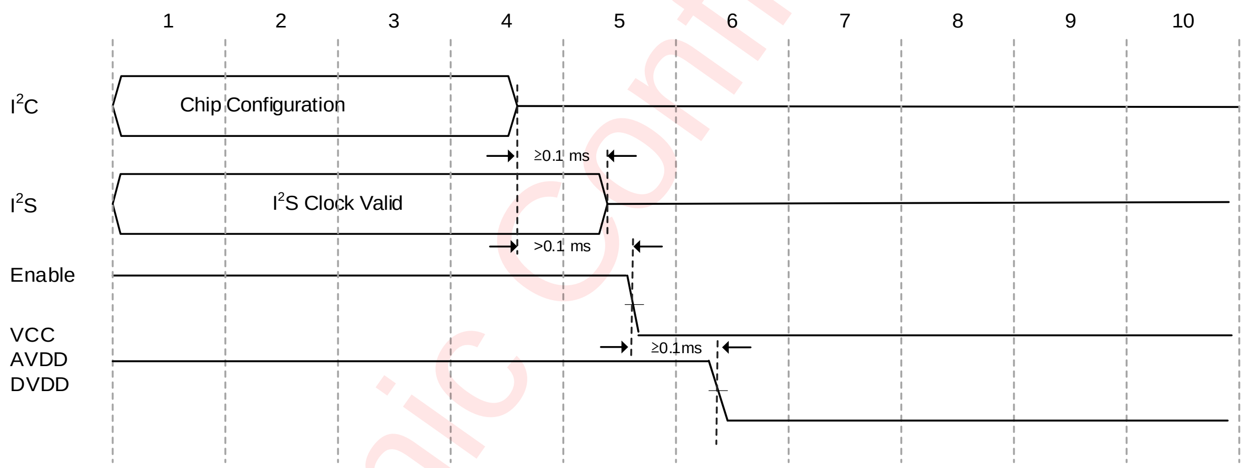
The transition from Eco-mode to Mute state (PWM-ON) must adhere to the following operational sequence:

- Single-Channel Processing: Only one channel can be switched at a time
- Interval Delay: Approximately 100 μs interval must be maintained between channel operations

Power up sequence considering I²S, I²C timing shows as below:



Power down sequence considering I²S, I²C timing shows as below:



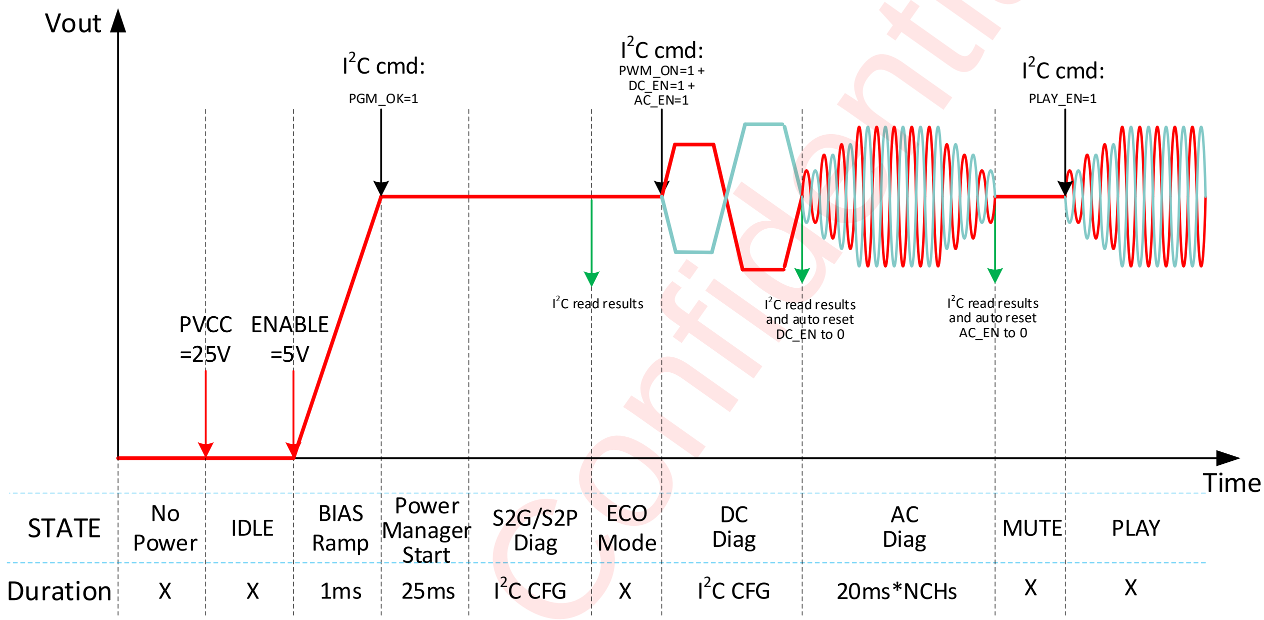
DIAGNOSTIC AND PROTECTION FUNCTION

AWD8904 amplifier provides diagnostic functions for detecting several possible fault conditions. Any warning information will be stored in the I²C interface and kept until the first I²C bus reading operation is performed.

Every channel of the amplifier can perform its own DC or AC diagnostics independently of the other channels. This flexibility allows the system to analyze one single channel while the other channels are operating. If DC diagnostic start commands are sent to all 4 channels in a single I²C instruction, all 4 diagnostics will be performed simultaneously; when AC diagnostic start commands are sent to all 4 channels similarly, the 4 diagnostics will be performed sequentially.

The DC/AC diagnostic results are NOT guaranteed to be valid when the VCC supply voltage is lower than 8V.

DC & AC Diag timeline:



Note1: HWMUTE pin connect to 5V supply at any time as needed.
Note2: CD/Diag pin connect to 3.3V supply for pull-up, after ENABLE=5V.

DC INTERNAL DIAGNOSTIC

The DC load diagnostics are used to verify the load connected. The DC diagnostics consists of four tests: short-to-power (S2P), short-to-ground (S2G), open-load (OL), and shorted-load (SL). The S2P and S2G tests trigger if the impedance to GND or a power rail is below. The diagnostic detects a short to vehicle battery, even when the supply is boosted. The SL test has an I²C-configurable threshold depending on the expected load to be connected. Because the motors connected to each channel might be different, each channel can be assigned a unique threshold value.

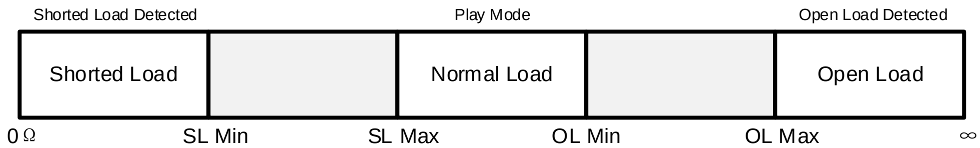
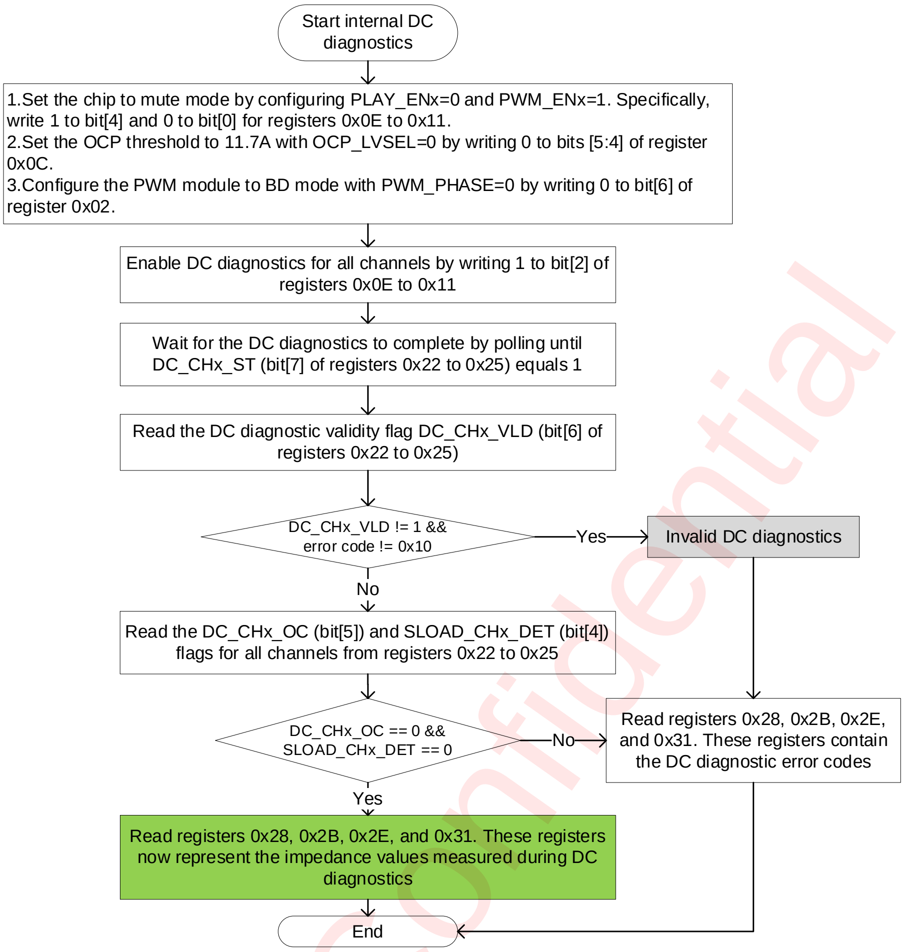


Figure 27 DC Load Diagnostic Reporting Thresholds



Error code can be read in 0x28/0x2B/0x2E/0x31 when test is ended but invalid (0x22[Bit7-6]/0x23[Bit7-6]/0x24[Bit7-6]/0x25[Bit7-6] ='10').

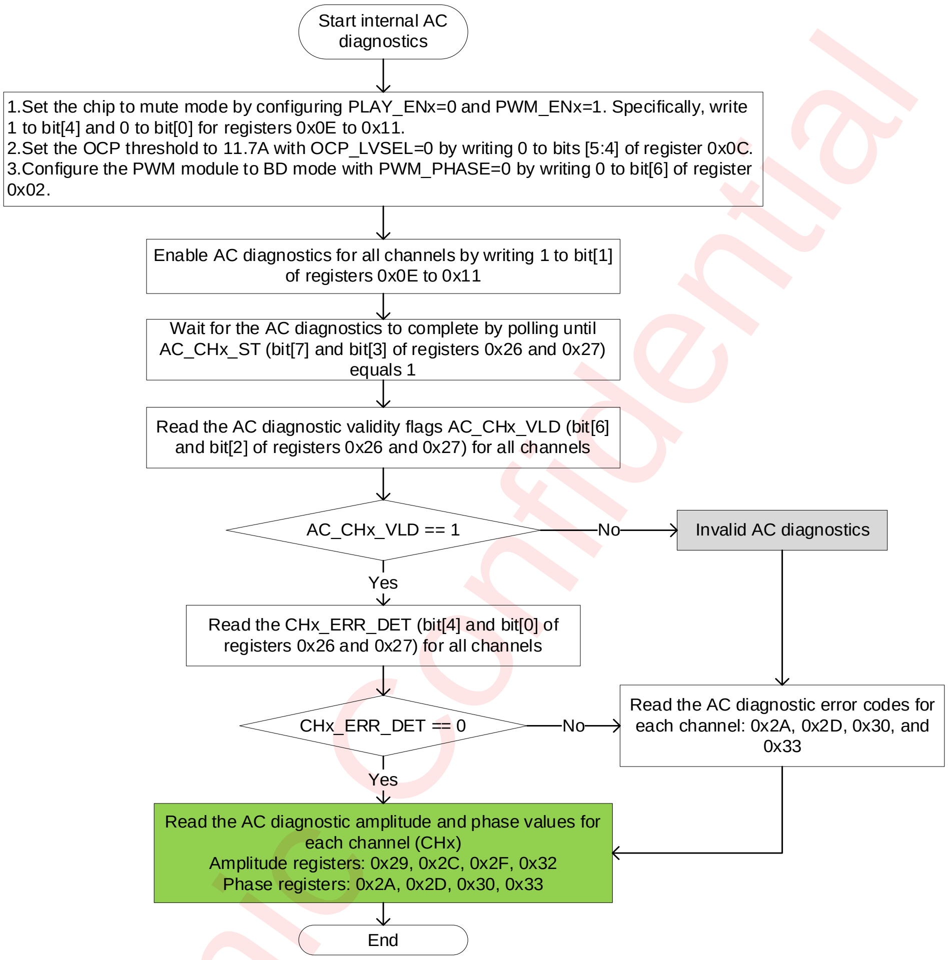
The first event in the table represents a particular case: error code can be read when test is ended and valid (0x22[Bit7-4]/ 0x23[Bit7-4]/ 0x24[Bit7-4]/ 0x25[Bit7-4] = '1111')

Error Code	What happened	Diagnostic Result
1000 0001	Overcurrent	Test not valid
1000 0010		
1000 0011	Supply voltage went low causing current measurement clipping or voltage clipping	Test not valid
1000 0100		
1000 0101	Abnormal current injection	Test not valid
1000 0110		
1000 0111		
1000 1000		

AC INTERNAL DIAGNOSTIC

The AC load diagnostic is used to determine the proper connection of the motor load when used with a passive crossover. Usually, the AC diagnostic uses a sinusoidal stimulus to verify if the tweeter is present measuring the impedance connected to the outputs and give a result according to a threshold. It is controlled through I²C. The AC diagnostic can be performed both with internally generated signals (AC internal diagnostic) and with externally generated signals (AC external diagnostic).

AC internal diagnostic requires an internal signal and reports the approximate load impedance and phase. When AC internal diagnostic is in progress, the positive output of AWD8904 is automatically fixed at half VCC in order to enhance diagnostic precision. During this time, Voltage gains GV are directly managed by the internal logic. The result is then independent from GV. If multiple channels must be tested, the diagnostics should be run in series.



Error code can be read in 0x2A/0x2D/0x30/0x33 when test is ended but invalid (0x26[Bit7-Bit6]/ 0x27[Bit7-Bit6] = ‘10’).

The last 2 events in the table represent a particular case: error code can be read when test is ended and valid

(0x26[Bit7-Bit4]/ 0x27[Bit7-Bit4] = ‘1101’). The flag on Bit 0x26[Bit4]/ 0x27[Bit4] indicates that the information written in the registers 0x2A/0x2D/0x30/0x33 is related to an error code and not to a phase value. Moreover, the load stored in 0x29/0x2C/0x2F/0x32 is always 0 Ω.

Error Code	What happened	Diagnostic Result
1000 1001	Overcurrent	Test not valid
1000 1010	Supply voltage went low causing current measurement clipping or voltage clipping	Test not valid
1000 1011		
1000 1100	Abnormal current injection	Test not valid
1000 1101		

1000 1110		
1000 1111		
1001 0000	Short	Test not valid
1001 0001		

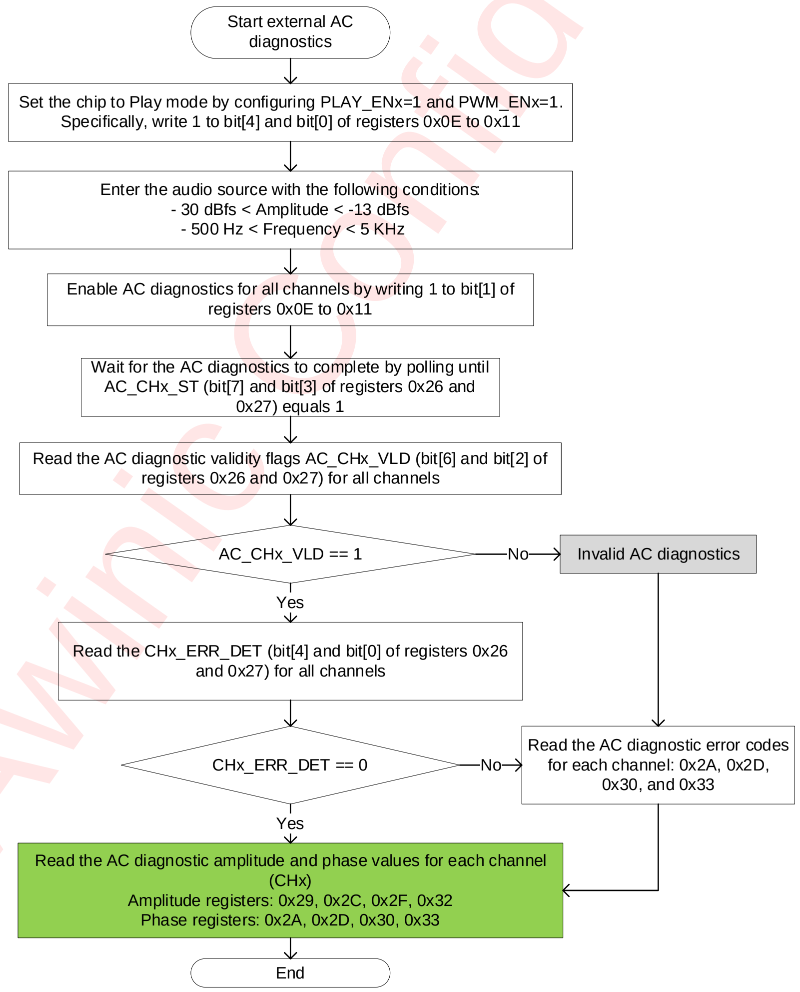
AC EXTERNAL DIAGNOSTIC

This kind of diagnostic allows to check the impedance of the load using a user-defined signal. The algorithm is the same used for the AC diagnostic with internally generated signal and it permits to measure the load impedance magnitude and phase at a desired frequency.

It is needed to send a sinusoidal signal by I²S, put the device in play selecting the channels to be tested and set the AC diagnostic I²C bits to “1” keeping the play/mute bit set to “1”.

At the end of the diagnostic cycle the “Start Diag AC” instruction bits are set back to “0” by the device itself.

Since the algorithm works when the device is in “PLAY” state, any I²C setting that influences signal also impacts the results of the diagnostics. Therefore, it is important that the signal will not be subjected to modifications in amplitude and frequency, during the whole test.



IMPEDANCE-METER RESULT COMMUNICATION

The impedance-meter is activated while “DC diagnostic” and “AC diagnostic with internal generated signals” are running and provides the user with the value of the load across the outputs. Impedance-meter results are communicated via I²C data register from 0x28h to 0x33h. Impedance-meter AC is activated running the AC diagnostic and the results are stored in module and phase.

• Magnitude is stored in: 0x29h (CH1), 0x2Ch (CH2), 0x2Fh (CH3), 0x32h (CH4).

• Phase is stored in: 0x2Ah (CH1), 0x2Dh (CH2), 0x30h (CH3), 0x33h (CH4)

The impedance-meter function is automatically activated running the DC diagnostic and the results are stored in:

• DC output load Resistance 0x28h (CH1), 0x2Bh (CH2), 0x2Eh (CH3), 0x31h (CH4).

The load resistance/AC-magnitude values written in the register are represented by 7 significant bits and 1bit as a multiplier, according to the following format representation:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0 → M = 0.1 1 → M = 1.0	C[6]	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]

The resistance could be calculated using this formula:

$R = M \times DP \times C[6:0]$

Where:

DP is the factor to be applied for parallel mode operation:

• 1 in standard mode

NOISE GATING

Noise gating is an automatic noise reduction feature that activates when output signal reaches not audible levels. When input signal levels fall below -120dBFS the system activity is automatically optimized in order to limit the output noise level as much as possible. The noise gating process has a 500ms watching time before turning on, in order to avoid spurious activations.

The feature is enabled by default and can be disabled selecting 0x02[Bit7].

PWM PULSE SKIPPING DETECTOR

The pulse skipping detector aim is to detect the PWM stage saturation.

When at least 6 consecutive PWM commutations have been skipped for each output, the feature detects pulse skipping.

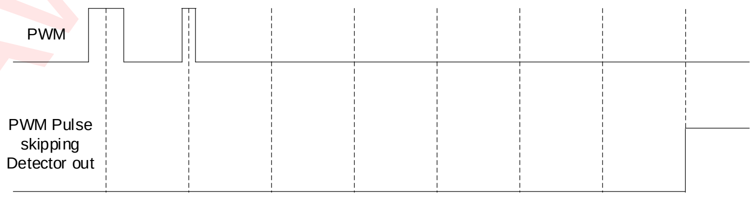


Figure 28 PWM pulse skipping detector operation

In order to enable the PWM pulse skipping detector on CD diag pin, the user must set 0x04 [Bit7:Bit6] = 'PWM pulse skipping detector'. The feature provides the output in two forms:

• Enables the pull down on CD diag pin if 0x04 [Bit6:Bit7] = 'PWM pulse skipping detector'

• The flag 0x21[Bit0:Bit3] = 4b'1111, for channel 1,2,3,4

As soon as the pulse skipping condition is removed, both the outputs are reset. The suggested utilization for this function is to connect a low-pass filter to CD diag pin, therefore comparing the output with a voltage threshold.

CONFIGURABLE CLIPPING DETECTOR

This block implements an algorithm to detect the presence of the clipping on an output larger than a selectable percentage of distortion on a sinewave signal.

This is obtained evaluating the time a clipping input is set with respect to a voltage signal considered as a sine wave.

You can enable/disable this function and choose thresholds by I^{2}C bits 0x0B[Bit2-Bit1] according to this table:

0x0B[Bit2-Bit1]	Threshold
00	Clipping detector disabled
01	CD1
10	CD2
11	CD3

Selecting by I^{2}C bits0x04 [Bit7:Bit6] = ‘Configurable Clipping Detector’, the “Configurable Clipping Detector” information on CD/Diag pin, the pin will go to low logic value, “0”, when the configurable clipping detector threshold selected is reached.

PROTECTION FUNCTION

OVER CURRENT PROTECTION (OCP)

Under severe short-circuit event, such as a short to VCC or ground, the device uses a peak-current detector, and the CLASSD Amplifier outputs enter high impedance immediately if the peak current increases to large enough. The Amplifier shutdown speed depends on some factors, such as the impedance of the short circuit, VCC supply voltage. The OCP event will be indicated on the CD/Diag pin, and the I^{2}C register saves a fault record.

INPUT OFFSET DETECTION

If the device detects the input offset higher than -18dBFS , the offset detector flag 0x20[Bit7] changed to “1”. And This function can enable or disable through set the 0x01[Bit2]. The input offset detector is working during PLAY and MUTE mode.

OUTPUT OFFSET DETECTION

if the different output exceed 1.5V for a long time, the device be judged as an output DC error, its activation when 0x01[Bit1]=”1”. The output offset time can set through 0x06[Bit3-Bit2]. The flag on I^{2}C bit (0x34[Bit5], 0x35[Bit5], 0x36[Bit5], 0x37[Bit5]). When the fault condition is removed, both the flag and the Offset Detection time, (0x06[Bit2-Bit3]), counter are reset.

OVERTEMPERATURE SHUTDOWN

The device shuts down when the die junction temperature reaches the overtemperature threshold. The device asserts the CD/Diag pin and updates I^2C register. Recovery is automatic when the temperature returns to a safe level.

UNDERVOLTAGE(UV)

The undervoltage (UV) protection detects low voltages on VCC (UVLO threshold can see electrical characteristics table). In the event of an undervoltage condition, the device evolves to “UVLO” state.

OVERVOLTAGE(OV) AND LOAD DUMP

The Overvoltage (OV) protection detects high voltages on VCC. If VCC reaches the overvoltage threshold, the device updates the I^2C register. The device can withstand 40V load-dump voltage spikes.

TEMPERATURE INFORMATION

The device has a thermal sensor to get the chip temperature via I^2C bus. The temperature can be read from the I^2C about register 0x3C[Bit0-Bit1] and 0x3D[Bit 0-Bit7], by means of 10 bits expressed in 2- complements, in which each bit represents about 1°C.

Die Temperature= 2complemet(0x3C[Bit 0-Bit 1] 0x3D[Bit 0-Bit 7])

Example:

0x3C = “xxxxxx00” 0x3D = “01000110” → Thermal reading= “0001000110” 10 bits-2complement →70°C

0x3C = “xxxxxx00” 0x3D = “00010111” → Thermal reading= “0000010111” 10 bits-2complement →23°C

0x3C = “xxxxxx11” 0x3D = “11101001” → Thermal reading= “1111101001” 10 bits-2complement →-23°C

LOCAL THERMAL PROTECTION

To protect the output stage of the device against local high temperature, a local thermal protection is embedded on each channel. Activation of the local thermal protection will cause the impacted channel to be muted and the related I^2C data bit is set to ‘1’ (0x20h[3] for channel 1, 0x20h[4] for channel 2, 0x20h[5] for channel 3, 0x20h[6] for channel 4).

Note: when the Local thermal protection is activated on a channel, also OCP flag is set. For example in case of thermal protection activation on channel 1, 0x20h[3] = 1, also 0x22h[5] = 1, OCP activated on channel 1.

OPEN LOAD WITH PLAY

The open load with play mode is implemented to monitor possible motor detachment during PLAY state. This feature reuses the existing data path without interrupting normal operation, while supporting both single-shot and real-time detection mechanisms.

This function will automatically detect whether the input signal is valid, which can be observed through 0x34-0x37[Bit1].

- Single mode, configure 0x0D[Bit7- Bit4] for each channel OL enable. After approximately 500ms, the detection is completed and 0x0D[Bit7- Bit4] will be automatically reset.
- Real-time mode, set 0x0B[Bit5] to 1’b1. 0x0D[Bit7- Bit4] still enable each channel OL, but will no longer be reset and the detection results will be updated in real-time.

Regardless of the detection mode, open load result value on 0x34-0x37[Bit0] is significant only if the test is valid (0x34-0x37[Bit1]) and test is finished (0x34-0x37[Bit2]).

SOFTWARE RESET

Writing 0xAA to register ID (0x41) via I²C interface will reset the device internal circuits and all configuration registers.

LOW LATENCY

AWD8904 supports low latency mode to meet customers' low latency requirements for ANC and other scenarios.

FS	Condition	Group Delay (Input 1kHz)
44.1kHz	Low Latency OFF	500μs
	Low Latency ON	110μs
48kHz	Low Latency OFF	460μs
	Low Latency ON	100μs
96kHz	Low Latency OFF	235μs
	Low Latency ON	60μs
192khz	Low Latency OFF	125μs
	Low Latency ON	35μs

MUTE

This module performs mute control for the output waveform.

EXTERNAL COMPONENTS GUIDELINE

Quantity	Designator	Value	Description	Function	Tolerance [%]	Rated Current[A]/ Voltage[V]/ Power [W]	Package
1	C1	4.7 µF	SMD MLCC X7R Capacitor	Floating Regulators	10%	25 V	0805
3	C2, C29, C33	100 nF	SMD MLCC X7R Capacitor	Floating Regulators	10%	25 V	0603
8	C5, C8, C10, C15, C17, C20, C22, C27	220 nF	SMD MLCC X7R Capacitor	Damping network	10%	50 V 0.25 W	0805
8	C7, C9, C11, C14, C19, C21, C23, C26	150 nF	SMD MLCC X7R Capacitor	Demodulator filter	10%	50 V	0805
11	C28, C42, C44, C48, C49, C58, C59, C62, C63, C64, C65	100 nF	SMD MLCC X7R Capacitor	Floating Regulators	10%	50 V	0603
2	C47, C61	2.2 µF	SMD MLCC X7R Capacitor	Supply filter	10%	50 V	1210
2	C41, C43	1 µF	SMD MLCC X7R Capacitor	Supply filter	10%	50 V	0805
1	C30	22 µF	SMD MLCC X7S Capacitor	Floating Regulators	10%	25 V	0805
1	C31	10 pF	SMD MLCC C0G/NP0 Capacitor	Floating Regulators	10%	25 V	0603
1	C32	10 µF	SMD MLCC X7R Capacitor	Floating Regulators	20%	50 V	1210
1	C36	2.2 µF	SMD MLCC X7R Capacitor	Floating Regulators	10%	25 V	0805
1	C38	47 pF	SMD MLCC C0G/NP0 Capacitor	Floating Regulators	5%	25 V	0603
8	L1, L2, L3, L4, L5, L6, L7, L8	3.3 µH	SMD Power Inductor	Demodulator filter	20%	11.6 A	
1	L9	10 µH	SMD Power Inductor	Floating regulators	20%	2 A	
8	R4, R6, R9, R10, R12, R14, R17, R18	4.7 Ω	Surface mount chip resistor	Damping network	1%	200 V 0.25 W	1210
1	R21	10 Ω	Surface mount chip resistor	Floating regulators	1%	150 V 0.5 W	0805

DIGITAL INTERFACE

The state of each digital input and output are shown in below table. After power on, the input signal pin BCK, WCK, DATAI are set to high impedance by default. If I²S TXEN bit is enabled, DATAO is actively driven when outputting data otherwise it is high impedance by default.

Digital I/O	Type	Description (Default State)
SCL	Input	Hi-Z
SDA	Input	Hi-Z
INTN	Output	Hi-Z
AD	Input	Weak pull down
BCK	Input	Hi-Z
WCK	Input	Hi-Z
DATA1	Input	Hi-Z
DATA2	Input/Output	Hi-Z

DIGITAL INTERFACE

Wave data is transferred between the host processor and the device via the Digital Interface. The digital interface is in full-duplex via 4 dedicated pins:

- BCK
- WCK
- DATA1
- DATA2

Two-slot I²S and 4/8/16-slot TDM are supported in this device. The digital Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via 0x46[Bit3-Bit2]. These modes are all MSB-first, with data width programmable via 0x46[Bit5-Bit4].

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 44.1 kHz, 48 kHz, 96 kHz and 192kHz. The max output signal frequency is 80kHz. It is selected via configurable register I²S CTRL1. I²S SR.

The bit clock BCK is used to sample the digital wave data across the digital interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register 0x46[Bit1-Bit0]. The frequency of BCK can be calculated according to the following equation:

BCK frequency = ***SampleRate * SlotLength * SlotNumber***

SampleRate: Sample rate for this digital interface;

SlotLength: The length of one wave slot in unit of BCK clock;

SlotNumber: How many slots supported in this interface. For example: 2-slot supported in I²S mode, 4/8/16-slot supported in TDM mode.

The word selects and bit clock signals of the I²S input are the reference signals for the digita interface and Phased Locked Loop (PLL).

The waveform source can be from left channel, right channel or the average of the left and right channel, which is controlled by I²S CTRL1.CHSEL.

Interface format(MSB first)	Data width	BCK frequency
Standard I²S	16b/20b/24b/32b	32fs/48fs /64fs
left-justified	16b/20b/24b/32b	32fs/48fs /64fs
right-justified	16b/20b/24b/32b	32fs /48fs /64fs

The output port DATAO, can be enabled or disabled via bit SYSCTRL. I²S TXEN. The unused slots can be set to Hi-z or zero, which is controlled by I²S CTRL3.DOHZ.

STANDARD I²S MODE

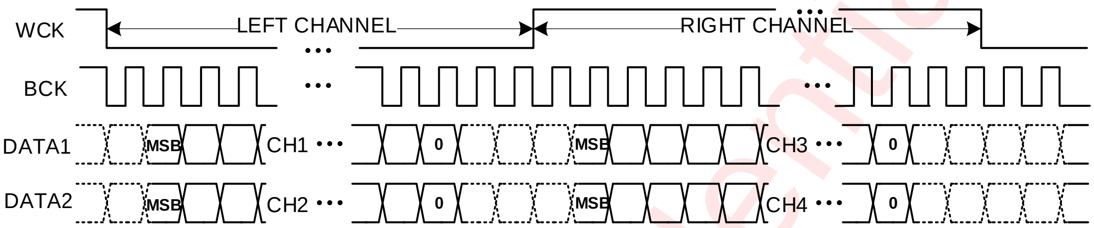


Figure 29 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

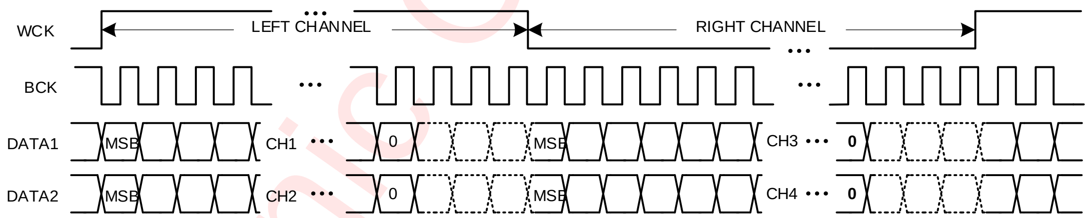


Figure 30 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

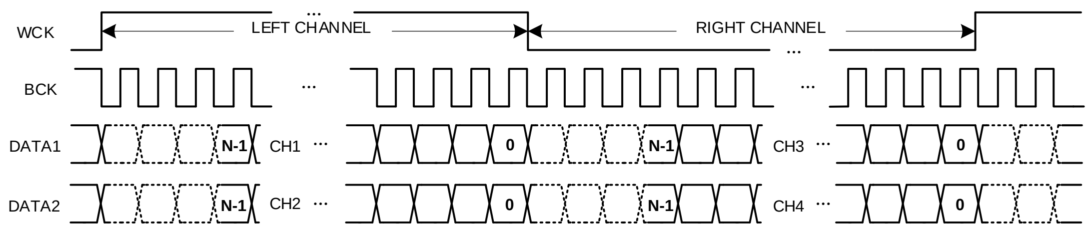


Figure 31 I²S Timing for Right-Justified Mode

- When WCK is high indicating the left channel data, and WCK=0 indicating the right channel data.
- The LSB (Bit0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (Bit0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

TDM MODE

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 1/2/4/6/8/16-slot is supported in TDM mode, while 2-slot is supported in I²S mode. 4-slot in TDM mode for example:

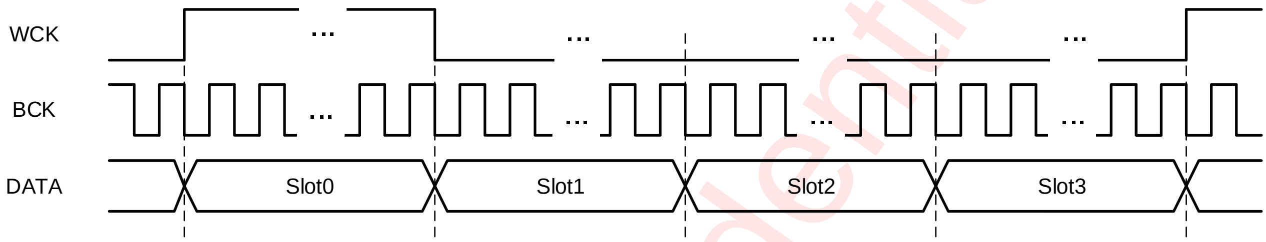


Figure 32 TDM Timing

Note: The high level pulse width of WCK signal can be one slot time or one period of BCK.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode plus at 1MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ.

DEVICE ADDRESS

The I²C device address (7-Bit) can be set using the AD pin according to the following table: The AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 11011xx. The permitted I²C addresses are 0x6C(7-Bit) through 0x6F(7-Bit).

AWD8904 supports legacy mode which can work without I²C. In legacy mode, The device automatically performs start-up sequence to work with a fixed configuration

Address	Address(7-Bit)
R_ADDSEL0	0x6C
R_ADDSEL1	0x6D
R_ADDSEL2	0x6E
R_ADDSEL3	0x6F
R_LEGACY	LEGACY Mode

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

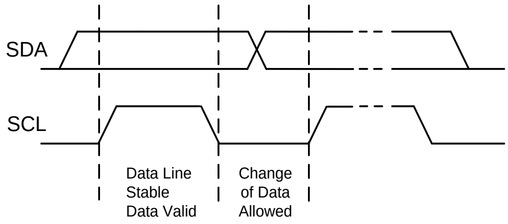


Figure 33 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

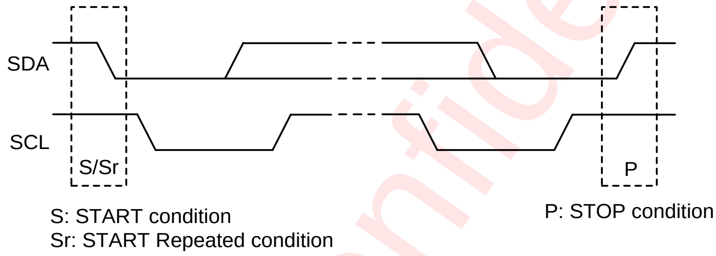


Figure 34 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

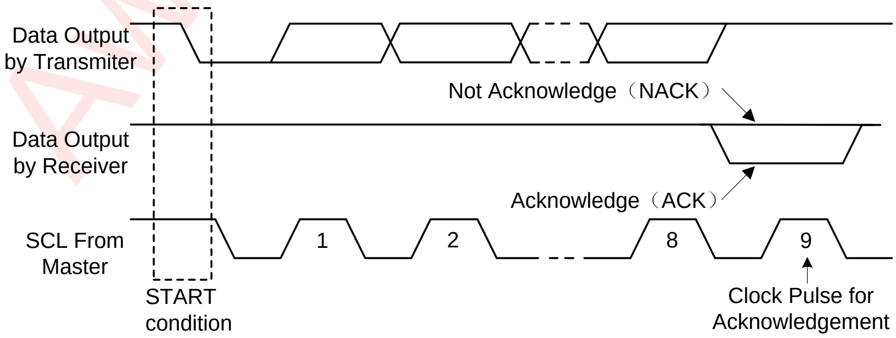


Figure 35 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-Bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-Bit)

e) Slave sends acknowledge signal

f) Master sends high data byte of 8-Bit data to be written to the addressed register

g) Slave sends acknowledge signal

h) Master sends low data byte of 8-Bit data to be written to the addressed register

i) Slave sends acknowledge signal

j) If master will send further 8-Bit data bytes, the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g)

k) Master generates STOP condition to indicate write cycle end

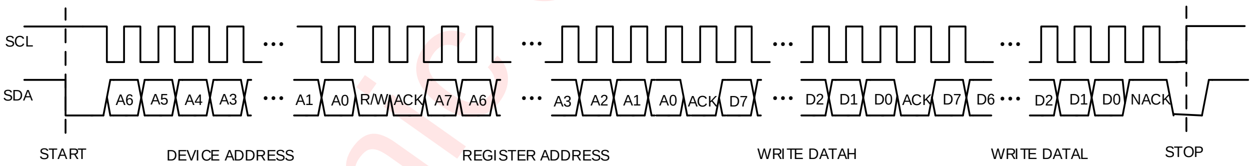


Figure 36 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-Bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-Bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-Bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 8-Bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 8-Bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 8-Bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.

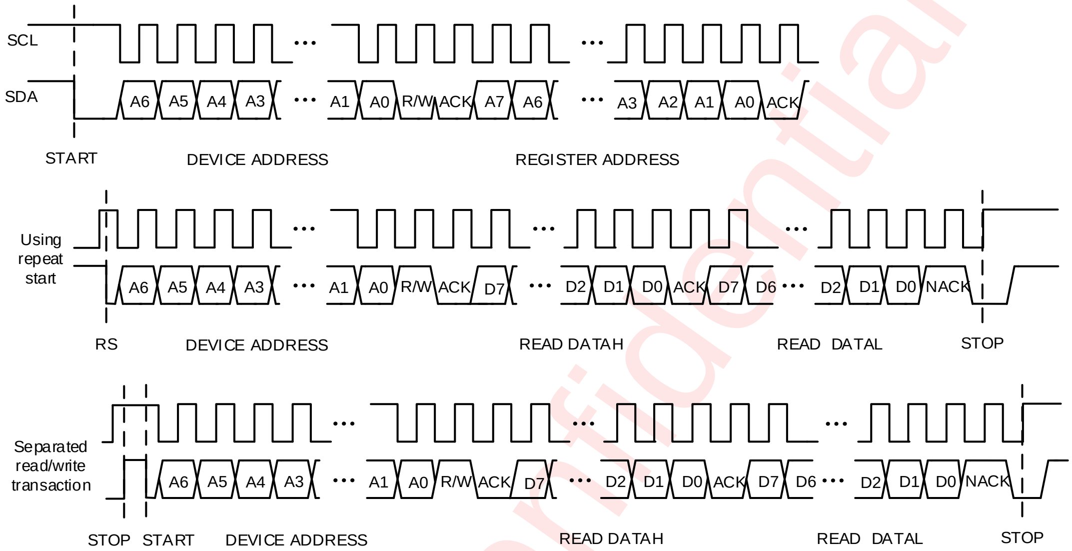


Figure 37 I²C Read Byte Cycle

REGISTER MAP

REGISTER DESCRIPTION

REGISTER LIST

Adress	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	RW	SLOT_NUM		SLOT_SEL		I2SSR		I2C_WEN	
0x01	RW					HDCCE	VOFFIN_EN	VOFFOUT_EN	
0x02	RW		PWM_PHASE						
0x03	RW		OT_DIAG_DISABLE	OT_DIAG_SEL		OC_DIAG_EN	VOFFIN_DIAG_EN	VOFFOUT_DIAG_EN	
0x04	RW	CLIP_DIAG_SEL		FAST_BOOST_EN					
0x05	RW	MUTE_SPEED							
0x06	RW	DIAG_RAMP_TTH		DIAG_HOLD_TTH		SHORT_TTH		VOL_UP	
0x07	RW	DIAG_RESULT_MODE							
0x0A	RW	ISN_IMAX							
0x0B	RW	SHORT_LOAD_TH	OPEN_LOAD_TH				CLIP_SEL		
0x0C	RW	MUTE_DISABLE	OCP_PLUS_EN	OCP_LVSEL		PWM_ON_DATA2			WTD_DISABLE
0x0D	RW	OPEN_LOAD_CH1	OPEN_LOAD_CH2	OPEN_LOAD_CH3	OPEN_LOAD_CH4				
0x0E	RW	IMONITOR_CH1	SET_GAIN1		PWM_ON1		DC_EN1	AC_EN1	PLAY_EN1
0x0F	RW	IMONITOR_CH2	SET_GAIN2		PWM_ON2		DC_EN2	AC_EN2	PLAY_EN2
0x10	RW	IMONITOR_CH3	SET_GAIN3		PWM_ON3		DC_EN3	AC_EN3	PLAY_EN3
0x11	RW	IMONITOR_CH4	SET_GAIN4		PWM_ON4		DC_EN4	AC_EN4	PLAY_EN4
0x13	RW						SLOPE_SPEED		
0x17	RW								PGM_OK
0x18	RW							PWM_FREQ_SEL	
0x20	RO	VOFFIN_DET	OTP_CH4_DET	OTP_CH3_DET	OTP_CH2_DET	OTP_CH1_DET	DUMP_DET	UVLO_VCC_DET	PLL_LOCK
0x21	RO	OTW1_DET	OTW2_DET	OTW3_DET	OTW4_DET	CLIP_CH1_DET	CLIP_CH2_DET	CLIP_CH3_DET	CLIP_CH4_DET
0x22	RO	DC_CH1_ST	DC_CH1_VLD	DC_CH1_OC	SLOAD_CH1_DET	S2P_CH1_DET	S2G_CH1_DET	OLOAD_CH1_ST	PLAY_CH1_DET
0x23	RO	DC_CH2_ST	DC_CH2_VLD	DC_CH2_OC	SLOAD_CH2_DET	S2P_CH2_DET	S2G_CH2_DET	OLOAD_CH2_ST	PLAY_CH2_DET
0x24	RO	DC_CH3_ST	DC_CH3_VLD	DC_CH3_OC	SLOAD_CH3_DET	S2P_CH3_DET	S2G_CH3_DET	OLOAD_CH3_ST	PLAY_CH3_DET
0x25	RO	DC_CH4_ST	DC_CH4_VLD	DC_CH4_OC	SLOAD_CH4_DET	S2P_CH4_DET	S2G_CH4_DET	OLOAD_CH4_ST	PLAY_CH4_DET
0x26	RO	AC_CH1_ST	AC_CH1_VLD	TWE_CH1_NPRESENT	CH1_ERR_DET	AC_CH2_ST	AC_CH2_VLD	TWE_CH2_NPRESENT	CH2_ERR_DET
0x27	RO	AC_CH3_ST	AC_CH3_VLD	TWE_CH3_NPRESENT	CH3_ERR_DET	AC_CH4_ST	AC_CH4_VLD	TWE_CH4_NPRESENT	CH4_ERR_DET
0x28	RO	DC_CH1_INFO							
0x29	RO	AC_CH1_INFO1							
0x2A	RO	AC_CH1_INFO2							
0x2B	RO	DC_CH2_INFO							
0x2C	RO	AC_CH2_INFO1							

0x2D	RO	AC_CH2_INFO2							
0x2E	RO	DC_CH3_INFO							
0x2F	RO	AC_CH3_INFO1							
0x30	RO	AC_CH3_INFO2							
0x31	RO	DC_CH4_INFO							
0x32	RO	AC_CH4_INFO1							
0x33	RO	AC_CH4_INFO2							
0x34	RO	FRAME_ERR_DET		VOFFOUT_CH1_DET	IOFFOUT_CH1_DET	IOFFOUT_CH1_VLD	OLOAD_CH1_FINISH	OLOAD_CH1_SIGVLD	OLOAD_CH1_DET
0x35	RO	IM_DIS_ST	CURR_DB_TXDIS	VOFFOUT_CH2_DET	IOFFOUT_CH2_DET	IOFFOUT_CH2_VLD	OLOAD_CH2_FINISH	OLOAD_CH2_SIGVLD	OLOAD_CH2_DET
0x36	RO			VOFFOUT_CH3_DET	IOFFOUT_CH3_DET	IOFFOUT_CH3_VLD	OLOAD_CH3_FINISH	OLOAD_CH3_SIGVLD	OLOAD_CH3_DET
0x37	RO			VOFFOUT_CH4_DET	IOFFOUT_CH4_DET	IOFFOUT_CH4_VLD	OLOAD_CH4_FINISH	OLOAD_CH4_SIGVLD	OLOAD_CH4_DET
0x3C	RO							TEMP_H	
0x3D	RO	TEMP_L							
SC		Note: The hardware can only set the flag, I²C read will clear the flag.							

DETAILED REGISTER DESCRIPTION

(Address 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	SLOT_NUM	RW	I²S slot number selection. 00: I²S standard 01: TDM4 10: TDM8 11: TDM16	0
5:4	SLOT_SEL	RW	I²S channel slot selection. 00: 1-4(TDM8/TDM16) 01: 5-8(TDM8/TDM16) 10: 9-12(TDM16) 11: 13-16(TDM16)	0
3:2	I²S SR	RW	I²S input sample rate selection. 00: 44.1kHz 01: 48kHz 10: 96kHz 11: 192kHz	0
1:0	I²C_WEN	RW	I²C write enable selection. 10: Enable Others: Disable	0

(Address 01h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RW	Not used	0
3	HDCCE	RW	Hardware DC Canceling enable selection. 0: Disable 1: Enable	0
2	VOFFIN_EN	RW	Input voltage offset detector enable selection. 0: Disable 1: Enable	0
1	VOFFOUT_EN	RW	Output voltage offset detector enable selection. 0: Disable 1: Enable	0
0	Reserved	RW	Not used	0

(Address 02h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0

6	PWM_PHASE	RW	CH1-CH4 AD_BD mode select: 0: BD mode 1: AD mode	0
5:0	Reserved	RW	Not used	0

(Address 03h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6	OT_DIAG_DISABLE	RW	Over thermal warning on CD/Diag pin disable seleciton. 0: OTW on CD/Diag 1: No OTW on CD/Diag	0
5:4	OT_DIAG_SEL	RW	OTW information on CD/Diag pin selection. 00: TW1 01: TW2 10: TW3 11: TW4	0
3	OC_DIAG_EN	RW	Overcurrent on CD/Diag pin enable selection. 0: Disable 1: Enable	0
2	VOFFIN_DIAG_EN	RW	Input voltage offset on CD/Diag pin enable selection. 0: Disable 1: Enable	0
1	VOFFOUT_DIAG_EN	RW	Output voltage offset on CD/Diag pin enable selection. 0: Disable 1: Enable	0
0	Reserved	RW	Not used	0

(Address 04h)

Bit	Symbol	R/W	Description	Default
7:6	CLIP_DIAG_SEL	RW	Clipping information on CD/Diag selection. 00: No clipping 01: PWM pulse skipping detector 10: Configurable clipping detector 11: Reserved	0
5	FAST_BOOST_EN	RW	Fast Boost turn on enable selection. 0: Disable 1: Enable	0
4:0	Reserved	RW	Not used	0

(Address 05h)

Bit	Symbol	R/W	Description	Default

7:6	MUTE_SPEED	RW	Digital mute timing selection.(values with fs=44.1KHz) 00: 3ms 01: 45ms 10: 90ms 11: 185ms	0
5:0	Reserved	RW	Not used	0

(Address 06h)

Bit	Symbol	R/W	Description	Default
7:6	DIAG_RAMP_TTH	RW	Diagnostic signal ramp time selection. 00: 42ms 01: 83ms 10: 187ms 11: 21ms	0
5:4	DIAG_HOLD_TTH	RW	Diagnostic signal ramp time selection. 00: 10ms 01: 21ms 10: 42ms 11: 5ms	0
3:2	SHORT_TTH	RW	Diagnostic S2P/S2G and Output voltage offset timing selection. 00: 90ms 01: 70ms 10: 45ms 11: 20ms	0
1:0	VOL_UP	RW	Digital gain up selection. 00: 0dB 01: +6dB 10: +12dB 11: +18dB	0

(Address 07h)

Bit	Symbol	R/W	Description	Default
7	DIAG_RESULT_MODE	RW	Diagnostic results display mode selection. 0: AC diagnostic results on STATUS9-STATUS19 1: Load current values on STATUS9-STATUS19	0
6:0	Reserved	RW	Not used	0

(Address 08h)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RW	Not used	0

(Address 09h)

Bit	Symbol	R/W	Description	Default

7:0	Reserved	RW	Not used	0

(Address 0Ah)

Bit	Symbol	R/W	Description	Default
7:6	ISN_IMAX	RW	Current sense imax selection. 00: 1A 01: 2A 10: 4A 11: 8A	0
5:0	Reserved	RW	Not used	0

(Address 0Bh)

Bit	Symbol	R/W	Description	Default
7	SHORT_LOAD_TH	RW	Short load impedance threshold selection. (DC Diag) 0: 0.75Ω 1: 0.5Ω	0
6	OPEN_LOAD_TH	RW	Open load impedance threshold selection. (DC Diag & Open load) 0: 25Ω 1: 15Ω	0
5:3	Reserved	RW	Not used	0
2:1	CLIP_SEL	RW	Clipping detector basic threshold selection. 00: Clipping detector disabled 01: CD1 10: CD2 11: CD3	0
0	Reserved	RW	Not used	0

(Address 0Ch)

Bit	Symbol	R/W	Description	Default
7	MUTE_DISABLE	RW	Digital mute disable selection. 0: Work 1: Disable	0
6	OCP_PLUS_EN	RW	OCP protection threshold plus selection. 0: Standard 1: OCP_TH+1A	0
5:4	OCP_LVSEL	RW	OCP protection basic threshold selection. 00: 11.7A 01: 8.4A 10: 6.2A 11: 3.7A	0
3	PWM_ON_DATA2	RW	PWM clock output on I^2S Data2 pin enable selection. 0: I^2S Data2 standard 1: PWM clock on I^2S Data2	0

2	Reserved	RW	Reserved	0
1	Reserved	RW	Reserved	0
0	WCK_ERR_DISABLE	RW	I^2S_WS error module control. 0: Enable 1: Disable	0

(Address 0Dh)

Bit	Symbol	R/W	Description	Default
7	OPEN_LOAD_CH1	RW	CH1 Open load enable selection. 0: Disable 1: Enable	0
6	OPEN_LOAD_CH2	RW	CH2 Open load enable selection. 0: Disable 1: Enable	0
5	OPEN_LOAD_CH3	RW	CH3 Open load enable selection. 0: Disable 1: Enable	0
4	OPEN_LOAD_CH4	RW	CH4 Open load enable selection. 0: Disable 1: Enable	0
3:0	Reserved	RW	Reserved	0

(Address 0Eh)

Bit	Symbol	R/W	Description	Default
7	IMONITOR_CH1	RW	CH1 current monitor enable selection. 0: Disable 1: Enable	0
6:5	SET_GAIN1	RW	CH1 gain selection. 00: GV1-26.2V/V 01: GV2-19.3V/V 10: GV3-11.1V/V 11: GV4-7.9V/V	0
4	PWM_ON1	RW	CH1 PWM enable selection. 0: Disable 1: Enable	0
3	Reserved	RW	Not used	0
2	DC_EN1	RW	CH1 DC diag enable selection. 0: Disable 1: Enable	0

1	AC_EN1	RW	CH1 AC(Internal & External) diag enable selection. 0: Disable 1: Enable	0
0	PLAY_EN1	RW	CH1 play enable selection. 0: Mute 1: Play	0

(Address 0Fh)

Bit	Symbol	R/W	Description	Default
7	IMONITOR_CH2	RW	CH2 current monitor enable selection. 0: Disable 1: Enable	0
6:5	SET_GAIN2	RW	CH2 gain selection. 00: GV1-26.2V/V 01: GV2-19.3V/V 10: GV3-11.1V/V 11: GV4-7.9V/V	0
4	PWM_ON2	RW	CH2 PWM enable selection. 0: Disable 1: Enable	0
3	Reserved	RW	Not used	0
2	DC_EN2	RW	CH2 DC diag enable selection. 0: Disable 1: Enable	0
1	AC_EN2	RW	CH2 AC(Internal & External) diag enable selection. 0: Disable 1: Enable	0
0	PLAY_EN2	RW	CH2 play enable selection. 0: Mute 1: Play	0

(Address 10h)

Bit	Symbol	R/W	Description	Default
7	IMONITOR_CH3	RW	CH3 current monitor enable selection. 0: Disable 1: Enable	0
6:5	SET_GAIN3	RW	CH3 gain selection. 00: GV1-26.2V/V 01: GV2-19.3V/V 10: GV3-11.1V/V 11: GV4-7.9V/V	0
4	PWM_ON3	RW	CH3 PWM enable selection. 0: Disable 1: Enable	0

3	Reserved	RW	Not used	0
2	DC_EN3	RW	CH3 DC diag enable selection. 0: Disable 1: Enable	0
1	AC_EN3	RW	CH3 AC(Internal & External) diag enable selection. 0: Disable 1: Enable	0
0	PLAY_EN3	RW	CH3 play enable selection. 0: Mute 1: Play	0

(Address 11h)

Bit	Symbol	R/W	Description	Default
7	IMONITOR_CH4	RW	CH4 current monitor enable selection. 0: Disable 1: Enable	0
6:5	SET_GAIN4	RW	CH4 gain selection. 00: GV1-26.2V/V 01: GV2-19.3V/V 10: GV3-11.1V/V 11: GV4-7.9V/V	0
4	PWM_ON4	RW	CH4 PWM enable selection. 0: Disable 1: Enable	0
3	Reserved	RW	Not used	0
2	DC_EN4	RW	CH4 DC diag enable selection. 0: Disable 1: Enable	0
1	AC_EN4	RW	CH4 AC(Internal & External) diag enable selection. 0: Disable 1: Enable	0
0	PLAY_EN4	RW	CH4 play enable selection. 0: Mute 1: Play	0

(Address 12h)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RW	Not used	0

(Address 13h)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RW	Not used	0

2	SLOPE_SPEED	RW	Slope speed selection. 0: Slow 1: Fast	0
1:0	Reserved	RW	Not used	0

CFG20: (Address 14h)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RW	Not used	0

(Address 15h)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RW	Not used	0

(Address 16h)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RW	Not used	0

(Address 17h)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RW	Not used	0
0	PGM_OK	RW	System power up control bit. 0: Power down 1: Work	0

(Address 18h)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1:0	PWM_FREQ_SEL	RW	PWM frequency selection. 00: 2.286MHz 01: 2.137MHz 10: 2.457MHz 11: Reserved	0

(Address 20h)

Bit	Symbol	R/W	Description	Default
7	VOFFIN_DET	SC	Input voltage offset detect indicator. 0: Normal 1: Offset at input present	0
6	OTP_CH4_DET	SC	CH4 OTP detect indicator. 0: Normal 1: OTP on CH4	0

5	OTP_CH3_DET	SC	CH3 OTP detect indicator. 0: Normal 1: OTP on CH3	0
4	OTP_CH2_DET	SC	CH2 OTP detect indicator. 0: Normal 1: OTP on CH2	0
3	OTP_CH1_DET	SC	CH1 OTP detect indicator. 0: Normal 1: OTP on CH1	0
2	DUMP_DET	SC	Dump detect indicator. 0: Normal 1: Dump	0
1	UVLO_VCC_DET	SC	VCC UVLO indicator. 0: Normal 1: VCC_UVLO	0
0	PLL_LOCK	RO	PLL locked status indicator. 0: Unlocked 1: Locked	0

(Address 21h)

Bit	Symbol	R/W	Description	Default
7	OTW1_DET	RO	TW1 indicator. 0: Normal 1: TW1 detect	0
6	OTW2_DET	RO	TW2 indicator. 0: Normal 1: TW2 detect	0
5	OTW3_DET	RO	TW3 indicator. 0: Normal 1: TW3 detect	0
4	OTW4_DET	RO	TW4 indicator. 0: Normal 1: TW4 detect	0
3	CLIP_CH1_DET	SC	CH1 PWM pulse skipping detect indicator. 0: Normal 1: PWM pulse skipping on CH1	0
2	CLIP_CH2_DET	SC	CH2 PWM pulse skipping detect indicator. 0: Normal 1: PWM pulse skipping on CH2	0
1	CLIP_CH3_DET	SC	CH3 PWM pulse skipping detect indicator. 0: Normal 1: PWM pulse skipping on CH3	0
0	CLIP_CH4_DET	SC	CH4 PWM pulse skipping detect indicator. 0: Normal 1: PWM pulse skipping on CH4	0

(Address 22h)

Bit	Symbol	R/W	Description	Default
7	DC_CH1_ST	RO	CH1 DC diagnostic status. 0: Normal 1: DC pulse ended	0
6	DC_CH1_VLD	RO	CH1 DC diagnostic data valid. 0: Not valid or Diag not activated 1: Valid	0
5	DC_CH1_OC	SC	CH1 OC indicator. 0: Normal 1: OC on CH1	0
4	SLOAD_CH1_DET	RO	CH1 Short load indicator. 0: Normal 1: Shor Load on CH1	0
3	S2P_CH1_DET	RO	CH1 S2P indicator. 0: Normal 1: S2P on CH1	0
2	S2G_CH1_DET	RO	CH1 S2G indicator. 0: Normal 1: S2G on CH1	0
1	OLOAD_CH1_ST	RO	CH1 open load indicator. 0: Normal 1: Open load on CH1	0
0	PLAY_CH1_DET	RO	CH1 play status. 0: MUTE 1: PLAY	0

(Address 23h)

Bit	Symbol	R/W	Description	Default
7	DC_CH2_ST	RO	CH2 DC diagnostic status. 0: Normal 1: DC pulse ended	0
6	DC_CH2_VLD	RO	CH2 DC diagnostic data valid. 0: Not valid or Diag not activated 1: Valid	0
5	DC_CH2_OC	SC	CH2 OC indicator. 0: Normal 1: OC on CH2	0
4	SLOAD_CH2_DET	RO	CH2 Short load indicator. 0: Normal 1: Shor Load on CH2	0

3	S2P_CH2_DET	RO	CH2 S2P indicator. 0: Normal 1: S2P on CH2	0
2	S2G_CH2_DET	RO	CH2 S2G indicator. 0: Normal 1: S2G on CH2	0
1	OLOAD_CH2_ST	RO	CH2 open load indicator. 0: Normal 1: Open load on CH2	0
0	PLAY_CH2_DET	RO	CH2 play status. 0: MUTE 1: PLAY	0

(Address 24h)

Bit	Symbol	R/W	Description	Default
7	DC_CH3_ST	RO	CH3 DC diagnostic status. 0: Normal 1: DC pulse ended	0
6	DC_CH3_VLD	RO	CH3 DC diagnostic data valid. 0: Not valid or Diag not activated 1: Valid	0
5	DC_CH3_OC	SC	CH3 OC indicator. 0: Normal 1: OC on CH3	0
4	SLOAD_CH3_DET	RO	CH3 Short load indicator. 0: Normal 1: Shor Load on CH3	0
3	S2P_CH3_DET	RO	CH3 S2P indicator. 0: Normal 1: S2P on CH3	0
2	S2G_CH3_DET	RO	CH3 S2G indicator. 0: Normal 1: S2G on CH3	0
1	OLOAD_CH3_ST	RO	CH3 open load indicator. 0: Normal 1: Open load on CH3	0
0	PLAY_CH3_DET	RO	CH3 play status. 0: MUTE 1: PLAY	0

(Address 25h)

Bit	Symbol	R/W	Description	Default

7	DC_CH4_ST	RO	CH4 DC diagnostic status. 0: Normal 1: DC pulse ended	0
6	DC_CH4_VLD	RO	CH4 DC diagnostic data valid. 0: Not valid or Diag not activated 1: Valid	0
5	DC_CH4_OC	SC	CH4 OC indicator. 0: Normal 1: OC on CH4	0
4	SLOAD_CH4_DET	RO	CH4 Short load indicator. 0: Normal 1: Shor Load on CH4	0
3	S2P_CH4_DET	RO	CH4 S2P indicator. 0: Normal 1: S2P on CH4	0
2	S2G_CH4_DET	RO	CH4 S2G indicator. 0: Normal 1: S2G on CH4	0
1	OLOAD_CH4_ST	RO	CH4 open load indicator. 0: Normal 1: Open load on CH4	0
0	PLAY_CH4_DET	RO	CH4 play status. 0: MUTE 1: PLAY	0

(Address 26h)

Bit	Symbol	R/W	Description	Default
7	AC_CH1_ST	RO	CH1 AC diagnostic status. 0: Normal 1: AC pulse ended	0
6	AC_CH1_VLD	RO	CH1 AC diagnostic data valid. 0: Not valid or Diag not activated 1: Valid	0
5	TWE_CH1_NPRESENT	RO	CH1 tweeter status. 0: Tweeter on CH1 1: Normal	0
4	CH1_ERR_DET	RO	CH1 Error code status when AC_CH1_VLD = 1. 0: Normal 1: Error-warning code reported in STATUS10	0

3	AC_CH2_ST	RO	CH2 AC diagnostic status. 0: Normal 1: AC pulse ended	0
2	AC_CH2_VLD	RO	CH2 AC diagnostic data valid. 0: Not valid or Diag not activated 1: Valid	0
1	TWE_CH2_NPRESENT	RO	CH2 tweeter status. 0: Tweeter on CH2 1: Normal	0
0	CH2_ERR_DET	RO	CH2 Error code status when AC_CH2_VLD = 1. 0: Normal 1: Error-warning code reported in STATUS13	0

(Address 27h)

Bit	Symbol	R/W	Description	Default
7	AC_CH3_ST	RO	CH3 AC diagnostic status. 0: Normal 1: AC pulse ended	0
6	AC_CH3_VLD	RO	CH3 AC diagnostic data valid. 0: Not valid or Diag not activated 1: Valid	0
5	TWE_CH3_NPRESENT	RO	CH3 tweeter status. 0: Tweeter on CH3 1: Normal	0
4	CH3_ERR_DET	RO	CH3 Error code status when AC_CH3_VLD = 1. 0: Normal 1: Error-warning code reported in STATUS16	0
3	AC_CH4_ST	RO	CH4 AC diagnostic status. 0: Normal 1: AC pulse ended	0
2	AC_CH4_VLD	RO	CH4 AC diagnostic data valid. 0: Not valid or Diag not activated 1: Valid	0
1	TWE_CH4_NPRESENT	RO	CH4 tweeter status. 0: Tweeter on CH4 1: Normal	0
0	CH4_ERR_DET	RO	CH4 Error code status when AC_CH4_VLD = 1. 0: Normal 1: Error-warning code reported in STATUS19	0

(Address 28h)

Bit	Symbol	R/W	Description	Default

7:0	DC_CH1_INFO	RO	CH1 DC information. When STATUS2[6] = 0, CH1 DC Diagnostic error code When STATUS2[6] = 1, CH1 Output Load Resistance	0

(Address 29h)

Bit	Symbol	R/W	Description	Default
7:0	AC_CH1_INFO1	RO	CH1 AC information. When CFG7[7] = 0, CH1 AC Diagnostic load magnitude When CFG7[7] = 1, CH1 Realtime Current Monitor(Bit[10:8])	0

(Address 2Ah)

Bit	Symbol	R/W	Description	Default
7:0	AC_CH1_INFO2	RO	CH1 AC information. When CFG7[7] = 0, CH1 AC Diagnostic error code or load phase When CFG7[7] = 1, CH1 Realtime Current Monitor(Bit[7:0])	0

(Address 2Bh)

Bit	Symbol	R/W	Description	Default
7:0	DC_CH2_INFO	RO	CH2 DC information. When STATUS3[6] = 0, CH2 DC Diagnostic error code When STATUS3[6] = 1, CH2 Output Load Resistance	0

(Address 2Ch)

Bit	Symbol	R/W	Description	Default
7:0	AC_CH2_INFO1	RO	CH2 AC information. When CFG7[7] = 0, CH2 AC Diagnostic load magnitude When CFG7[7] = 1, CH2 Realtime Current Monitor(Bit[10:8])	0

(Address 2Dh)

Bit	Symbol	R/W	Description	Default
7:0	AC_CH2_INFO2	RO	CH2 AC information. When CFG7[7] = 0, CH2 AC Diagnostic error code or load phase When CFG7[7] = 1, CH2 Realtime Current Monitor(Bit[7:0])	0

(Address 2Eh)

Bit	Symbol	R/W	Description	Default
7:0	DC_CH3_INFO	RO	CH3 DC information. When STATUS4[6] = 0, CH3 DC Diagnostic error code When STATUS4[6] = 1, CH3 Output Load Resistance	0

(Address 2Fh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	AC_CH3_INFO1	RO	CH3 AC information. When CFG7[7] = 0, CH3 AC Diagnostic load magnitude When CFG7[7] = 1, CH3 Realtime Current Monitor(Bit[10:8])	0

(Address 30h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	AC_CH3_INFO2	RO	CH3 AC information. When CFG7[7] = 0, CH3 AC Diagnostic error code or load phase When CFG7[7] = 1, CH3 Realtime Current Monitor(Bit[7:0])	0

(Address 31h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	DC_CH4_INFO	RO	CH4 DC information. When STATUS5[6] = 0, CH4 DC Diagnostic error code When STATUS5[6] = 1, CH4 Output Load Resistance	0

(Address 32h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	AC_CH4_INFO1	RO	CH4 AC information. When CFG7[7] = 0, CH4 AC Diagnostic load magnitude When CFG7[7] = 1, CH4 Realtime Current Monitor(Bit[10:8])	0

(Address 33h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	AC_CH4_INFO2	RO	CH4 AC information. When CFG7[7] = 0, CH4 AC Diagnostic error code or load phase When CFG7[7] = 1, CH4 Realtime Current Monitor(Bit[7:0])	0

(Address 34h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	FRAME_ERR_DET	SC	I^2S_WS error indicator. 0: Normal 1: Error Frame	0

6	Reserved	RO	Not used	0
5	VOFFOUT_CH1_DET	SC	CH1 output voltage offset indicator. 0: Normal 1: VOFFOUT on CH1	0
4	IOFFOUT_CH1_DET	RO	CH1 output current offset indicator. 0: Normal 1: IOFFOUT on CH1	0
3	IOFFOUT_CH1_VLD	RO	CH1 output current offset valid status. 0: Not valid 1: Valid	0
2	OLOAD_CH1_FINISH	RO	CH1 open load test finish indicator. 0: Not ended 1: Finished	0
1	OLOAD_CH1_SIGVLD	RO	CH1 open load test signal valid indicator. 0: Not valid 1: Valid	0
0	OLOAD_CH1_DET	SC	CH1 open load result indicator. 0: Normal 1: Open load on CH1	0

(Address 35h)

Bit	Symbol	R/W	Description	Default
7	IM_DIS_ST	RO	IM status. 0: Enable 1: Disable	0
6	CURR_DB_TXDIS	RO	Current sense monitor indicator. 0: Monitor enable on STATUS 1: Monitor disable on STATUS	0
5	VOFFOUT_CH2_DET	SC	CH2 output voltage offset indicator. 0: Normal 1: VOFFOUT on CH2	0
4	IOFFOUT_CH2_DET	RO	CH2 output current offset indicator. 0: Normal 1: IOFFOUT on CH2	0
3	IOFFOUT_CH2_VLD	RO	CH2 output current offset valid status. 0: Not valid 1: Valid	0
2	OLOAD_CH2_FINISH	RO	CH2 open load test finish indicator. 0: Not ended 1: Finished	0
1	OLOAD_CH2_SIGVLD	RO	CH2 open load test signal valid indicator. 0: Not valid 1: Valid	0

0	OLOAD_CH2_DET	SC	CH2 open load result indicator. 0: Normal 1: Open load on CH2	0

(Address 36h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	VOFFOUT_CH3_DET	SC	CH3 output voltage offset indicator. 0: Normal 1: VOFFOUT on CH3	0
4	IOFFOUT_CH3_DET	RO	CH3 output current offset indicator. 0: Normal 1: IOFFOUT on CH3	0
3	IOFFOUT_CH3_VLD	RO	CH3 output current offset valid status. 0: Not valid 1: Valid	0
2	OLOAD_CH3_FINISH	RO	CH3 open load test finish indicator. 0: Not ended 1: Finished	0
1	OLOAD_CH3_SIGVLD	RO	CH3 open load test signal valid indicator. 0: Not valid 1: Valid	0
0	OLOAD_CH3_DET	SC	CH3 open load result indicator. 0: Normal 1: Open load on CH3	0

(Address 37h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	VOFFOUT_CH4_DET	SC	CH4 output voltage offset indicator. 0: Normal 1: VOFFOUT on CH4	0
4	IOFFOUT_CH4_DET	RO	CH4 output current offset indicator. 0: Normal 1: IOFFOUT on CH4	0
3	IOFFOUT_CH4_VLD	RO	CH4 output current offset valid status. 0: Not valid 1: Valid	0
2	OLOAD_CH4_FINISH	RO	CH4 open load test finish indicator. 0: Not ended 1: Finished	0
1	OLOAD_CH4_SIGVLD	RO	CH4 open load test signal valid indicator. 0: Not valid 1: Valid	0

0	OLOAD_CH4_DET	SC	CH4 open load result indicator. 0: Normal 1: Open load on CH4	0

(Address 3Ch)

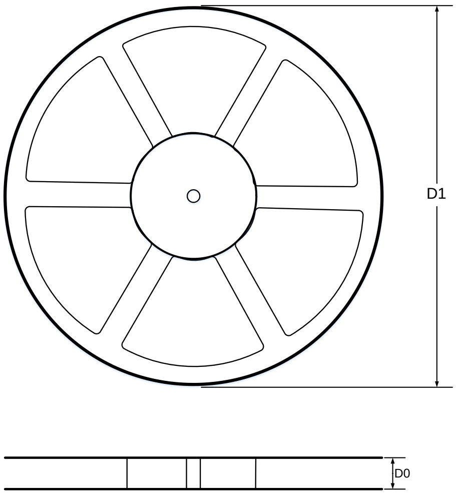
Bit	Symbol	R/W	Description	Default
7:2	Reserved	RO	Not used	0
1:0	TEMP_H	RO	Chip temperature(Bit[9:8])	0

(Address 3Dh)

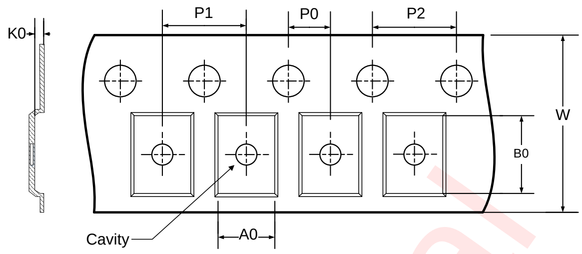
Bit	Symbol	R/W	Description	Default
7:0	TEMP_L	RO	Chip temperature(Bit[7:0])	0

Tape And Reel Information

REEL DIMENSIONS

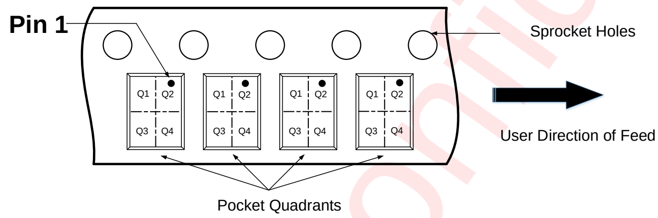


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



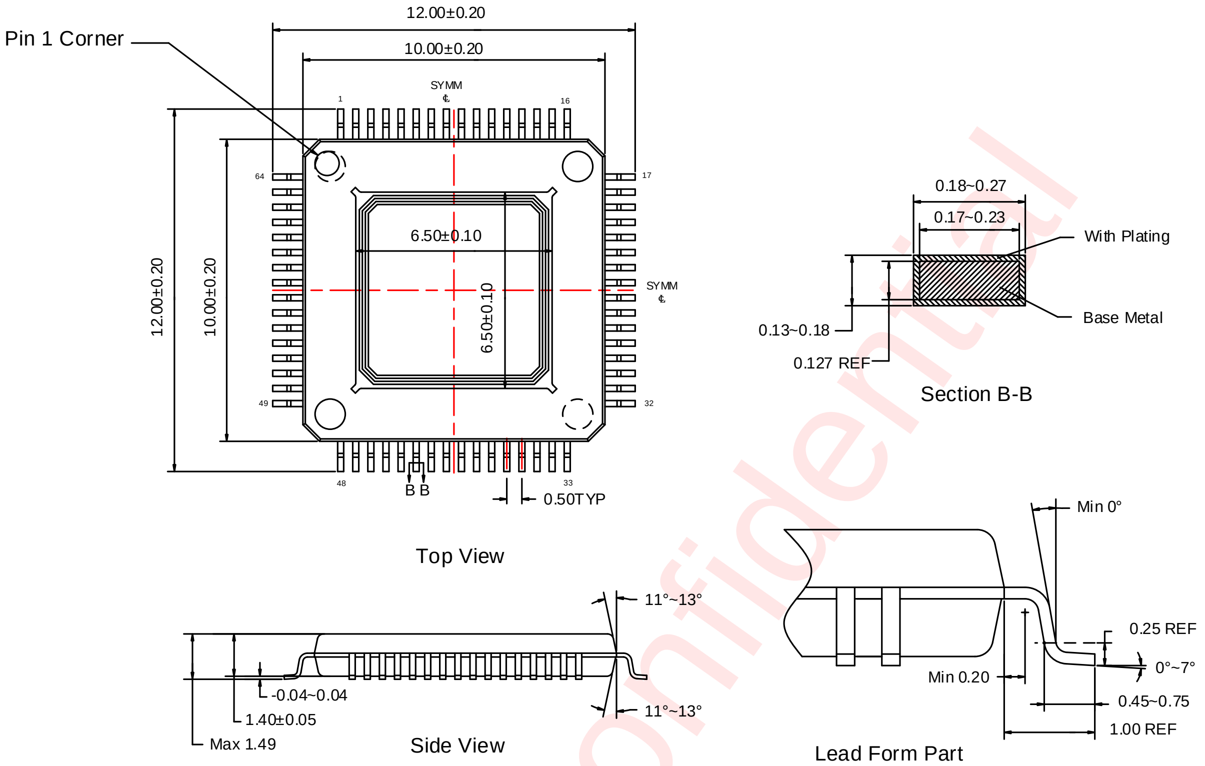
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	24.4	12.5	12.5	2.05	2	16	4	24	Q2

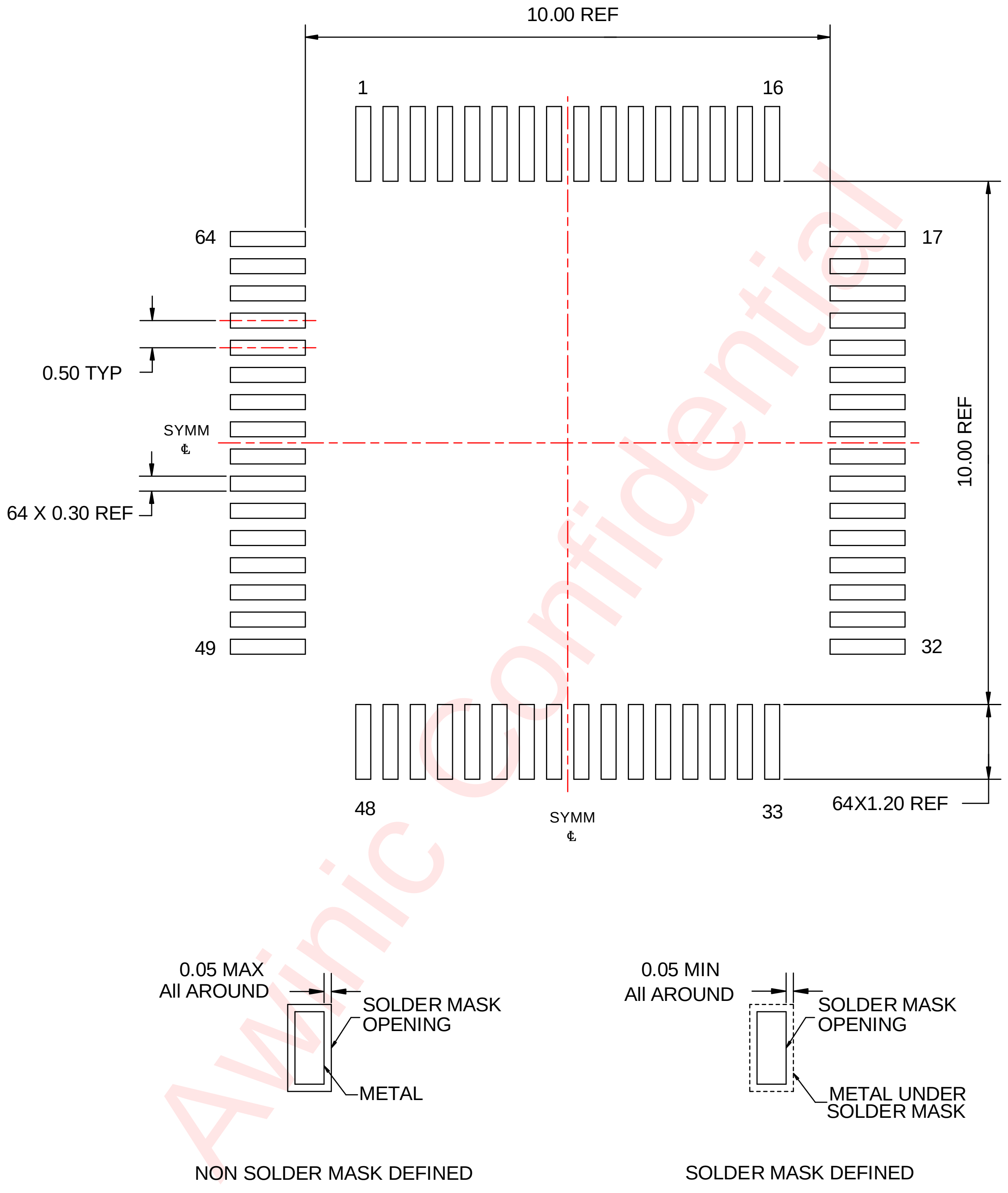
All dimensions are nominal

Package Description



Unit: mm

Land Pattern Data



Unit: mm

Revision History

Version	Date	Change Record
V1.0	February 2026	Officially released

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

