钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65LBC175A, SN75LBC175A

Four-channel RS-485 differential line receiver

网址 www.sztdbdt.com

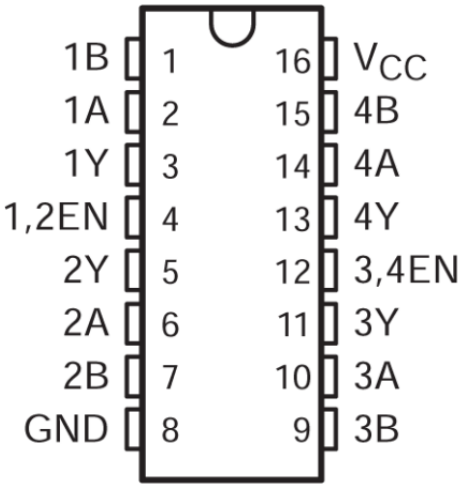
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

● Designed specifically for TIA/EIA-485, TIA/EIA-422, and ISO 842 applications
●Signal transmission rate exceeds 50Mbps
● Provides fail-safe protection for bus short, open, and idle bus conditions
●Provides 6kV ESD for bus inputs
● Common-mode bus voltage input range: -7V to 12V
●Propagation delay time < 16ns
● Low standby power consumption 20μA
●Pin-compatible upgrade for MC3486, DS96F175, LTC489, and SN7515



D or N Package (Top View)

Applications

●Factory automation
● ATMs and bill counters
●Smart grids
● AC and servo motor drives

Description

The SN65LBC175A and SN75LBC175A are quad-channel differential line with three-state outputs, specifically designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS422), and ISO 8482 (Euro RS-485) applications.
This device is optimized for equalized multi-point bus communication at data up to and even exceeding 50 Mbps. Transmission media can include twisted-pair cables, printed circuit board traces, or backplanes. The final data transmission rate and distance depend the attenuation characteristics of the medium and environmental noise coupling.Each receiver can operate over a wide range of positive and negative common-mode input voltages and features up to 6kV protection, making it suitable for high-speed multi-point data transmission applications in harsh environments. These devices are designed using LinBiCMOS™, which helps achieve low power consumption and robustness.The two EN inputs allow for paired enable control, or they can be externally tied together to enable all four drivers with the same signal.
The SN75LBC75A operates over an operating temperature range of 0°C to 70°C. The SN65LBC175A operates over a temperature range of -4°C to 85°C.

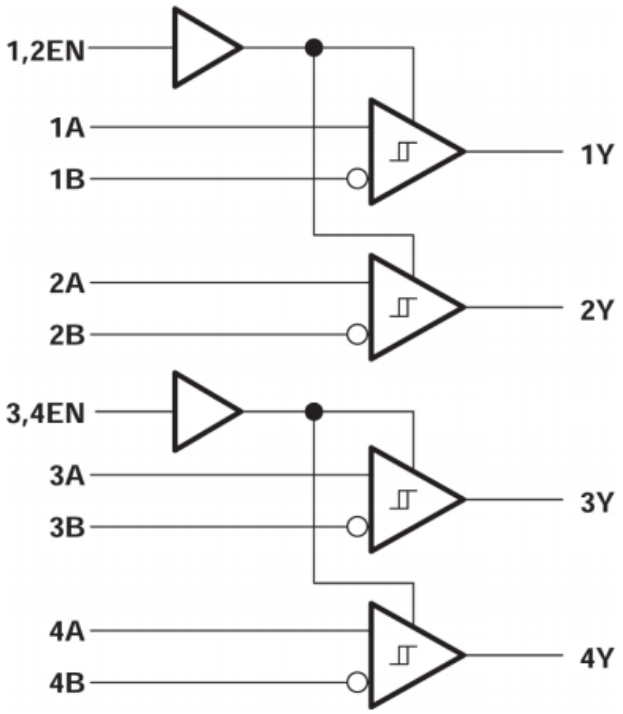


表 **4-1. Pin Functions**

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Inverting Differential Input
1A	2	I	Channel 1 Non-Inverting Differential Input
1Y	3	O	Channel 1 Output
1,2 EN	4	I	Channel 1 and 2 Active High Enable
2Y	5	O	Channel 2 Output
2A	6	I	Channel 2 Non-Inverting Differential Input
2B	7	I	Channel 2 Inverting Differential Input
GND	8	GND	Device Ground
3B	9	I	Channel 3 Inverting Differential Input
3A	10	I	Channel 3 Non-Inverting Differential Input
3Y	11	O	Channel 3 Output
3,4 EN	12	I	Channel 3 and 4 Active High Enable
4Y	13	O	Channel 4 Output
4A	14	I	Channel 4 Non-Inverting Differential Input
4B	15	I	Channel 4 Inverting Differential Input
V_{CC}	16	POW	Device Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} (see (2))	Supply voltage range		−0.3	6	V
	Voltage range at any bus input (steady state)	A and B	−10	15	V
	Voltage range at any bus input	transient pulse through 100 Ω, see 图 6-5	−30	30	V
V_I	Voltage input range at 1,2EN and 3,4EN		−0.5	V_{CC} + 0.5	V
I_O	Receiver output current		±10	mA	
	Electrostatic discharge:				
	Continuous power dissipation		See Power Dissipation Rating Table		

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND, and are steady-state (unless otherwise specified).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A and B to GND	±6000	V
		All pins	±5000	
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±2000	

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(2) Tested in accordance with JEDEC Standard 22, Test Method C101.

5.3 Dissipation Rating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	1080 mW	8.7 mW/°C	690 mW	560 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.4 Thermal Information

THERMAL METRIC(1)		SOIC (D)	PDIP (N)	UNIT
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	40.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	27.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	A, B	−7		12	V
High-level input voltage, V_{IH}	EN	2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	mA
Output current	Y	−8		8	
Operating free-air temperature, T_A	SN75LBC175A	0		70	°C
	SN65LBC175A	−40		85	

5.6 Electrical Characteristics

over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		-7 V ≤ V_{CM} ≤ 12 V (V_{CM} = (V_A + V_B) / 2)			-80	-10	mV
V_{IT-}	Negative-going differential input voltage threshold				-200	-120		
V_{HYS}	Hysteresis voltage (V_{IT+} - V_{IT-})					-40		mV
V_{IK}	Input clamp voltage		I_I = -18 mA		-1.5	-0.8		V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = -8 mA	See 图 6-1	2.7	4.8		V
V_{OL}	Low-level output voltage		V_{ID} = -200 mV, I_{OL} = 8 mA			0.2	0.4	
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}		-1		1	μA
I_I	Line input current		Other input at 0 V, V_{CC} = 0 V or 5 V	V_I = 12 V			0.9	mA
				V_I = -7 V	-0.7			
I_{IH}	High-level input current	Enable inputs					100	μA
I_{IL}	Low-level input current				-100			μA
R_I	Input resistance		A, B		12			kΩ
I_{CC}	Supply current		V_{ID} = 5 V	1,2EN, 3,4EN at 0 V			20	mA
			No load	1,2EN, 3,4EN at V_{CC}	11		16	mA

(1) All typical values are at V_{CC} = 5 V and 25°C.

5.7 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_r	output rise time			2	4	ns
t_f	output fall time	V_{ID} = -3 V to 3 V, See 图 6-2		2	4	ns
t_{PLH}	Propagation delay time, low-to-high level output			9 12	16	ns
t_{PHL}	Propagation delay time, high-to-low level output			9 12	16	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output	See 图 6-3		27	38	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output			7	16	ns
t_{PZL}	Propagation delay time, high-impedance to low level output	See 图 6-4		29	38	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output			12	16	ns
$t_{sk(P)}$	Pulse skew ($\|(t_{PLH} - t_{PHL})\|$)			0.2	1	ns
$t_{sk(o)}$	output skew (see Note 4)				2	ns
$t_{sk(PP)}$	Part-to-part skew (see Note 5)				2	ns

(1) All typical values are at V_{CC} = 5 V and 25°C.
(2) Outputs skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(3) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

6 Parameter Measurement Information

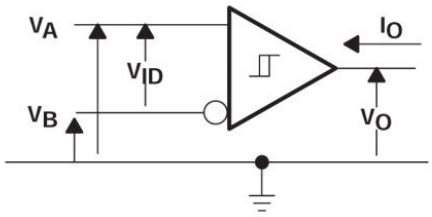
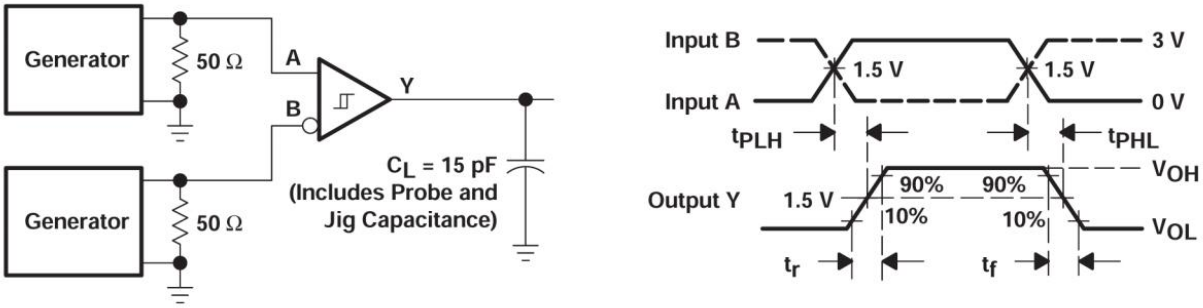
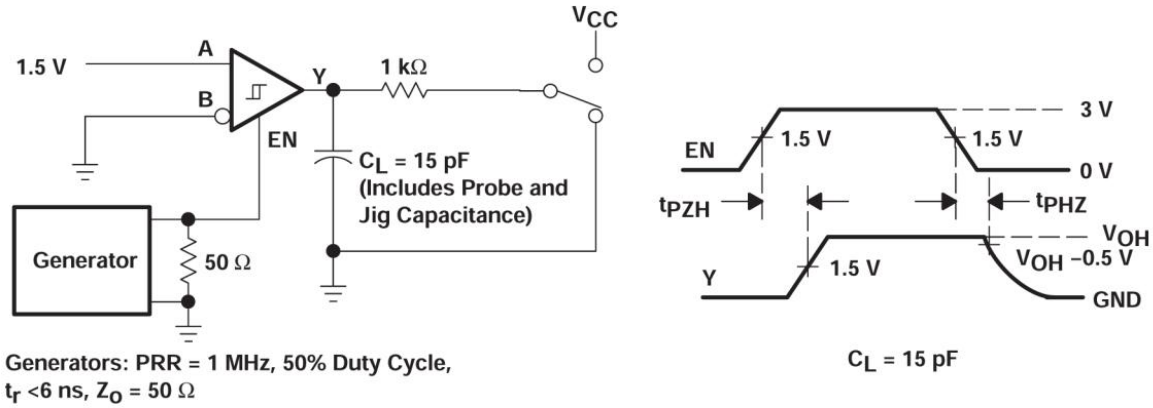


图 6-1. Voltage and Current Definitions



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

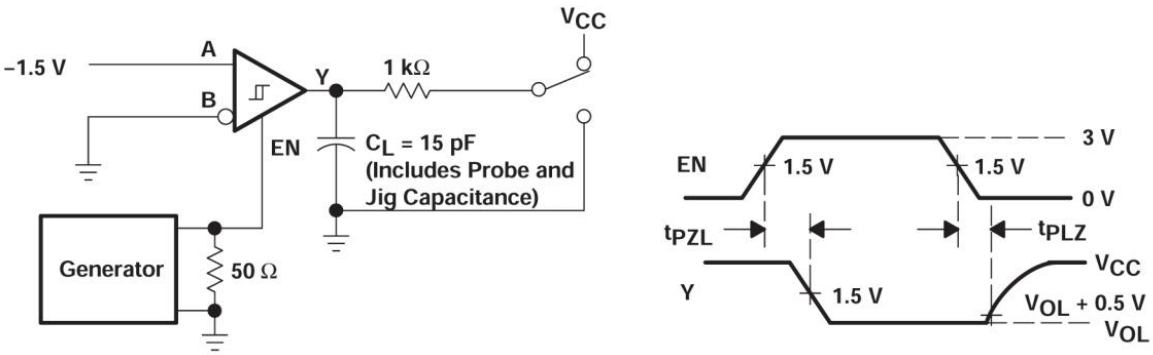
图 6-2. Switching Test Circuit and Waveforms



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

C_L = 15 pF

图 6-3. Test Circuit Waveforms, t_{PZH} and t_{PHZ}



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

图 6-4. Test Circuit Waveforms, t_{PZL} and t_{PLZ}

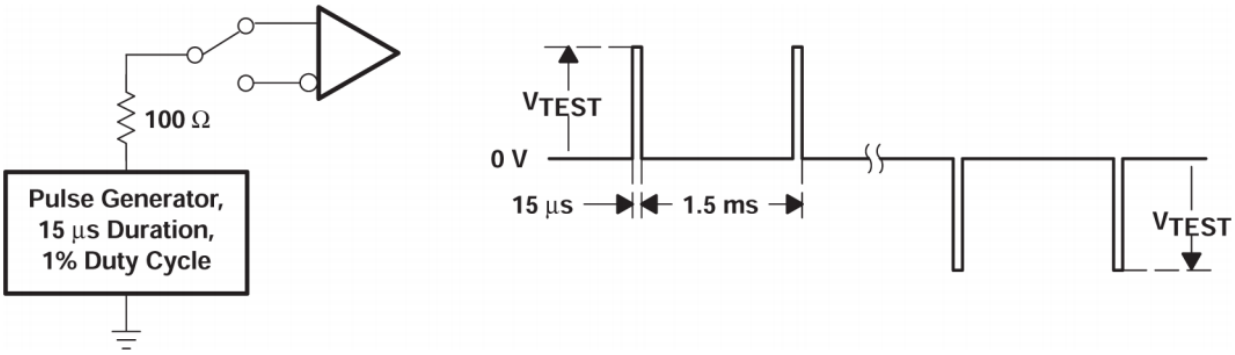


图 6-5. Test Circuit and Waveform, Transient Over-Voltage Test

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Functional Table (Each Receiver)

DIFFERENTIAL INPUTS A – B (V_{ID})	ENABLE EN(1)	OUTPUT Y
$V_{ID} \leq -0.2$ V	H	L
-0.2 V < V_{ID} < -0.01 V	H	?
-0.01 V ≤ V_{ID}	H	H
X	L	Z
X	OPEN	Z
Short circuit	H	H
Open circuit	H	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

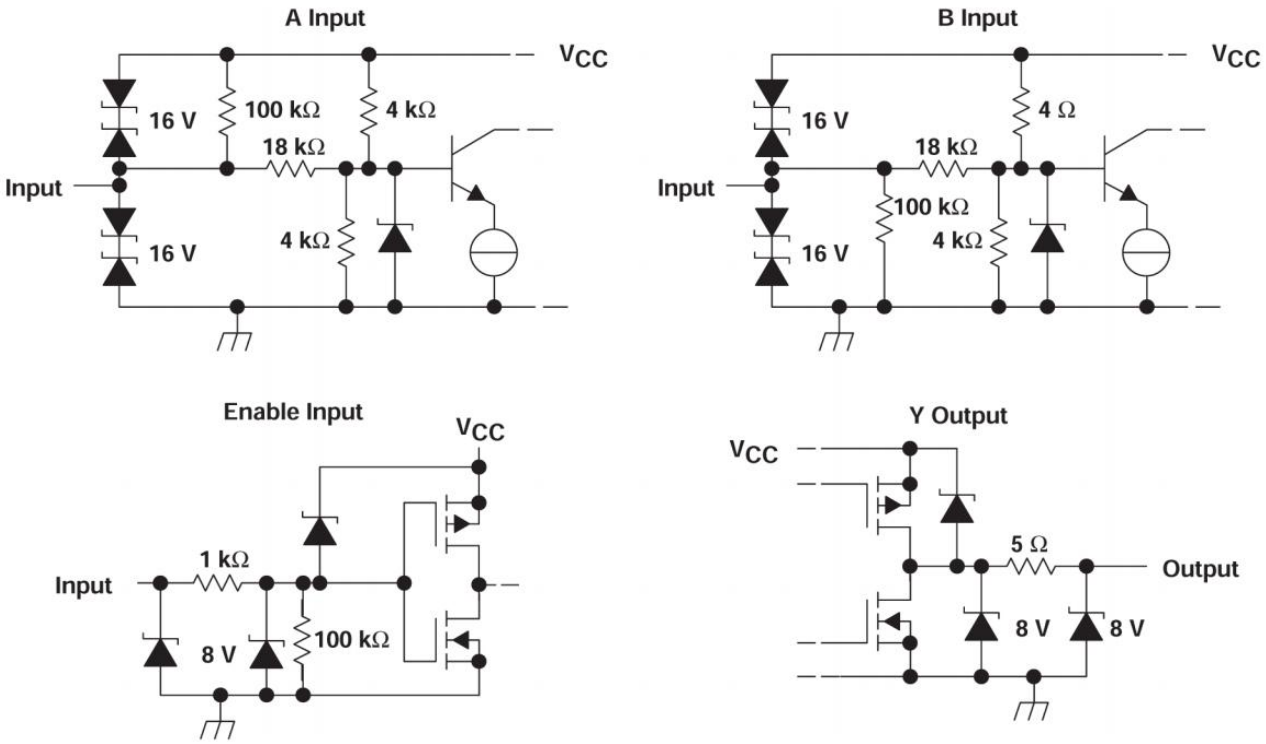
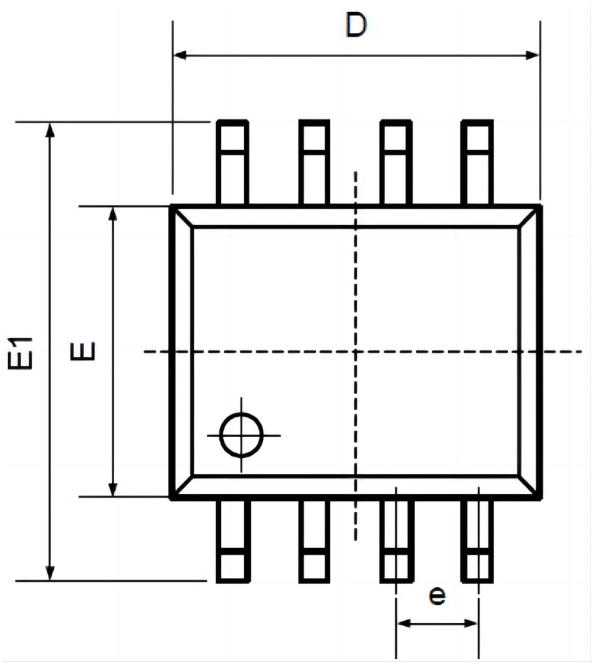


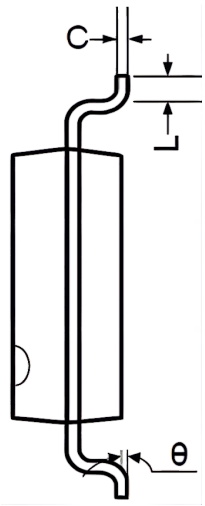
图 7-1. Equivalent Input and Output Schematic Diagrams

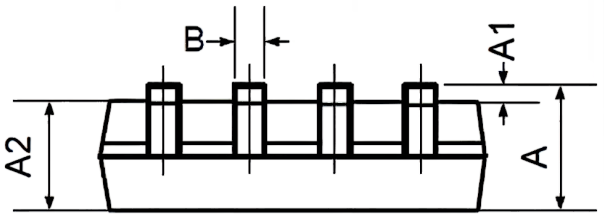
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65LBC175ADR-TUDI	SOP8	Tape,Reel,2500	SN65LBC175ADR
SN75LBC175ADR-TUDI	SOP8	Tube,50,A box of 2000	SN75LBC175ADR
SN75LBC175AN-TUDI	DIP8	Tube,50,A box of 2000	SN75LBC175AN

Package SOP8

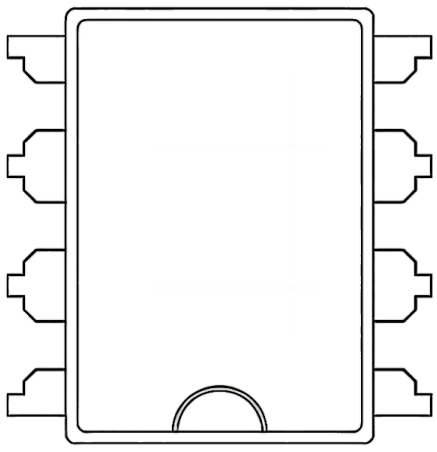


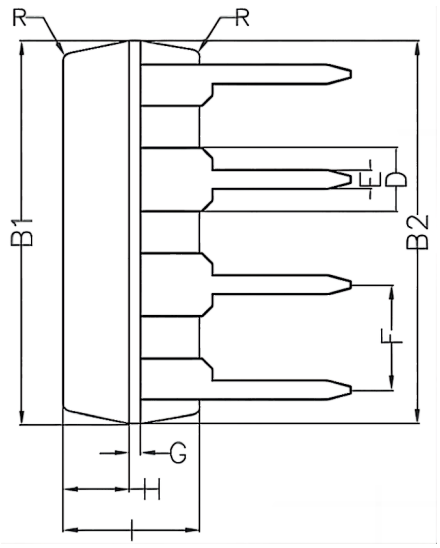


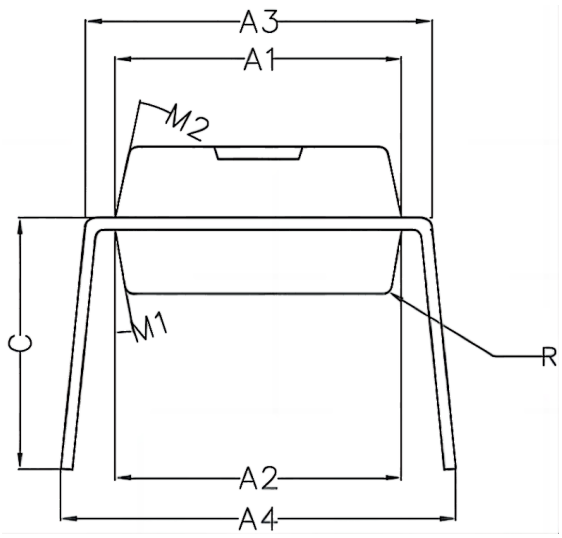


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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