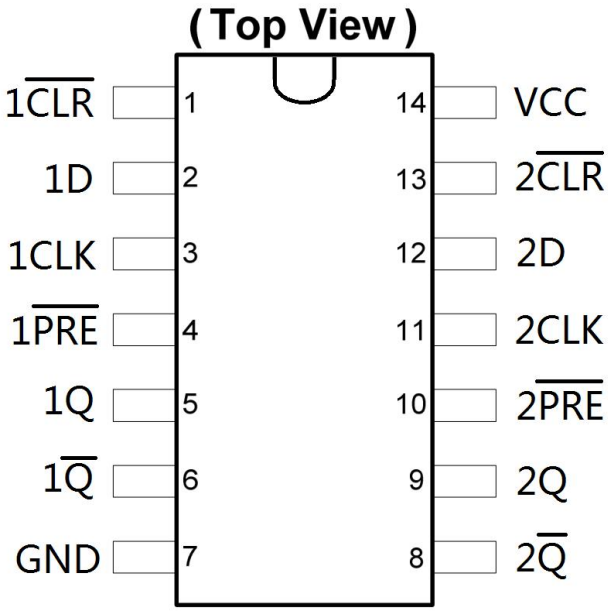
1. DESCRIPTION

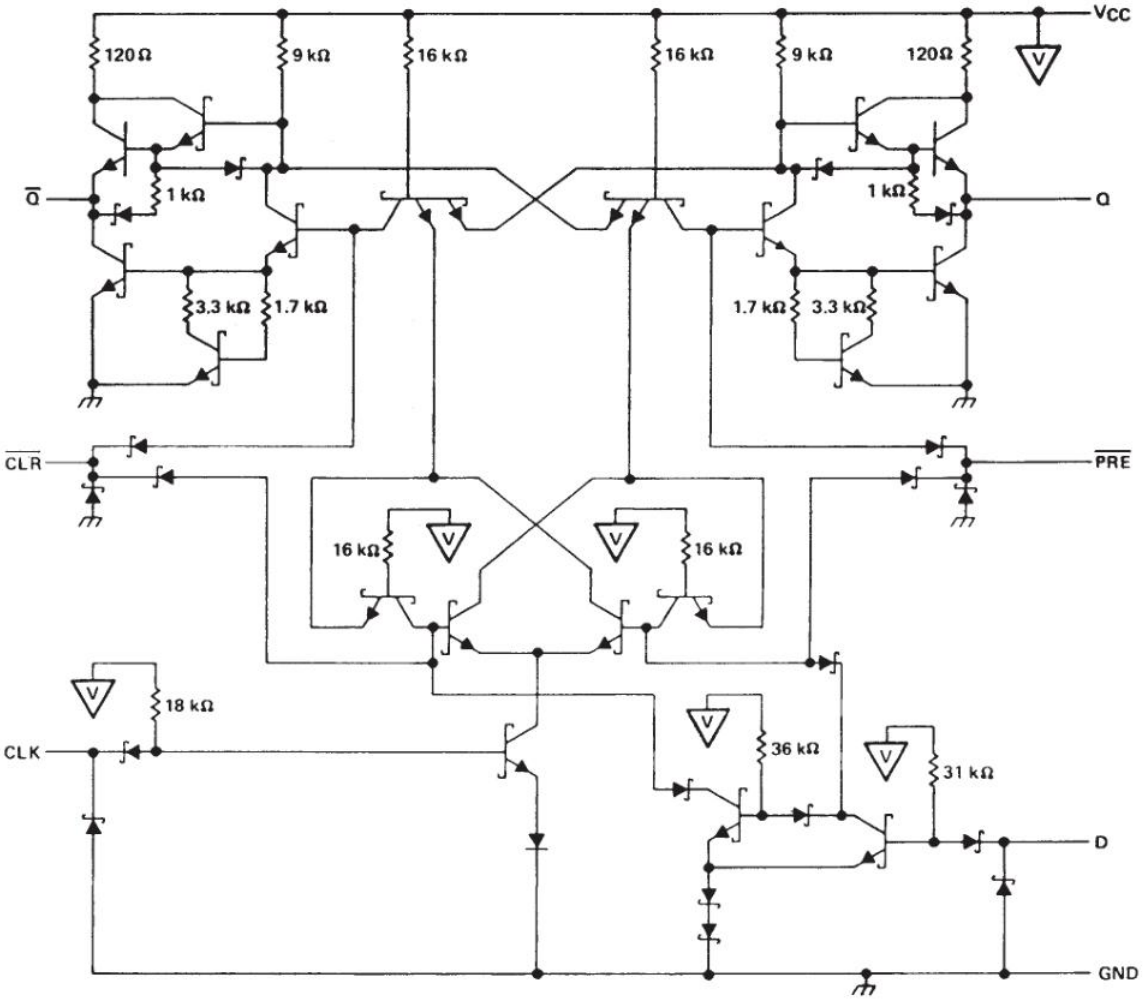
These devices contain two independent D-type positive-edge-triggered flip-flops.A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs.When preset and clear are inactive(high),data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse.Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse.Following the hold time interval ,data at the D input may be changed without affecting the levels at the outputs.

2. PIN CONFIGURATIONS

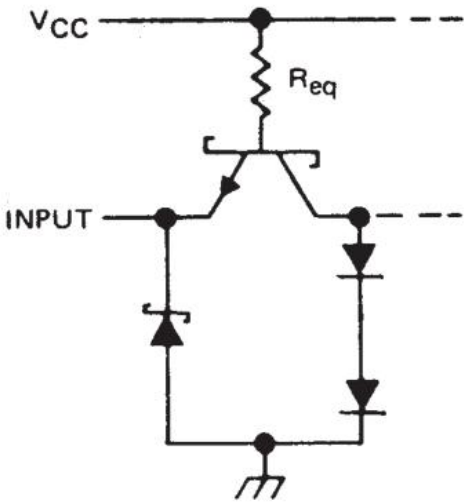


INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H↑	H↑
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

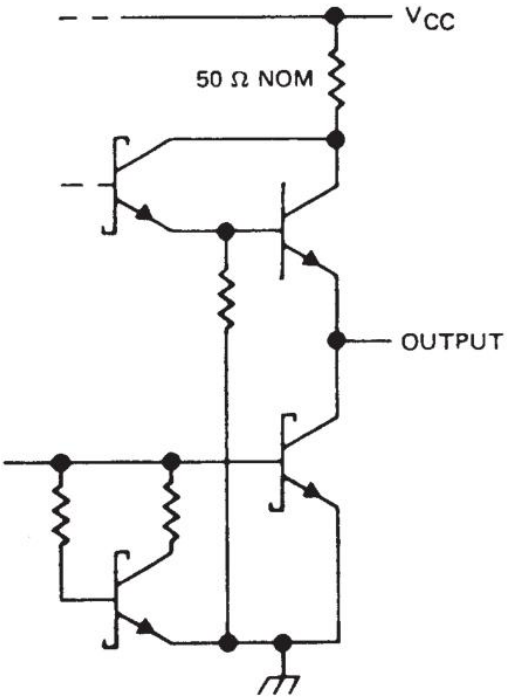
3. SCHEMATICS



4. SCHEMATICS OF INPUTS AND OUTPUTS



EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS

5. ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTES)

Supply voltage, V_{CC} (see Note 1)..... 7V

Input voltage, VI: 74LS74..... 7V

Operating free-air temperature range: DIP package..... 0°C to 70°C

Storage temperature range, Tstg..... −65°C to 150°C

NOTES 1: Voltage values are with respect to the network ground terminal.

6. RECOMMENDED OPERATING CONDITIONS

			74LS74			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−0.4	mA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency		0		25	MHz
t_w	Pulse duration	CLK high	25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			
t_{su}	Set up time-before CLK↑	High-level data	20			ns
		Low-level data	20			
t_h	Hold time-data after CLK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

7. ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†	74LS74			UNIT
			MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −0.4 mA, V_{IL}=MAX	2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OL} = 8mA		0.25	0.4	V
				0.35	0.5	
I_I	D or CLK	V_{CC} = MAX, V_I = 7 V			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$				0.2	
IIH	D or CLK	V_{CC} = MAX, V_I = 2.7 V			20	μA
	$\overline{CLR}$ or $\overline{PRE}$				40	
I_{IL}	D or CLK	V_{CC} = MAX, V_I = 0.4 V			−0.4	mA
	$\overline{CLR}$ or $\overline{PRE}$				−0.8	
I_{OS}§		V_{CC} = MAX See Note 4	−20		−100	mA
I_{CC} (Totall)		V_{CC} = MAX See Note 2		4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at VCC = 5 V, TA = 25 C.
§ Not more than one output should be shorted at a time.
NOTES 2: With all outputs open,ICC is measured with the Q and $\overline{Q}$ outputs high in turn.At the time of measurement,the clock input is grounded.
NOTES 4: For certain devices where state commutation can be caused by shorting an output to ground,an equivalent test may be performed with V_O=2.25V and 2.125V for the 54 family and the 74 family,respectively,with the minimum and maximum limits reduced to one half of their stated values.

8. SWITCHING CHARACTERISTICS,VCC = 5 V, TA = 25℃

PARAMETER	FROM(INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L=15 pF,R_L=2kΩ, See Note 3	25	33		MHz
t_{PLH}	$\overline{CLR}$ or CLK	Q or $\overline{Q}$			13	25	ns
t_{PHL}					25	40	ns

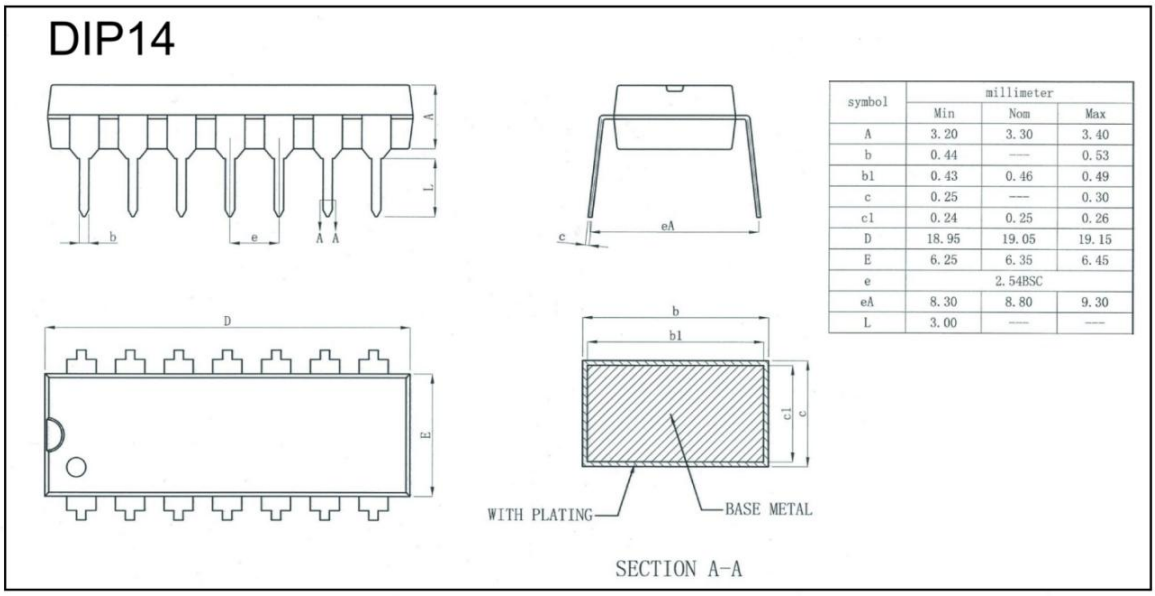
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

9. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD74LS74	XD74LS74	DIP14	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

10. DIMENSIONAL DRAWINGS



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	——	0.53
b1	0.43	0.46	0.49
c	0.25	——	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	——	——