

NVH4L070N120M3S-VB Datasheet

N-Channel 1200V (D-S) SiC Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	1200	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 18$ V	0.080
Q_g (nC)	108	

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



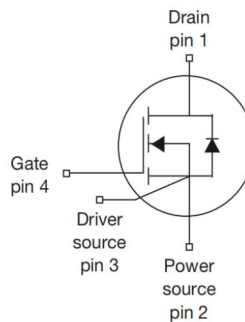
APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- DC/DC converter

TO-247-4L



- Pin1 D - Drain
- Pin2 S - Source(Power)
- Pin3 S - Source(Driver)
- Pin4 G - Gate



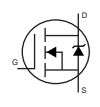
N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	1200	V
Gate-Source Voltage	V_{GS}	-10 / +22	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 18 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	90	
Linear Derating Factor		2.1	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	1200	mJ
Maximum Power Dissipation	P_D	320	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C
Drain-Source Voltage Slope	dV/dt	$T_J = 125$ °C	V/ns
Reverse Diode dV/dt ^d			
Soldering Recommendations (Peak Temperature) ^c	for 10 s	260	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 100$ V, starting $T_J = 25$ °C, $L = 30$ mH, $R_g = 25$ Ω , $I_{AS} = 9$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.47	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ °C}, I_D = 1\text{ mA}$	-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 10\text{ mA}$	2.5	-	4.5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = +22\text{ V}$	-	-	100	nA
		$V_{GS} = -10\text{ V}$	-	-	100	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	-	10	-	μA
		$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 18\text{ V}, I_D = 30\text{ A}$	-	0.080	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 0\text{ V}, I_D = 30\text{ A}$	-	16	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$	-	2800	-	pF
Output Capacitance	C_{oss}		-	123	-	
Reverse Transfer Capacitance	C_{rss}		-	10	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 800\text{ V}, V_{GS} = 0\text{ V}$	-	156	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	268	-	
Total Gate Charge	Q_g	$V_{GS} = -5/18\text{ V}, I_D = 20\text{ A}, V_{DS} = 800\text{ V}$	-	108	-	nC
Gate-Source Charge	Q_{gs}		-	29	-	
Gate-Drain Charge	Q_{gd}		-	33	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 800\text{ V}, I_D = 20\text{ A}, V_{GS} = -5/18\text{ V}, R_g = 2\text{ Ω}$	-	18	25	ns
Rise Time	t_r		-	24	55	
Turn-Off Delay Time	$t_{d(off)}$		-	80	-	
Fall Time	t_f		-	12	-	
Gate Input Resistance	R_g		$f = 1\text{ MHz}, \text{ open drain}$	-	3.2	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	30	A
Pulsed Diode Forward Current	I_{SM}		-	-	90	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ °C}, I_S = 30\text{ A}, V_{GS} = 0$	-	-	4.1	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}, I_F = I_S = 30\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}, V_R = 800\text{ V}$	-	70	-	ns
Reverse Recovery Charge	Q_{rr}		-	220	-	μC
Reverse Recovery Current	I_{RRM}		-	60	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

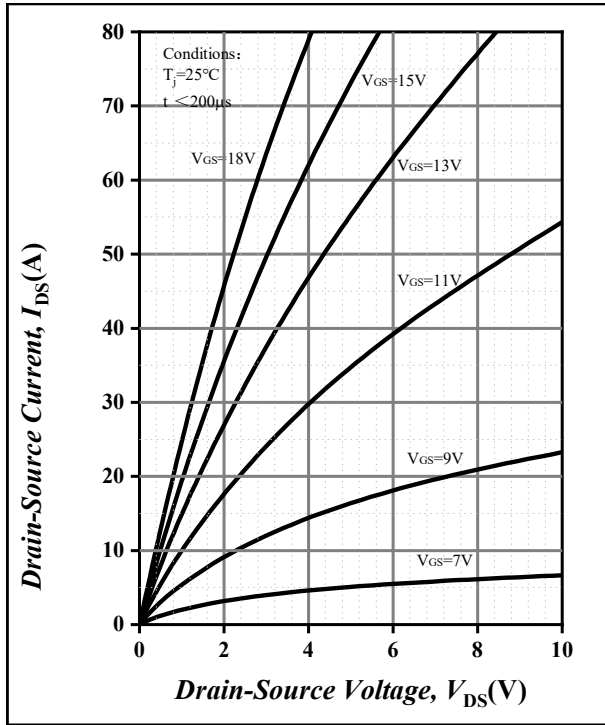


Fig.1 Output characteristics $T_j=25^\circ\text{C}$

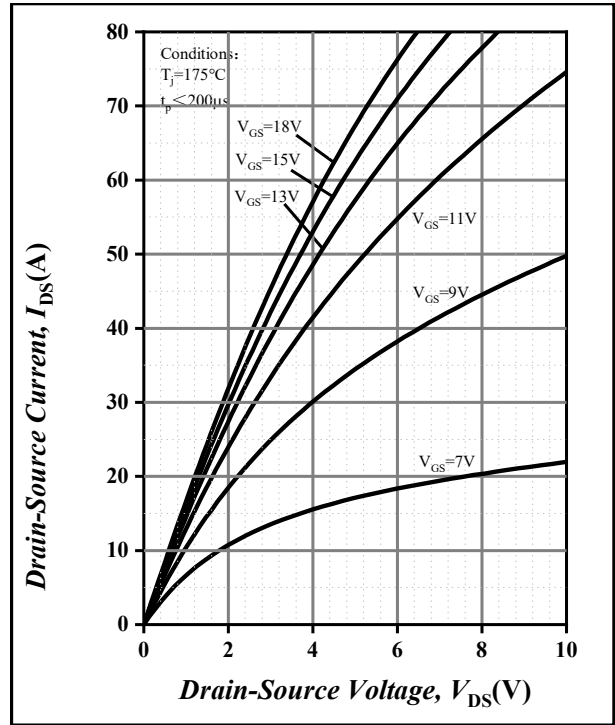


Fig.2 Output characteristics $T_j=175^\circ\text{C}$

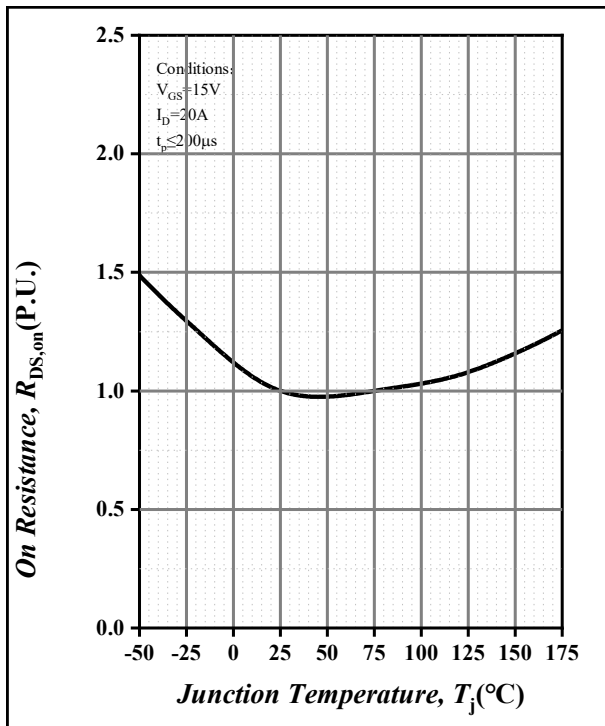


Fig.3 Normalized On-Resistance vs. Temperature

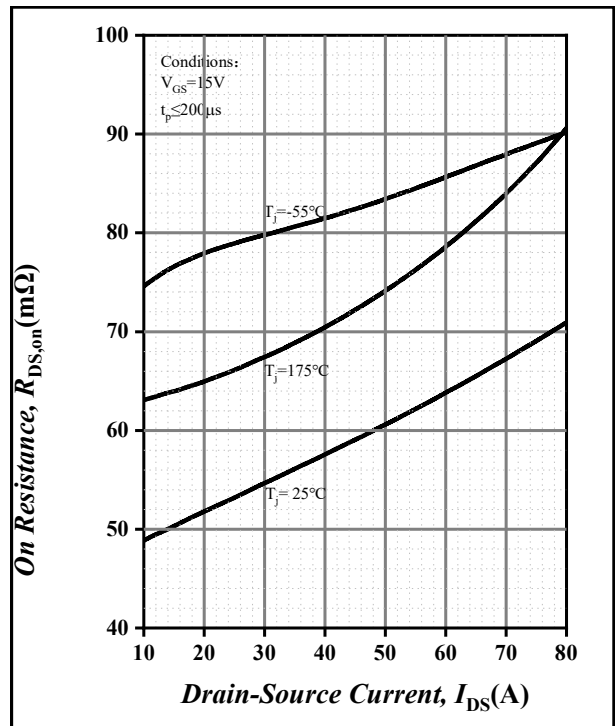


Fig.4 On-Resistance vs. Drain Current For Various Temperatures

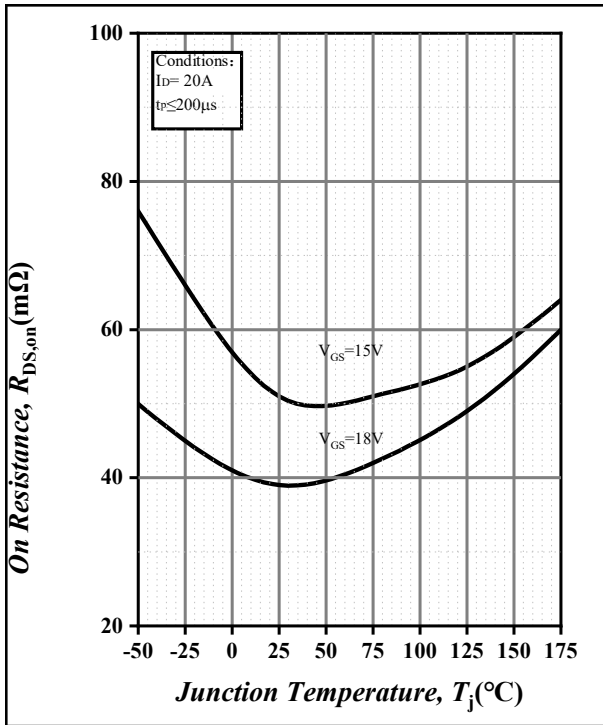


Fig.5 On-Resistance vs. Temperature For Various Gate Voltage

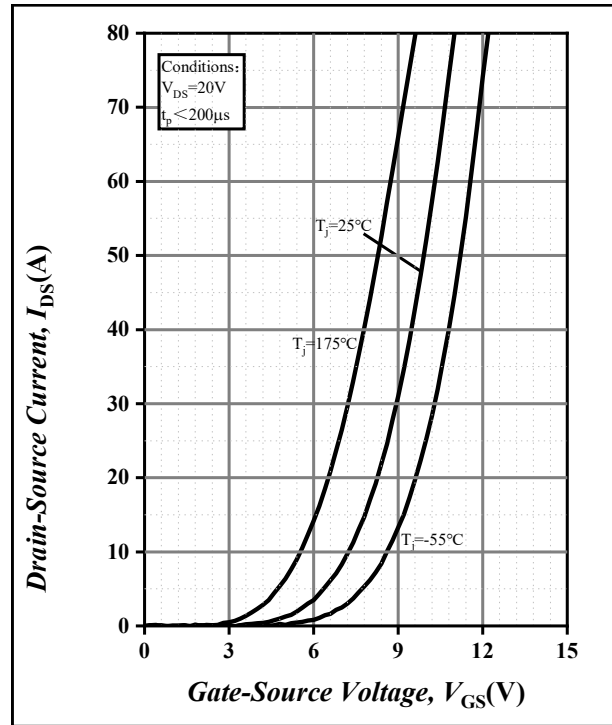


Fig.6 Transfer Characteristic For Various Junction Temperatures

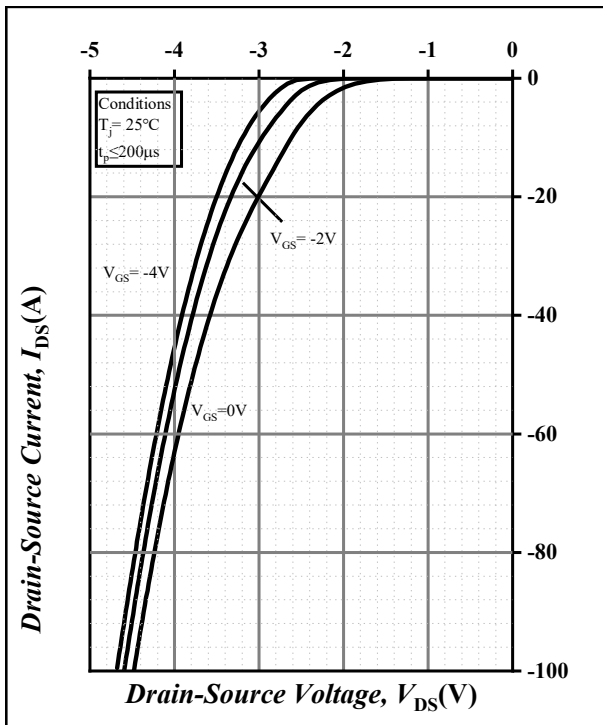


Fig.7 Body Diode Characteristic at 25 $^{\circ}$ C

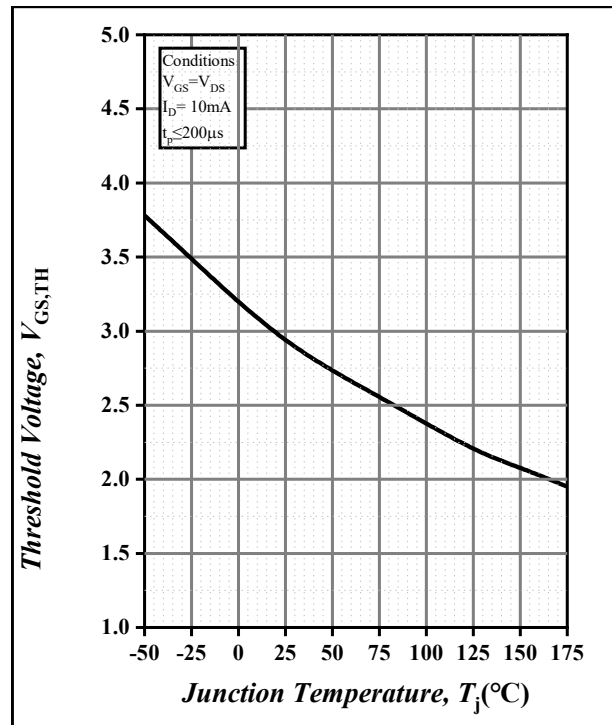


Fig.8 Threshold Voltage vs. Temperature



Fig.9 Gate Charge Characteristics

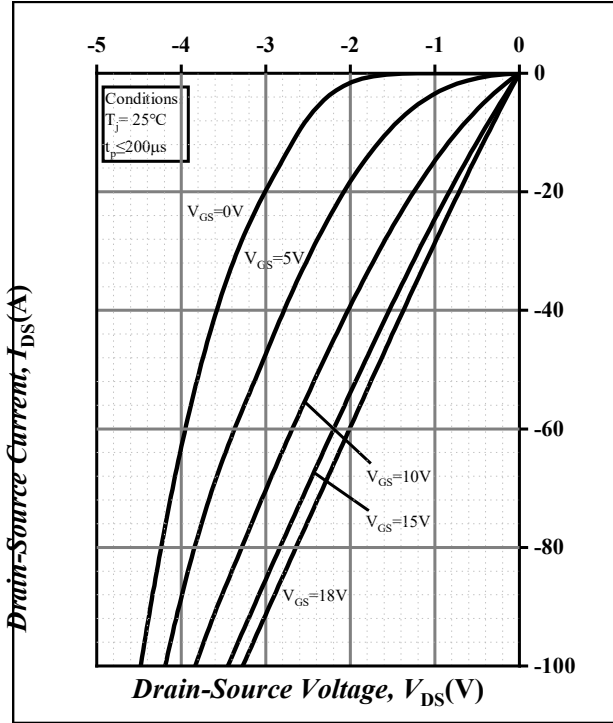


Fig.10 3rd Quadrant Characteristic at 25°C

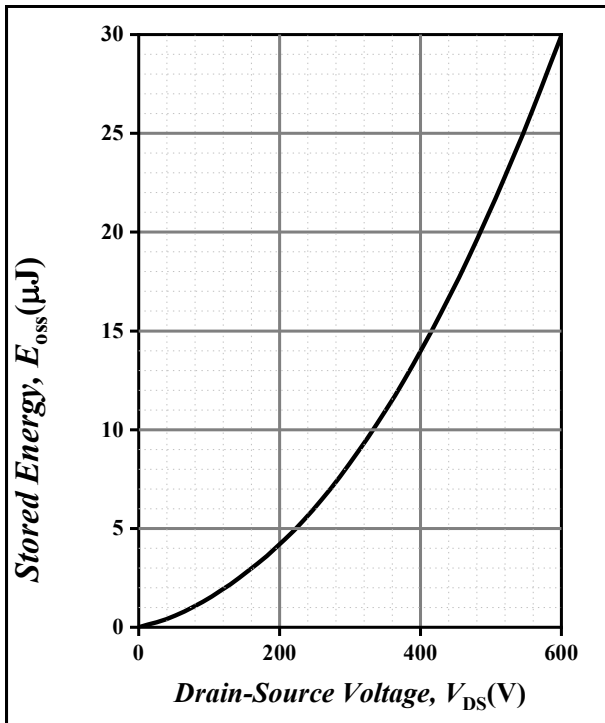


Figure 11. Output Capacitor Stored Energy



Fig.12 Capacitances vs. Drain-Source Voltage(0-200V)

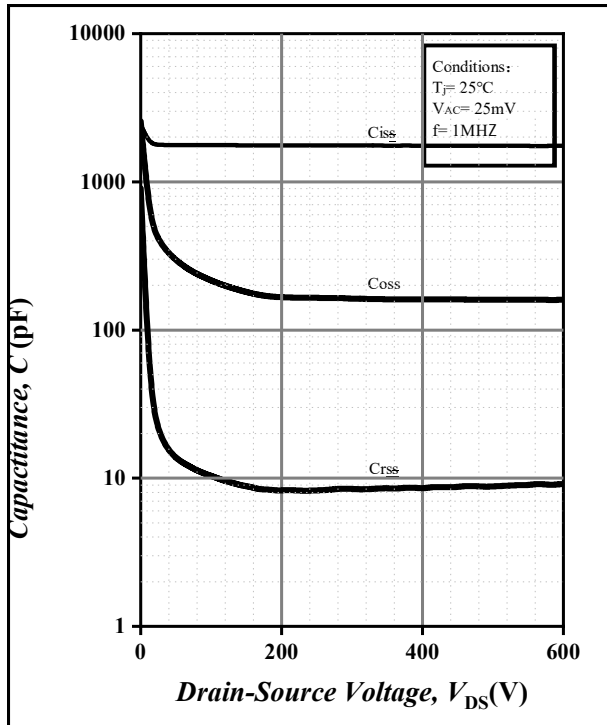


Fig.13 Capacitances vs. Drain-Source Voltage(0-600V)

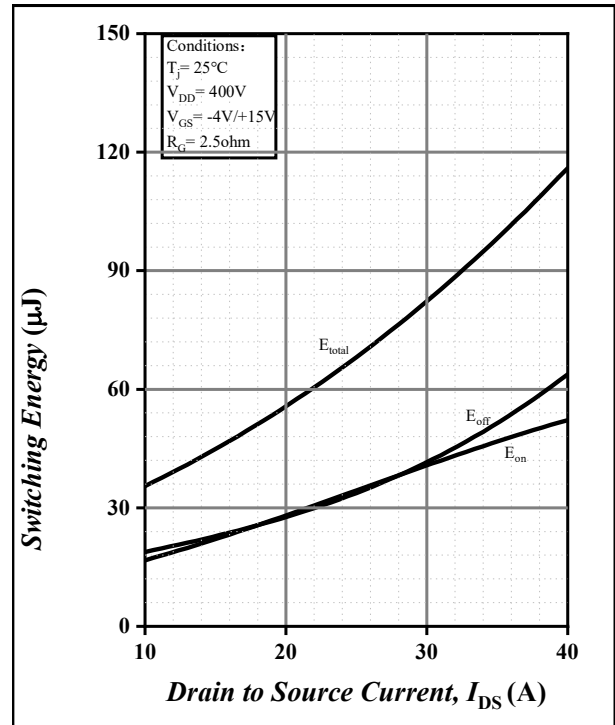


Figure 14. Clamped Inductive Switching Energy vs. Drain Current($V_{DD}=400\text{V}$)

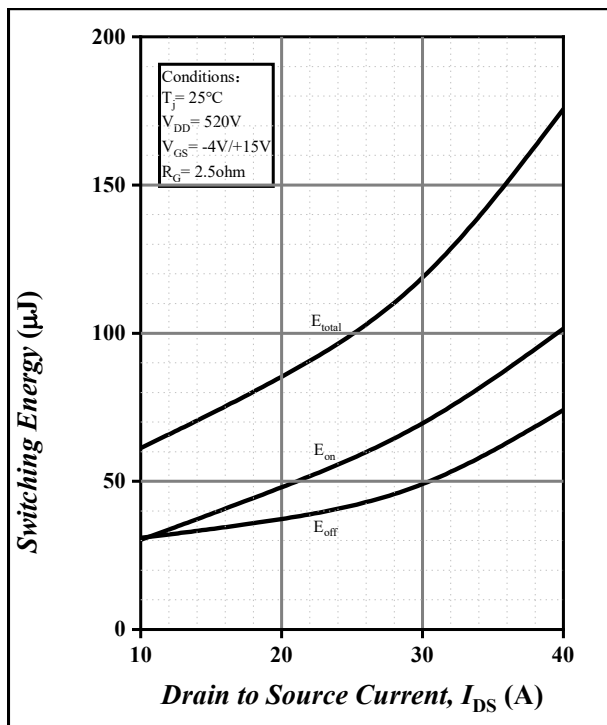


Figure 15. Clamped Inductive Switching Energy vs. Drain Current($V_{DD}=520\text{V}$)

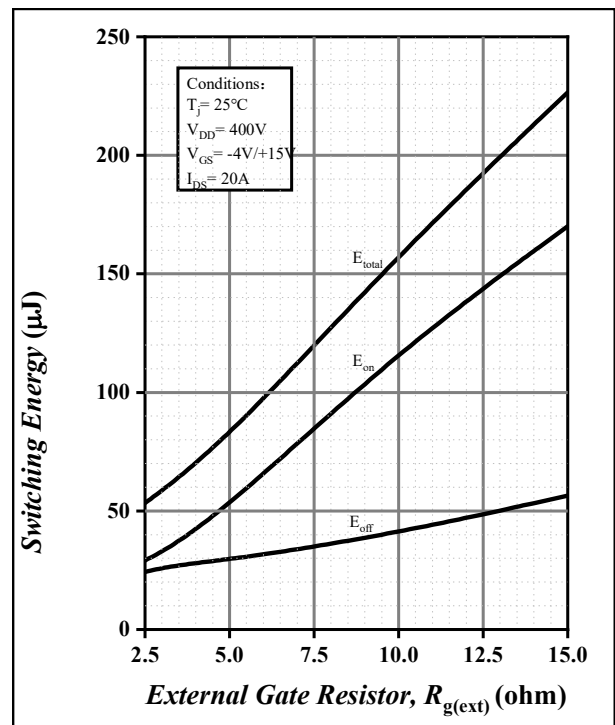


Figure 16. Clamped Inductive Switching Energy vs. $R_{g(\text{ext})}$

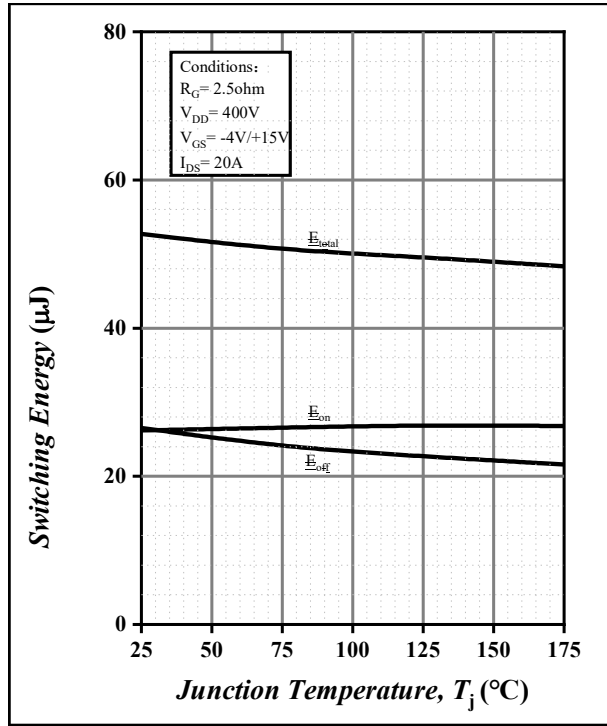


Figure 17. Clamped Inductive Switching Energy vs. Temperature

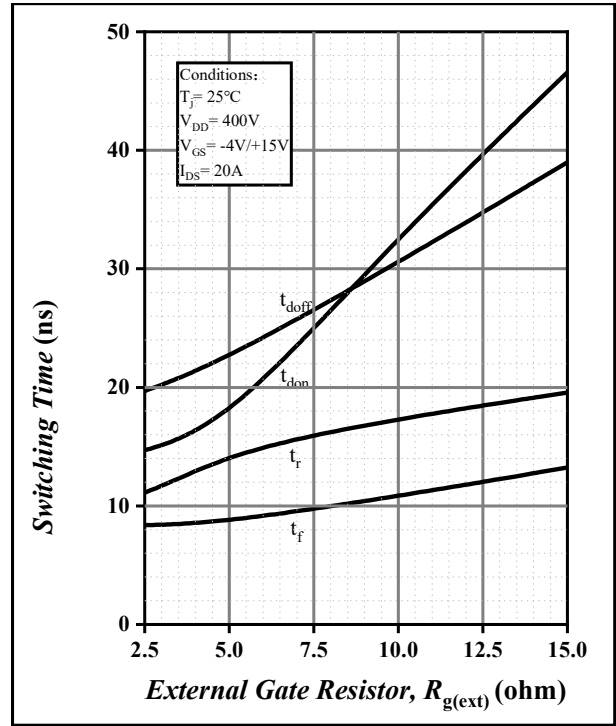
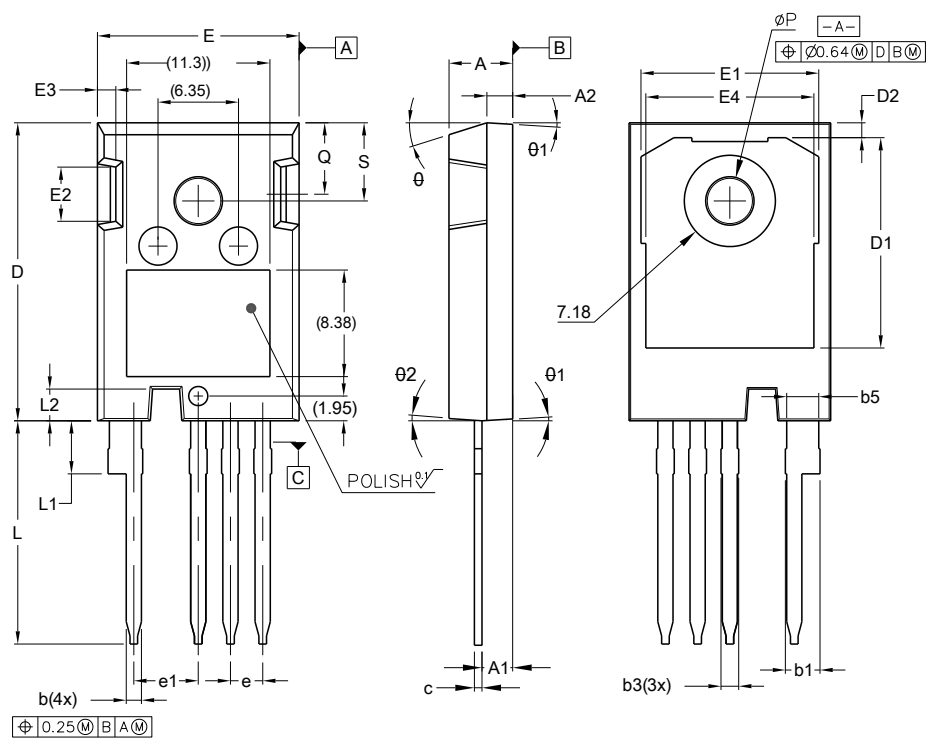


Figure 18. Switching Times vs. $R_{g(ext)}$

TO247-4L Package Outline Dimensions



TO247-4 Standard		
Dim	Min	Max
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b	1.07	1.33
b1	2.39	2.94
b3	1.07	1.60
b5	2.39	2.69
c	0.55	0.68
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.30
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
θP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
θ	17.5° - 20° REF	
θ_1	3.5° - 5° REF	
θ_2	4° - 5° REF	
All Dimensions in mm		

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