

Description

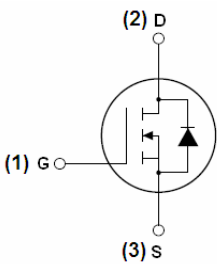
The 4402 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

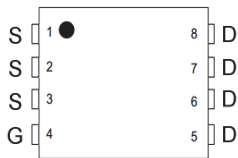
- | V_{DSS} | $R_{DS(ON)}$
@ 4.5V(Typ) | $R_{DS(ON)}$
@ 2.5V(Typ) | I_D |
|-----------|-----------------------------|-----------------------------|-------|
| 20V | 6.8mΩ | 8 mΩ | 30A |
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic diagram



Marking and pin Assignment



SOP-8 top view

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D (100^{\circ}C)$	21	A
Pulsed Drain Current	I_{DM}	80	A
Maximum Power Dissipation	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	50	°C/W
--	-----------------	----	------

Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

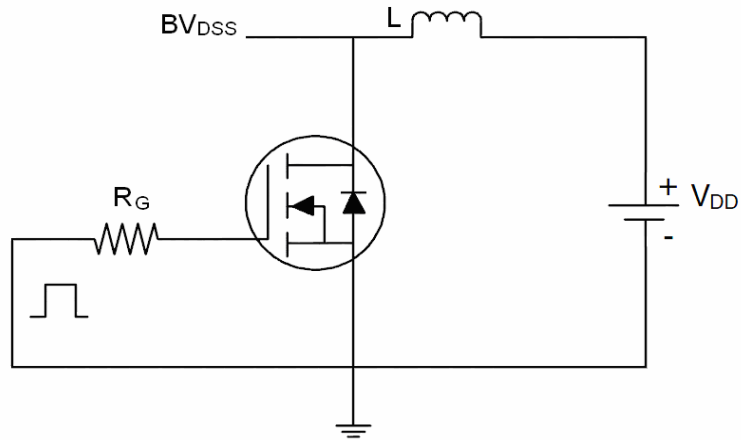
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V	-	-	500	nA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.5	0.64	1	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =8A	-	6.8	16	mΩ
		V _{GS} =2.5V, I _D =6A	-	8	25	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	26	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	938	-	PF
Output Capacitance	C _{oss}		-	142	-	PF
Reverse Transfer Capacitance	C _{rss}		-	99	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, R _L =0.75Ω V _{GS} =10V, R _G =3Ω	-	5	-	nS
Turn-on Rise Time	t _r		-	12	-	nS
Turn-Off Delay Time	t _{d(off)}		-	19	-	nS
Turn-Off Fall Time	t _f		-	6	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =20A, V _{GS} =10V	-	17.5		nC
Gate-Source Charge	Q _{gs}		-	3		nC
Gate-Drain Charge	Q _{gd}		-	4.1		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =1A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	30	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =20A di/dt = 100A/μs ^(Note3)	-	19	-	nS
Reverse Recovery Charge	Q _{rr}		-	10	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

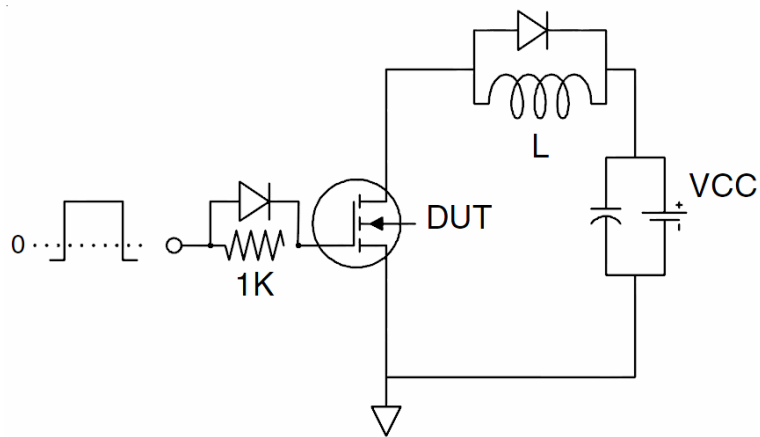
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test circuit

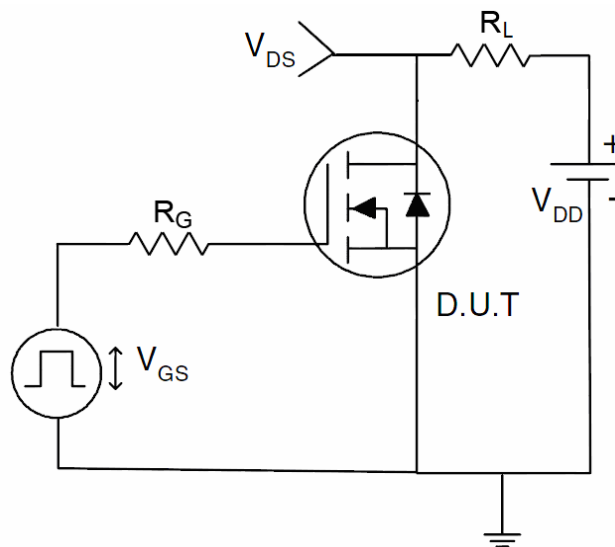
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

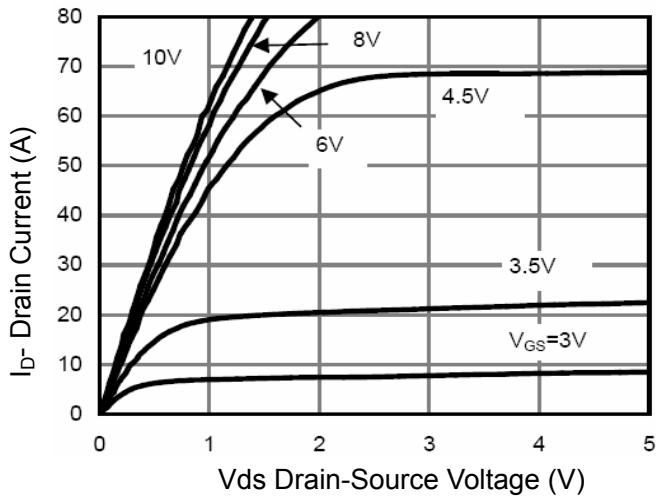


Figure 1 Output Characteristics

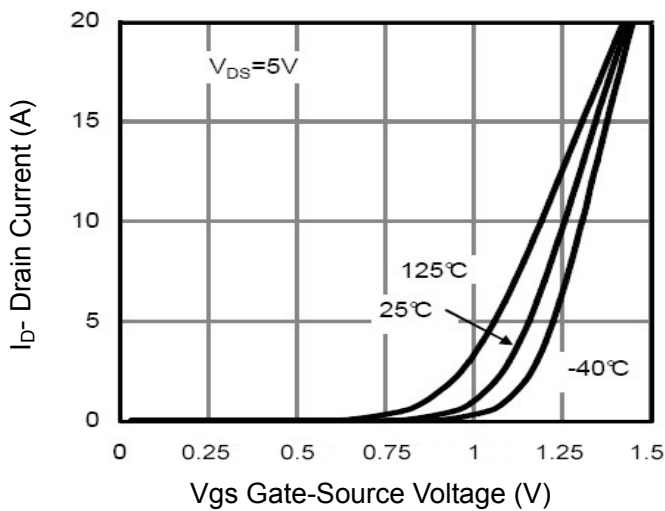


Figure 2 Transfer Characteristics

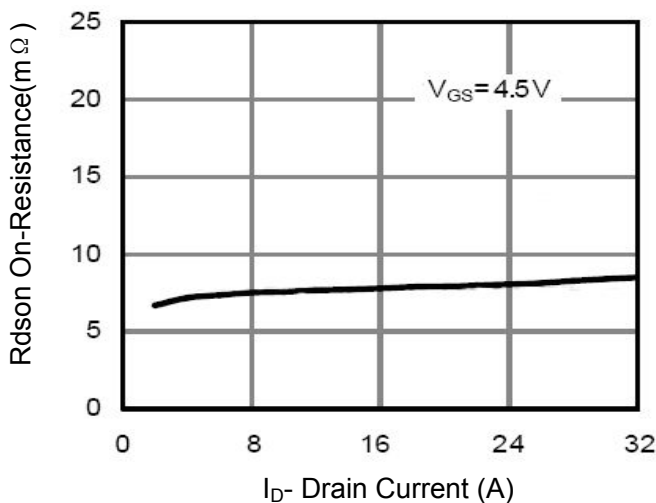


Figure 3 Rdson- Drain Current

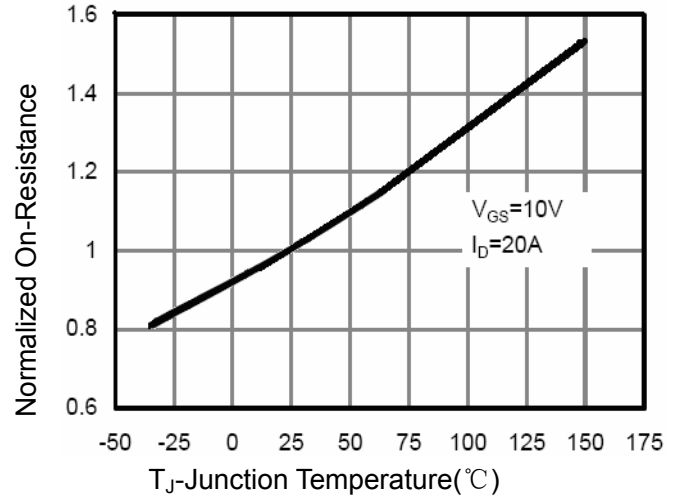


Figure 4 Rdson-Junction Temperature

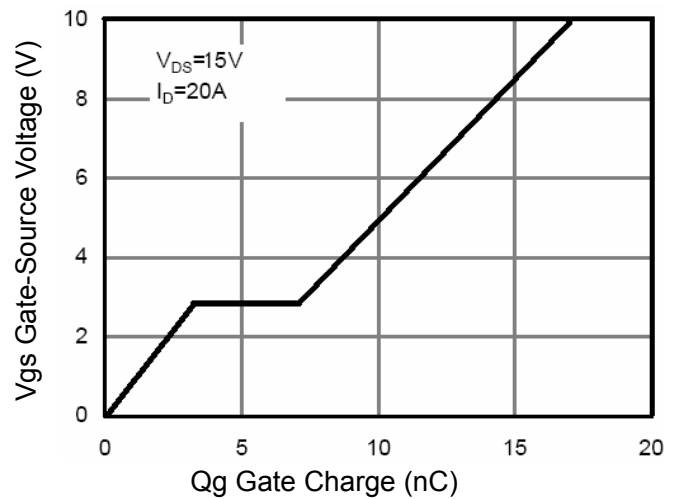


Figure 5 Gate Charge

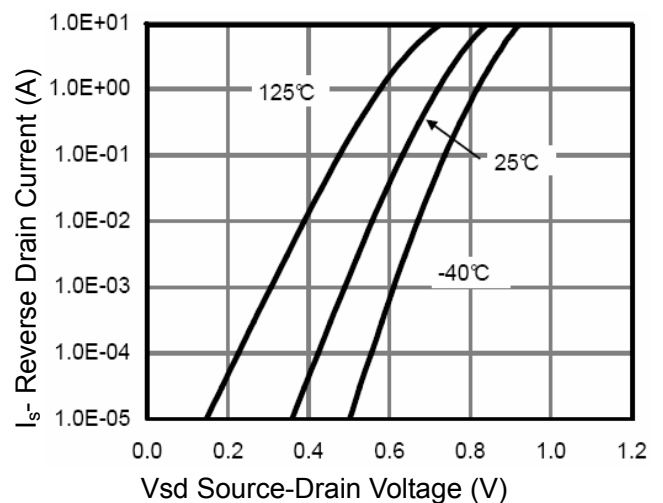


Figure 6 Source- Drain Diode Forward

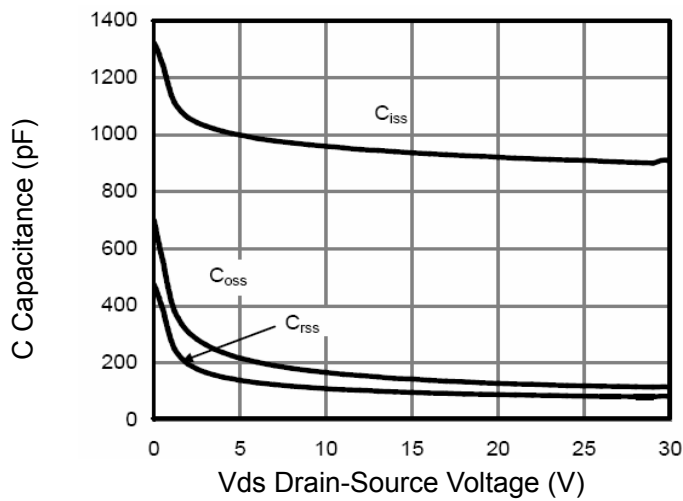


Figure 7 Capacitance vs Vds

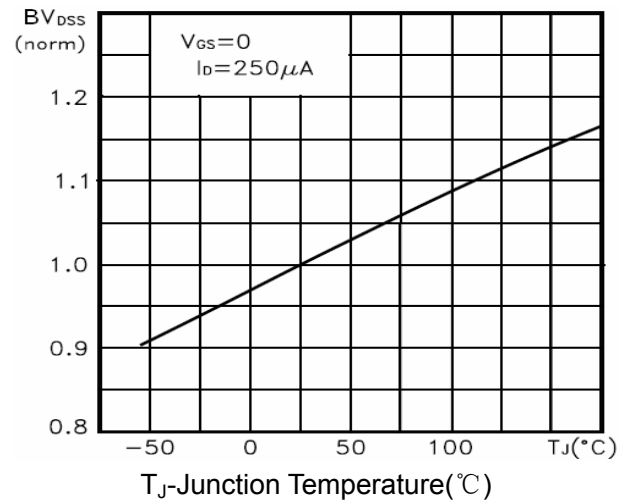


Figure 9 BV_{DSS} vs Junction Temperature

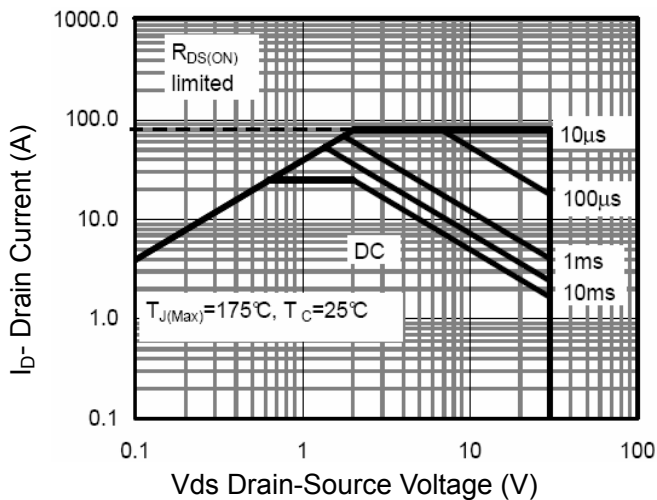


Figure 8 Safe Operation Area

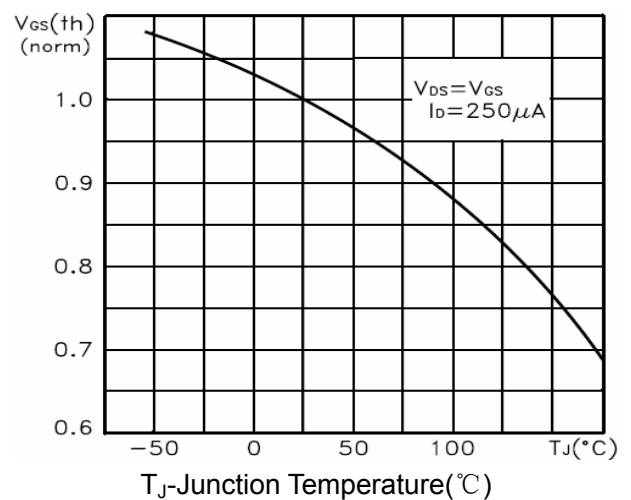


Figure 10 $V_{GS(th)}$ vs Junction Temperature

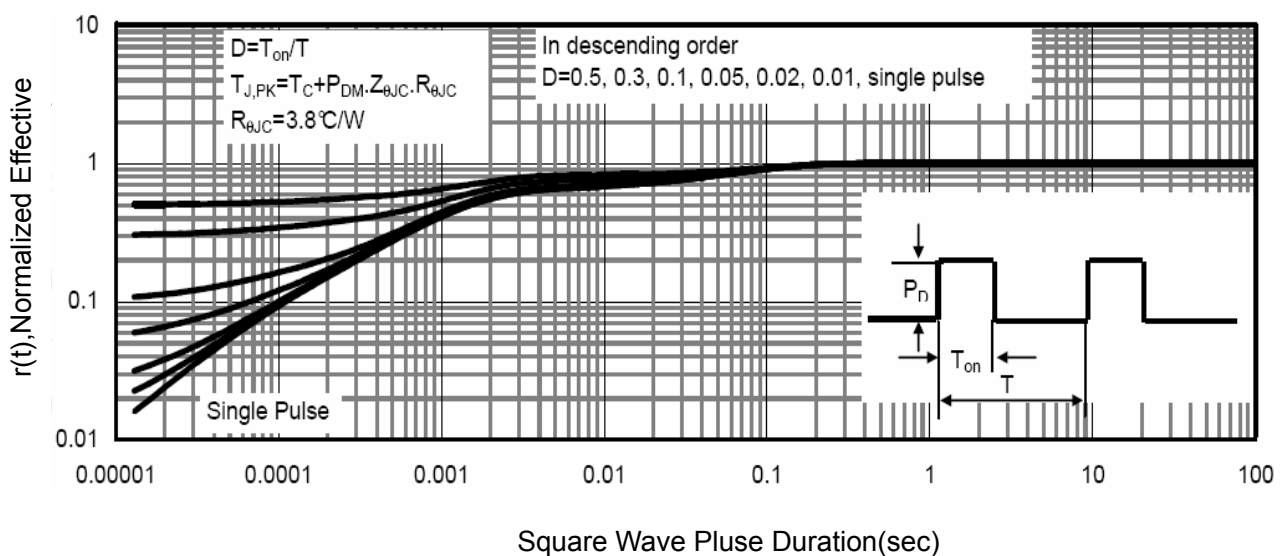
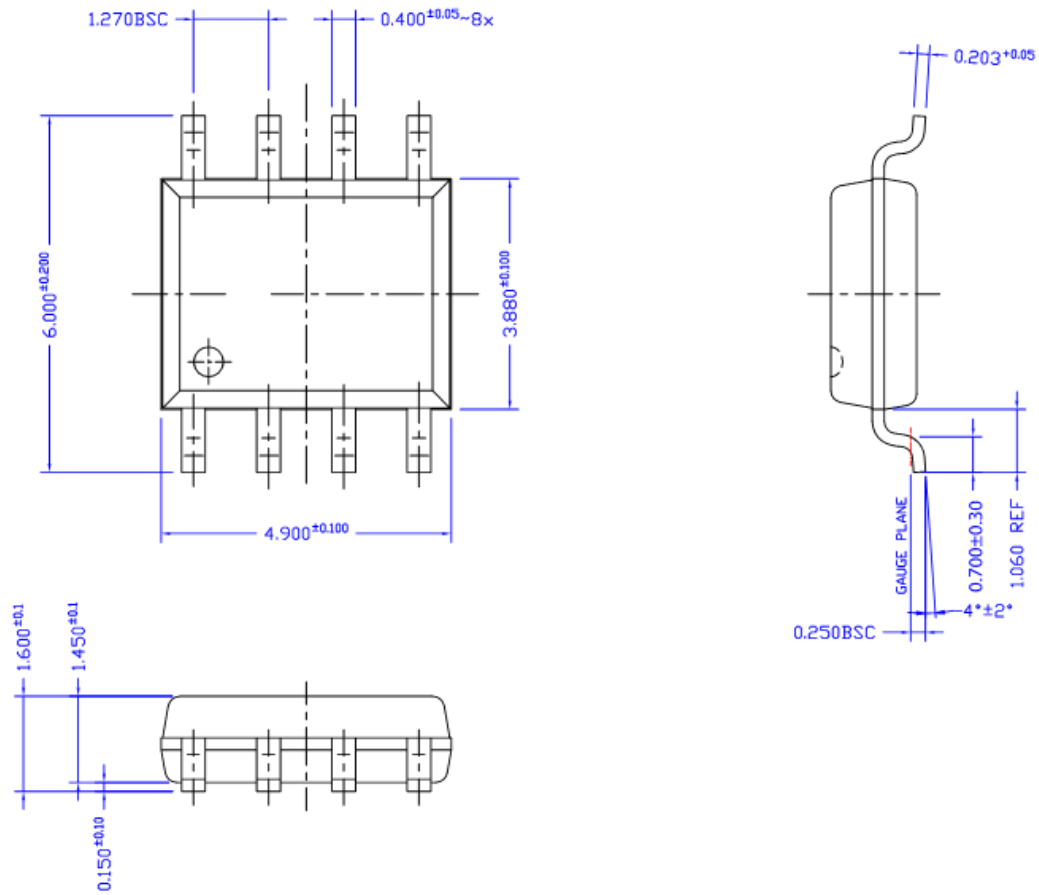


Figure 11 Normalized Maximum Transient Thermal Impedance



subject to real sample