

Sensor for Capacitive Touch/Proximity Detection

Features

- 3/5/7/10/12-channel capacitive sensor
- Self/Mutual capacitive sensing techniques
- Capacitance resolution down to 1aF
- Capacitance offset compensation up to 220pF
- Auto-Offset-Tuning (AOT)
- Adaptive temperature compensation
- Multi-threshold judgment
- Effective waterproof
- Independent configurations per channel
- Built-in gesture/event recognition
- 1.2V/1.8V 400kHz I²C interface
- Embedded 8KB DATARAM and 12KB CODERAM
- Ultra-low power consumption^(NOTE1)
 - Active mode: 21.9μA
 - Doze mode: 9.7μA
 - Sleep mode: 7.9μA
 - DeepSleep mode: 6.1μA
- 1.65V~3.6V power supply
- Package
 - AW93303FDR: FCDFN 1.6X1.0-8L
 - AW93303BFOR: FOWLFP 1.376X1.14-9B
 - AW93305DNR: DFN 2.1X1.8-10L
 - AW93305BFOR: FOWLFP 1.376X1.14-9B
 - AW93307QNR: QFN 1.9X1.8-12L
 - AW93310QNR: QFN 2X2-14L
 - AW93312QNR: QFN 3X3-24L

NOTE1: Power test configuration of each mode is shown in Table Electrical Characteristics.

Applications

- Wearable devices
- Mobile phones
- Tablets
- Notebooks

General Description

AW93303FDR, AW93303BFOR, AW93305DNR, AW93305BFOR, AW93307QNR, AW93310QNR and AW93312QNR are mul-channel capacitive sensors and mainly used for wear detection, touch key, linear slider, wheel slider, etc.

Advanced self/mutual capacitance technology is adopted in AW933XX. With a high-resolution ADC and advanced digital signal processing (DSP) algorithm, the minimal capacitance that can be detected is as low as 1aF in typical application.

AW933XX contains the I²C serial communication bus. Through I²C, Host can configure the chip to work. Upon event detection, the interrupt pin outputs asserts, enabling Host to receive the event information such as distance.

A built-in ultra-low power MCU realizes AFE sampling control, signal filtering, RF noise suppression, adaptive temperature compensation, baseline tracking, touch/wearing status determination, etc.

With the advanced DSP algorithm, AW933XX is able to track gradual environmental variations (such as temperature, humidity, etc.).

AW933XX can recognize various gestures, such as single/double/triple click, short/long press, linear slide and wheel slide with the high-resolution capacitive sensing. The chip integrates mutual capacitive technology and dedicated algorithm, which greatly improve the waterproof performance for touch key.

Typical Application Circuit

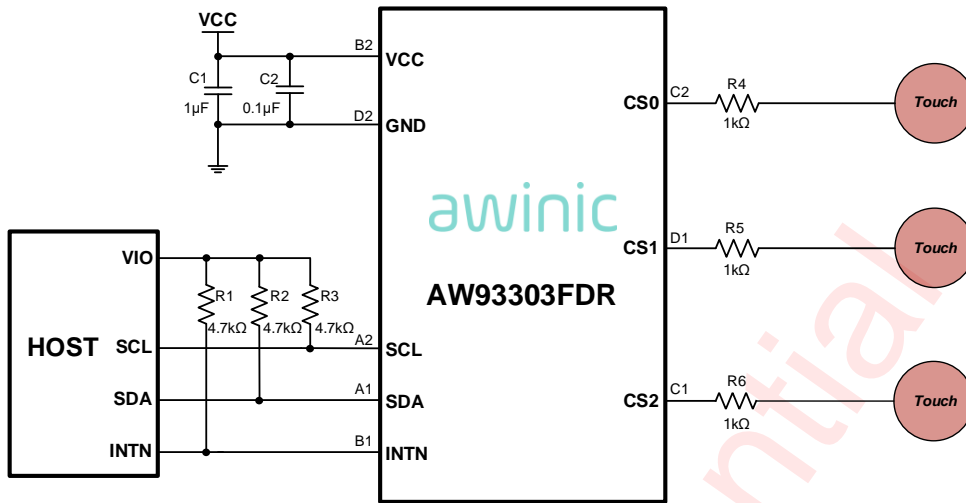


Figure 1 AW93303FDR Typical Application Circuit

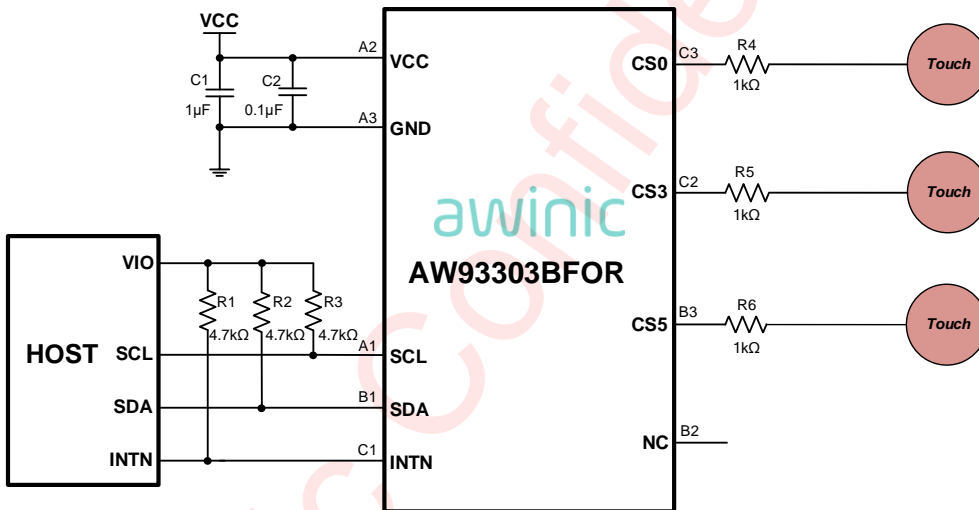


Figure 2 AW93303BFOR Typical Application Circuit

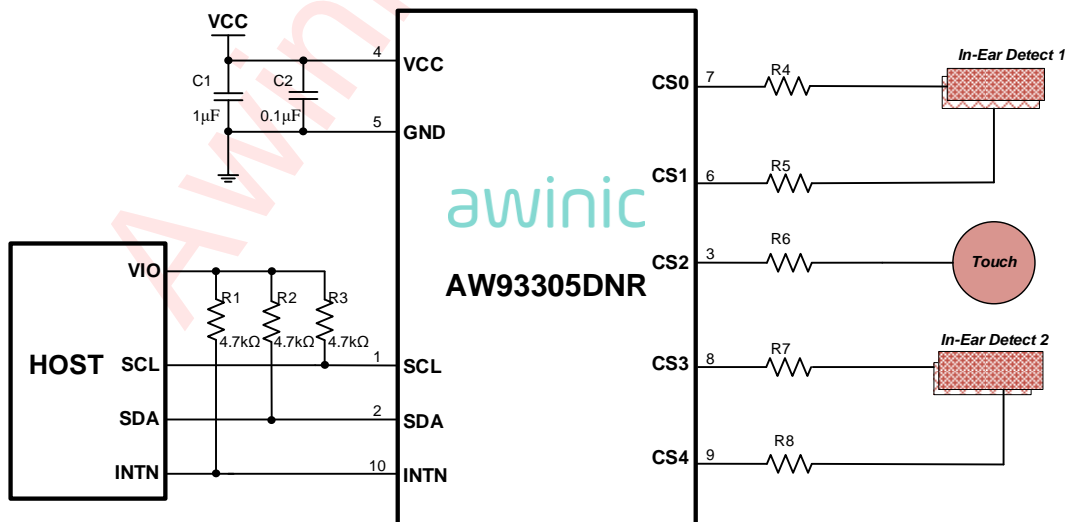


Figure 3 AW93305DNR Typical Application Circuit

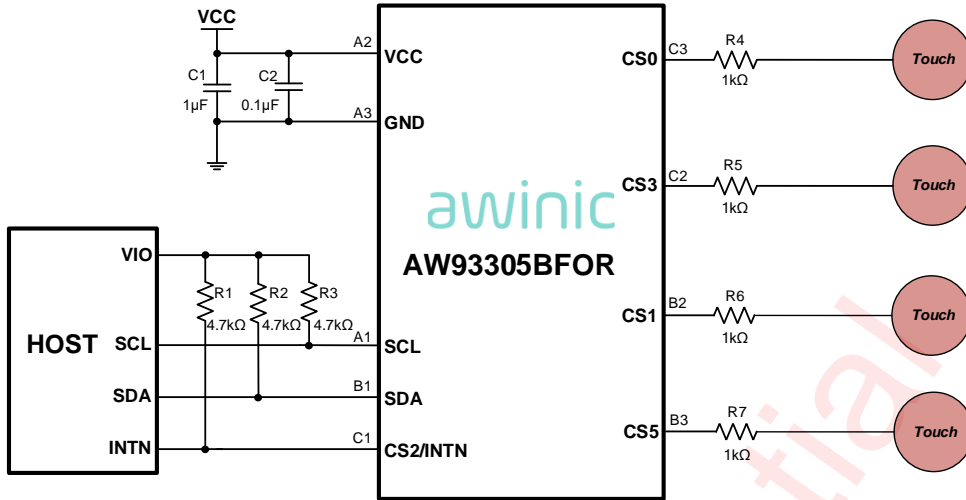


Figure 4 AW93305BFOR Typical Application Circuit

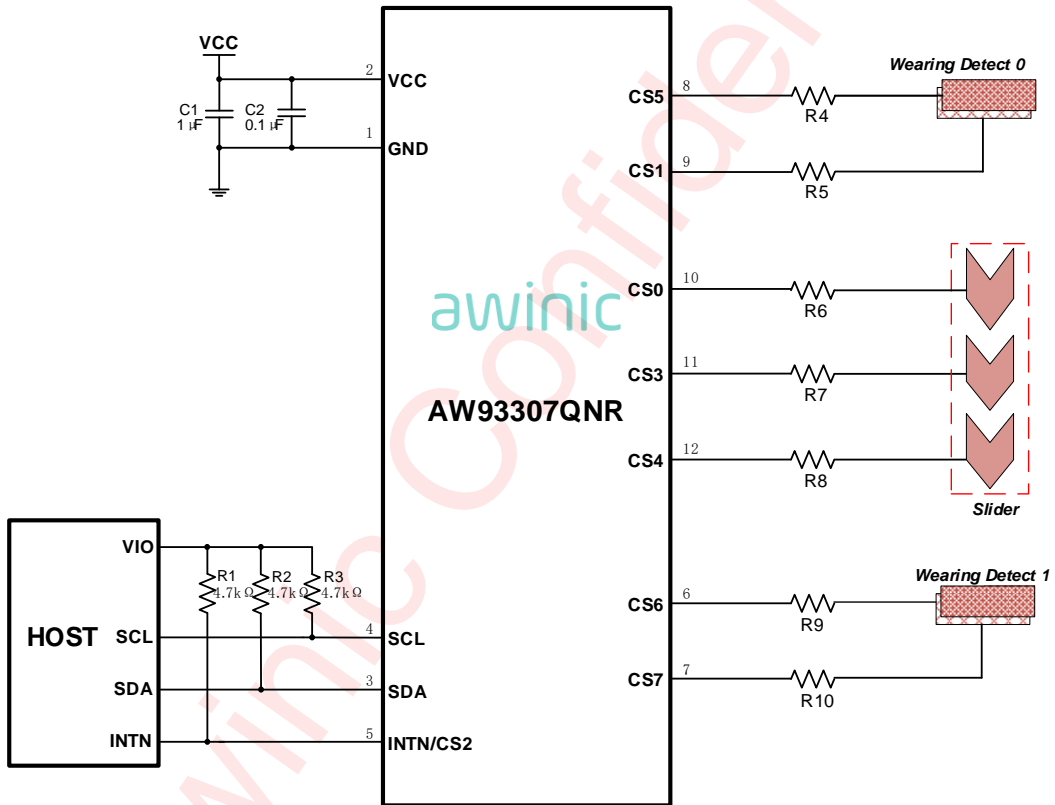


Figure 5 AW93307QNR Typical Application Circuit

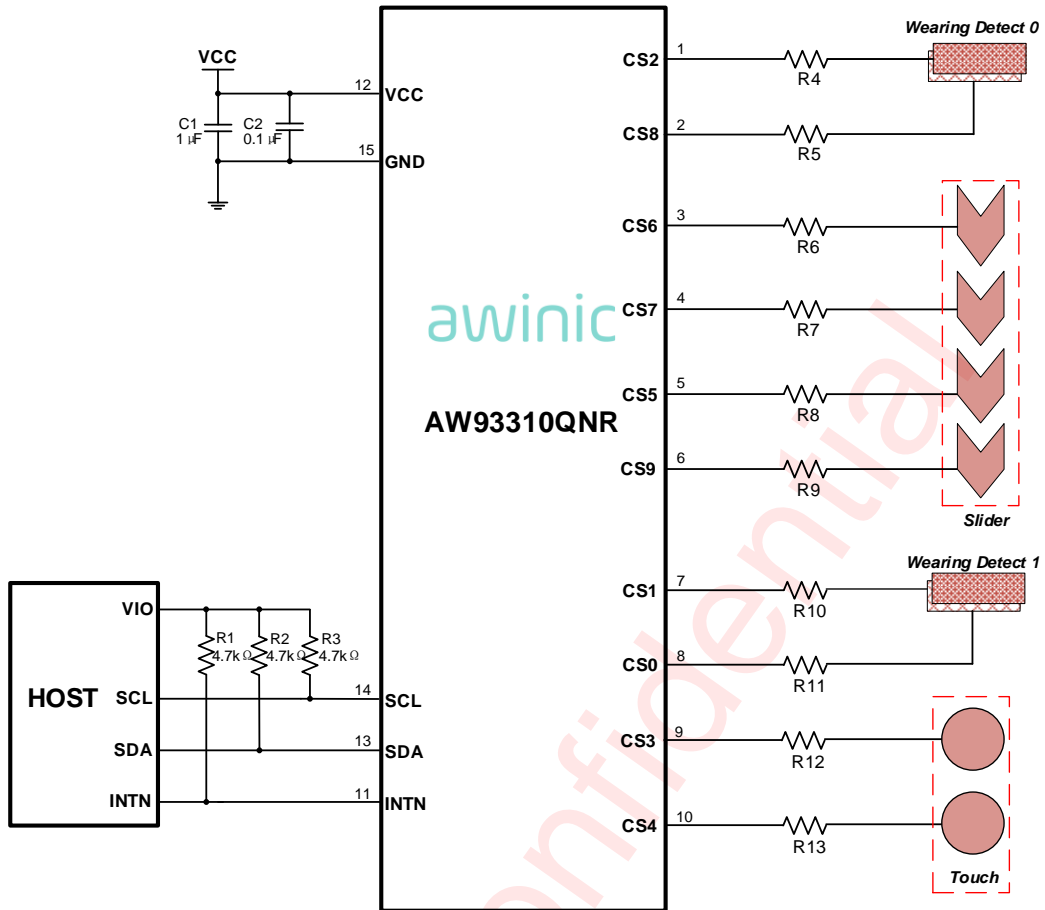


Figure 6 AW93310QNR Typical Application Circuit

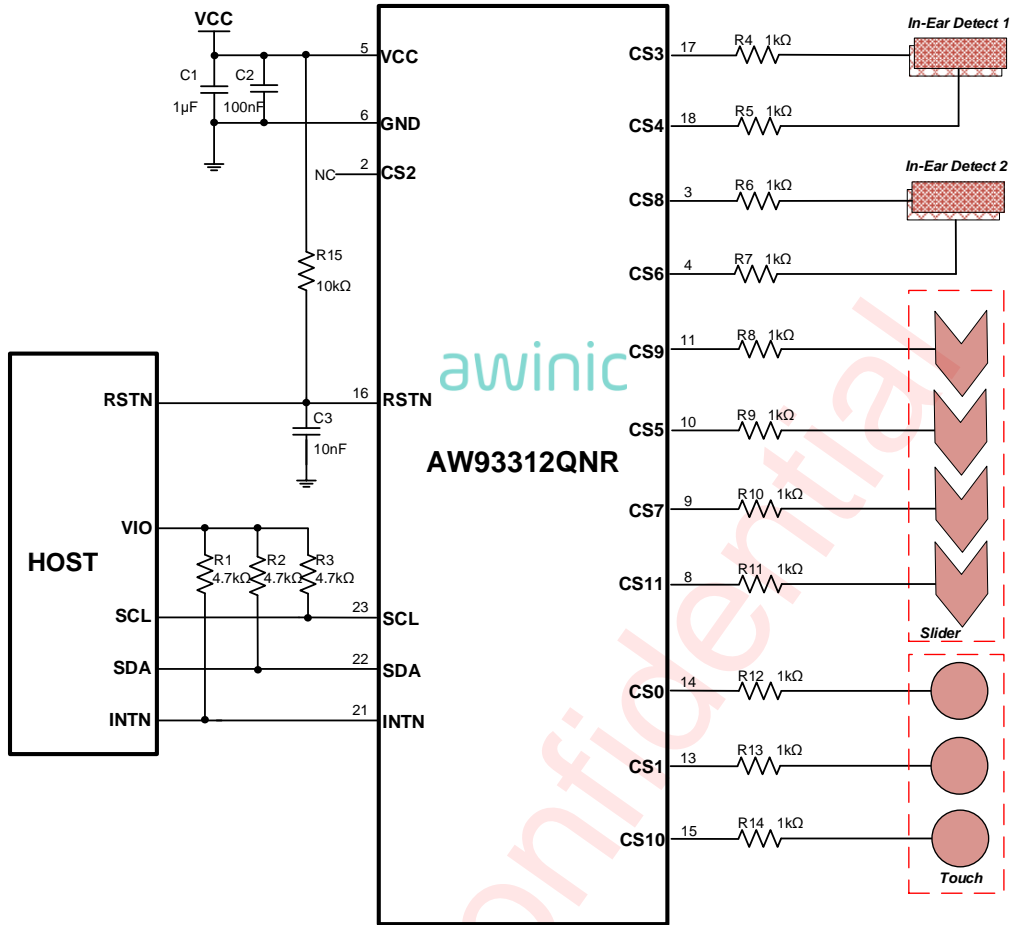
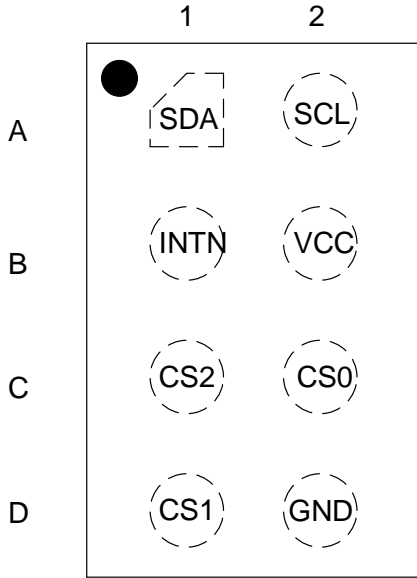


Figure 7 AW93312QNR Typical Application Circuit

Pin Configuration And Top Mark

AW93303FDR
(Top View)

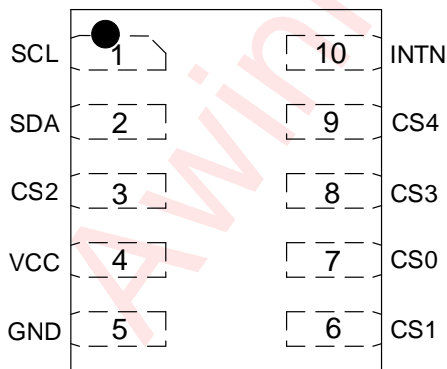


AW93303FDR Marking
(Top View)

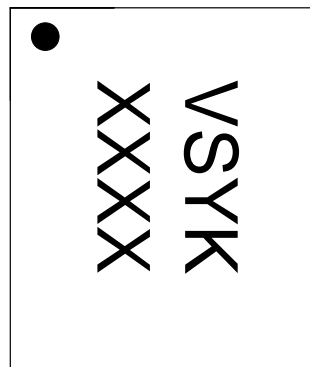


VZ — AW93303FDR
XX — Production Tracing Code

AW93305DNR
(Top View)

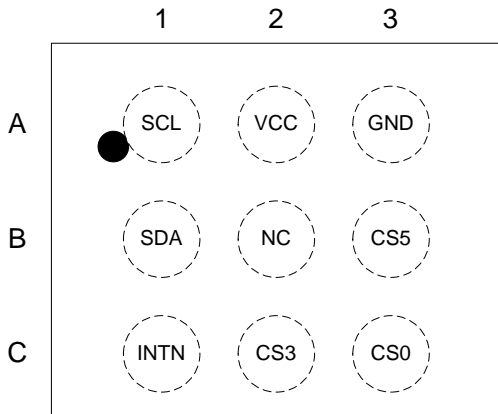


AW93305DNR Marking
(Top View)

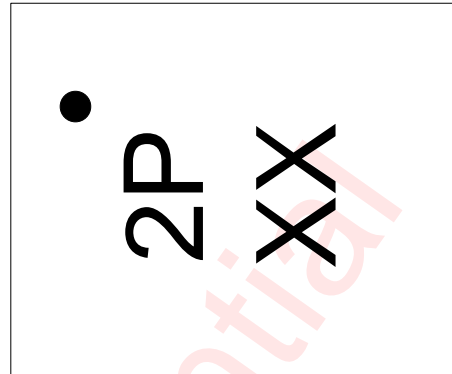


VSYK - AW93305DNR
XXXX - Production Tracing Code

AW93303BFOR
(Top View)

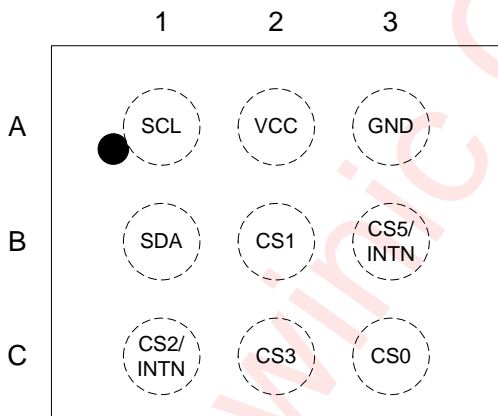


AW93303BFOR Marking
(Top View)

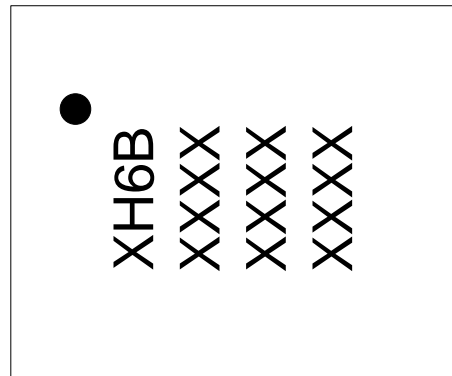


2P - AW93303BFOR
XX - Production Tracing Code

AW93305BFOR
(Top View)

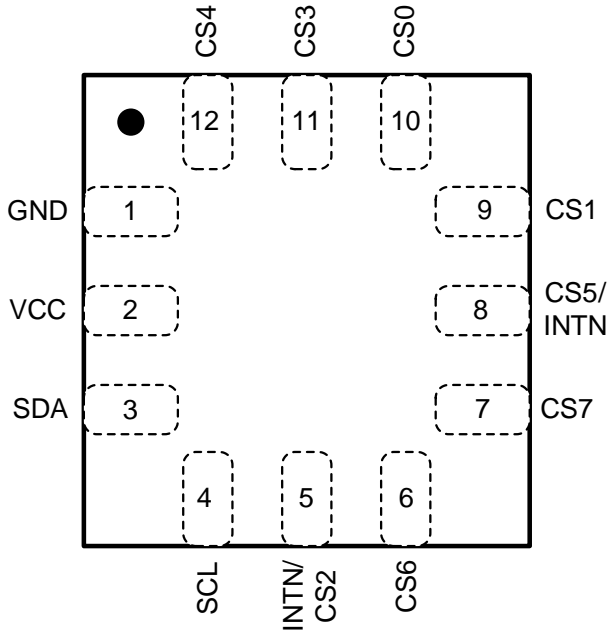


AW93305BFOR Marking
(Top View)

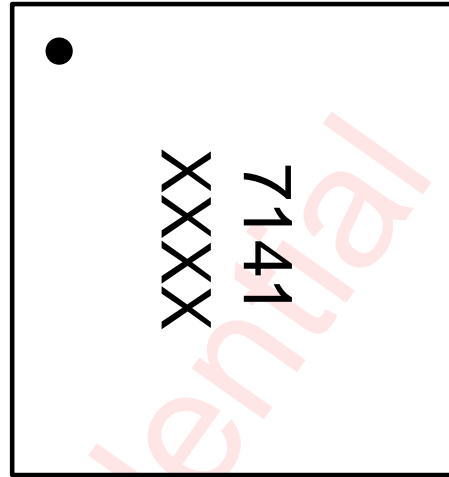


XH6B - AW93305BFOR
XXXX/XXXX/XXXX - Production Tracing Code

AW93307QNR
(Top View)

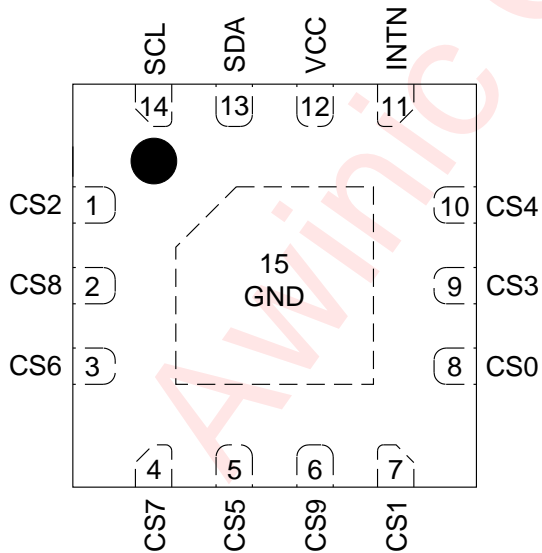


AW93307QNR Marking
(Top View)

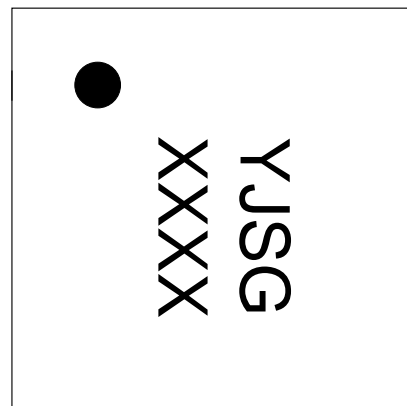


7141 - AW93307QNR
XXXX - Production Tracing Code

AW93310QNR
(Top View)



AW93310QNR Marking
(Top View)



YJSG - AW93310QNR
XXXX - Production Tracing Code

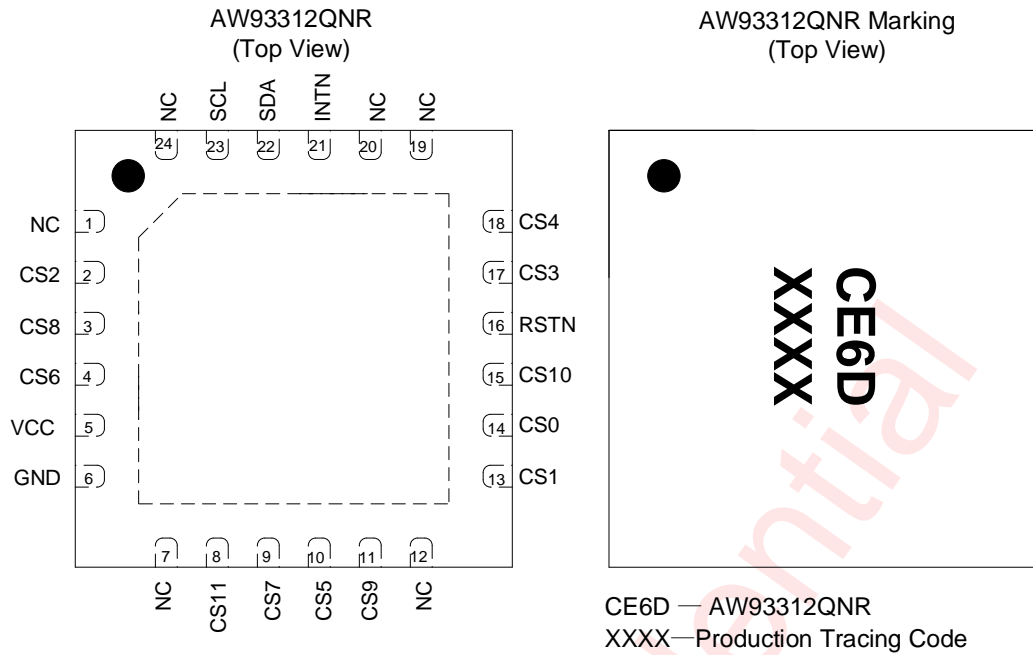


Figure 8 Pin Configuration and Marking

Pin Definition

Name	Pin No.		Description
	AW93303FDR	AW93305DNR	
SCL	A2	1	I ² C clock, requires pull-up resistor
SDA	A1	2	I ² C data, requires pull-up resistor
CS2	C1	3	Capacitive sensor input or I ² C address select input
VCC	B2	4	Power supply (1.65V~3.6V), requires decoupling capacitor
GND	D2	5	Ground
CS1	D1	6	Capacitive sensor input
CS0	C2	7	Capacitive sensor input
CS3	-	8	Capacitive sensor input
CS4	-	9	Capacitive sensor input
INTN	B1	10	Interrupt output, requires pull-up resistor

Name	Pin No.		Description
	AW93303BFOR		
SCL	A1		I ² C clock, requires pull-up resistor
VCC	A2		Power supply (1.65V~3.6V), requires decoupling capacitor
GND	A3		Ground
SDA	B1		I ² C data, requires pull-up resistor
NC	B2		Not connection
CS5	B3		Capacitive sensor input

Name	Pin No.	Description
	AW93303BFOR	
INTN	C1	Interrupt output, requires pull-up resistor
CS3	C2	Capacitive sensor input
CS0	C3	Capacitive sensor input

Name	Pin No.	Description
	AW93305BFOR	
SCL	A1	I ² C clock, requires pull-up resistor
VCC	A2	Power supply (1.65V~3.6V), requires decoupling capacitor
GND	A3	Ground
SDA	B1	I ² C data, requires pull-up resistor
CS1	B2	Capacitive sensor input
CS5/INTN	B3	Capacitive sensor input or interrupt output
CS2/INTN	C1	Capacitive sensor input or interrupt output
CS3	C2	Capacitive sensor input
CS0	C3	Capacitive sensor input

Name	Pin No.	Description
	AW93307QNR	
GND	1	Ground
VCC	2	Power supply (1.65V~3.6V), requires decoupling capacitor
SDA	3	I ² C data, requires pull-up resistor
SCL	4	I ² C clock, requires pull-up resistor
INTN/CS2	5	Interrupt output or capacitive sensor input
CS6	6	Capacitive sensor input
CS7	7	Capacitive sensor input
CS5/INTN	8	Capacitive sensor input or interrupt output
CS1	9	Capacitive sensor input
CS0	10	Capacitive sensor input or I ² C address control bit
CS3	11	Capacitive sensor input or I ² C address control bit
CS4	12	Capacitive sensor input

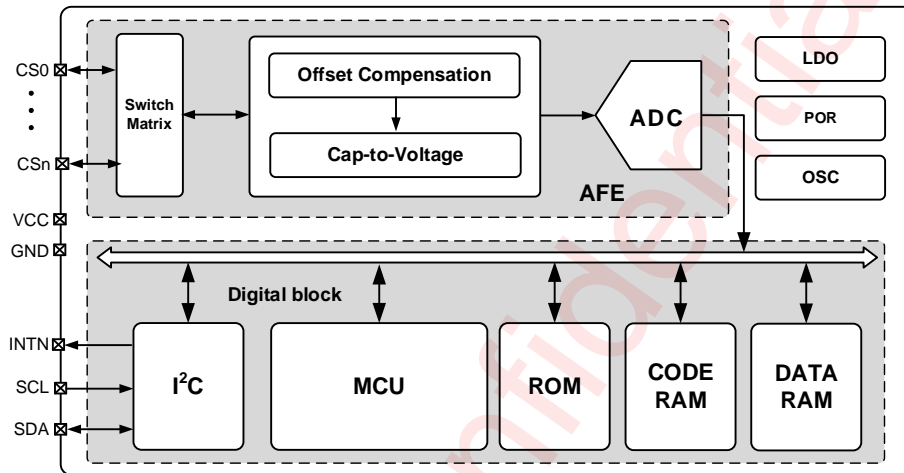
Name	Pin No.	Description
	AW93310QNR	
CS2	1	Capacitive sensor input or I ² C address control bit
CS8	2	Capacitive sensor input

Name	Pin No.	Description
	AW93310QNR	
CS6	3	Capacitive sensor input
CS7	4	Capacitive sensor input
CS5	5	Capacitive sensor input
CS9	6	Capacitive sensor input
CS1	7	Capacitive sensor input
CS0	8	Capacitive sensor input
CS3	9	Capacitive sensor input
CS4	10	Capacitive sensor input
INTN	11	Interrupt output, requires pull-up resistor
VCC	12	Power supply (1.65V~3.6V), requires decoupling capacitor
SDA	13	I ² C data, requires pull-up resistor
SCL	14	I ² C clock, requires pull-up resistor
GND	15	Ground

Name	Pin No.	Description
	AW93312QNR	
NC	1	Not connect
CS2	2	Capacitive sensor input or I ² C address select input
CS8	3	Capacitive sensor input
CS6	4	Capacitive sensor input
VCC	5	Power supply (1.65V~3.6V), requires decoupling capacitor
GND	6	Ground
NC	7	Not connect
CS11	8	Capacitive sensor input
CS7	9	Capacitive sensor input
CS5	10	Capacitive sensor input
CS9	11	Capacitive sensor input
NC	12	Not connect
CS1	13	Capacitive sensor input
CS0	14	Capacitive sensor input
CS10	15	Capacitive sensor input
RSTN	16	RESET pin, active low
CS3	17	Capacitive sensor input
CS4	18	Capacitive sensor input
NC	19	Not connect
NC	20	Not connect
INTN	21	Interrupt output, requires pull-up resistor

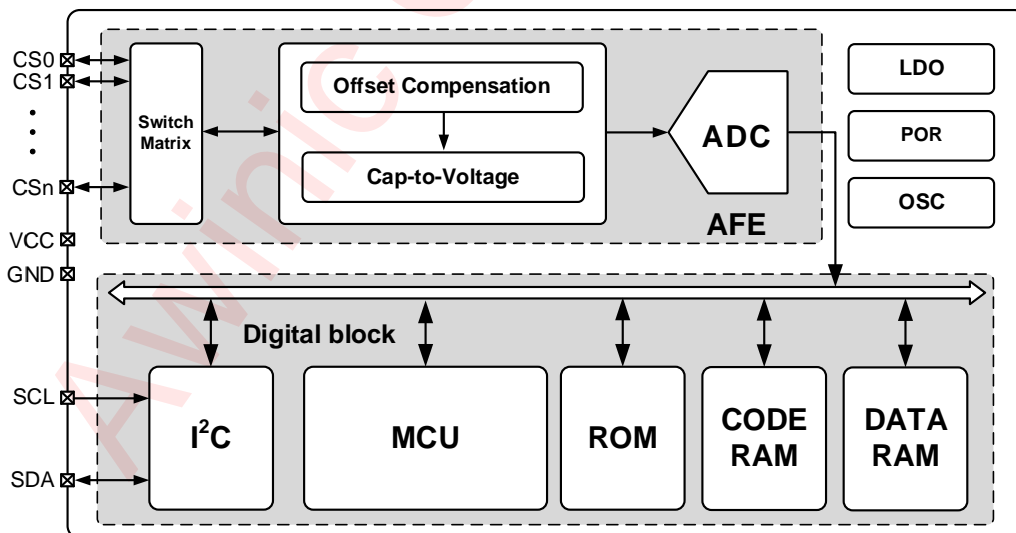
Name	Pin No.	Description
	AW93312QNR	
SDA	22	I ² C data, requires pull-up resistor
SCL	23	I ² C clock, requires pull-up resistor
NC	24	Not connect

Functional Block Diagram



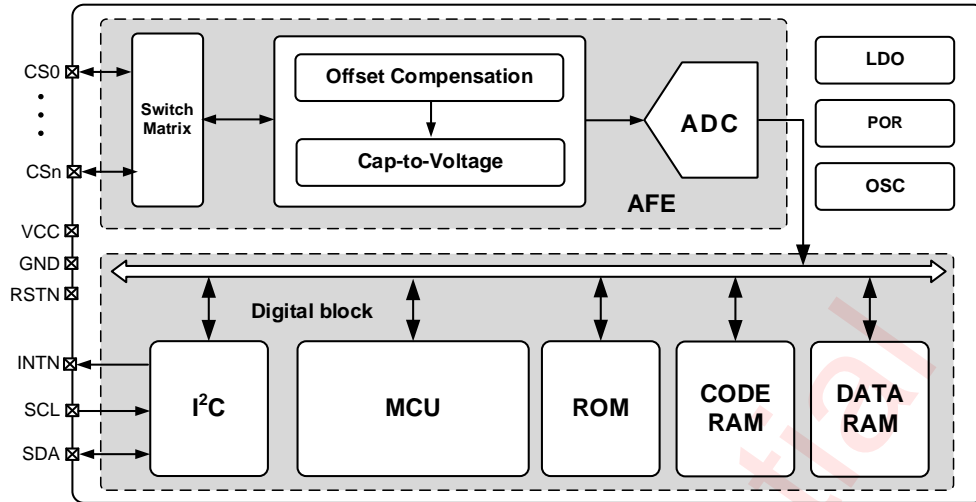
Note: AFE means Analog Front-End.

Figure 9 AW93303FDR/AW93303BFOR/AW93305DNR/AW93307QNR /AW93310QNR Functional Block Diagram



Note: AFE means Analog Front-End.

Figure 10 AW93305BFOR Functional Block Diagram



Notes: AFE means Analog Front-End.

Figure 11 AW93312QNR Functional Block Diagram

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Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW93303FDR	-40°C~85°C	FCDFN 1.6X1.0-8L	VZ	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93305DNR	-40°C~85°C	DFN 2.1X1.8- 10L	VSYK	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW93303BFOR	-40°C~85°C	FOWLP 1.376x1.14-9B	2P	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW93305BFOR	-40°C~85°C	FOWLP 1.376x1.14-9B	XH6B	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW93307QNR	-40°C~85°C	QFN 1.9X1.8- 12L	7141	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93310QNR	-40°C~85°C	QFN 2x2-14L	YJSG	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93312QNR	-40°C~85°C	QFN 3x3-24L	CE6D	MSL1	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings ^(NOTE2)

PARAMETERS	RANGE
Supply voltage range VCC	-0.5V to 4.0V
Input voltage range (non-supply pins)	-0.5V to VCC+0.3V
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature T _{JMAX}	150°C
Storage temperature T _{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD(Including HBM CDM) ^(NOTE3)	
HBM	±8kV
CDM	±1.5kV
Latch-Up	
Test condition: according to JEDEC78E	+IT: 350mA -IT: -350mA

NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE3: The HBM test method of AW93303FDR, AW93303BFOR, AW93305DNR, AW93305BFOR, AW93307QNR and AW93312QNR: ESDA/JEDEC JS-001-2017, the CDM test method of AW93303FDR, AW93303BFOR, AW93305DNR, AW93305BFOR, AW93307QNR and AW93312QNR: ESDA/JEDEC JS-002-2018. The HBM test method of AW93310QNR: ESDA/JEDEC JS-001-2023, the CDM test method of AW93310QNR: ESDA/JEDEC JS-002-2022.

Recommended Operating Conditions

Parameters	Symbol	TEST CONDITION	Min	Max	Unit
Supply voltage	VCC	-	1.65 ^(NOTE4)	3.6	V
Pull-up voltage	VIO	AW93303FDR, AW93305DNR, AW93310QNR, AW93312QNR	1.1	3.6	V
Pull-up voltage	VIO	AW93303BFOR, AW93305BFOR, AW93307QNR	1.1	VCC	V
Ambient temperature	T _A	-	-40	85	°C

NOTE4: Recommend VCC≥1.7V for optimum analog performance.

Electrical Characteristics

Note: Typical values are given for T_A = +25°C, VCC=1.8V unless otherwise specified.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
CHIP CURRENTS					
I _{DEEPSLEEP}	DeepSleep Mode Current LDO on, OSC off I ² C listening		6.1	15	μA
I _{SLEEP}	AW93303FDR/AW93305DNR: LDO on, OSC on I ² C listening		7.9	18	μA
	AW93303BFOR/ AW93305BFOR/ AW93307DNR/AW93310QNR/ AW93312QNR: LDO on, OSC on I ² C listening		8.9	18	μA
I _{DOZE}	AW93303FDR/AW93305DNR: SCANPERIOD = 400ms FREQ = 100kHz; CDCRES = 6 CVIREF=3 CHEN = b000001 Digital filter features off I ² C listening. No load		9.7	22	μA
	AW93303BFOR/ AW93305BFOR/ AW93307QNR/ AW93310QNR/AW93312QNR:		10.7	22	μA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		SCANPERIOD = 400ms FREQ = 100kHz; CDCRES = 6 CVIREF=3 CHEN = b000001 Digital filter features off I ² C listening. No load				
I _{ACTIVE}	Active Mode Current	AW93303FDR/AW93305DNR: SCANPERIOD = 30ms FREQ = 100kHz CDCRES = 6 CVIREF=3 CHEN = b000001 Digital filter features off I ² C listening. No load		21.9	42	μA
		AW93303BFOR/ AW93305BFOR/ AW93307QNR/ AW93310QNR/AW93312QNR: SCANPERIOD = 30ms FREQ = 100kHz CDCRES = 6 CVIREF=3 CHEN = b000001 Digital filter features off I ² C listening. No load		23.5	42	μA
CAPACITANCE SENSING						
C _{RANGE}	Measurement Range		±0.55	±2.2	±9.9	pF
N _{BIT}	Measurement Resolution			21		bits
C _{RES}					1	
F _{OSC}	Nominal OSC Frequency	AW93303FDR/AW93305DNR		4		MHz
		AW93303BFOR/ AW93305BFOR/ AW93307QNR/ AW93310QNR/AW93312QNR		8		MHz
F _{Trim}	OSC Trim Accuracy	Around Nominal Value, Ta=25°C, VCC=2.8V	-4		4	%
F _{Temp} (NOTE5)	OSC Temp. Dependency	Around Nominal Value, Full Ta range, VCC=2.8V	-1		1	%
F _{VCC} (NOTE5)	OSC VCC Dependency	Around Nominal Value, Ta=25°C, Full VCC range	-0.6		0.6	%
F _S	Nominal Sampling Freq	Programmable with FREQ AW93303FDR/AW93305DNR	F _{osc} /1024		F _{osc} / 16	kHz
		Programmable with FREQ AW93303BFOR/ AW93305BFOR/ AW93307QNR/ AW93310QNR/AW93312QNR	F _{osc} /2048		F _{osc} / 32	kHz
C _{DCEXT}	External DC Cap. to GND per Measurement Phase	One CSx as measured input			220	pF
R _{FILTIN}	Input driving Res		0		15	kΩ
I²C INTERFACE						
I _{OL} (SDA, INTN)	Output low current	V _{OL} ≤ 0.4V	8			mA
V _{OL} (SDA, INTN)	Output low voltage	I _{OL} = 3mA	-		0.25	V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IH}	Input high level	SCL, SDA	0.9		3.6	V
V _{IL}	Input low level	SCL, SDA	-0.5		0.36	V
t _{DEG_SDA}	SDA deglitch time	SDA		88		ns
t _{DEG_SCL}	SCL deglitch time	SCL		77		ns

NOTE5: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

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I2C Interface Timing

Parameter		Min	Typ	Max	Unit
F_{SCL}	Interface Clock frequency			400	kHz
$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μ S
t_{LOW}	Low level width of SCL	1.3			μ S
t_{HIGH}	High level width of SCL	0.6			μ S
$t_{SU:STA}$	(Repeat-start) Start condition setup time	0.6			μ S
$t_{HD:DAT}$	Data hold time	0			μ S
$t_{SU:DAT}$	Data setup time	0.1			μ S
t_R	Rising time of SDA and SCL			0.3	μ S
t_F	Falling time of SDA and SCL			0.3	μ S
$t_{SU:STO}$	Stop condition setup time	0.6			μ S
t_{BUF}	Time between start and stop condition	1.3			μ S

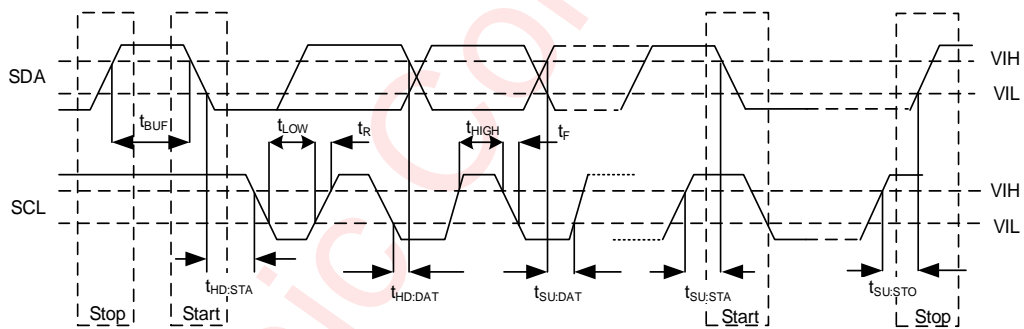


Figure 12 I²C Interface Timing

Detailed Functional Description

Overview

AW933XX is a capacitive proximity sensor with a built-in ultra-low-power MCU. It is comprised of high-performance self/mutual capacitance detecting Analog-Front-End (AFE), embedded 32-bit MCU, ROM, RAM, OSC and I²C interface, etc. The AFE drives the sensor electrode, and converts the capacitance of sensor to digital data. The MCU executes the algorithm program stored in ROM or CODERAM, and performs complete data process that contains signal filtering, baseline calculation, automatic compensation for environmental drift, radio frequency (RF) noise suppression, proximity decision, etc.

Capacitive Sensor Introduction

When a conductive object, such as a finger, comes in contact or close proximity with the sensing electrode, the capacitance of one or more sensors changes. The figure 10 shows the basic structure and equivalent model of a capacitive sensor. The top layer is the overlay, and the middle layer which is green is a copper sensor pad. The sensor is usually surrounded by ground with a parasitic capacitance(C_{PARA}).

There are two main operational modes in the capacitance sensing circuits: self-capacitance sensing and mutual capacitance sensing. An electric field is created around the sensor when system is working. In the self-capacitance sensing mode, with target object approaching, some of the electric field lines couple to the target object and a small amount of target object capacitance (C_{PROX}) adds to the existing C_{PARA} . This feature can be used to detect proximity or touch action.

At least two electrodes are needed in the mutual capacitance sensing mode: one is a transmitter (Tx) and the other is a receiver (Rx). Tx and ground will form a capacitance (C_{TX}); Rx and ground will form a capacitance (C_{RX}); Tx and Rx will form a capacitance (C_M). When target object approaches, Tx and Rx will form a capacitance (C_M') which is less than C_M .

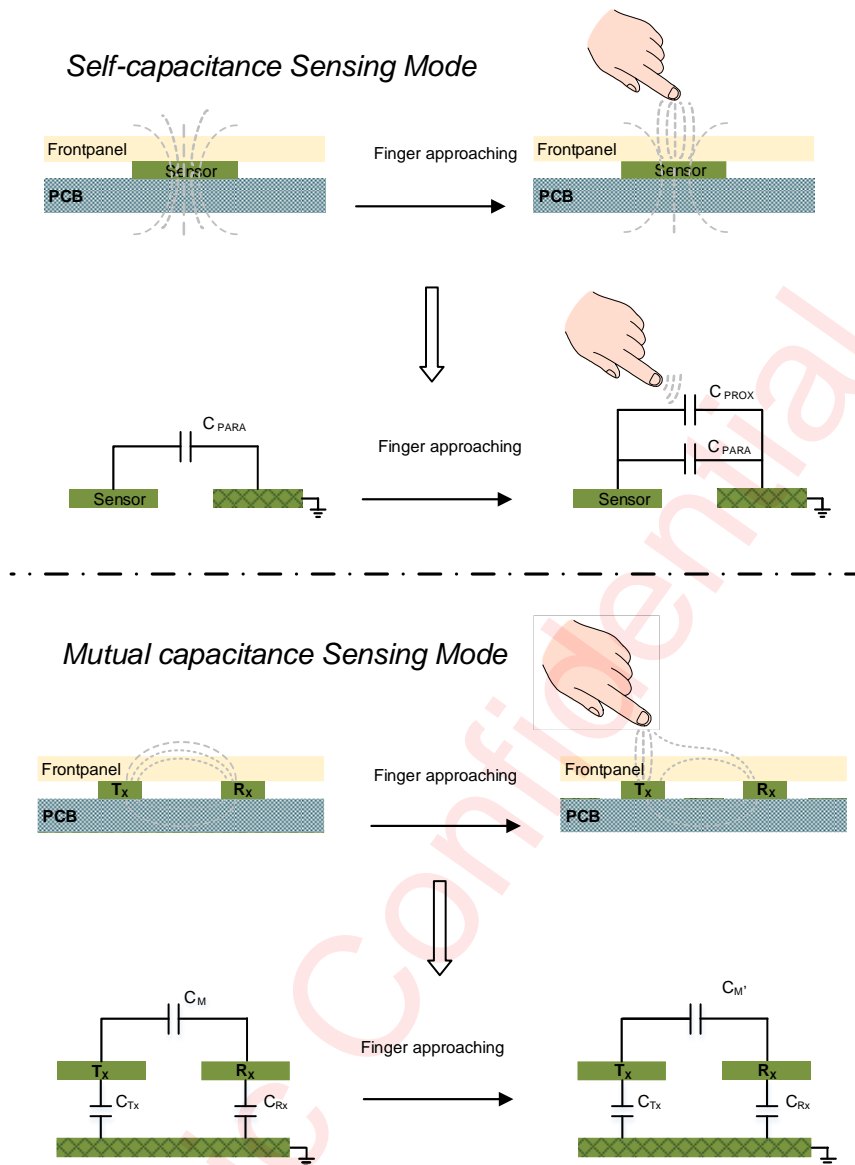


Figure 13 Capacitive Sensor Structure

Capacitive Sensing Techniques

The proximity sensing system consists of three parts: capacitive sensor, AFE and DSP. The function of AFE is to drive the capacitive sensor electrode, and convert the sensor capacitance to digital data. The function of DSP is to process the data from AFE and transmit the sensor capacitance value (*CapDiff*) together with proximity status (*status*) to the Host. When the target object is approaching or moving away, the proximity sensing system will transmit key information to the Host after dedicated processing.

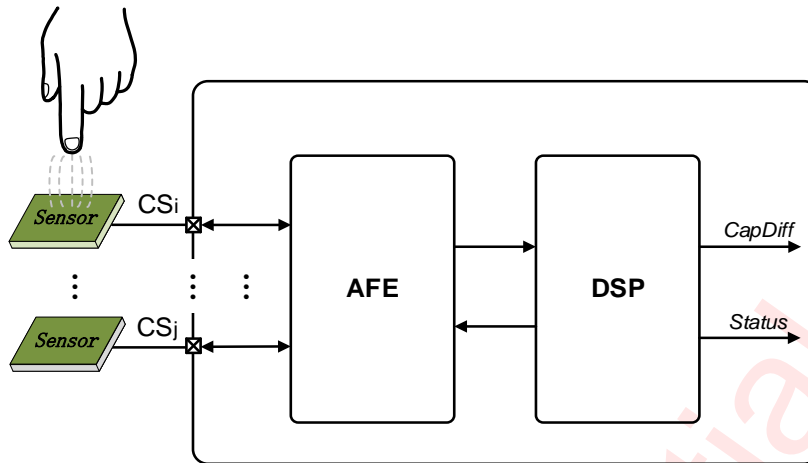


Figure 14 Proximity Sensor Operation Overview

AFE DESCRIPTION

- ※ Switch Matrix selects pin CSx as capacitance measurement input.
- ※ Block Cap-to-Voltage integrates a charge amplifier which detects the sensor capacitance with a charge-transfer method. The capacitance is converted into a voltage signal, which is the input of block ADC.
- ※ Block Offset Compensation measures parasitic capacitance (C_{PARA}), which is compensated during the process of charge transferring. Thus, the effective input capacitance of Cap-to-Voltage is approximately equal to C_{PROX} .
- ※ ADC converts voltage signals obtained from Cap-to-Voltage or Temp Sensor to digital data (*AdcData*).

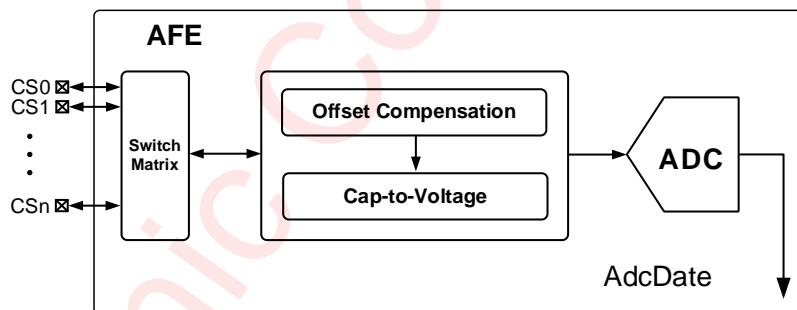
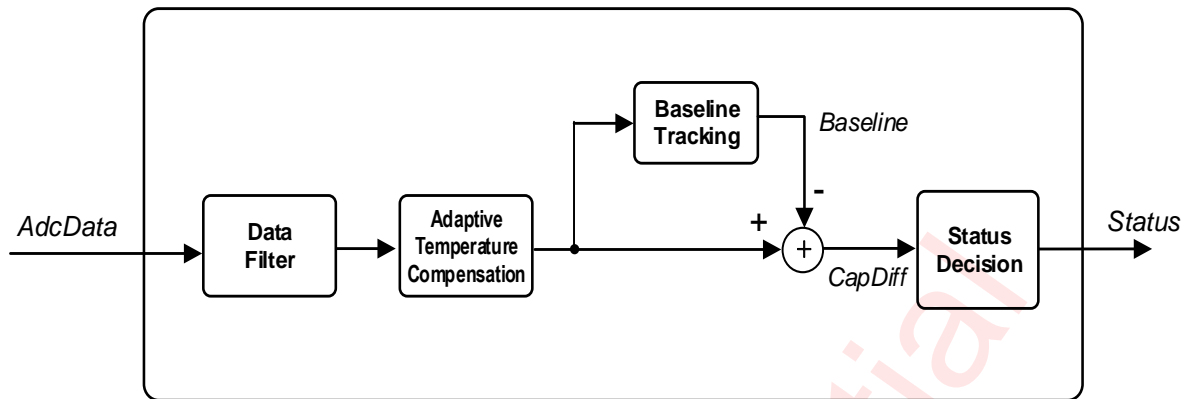
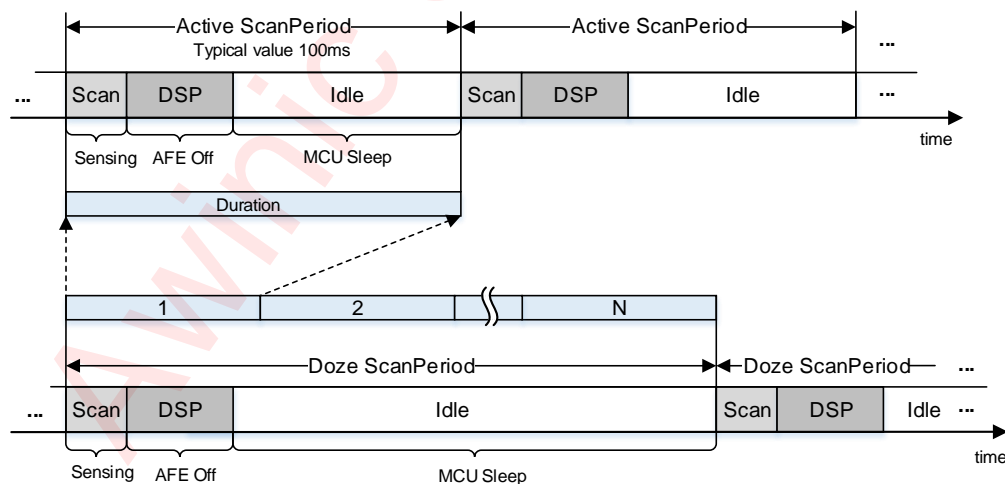


Figure 15 AFE Block Diagram

DSP DESCRIPTION**Figure 16 Digital Signal Processing Diagram**

- ※ DSP processes the *AdcData* from the AFE, and finally outputs a series of reliable proximity status.
- ※ Data Filter effectively filters the high-frequency noise and interference, which greatly improves the signal-to-noise ratio(SNR).
- ※ Block Adaptive Temperature Compensation can automatically compensate for environmental drift in real time, especially temperature drift. Thereby, the final proximity status will not be misjudged.
- ※ The role of the *Baseline* is to further track the slowly varying data caused by the residual temperature compensation or other gradual environmental drift.
- ※ Finally, block Status Decision outputs a certain and reliable proximity status based on the data *CapDiff* and the proximity threshold.

SCAN PERIOD**Figure 17 Active Mode and Doze Mode Scan Period**

Each scan period can be divided into three stages. In the first stage, the selected sensor channels are scanned and *AdcData* of each channel is generated. In the second stage, the AFE stops working and the DSP begins to process the obtained *AdcData*. In the last stage, all data processing has been completed and the chip enters idle status. In idle status, in order to reduce power consumption, neither AFE nor MCU works.

The figure 14 shows the composition and meaning of the Active mode and Doze mode scan periods. Generally, Doze mode consumes lower power than Active mode.

Reset

POWER ON RESET

When VIO and VCC are not on the same power source, VCC should be powered on no later than VIO. Reset operation is triggered during power up. When nRST (internal signal) is released, the initialization process starts to perform and will last for about 20ms. INTN will be set to low when the initialization process is completed, then I²C can communicate normally.

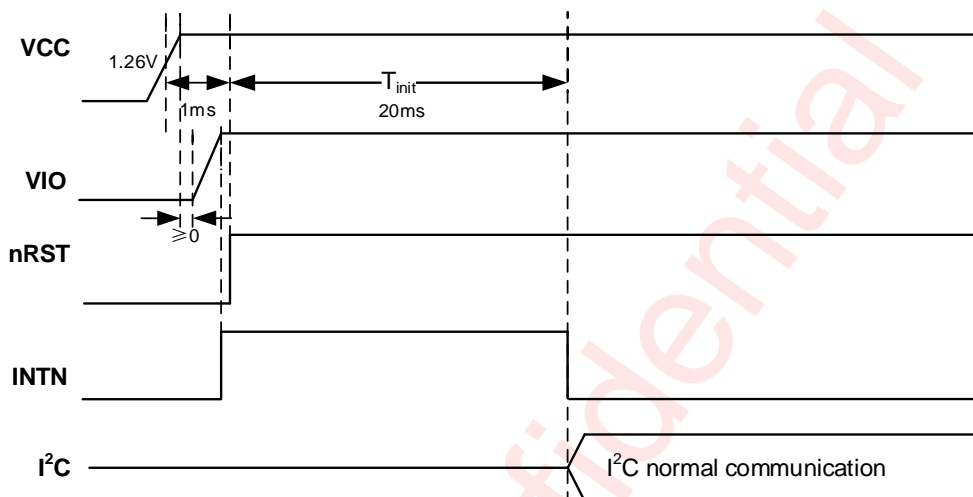


Figure 18 Power On Timing of AW93303FDR/AW93305DNR/AW93310QNR

When VIO and VCC are not on the same power source, VCC should be powered on no later than VIO. Reset operation is triggered during power up. When nRST (internal signal) released, the initialization process starts to perform and will last for about 20ms. INTN/CS2 is configured as an interrupt pin default, INTN/CS2 will be set to low when the initialization process is completed, then I²C can communicate normally.

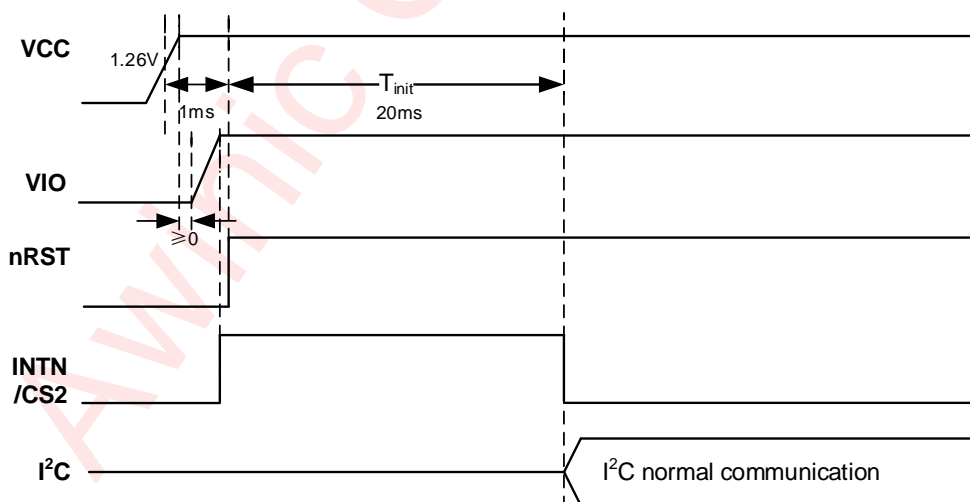


Figure 19 Power On Timing of AW93303BFOR/AW93305BFOR/AW93307QNR

When VIO and VCC are not on the same power source, VCC should be powered on no later than VIO. Reset operation is triggered during power up. When RSTN signal is released, the initialization process starts to perform and will last for about 20ms. INTN will be set to low when the initialization process is completed, then I²C can communicate normally.

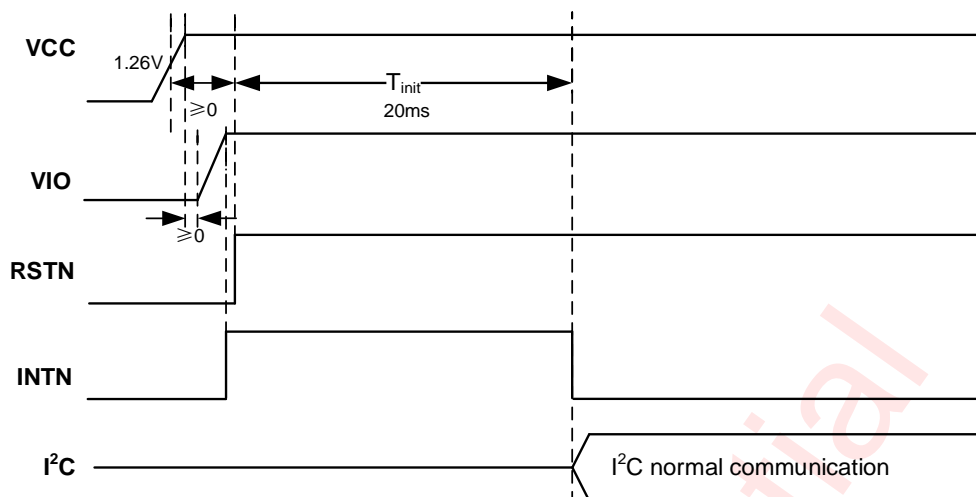


Figure 20 Power On Timing of AW93312QNR

SOFT RESET

The soft reset operation can be triggered by writing “0x0” to the soft reset register. After completion of soft reset operation, all the registers will be reset to the default value.

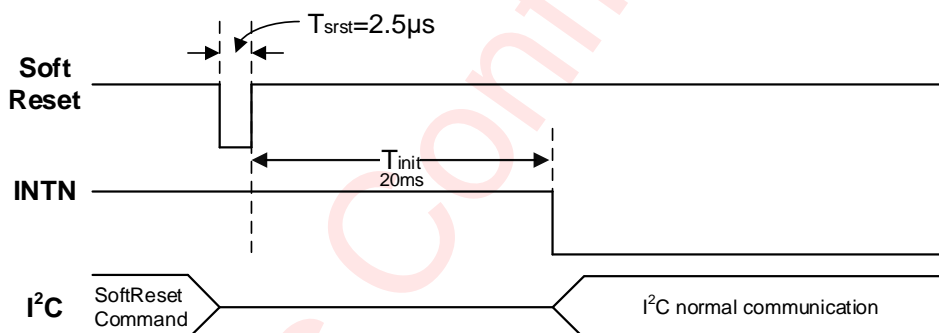


Figure 21 Soft Reset Timing

Clock

The chip of AW93303FDR/AW93305DNR uses a built-in 4MHz OSC clock.

The chip of AW93303BFOR/AW93305BFOR/AW93307QNR/AW93310QNR/AW93312QNR uses a built-in 8MHz OSC clock.

Initialization

After power on, first OSC runs, and then MCU starts to execute the initialization process in ROM or RAM. The initialization program contains the following operations.

- Read information from NVM
- Confirm and configure I²C device address according to pin CS2
- Interrupt message is wrote to state register of interrupt
- Enter into Sleep mode

Operation Mode

There are four operation modes in the chip: DeepSleep, Sleep, Active and Doze.

DEEPSLEEP

The chip power consumption is lowest in this mode. OSC, AFE and MCU are inactive, only I²C interface is active.

SLEEP

The chip is in a low power state. AFE and MCU are inactive, OSC is active, waiting for interrupt to wake up.

ACTIVE

The chip works at full speed. All modules including AFE, MCU, OSC, etc., are running normally. When touch or proximity has not been detected for a period of time, it will automatically switch to Doze mode. In this mode, the external Host can send Sleep command to switch the chip into Sleep mode.

DOZE

In this mode, MCU and AFE work intermittently with a longer scan period. During large part of a scan period, most modules are inactive. So the average power consumption is lower.

Once proximity is detected in Doze mode, it will automatically return to Active mode. The external Host can also send Sleep command to switch the chip to Sleep mode.

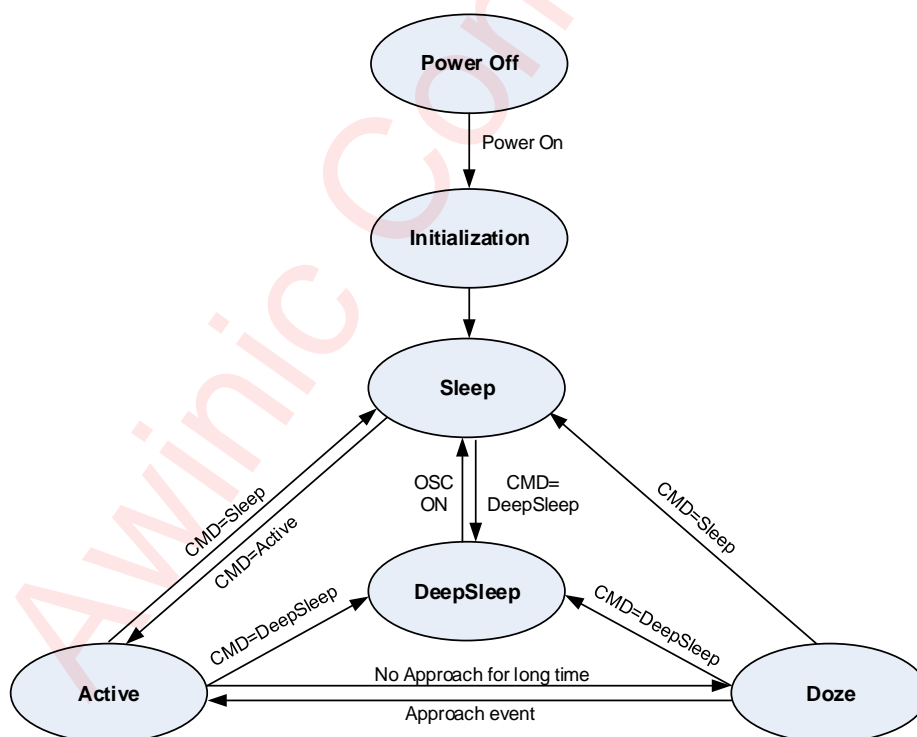


Figure 22 Operation Mode Switching

Interrupt

AW933XX report the interrupt signal to the host through the INTN pin. Register IRQSRC (Address: 0xF080) stores interrupt information, including the completion of parasitic capacitance calibration, scan cycle completion, and so on. Register IRQSRC is cleared after Host read. The specified interrupt signal can be masked by configuring register IRQEN(Address: 0xF084).

The chip of AW93305BFOR, pins CS2 and CS5 can be configured as interrupt pin. The chip reports the interrupt signal to the Host through the interrupt pin (CS2 or CS5). Register IRQSRC (Address: 0xF080) stores interrupt information, including the completion of parasitic capacitance calibration, scan cycle completion, and so on. Register IRQSRC is cleared after Host read. The specified interrupt signal can be masked by configuring register IRQEN(Address: 0xF084).

I²C Interface

AW933XX supports the serial I²C-bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. The I²C interface supports different pull-up voltage values. Additionally, the I²C device supports continuous read and write operations. The I²C register address is 16-bit and register data is 32-bit, and the data transmission is in big-endian mode.

DEVICE ADDRESS

**I²C Device Address Configuration of AW93303FDR/
AW93305DNR/AW93310QNR/AW93312QNR**

CS2 Connection	Device Address
Floating	0x12
GND	0x13
VCC	0x14

I²C Device Address Configuration of AW93307QNR

CS0 Connection	CS3 Connection	Device Address
Floating	Floating	0x12
GND	Floating	0x13
VCC	Floating	0x15
Floating	GND	0x13
GND	GND	0x14
VCC	GND	0x15
Floating	VCC	0x15
GND	VCC	0x15
VCC	VCC	0x15

The I²C device address of AW93303FDR/AW93305DNR/AW93310QNR/AW93312QNR depends on the status of pin CS2. The default value is 0x12. Connecting pin CS2 to GND or VCC will change the device address as showed in table above. Note that when pin CS2 is connected to GND or VCC, it can't be used as sensor pad. The power supply of the pin of CS2 and the chip power need to use the same power supply.

The I²C device address of AW93307QNR depends on the status of pins CS0 and CS3. The default value is 0x12. Connecting pin CS0 or CS3 to GND or VCC will change the device address as showed in table above. Note that when pin CS0 or CS3 is connected to GND or VCC, it can't be used as sensor pad. The power supply of the pin of CS0 or CS3 and the chip power need to use the same power supply.

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

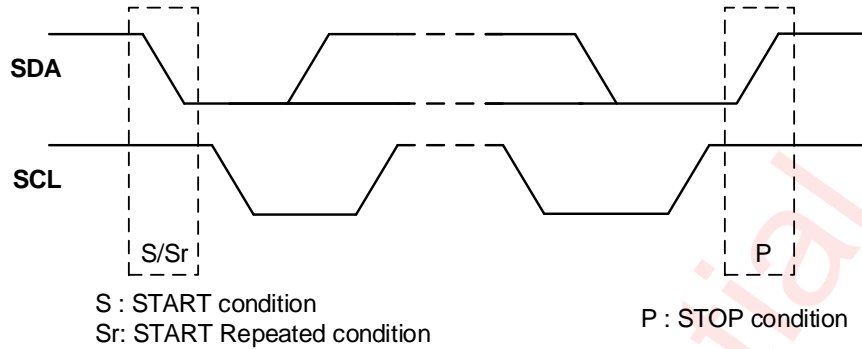


Figure 23 I²C Start/Stop Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

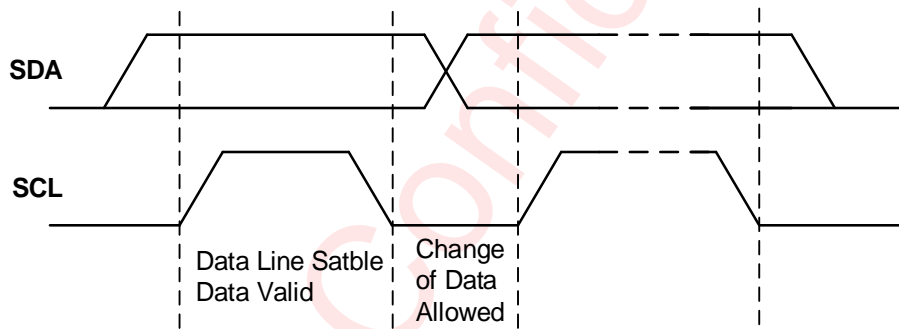


Figure 24 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled down to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

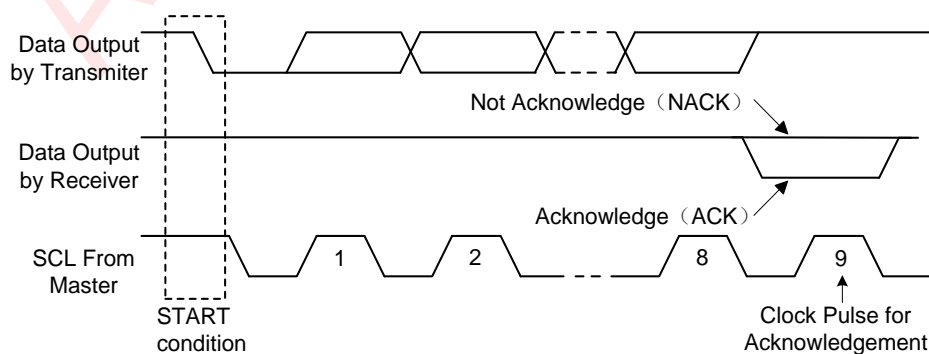


Figure 25 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 16-bit and register data is 32-bit. Writing process of I²C is shown as figure 23.

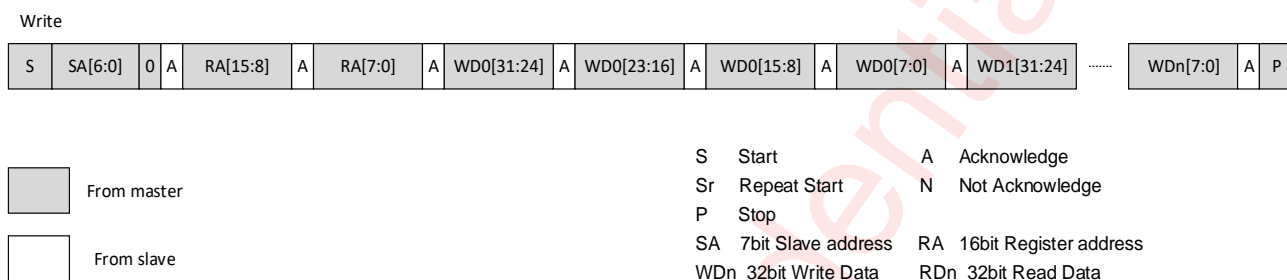


Figure 26 I²C Write Byte Cycle

READ CYCLE

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is shown as figure 24.

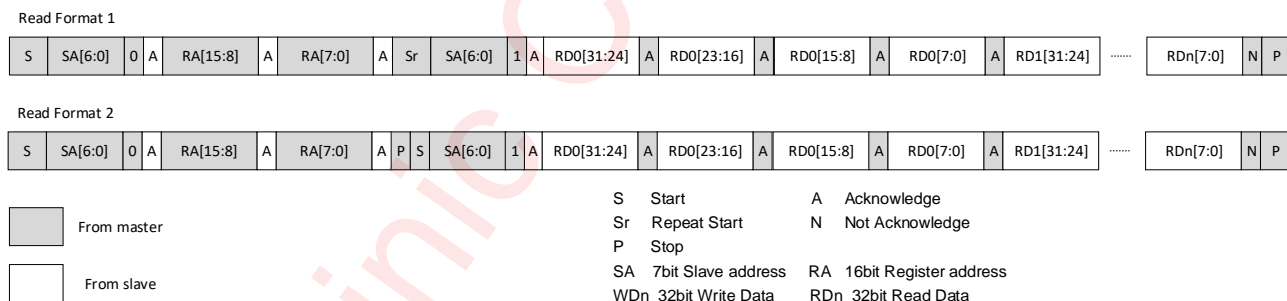


Figure 27 I²C Read Byte Cycle

Gestures

AW933XX can implement several gestures on the button and slider, including **single-click**, **double-click**, **triple-click**, **short-press**, **long-press** and **slide**.

Due to the different number of channels in the AW933XX series, the following table lists the function of each chip.

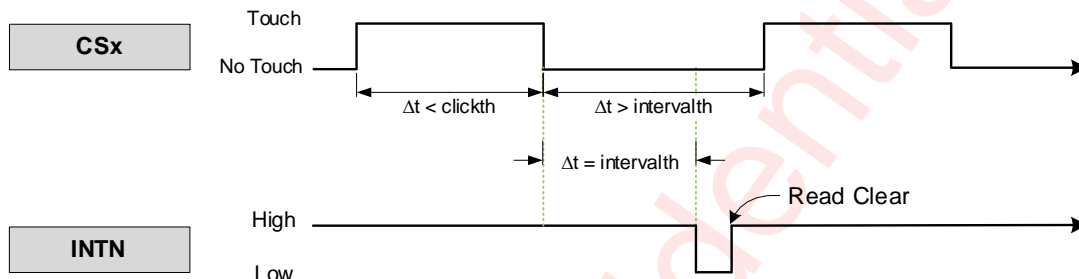
Part Number	Channels	function
AW93303FDR/AW93303BFOR	3	Click, 1D-slide, Wear detection
AW93305DNR/AW93305BFOR	5	Click, 1D-slide, Circle-slide, Wear detection
AW93307QNR	7	Click, 1D-slide, 2D-slide, Circle-slide, Wear

AW93310QNR	10	detection
AW93312QNR	12	

Single-click

Single-click refers to a quick tap event, when a touch is triggered and then released in the same location within a short period of time. The *clickth* and *intervalth* threshold can be adjusted according to practical application requirements. **Single-click** event is based on the following conditions:

- > 1st condition: The time of the touch state must be less than the *clickth*.
- > 2nd condition: The time between two touch states must be more than the *intervalth*.



Notes:

Clickth: the maximum touch time of a valid single-click event

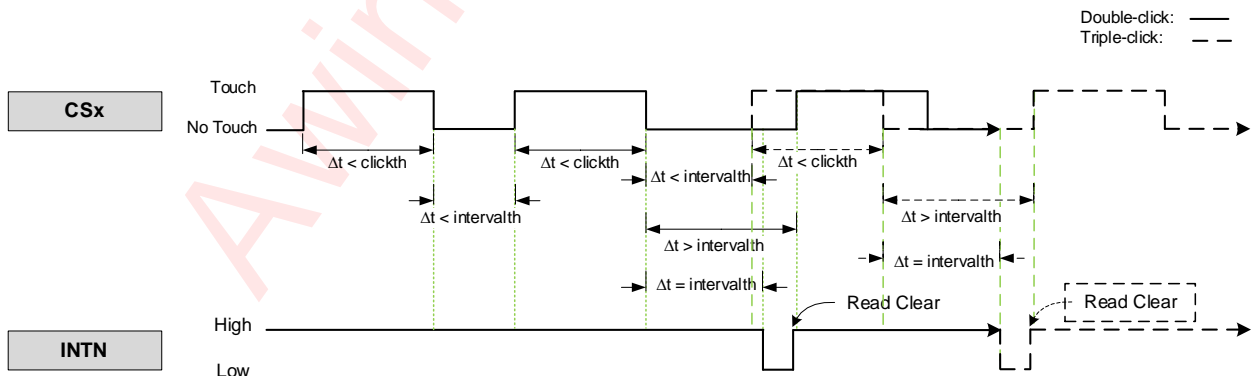
Intervalth: the maximum interval between two valid single-click events

Figure 28 Single-click Sequence Diagram

Double-click and Triple-click

Double-click refers to two quick tap events and **triple-click** refers to three quick tap events. The definition of **triple-click** and **double-click** are different in the number of taps. **Double-click** and **triple-click** events are based on the following conditions:

- > 1st condition: The time of the touch state must be less than the *clickth*.
- > 2nd condition: The time between two adjacent touch states must be less than the *intervalth*.



Notes:

Clickth: the maximum touch time of a valid single-click event

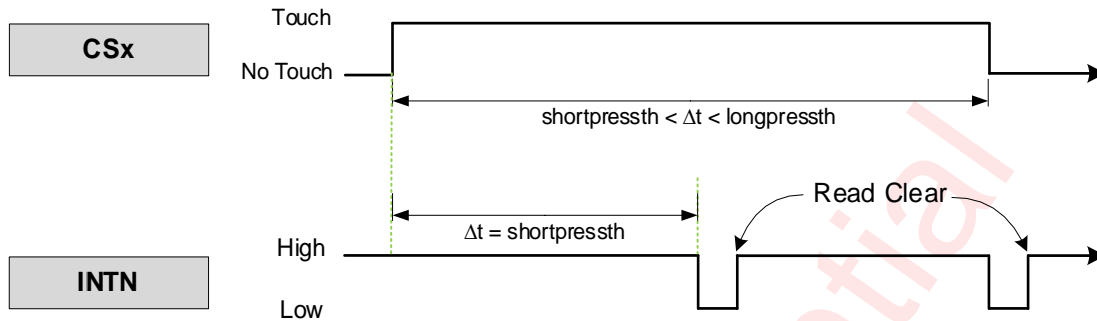
Intervalth: the maximum interval between two valid single-click events

Figure 29 Double-click and Triple-click Sequence Diagram

Short-press

Short-press refers to a short time touch event, **Short-press** gesture is based on the following condition: The time during the touch state must be less than the *longpressth* and more than *shortpressth*.

Short-press will generate two interrupt messages. The first interrupt is reported when the touch time reaches the *shortpressth*. The second interrupt is reported when the touch state is released.



Notes:

Shortpressth: the minimum touch time of a short-press event

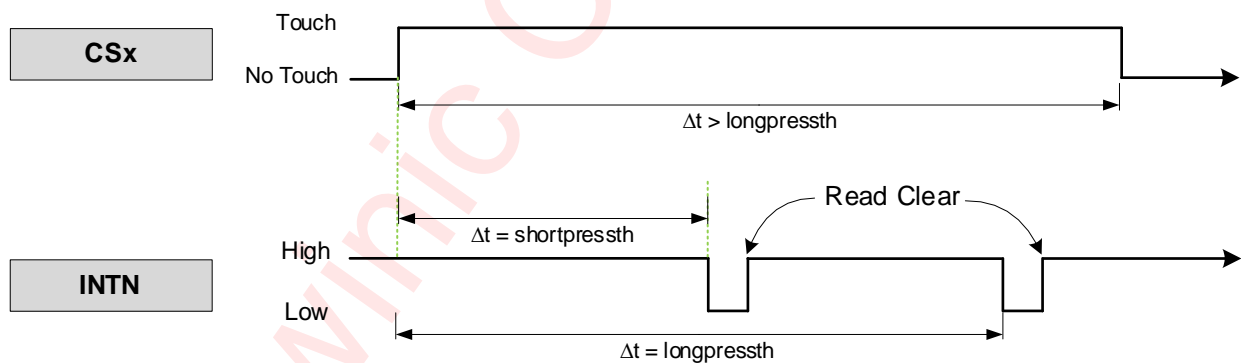
Longpressth: the minimum touch time of a long-press event

Figure 30 Short-press Sequence Diagram

Long-press

Long-press refers to a long time touch event. **Long-press** is based on the following condition: The time during the touch state must be more than the *longpressth*.

Long-press will generate two interrupt messages. The first interrupt is reported when the touch time reaches the *shortpressth*. The second interrupt is reported when the touch time reaches the *longpressth* threshold.



Notes:

Shortpressth: the minimum touch time of a short-press event

Longpressth: the minimum touch time of a long-press event

Figure 31 Long-press Sequence Diagram

Slide

Slide is based on the following condition: The coordinate change during the touch state must be more than the *slideth* (the minimum slip distance of a slide event).

A click (or press) is more difficultly recognized as a **slide** with a higher *slideth*. A **slide** is more difficultly recognized as a click (or press) with a lower *slideth*.

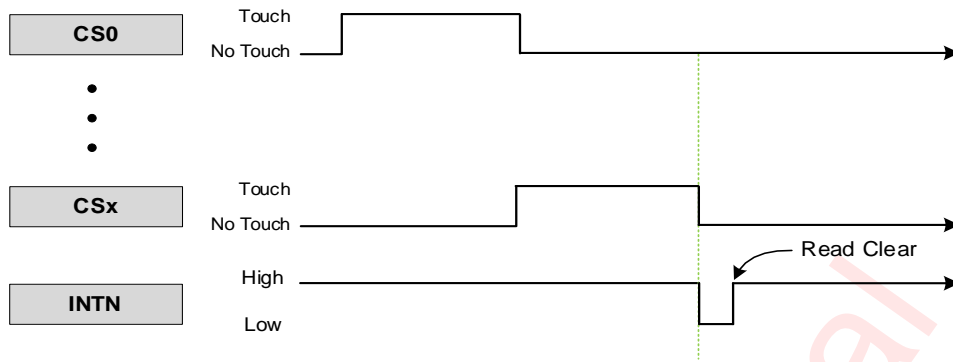


Figure 32 Slide Sequence Diagram

Single sliding definition: The finger touches the slide bar, slide for distance on the slide bar, and the sliding event is reported after the finger leaves.

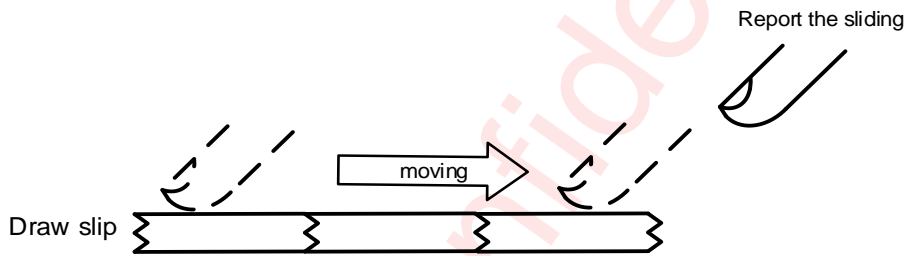


Figure 33 Single Sliding Diagram

Continuous sliding definition: The finger touches the slider without leaving the hand, sliding events will be reported every time the finger slide a certain distance (configurable).

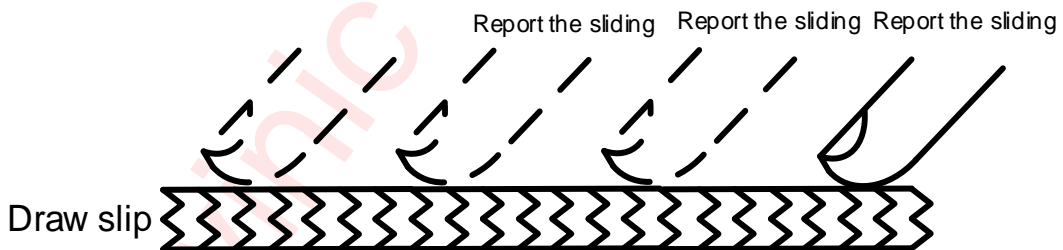


Figure 34 Continuous Sliding Diagram

The parameters of wheel sliders include **SlidePosition**, **MoveDistance**, **MoveDir**, and **CircleDir**. **SlidePosition** means the touch position; **MoveDistance** means the distance between the start position and the end position; **MoveDir** means the relationship between the start position and the end position of the slide; **CircleDir** means the direction of the sliding number of turns, such as counterclockwise or clockwise.

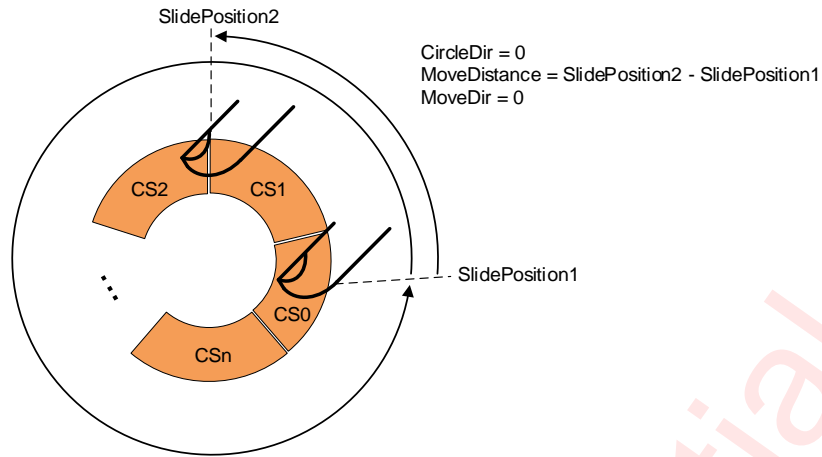


Figure 35 Counterclockwise Diagram

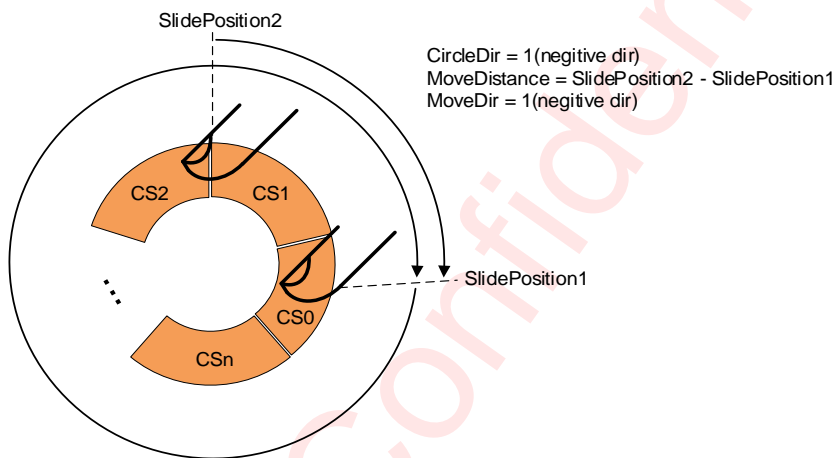


Figure 36 Clockwise Diagram

2D slider can report the event of sliding action in four directions, real time coordinates of sliding, move distance which means the distance between the start position and the end position.

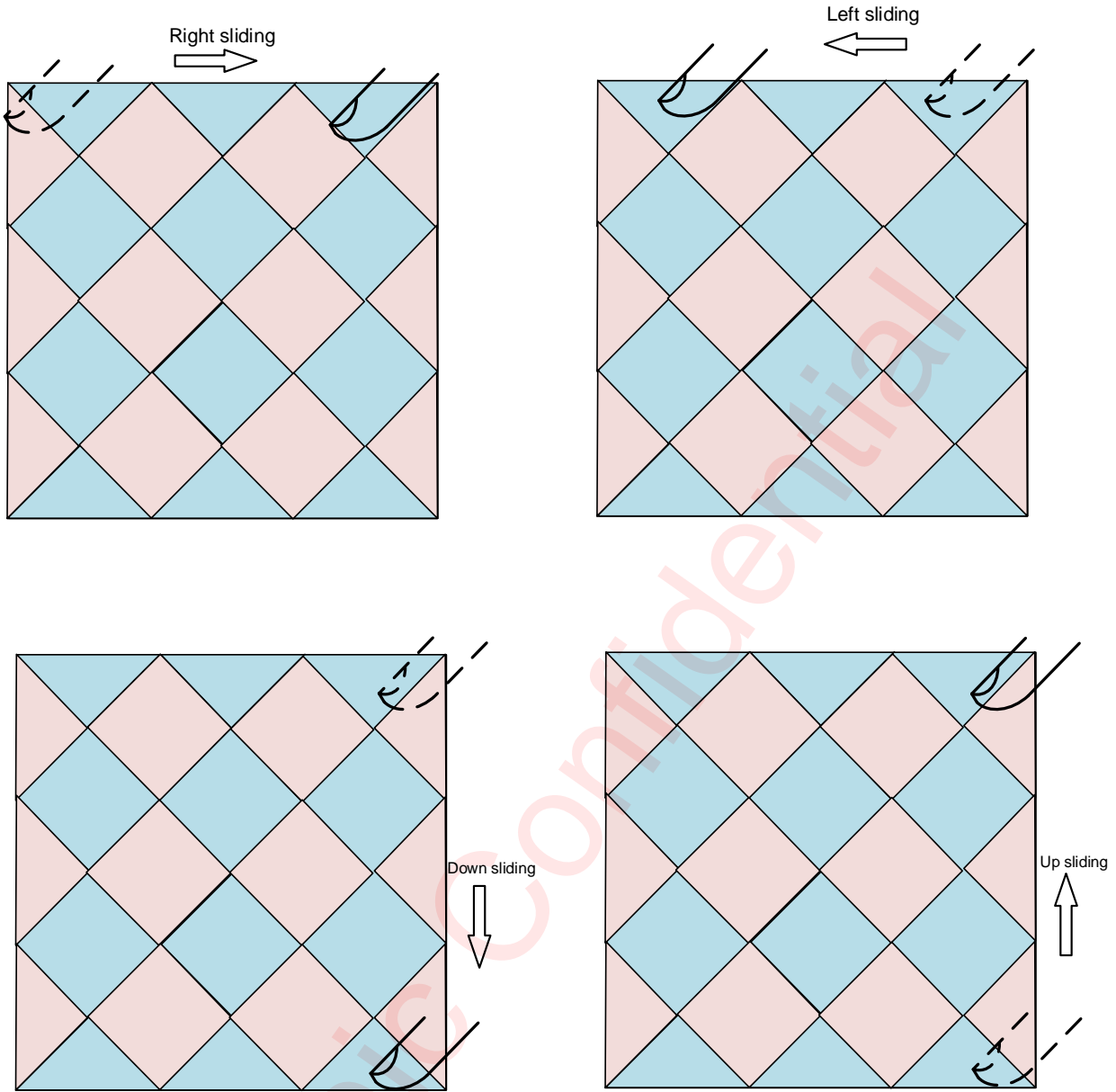


Figure 37 2D Sliding Diagram

Application Information

AW933XX is a multi-channel capacitive touch and proximity sensor. Taking AW93312QNR as an example.

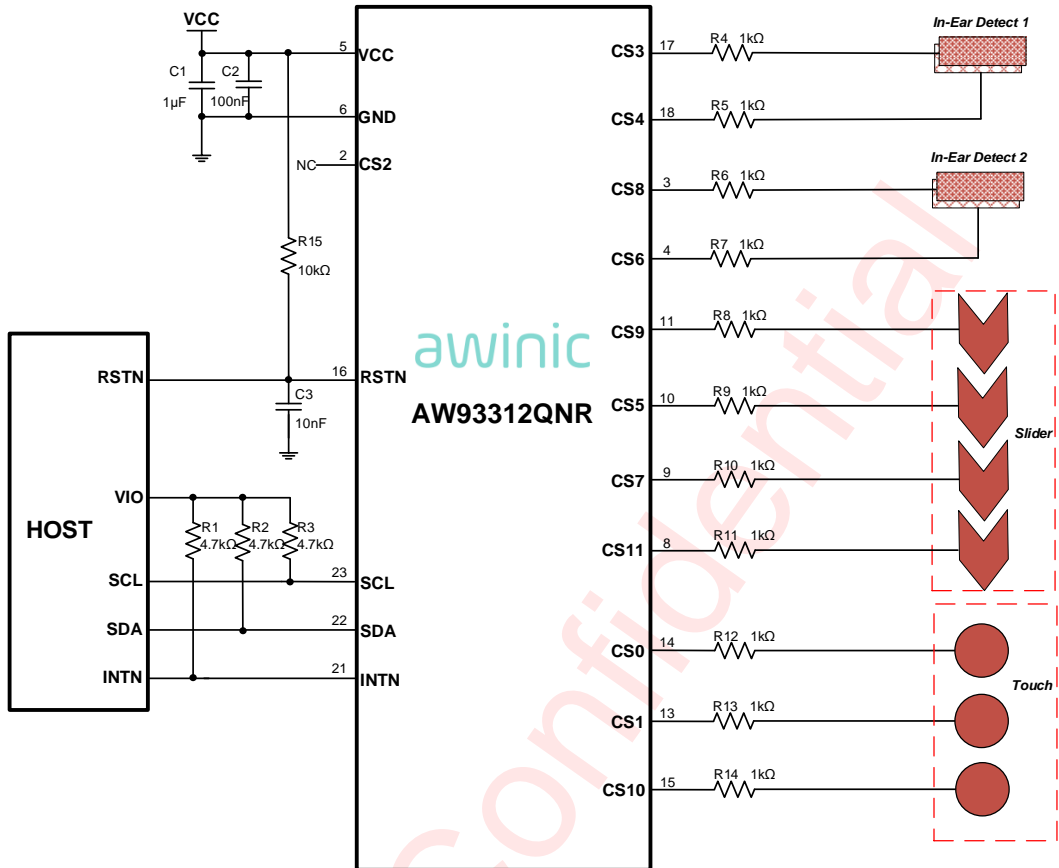


Figure 38 AW93312QNR Typical Application Circuit (wear, touch and 1D slide)

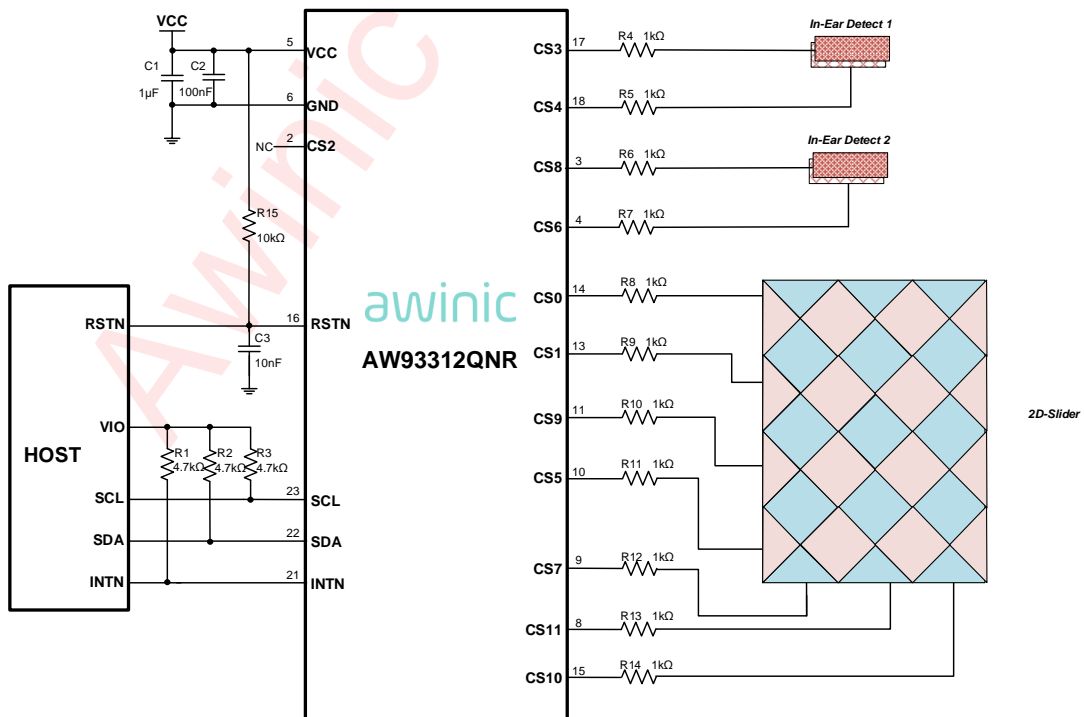


Figure 39 AW93312QNR Typical Application Circuit (wear and 2D slide)

Capacitors Selection

The recommended value of the capacitance C1 is 1 μ F, C2 is 0.1 μ F and C3 is 10nF.

Resistor Selection

The recommended values of the resistor R1~R3, which were applied in pin INTN, SDA and SCL, are 4.7k Ω .

The recommended values of the resistor R4~R14, which were applied in CSx channels, are 1k Ω .

The recommended values of the resistor R15, which is a pull-up resistor applied to RSTN signal, is 10k Ω .

Recommended Components List

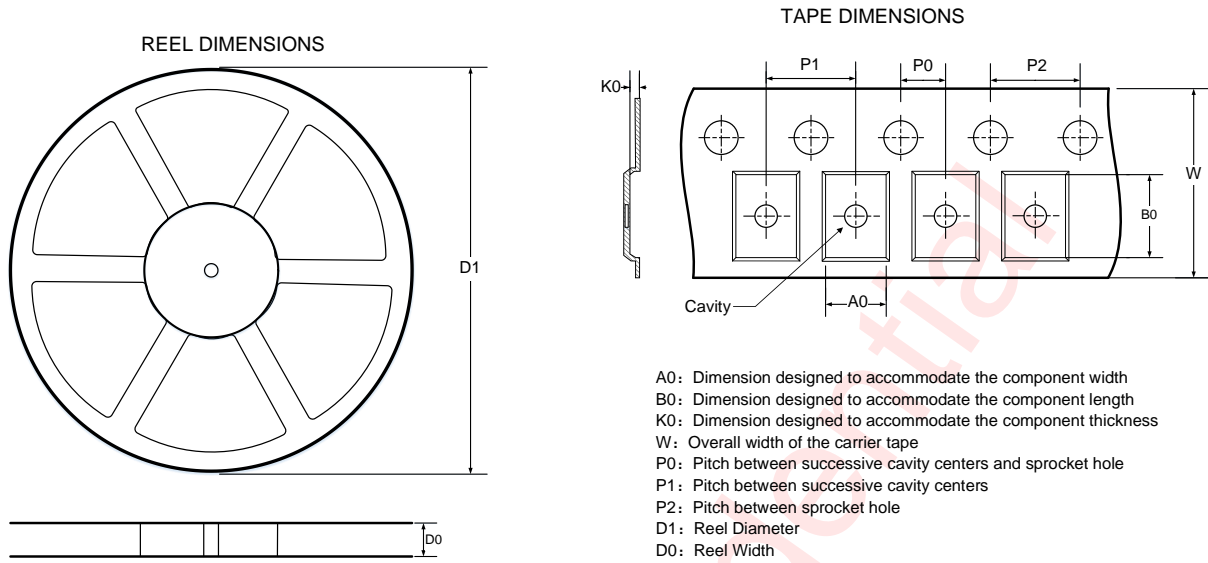
Component	Name	Description	Typ.	Unit
C	C1	-	1	μ F
	C2	-	0.1	μ F
	C3	-	10	nF
R	R1~R3	$\pm 5\%$	4.7	k Ω
	R4~R14	$\pm 5\%$	1	k Ω
	R15	$\pm 5\%$	10	k Ω

PCB Layout Consideration

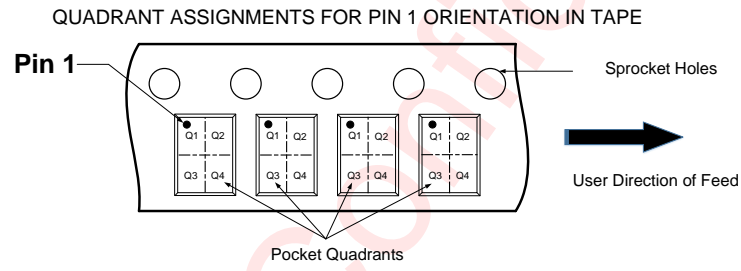
AW933XX is a multi-channel capacitive touch and proximity sensor. To obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All peripheral components should be placed as close to the chip as possible. C1 and C2 should be close to VCC.
2. Place the chip close to capacitive sensor and make trace as short as possible.
3. Make sure the sensor and traces be away from mic, earphone line in case of disturbing audio line.
4. Place differential channel (in Figure 35 and Figure 36, pins CS3, CS4 and CS6, CS8 as shown) along with sensor channel to get better performance.
5. In-ear detection channel and differential channel is recommended to use the differential lines.
6. Use LDO for VCC supply.

Tape And Reel Information



A0: Dimension designed to accommodate the component width
 B0: Dimension designed to accommodate the component length
 K0: Dimension designed to accommodate the component thickness
 W: Overall width of the carrier tape
 P0: Pitch between successive cavity centers and sprocket hole
 P1: Pitch between successive cavity centers
 P2: Pitch between sprocket hole
 D1: Reel Diameter
 D0: Reel Width

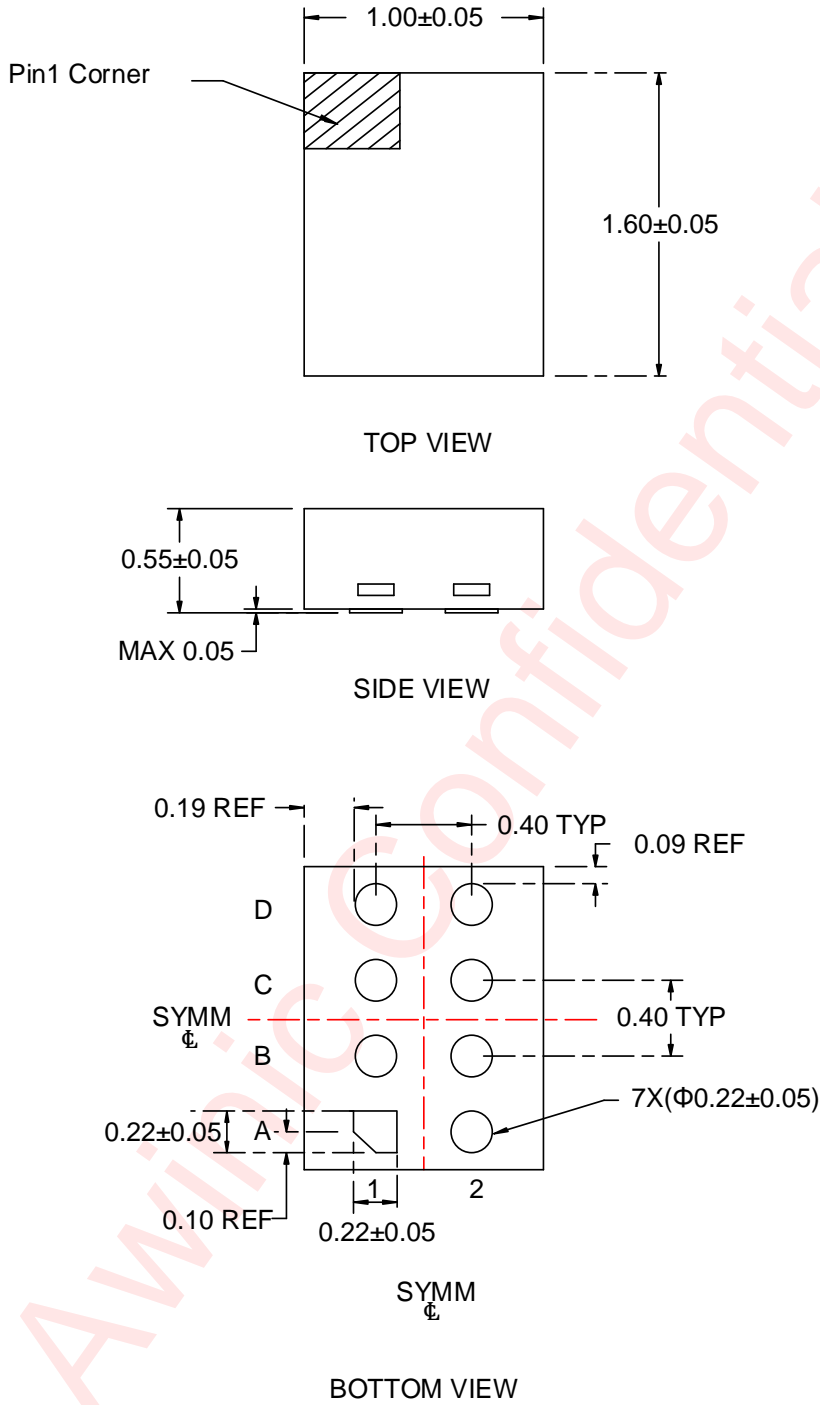


Note: The above picture is for reference only. Please refer to the value in the table below for the actual size DIMENSIONS AND PIN1 ORIENTATION

Device Name	D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
AW93303FDR	178.00	8.40	1.12	1.72	0.70	2.00	4.00	4.00	8.00	Q1
AW93303BFOR	179.00	9.20	1.50	1.26	0.67	2.00	4.00	4.00	8.00	Q1
AW93305DNR	178.00	8.40	2.00	2.30	0.75	2.00	4.00	4.00	8.00	Q1
AW93305BFOR	179.00	9.20	1.50	1.26	0.67	2.00	4.00	4.00	8.00	Q1
AW93307QNR	178.00	8.40	2.00	2.30	0.75	2.00	4.00	4.00	8.00	Q1
AW93310QNR	178.00	8.40	2.25	2.25	0.75	2.00	4.00	4.00	8.00	Q1
AW93312QNR	330.00	12.40	3.25	3.25	0.75	2.00	8.00	4.00	12.00	Q1

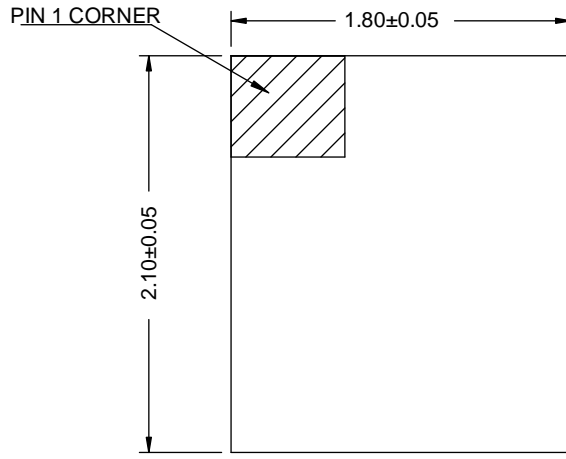
All dimensions are nominal

Package Description

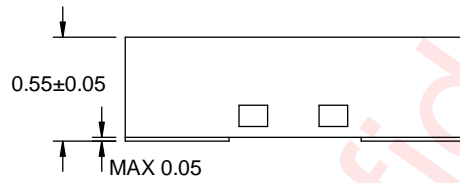


Unit:mm

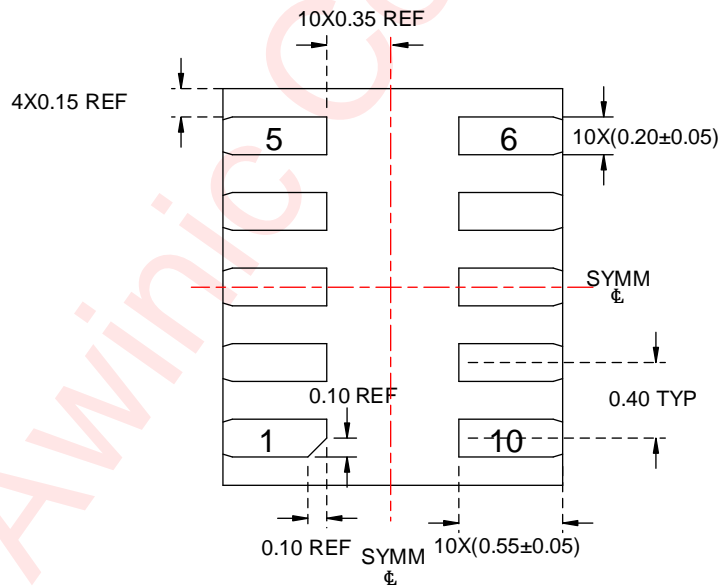
AW93303FDR Package Description



TOP VIEW



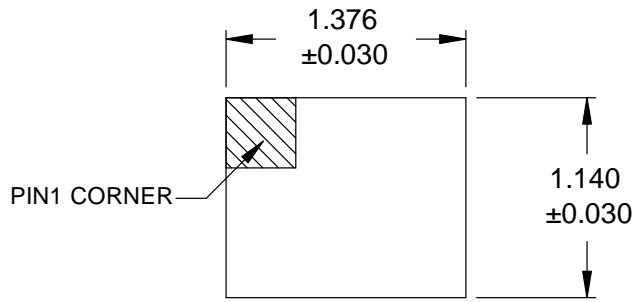
SIDE VIEW



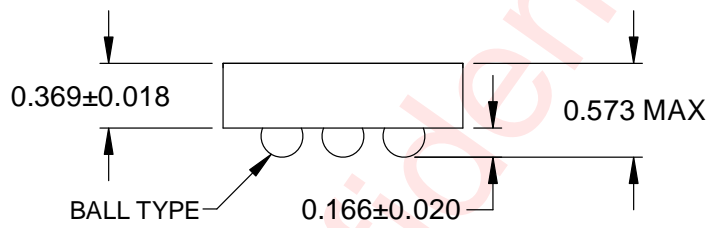
BOTTOM VIEW

Unit: mm

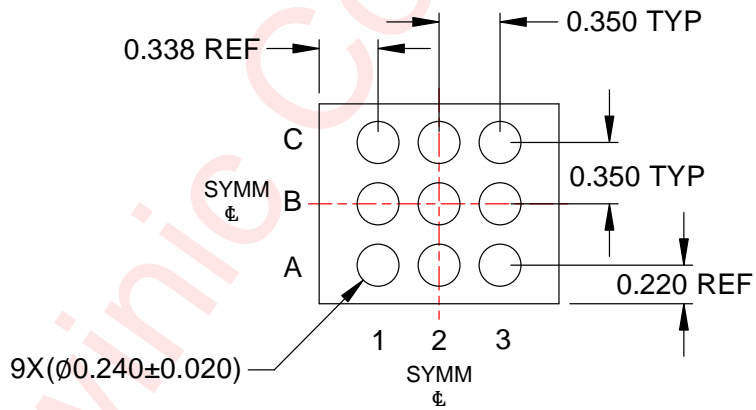
AW93305DNR Package Description



Top View



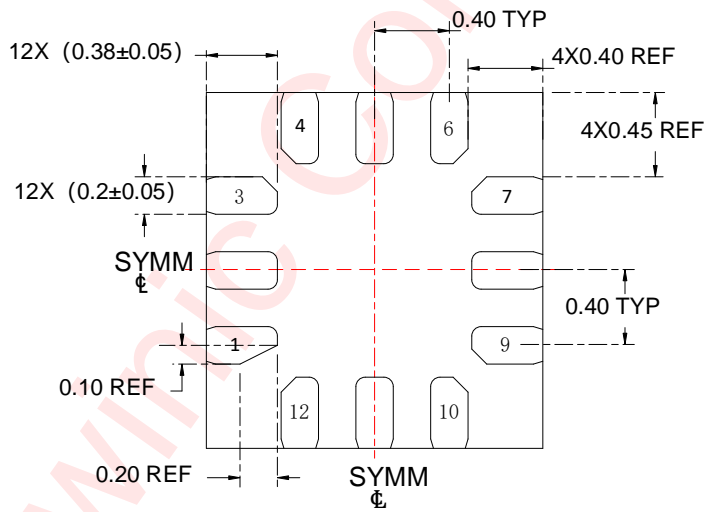
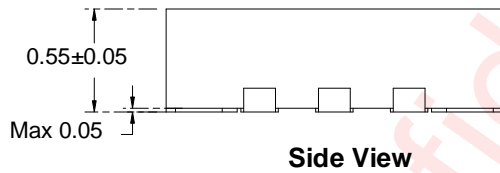
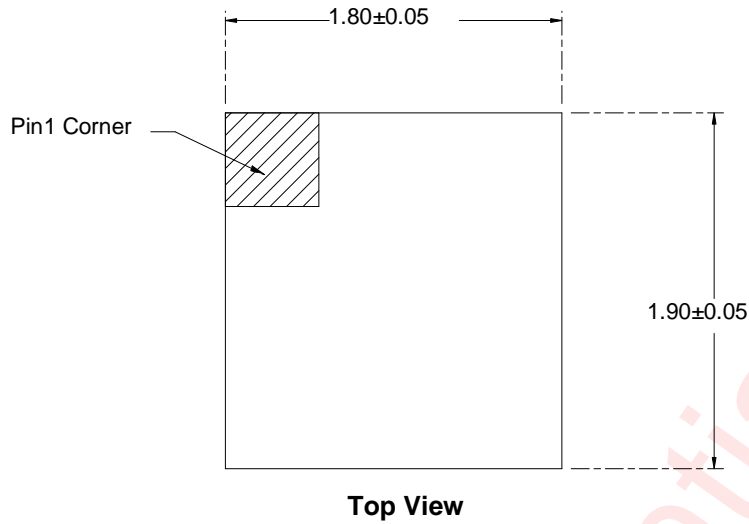
Side View



Bottom View

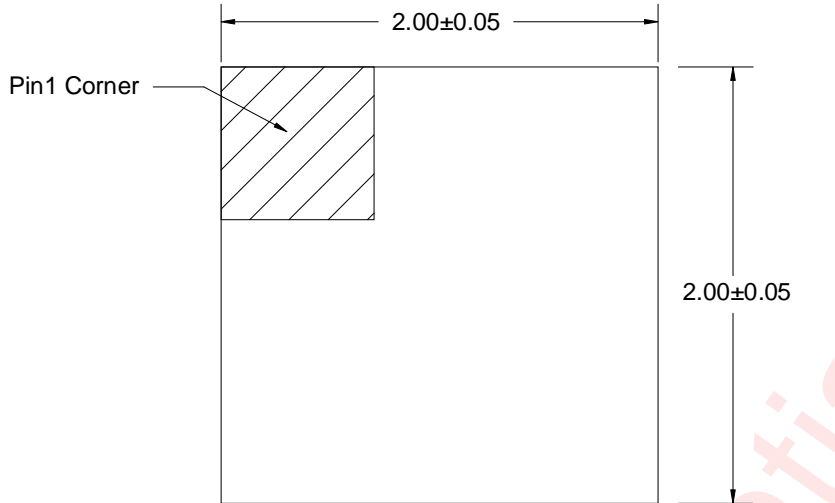
Unit:mm

AW93303BFOR/AW93305BFOR Package Description

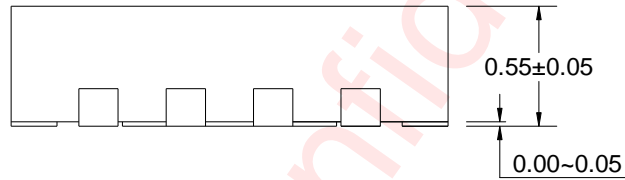


Unit:mm

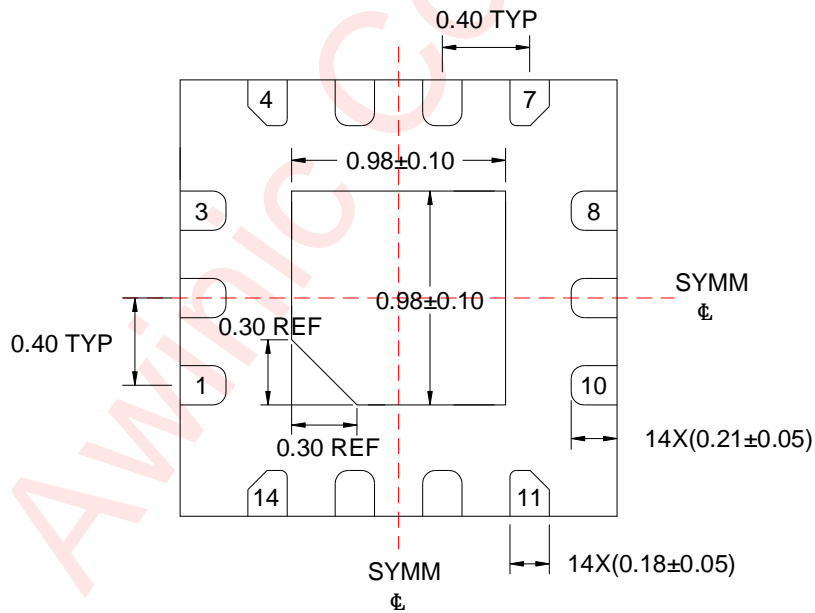
AW93307QNR Package Description



TOP VIEW



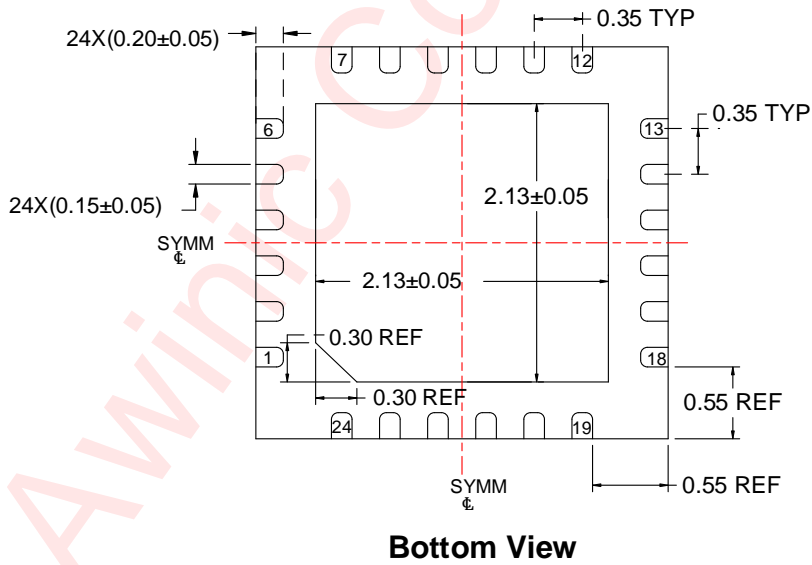
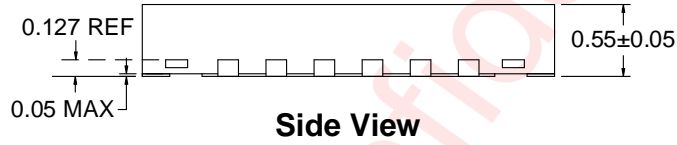
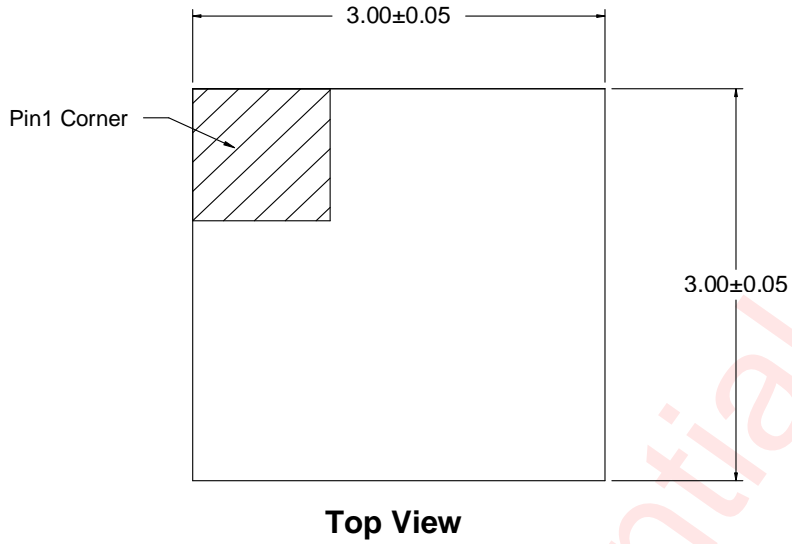
SIDE VIEW



BOTTOM VIEW

Unit: mm

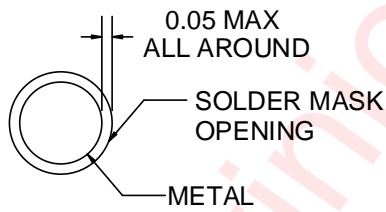
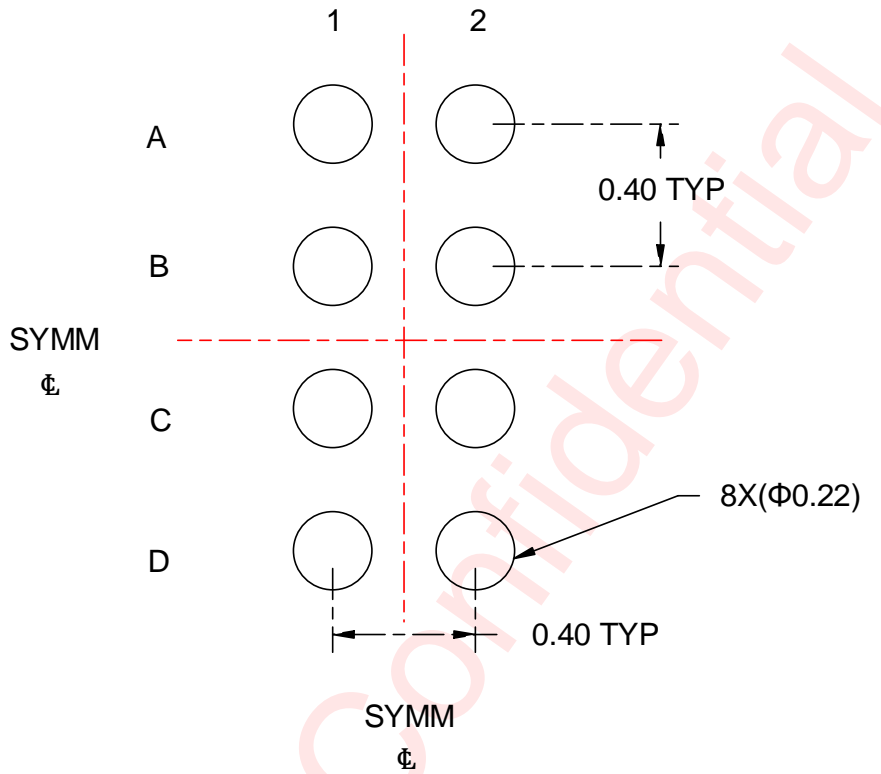
AW93310QNR Package Description



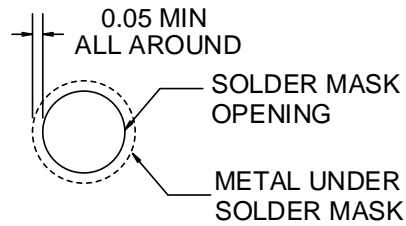
Unit:mm

AW93312QNR Package Description

Land Pattern Data



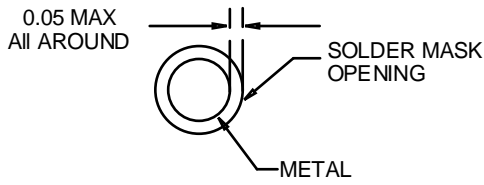
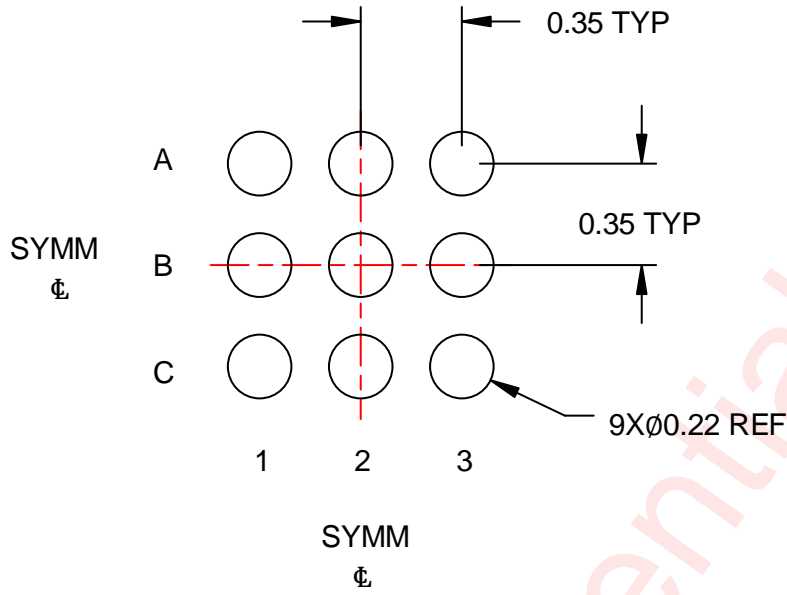
NON SOLDER MASK DEFINED



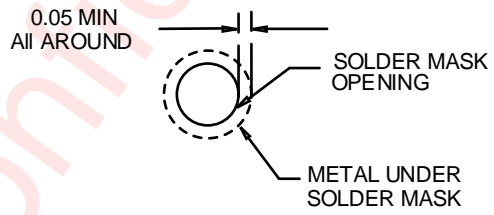
SOLDER MASK DEFINED

Unit: mm

AW93303FDR Land Pattern Data



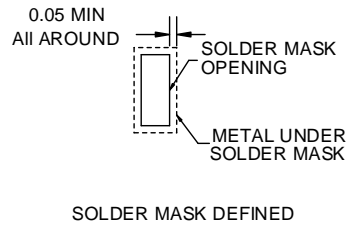
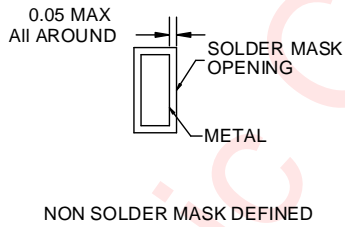
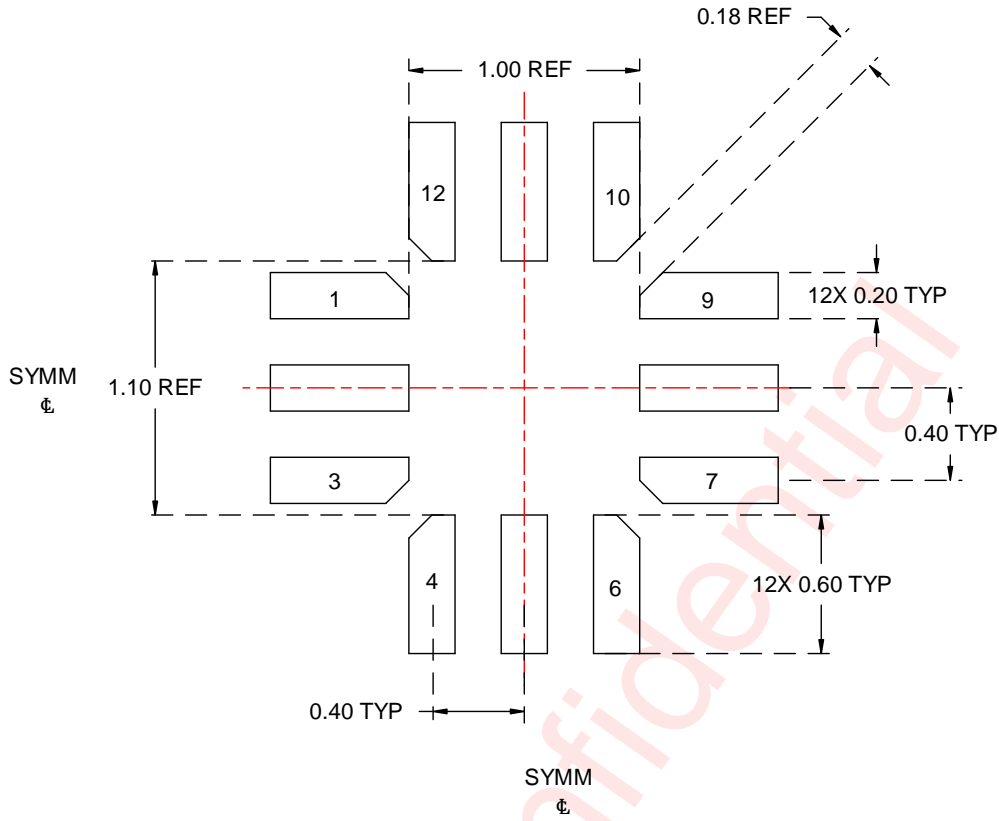
NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

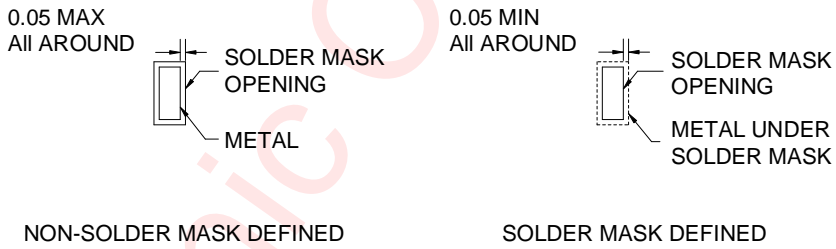
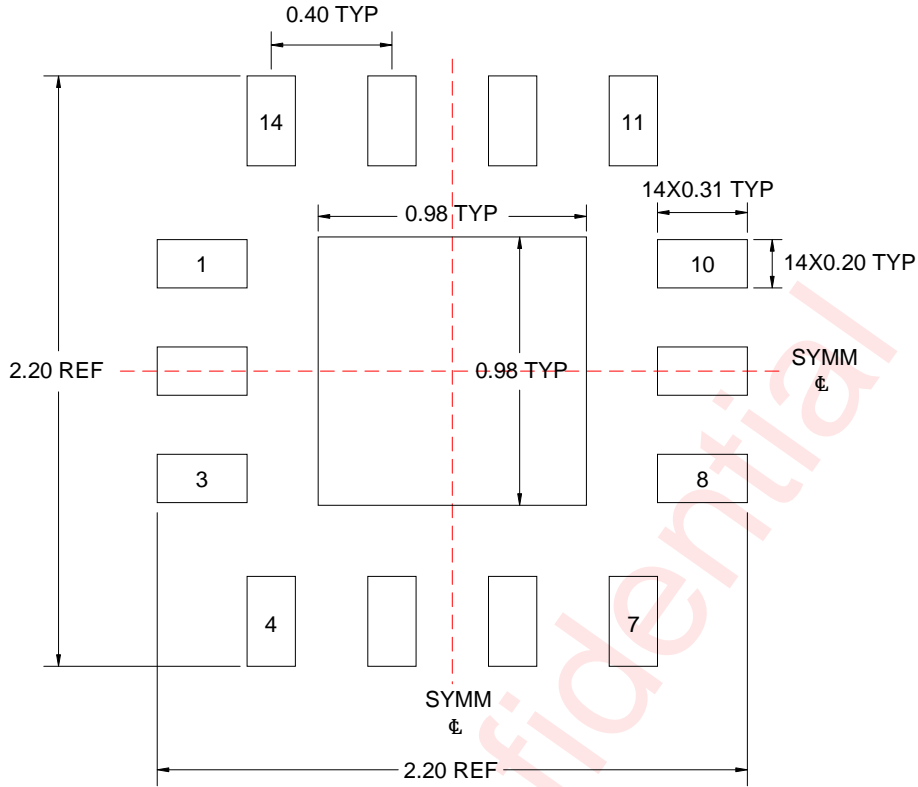
Unit: mm

AW93303BFOR/AW93305BFOR Land Pattern Data



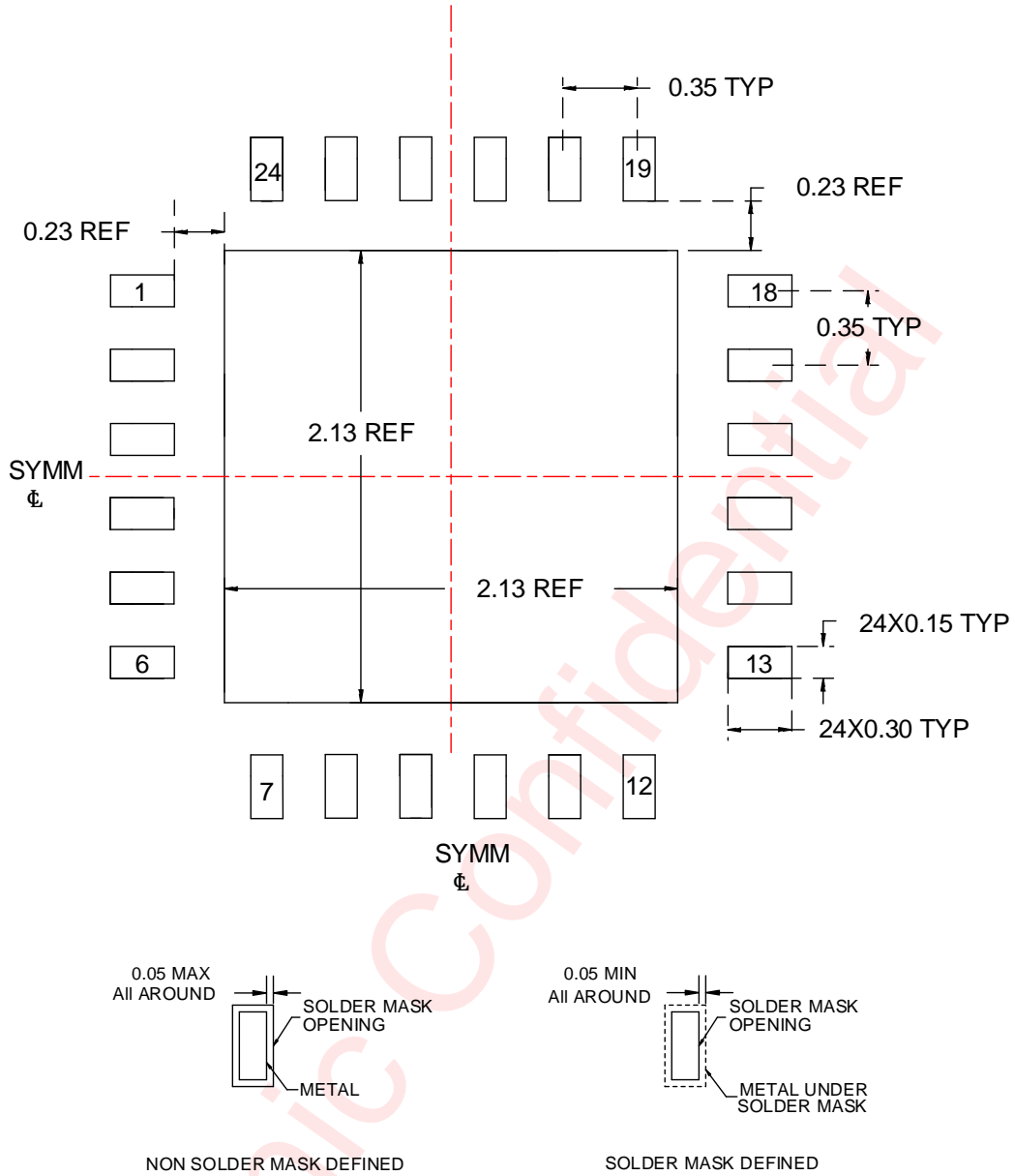
Unit: mm

AW93307QNR Land Pattern Data



Unit: mm

AW93310QNR Land Pattern Data



Unit: mm

AW93312QNR Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Jan 2022	Officially released.
V1.1	Nov 2022	Update the Pull-up voltage in Recommended Operating Conditions. (P6) Update Land Pattern Data. (P29)
V1.2	Apr 2023	Update Capacitance offset.(P1 and P7) Update power consumption.(P1 and P7) Updated ESD performance parameters. (P6)
V1.3	Jul 2023	Update the description of the features.(P1) Update the typical application circuit.(P2 and P22) Update the Figure 20.(P17)
V1.4	Jan 2024	Update the description of features (P1). Changed VCC min from 1.7V to 1.65V (P1, P3 and P5). Update the input voltage range in the table of Absolute Maximum Ratings (P5). Update the typical value of active mode current (P1, P6). Add the maximum value of chip currents (P6). Update the test condition of doze mode current and active mode current (P6). Update the figure of Power On Timing and the description (P12). Update the description of wheel sliders (P27).
V1.5	Jul. 2024	Update the figure of Power On Timing and the description(P12).
V1.6	Aug. 2024	Update the typical application circuit.(P2 and P22)
V1.7	Mar. 2025	gather together for AW93303FDR, AW93305DNR, AW93307QNR, AW93310QNR and AW93312QNR; Update the functional block diagram; Update the Electrical Characteristics; Add the V _{OL} (SDA/INTN)
V1.8	May. 2025	Add AW93303BFOR/AW93305BFOR

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