

2.9-16V Input, 15A Output, Step Down DC/DC Converter

General Description

The XPM6615 operates over a wide input voltage range from 2.9V to 16V which is suitable for 12V input voltage application. And it is capable of delivering 15A output current over a wide ambient temperature range. The efficiency is pretty high because it integrates high quality main switch, synchronous switch and inductor inside to minimize the conduction loss. It provides accurate regulation for a variety of loads over all operation temperature range.

The XPM6615 adopts the COT architecture to achieve fast transient responses for high step down applications. The device is also equipped with cycle-by-cycle current limit, hiccup over current protection and thermal shutdown protection.

Features

- Wide Input Voltage Range:
 - 2.9V to 3.6V if VCC is Connected to VIN (RC filter is needed from VIN to VCC)
 - 2.9V to 16V if VCC is Supplied by External Source
 - 4.5V to 16V if VCC is Supplied by Internal LDO
- Capable of 15A constant output current.
- High Reference Voltage Accuracy Over Temperature Range (T_J : -40°C to 125°C).
- Pseudo 600kHz, 800kHz and 1000kHz Switching Frequency Selection.
- Reliable Protection Mode:
 - Auto-retry Mode for input UVLO, output UVP and OTP.
 - Cycle-by-cycle Valley and Peak Current Limit (OCP)
- Start-Up with Pre-biased Voltage.
- Adjustable Input Voltage UVLO by EN Pin.
- Adjustable Soft-start Time Limits the Inrush Current.
- Remote Sensing at Point of Load Side.
- Power good indicator.
- Compact Package: MQFN5×5-32 (Height=2.8mm max)

Applications

- Telecom and Networking Systems
- Servers
- POLs

Typical Applications

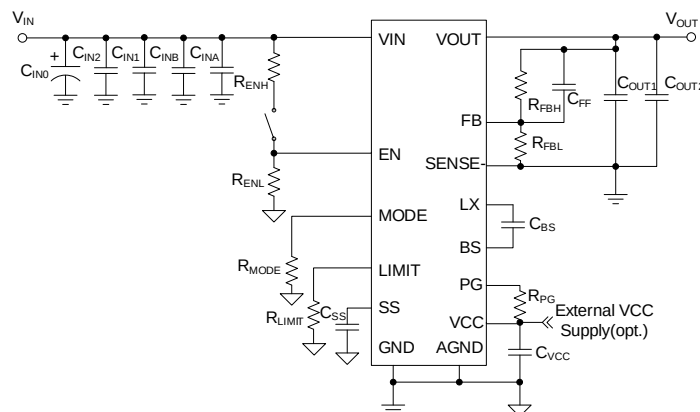
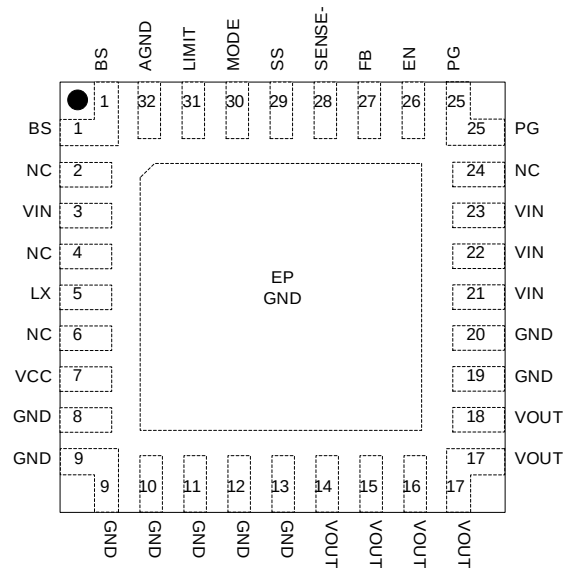


Figure 1. Schematic Diagram

Pinout (top view)



(MQFN5×5-32)

Pin Number	Pin Name	Pin Description
1	BS	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
3,21-23	VIN	Input Pins. Besides at least 20μF ceramic capacitors, two additional 0.1μF capacitors with small package (such as 0402 or 0603) are recommended strongly to be placed between VIN and GND pins. Refer to layout suggestion for details.
5	LX	Switching pins.
7	VCC	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with at least 1μF ceramic capacitor.
8-13, 19-20,EP	GND	Ground Pins.
14-18	VOUT	Output Pins.
25	PG	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of regulation point.
26	EN	Enable control. Pull this pin high to turn on the IC. Can be used to set the on and off threshold (adjust UVLO) with two additional resistors. Do not leave this pin floating.
27	FB	Output Feedback Pin. Connect this pin (as shown in Figure 1) to program the output voltage.
28	SENSE-	Negative output voltage sensing pin. It can be connected to the load negative terminal to compensate power line voltage drop. If this function is not needed, connect this pin to the closest GND pin.
29	SS	Soft-start programming pin. Connect a capacitor from this pin to AGND to program the soft-start time. Leave this pin open for default 0.9ms (from 10% to 90% of $V_{out,setpoint}$) soft-start time.

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30	MODE	Operation mode selection pin. Connect a resistor to AGND to set the switching frequency and mode. Program this pin to select FCCM or PFM mode, and the switching frequency.
31	LIMIT	Bottom MOSFET current limit set pin. Connect a resistor to AGND to set the inductor valley current limit value.
32	AGND	Analog ground pins. AGND needs to be connected to GND directly.

Layout Suggestion

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN} , C_{OUT} , C_{VCC} .

- 1) C_{IN} must be close to each VIN pins and GND. The loop area formed by C_{IN} and GND must be minimized. Despite at least 20 μ F ceramic capacitors (such as 0603 package, C_{IN1} and C_{IN2} shown in Fig. 3 and 4), additional 0.1 μ F capacitors with small package (such as 0402 or 0603, C_{INA} and C_{INB} shown in Fig.3 and 4) are recommended strongly to be placed as close as possible to VIN pin4 and VIN pin22 separately, and all C_{IN} GND terminals are connected by a dedicated GND plane.
- 2) C_{OUT} must be close to the VOUT pins and GND. The loop area formed by C_{OUT} and GND must be minimized.
- 3) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. A ground plane is highly desirable.
- 4) The FB trace should be kept as short as possible.

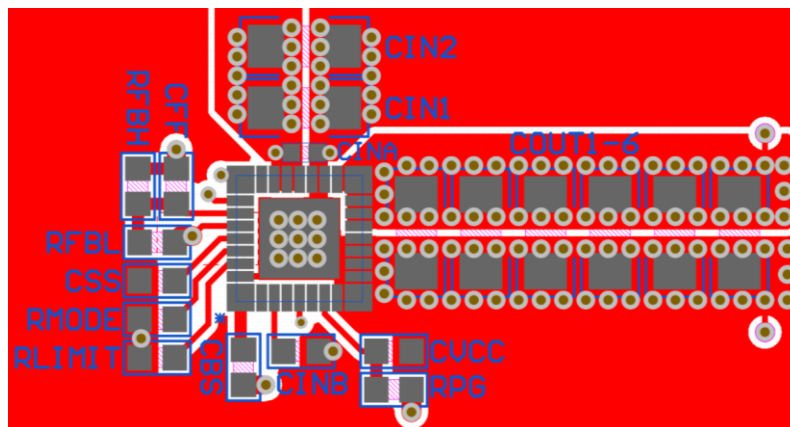
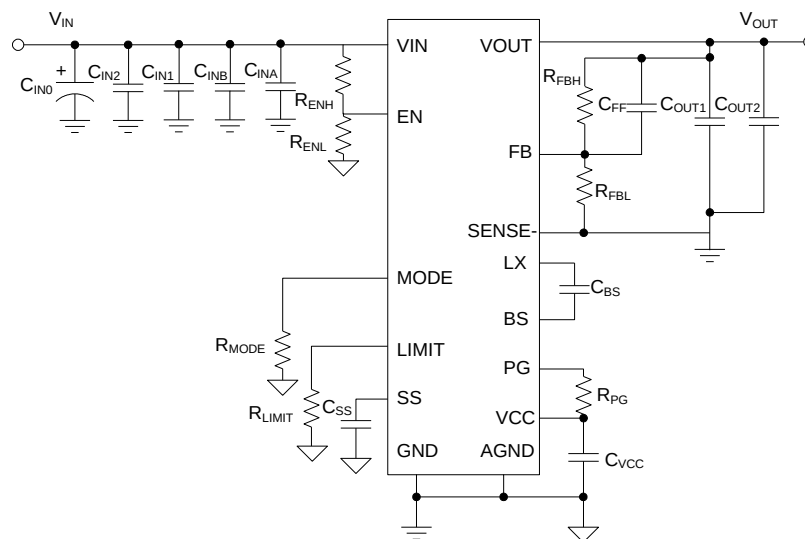
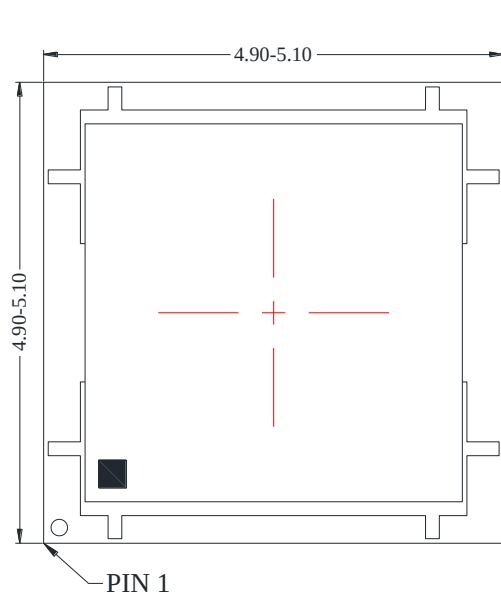


Figure 6. PCB Layout Suggestion

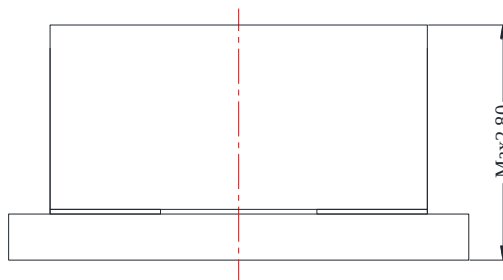
BOM List

Reference Designator	Description	Part Number	Manufacturer
C _{IN0}	100μF/25V Electrolytic Cap		
C _{INA}	100nF, 50V, 0402	GRM155R71H104KE14D	Murata
C _{INB}	100nF, 50V, 0603	GCM188L81H104KA57D	Murata
C _{IN1} , C _{IN2}	10μF, 25V, 1206	GRM31CR71E106KA12L	Murata
C _{OUT1} , C _{OUT2}	22μF, 16V, 1206	GRM31CC71C226ME11L	Murata
C _{VCC}	1μF, 6.3V, 0603	GGM188R71C105MA64#	Murata
C _{BS} , C _{SS}	100nF, 50V, 0603	GCM188L81H104KA57D	Murata
C _{FF}	3.3nF, 6.3V, 0603	GCH188R71H332KE01#	Murata
R _{PG} , R _{ENL}	100kΩ, 0603		
R _{ENH}	10kΩ, 0603		
R _{MODE}	0Ω, 0603(fs=600kHz)		
	30kΩ, 0603(fs=800kHz)		
	60kΩ, 0603(fs=1MHz)		
R _{LIMIT}	7.2kΩ, 0603 (for V _{OUT} =3.3V)		
R _{FBH}	2kΩ, 0603		
R _{FBL}	Not placed(V _{OUT} =0.6V)		
	3kΩ, 0603(V _{OUT} =1V)		
	2kΩ, 0603(V _{OUT} =1.2V)		
	1kΩ, 0603(V _{OUT} =1.8V)		
	442Ω, 0603(V _{OUT} =3.3V)		
	270Ω, 0603(V _{OUT} =5V)		

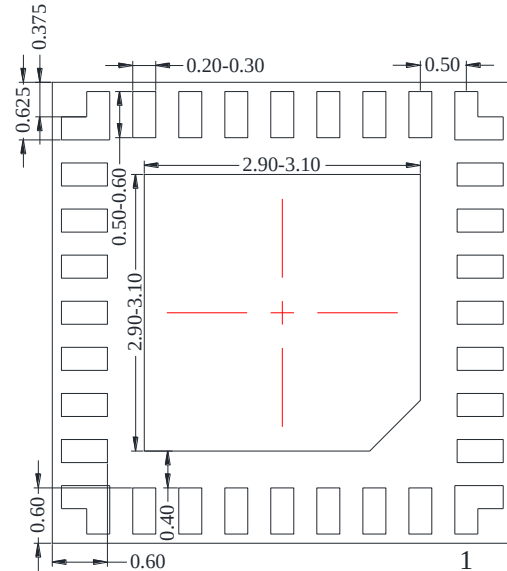
MQFN5X5-32 Package Outline Drawing



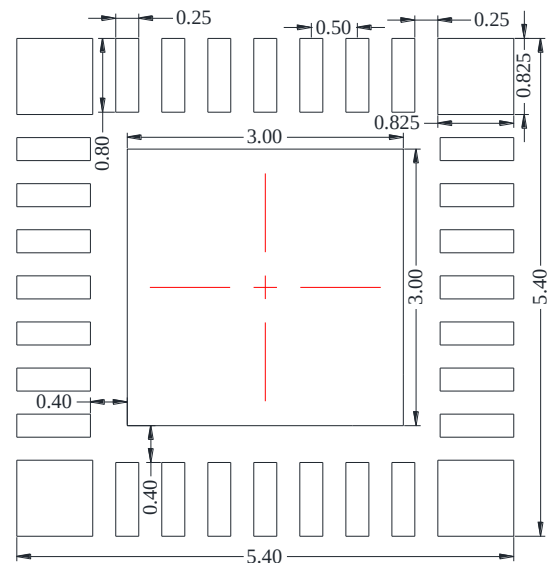
Top View



Front View



Bottom View



Recommended PCB layout
(Reference only)

Notes: 1.All dimension in millimeter and exclude mold flash & metal burr.
2.Center line on drawing refers to the chip body center.