10W, 4.5V to 18V, High efficiency Class D Audio Amplifier with Low Idle Power Dissipation and I²C Diagnostics

Features

- Qualified for Automotive Applications
- AEC-Q100 qualified for automotive applications
  Temperature grade 1: –40°C to +125°C, TA
- Meet CISPR25-L5 EMC specification
- Mono BTL Class-D Power Amplifier
- Wide Voltage Range: 4.5V – 18V
- PWM 400KHz/500KHz switching PWM
- Output Power
  1X10W@4Ω，14.4V，THD+N＜1%
- Overall efficiency up to 83%
- Supports 2-16Ω Speaker
- 15mA Idle Current in Low-Loss Mode
- Support 1. 8V&3.3V&5V I²C-bus control interface
- Thermal Foldback
- 45V Load–Dump Protection per ISO-7637-2
- Integrated self-protection：
  - Over-voltage and Under-voltage protection
  - Over-temperature protection
  - DC-detect protection
  - Short-circuit protection
- Load Diagnostic Functions：
  - Output to Power
  - Output to GND
  - Shorted Output Load
  - Open Output Load
- ETSSOP-16L package

Applications

- Automotive Emergency Call (eCall) Amplifier
- Telematics Systems
- Instrument Cluster Systems

General Description

The AW83611TSR-Q1 is a Class D mono-channel high-efficiency audio power amplifier with I²C control that delivers up to 10W of power at 14.4V power with 4Ω load. In Low-Loss mode, it consumes a low idle current, allowing for longer audio play and improved speaker performance.

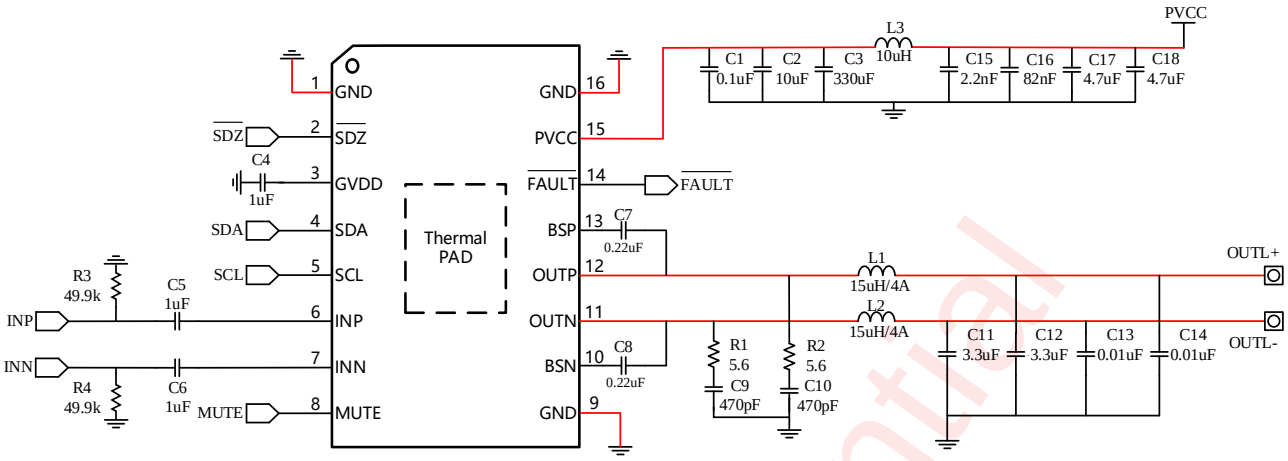
AW83611TSR-Q1 improves the heat dissipation capacity of the package to ensure that the chip can work normally at high temperature.

The AW83611TSR-Q1 features the EEE (Enhanced Emission Elimination) function which greatly reduces EMI over the full bandwidth.

The AW83611TSR-Q1 built-in over-voltage, under-voltage protection, DC protection, thermal protection, short-circuit protection and load dump protection, effectively prevent it from being damaged. With load diagnosis function, the speaker status can be reported through the I²C.

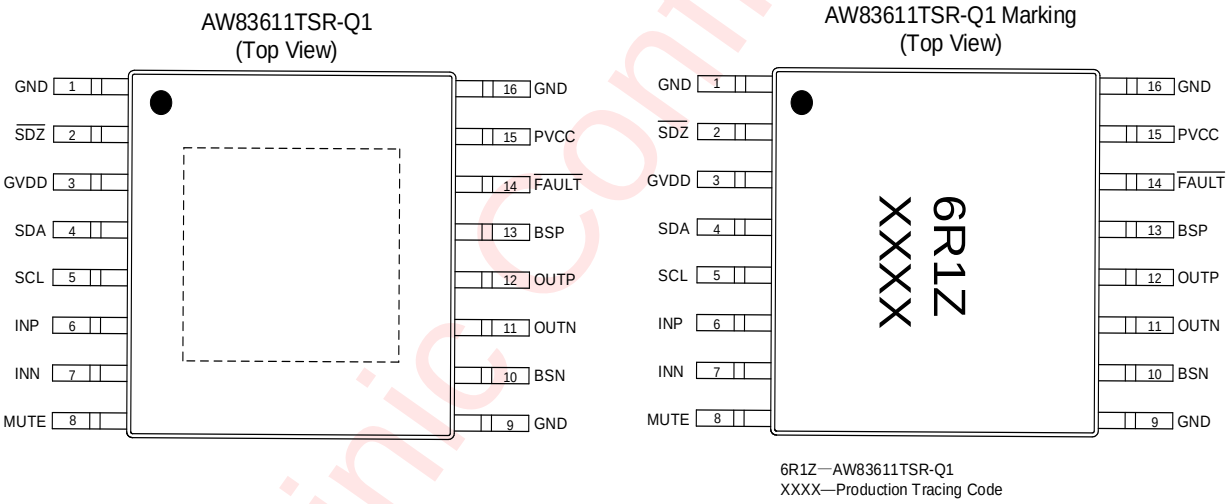
AW83611TSR-Q1 is available in ETSSOP-16L package.

Typical Application Circuit



Note: Traces carry high current are marked in red in the above figure

Pin Configuration And Top Mark



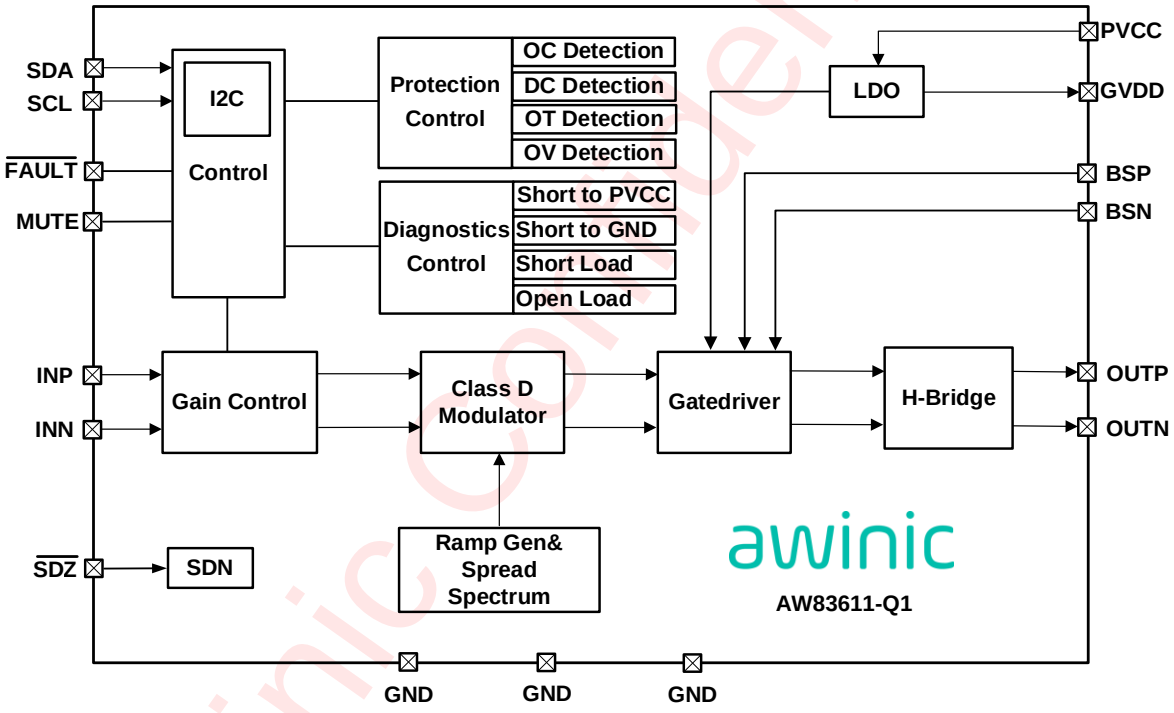
6R1Z—AW83611TSR-Q1
XXXX—Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
1	GND	Ground
2	$\overline{SDZ}$	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to PVCC.
3	GVDD	Internally generated FET gate drive supply.
4	SDA	I^2C data
5	SCL	I^2C clock
6	INP	Positive audio input
7	INN	Negative audio input
8	MUTE	Mute input
9	GND	Ground

10	BSN	Bootstrap supply for negative-output high-side FET.
11	OUTN	Negative output
12	OUTP	Positive output
13	BSP	Bootstrap supply for positive-output high-side FET.
14	$\overline{\text{FAULT}}$	Open drain output used to display short circuit or dc detect fault status. $\overline{\text{FAULT}}$ = High, normal operation, $\overline{\text{FAULT}}$ = LOW, fault condition.
15	PVCC	Power supply
16	GND	Ground

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW83611TSR-Q1	-40℃～125℃	ETSSOP-16L	6R1Z	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range PVCC		-0.3V~30V
Input voltage range	INP，INN，MUTE	-0.3V to 6.5V
	SCL，SDA，$\overline{SDZ}$	-0.3V to 5V
Output voltage range	OUTN，OUTP	-0.3V to PVCC
	$\overline{FAULT}$	-0.3V to 5V
	BSN，BSP(Relative to GND)	-0.3V to 36.3V
	BSN，BSP(Relative to GVDD)	-0.3V~30V
	GVDD	-0.3V~7V
Junction-to-ambient thermal resistance θ_{JA}		26.87°C /W
Junction-to-board characterization parameter θ_{JB}		19.08°C /W
Junction-to-top characterization parameter θ_{JC}		39.47°C /W
operating junction temperature T_J		-40°C to 150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM MM)(NOTE 2)		
PVCC PIN HBM:AEC Q100-002		±4kV
Other PINS HBM:AEC Q100-002		±4kV
CDM:AEC Q100-011		±1.5kV
Latch-Up		
Test condition:AEC_Q100-004		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Electrical Characteristics

PVCC=14.4V, R_L=4Ω, T_C=25°C, default I^2C settings (unless otherwise noted)

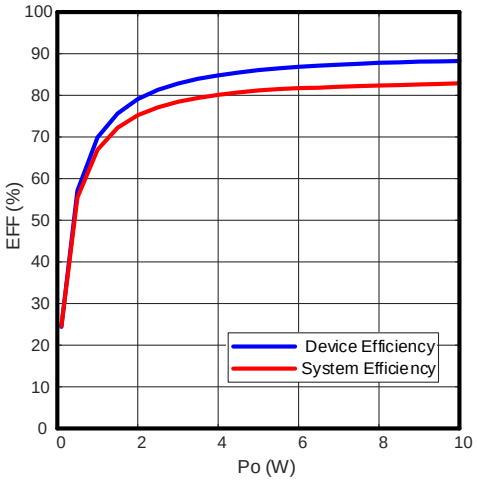
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
OPERATING CURRENT					
PVCC idle current	BD Modulation, In PLAY mode, no audio present		18		mA
	BD Modulation, In PLAY mode, no audio present, no snubber		14		mA
	LLM Modulation, In PLAY mode, no audio present		15		mA
PVCC standby current	Standby mode, MUTE = 0 V		12	20	μA
OUTPUT POWER					
Output power	4 Ω, THD+N<1%, 1 kHz, T_C = 75°C		10		W
Power efficiency	4 Ω, Po = 10W		83		%
AUDIO PERFORMANCE					
Noise voltage at output	Gain = 20 dB, zero input, and A-weighting		65		μV
Common-mode rejection ratio	f = 1 kHz, 100 mVrms referenced to GND, Gain = 20 dB		70		dB
Power-supply rejection ratio	PVCC = 14.4, V_{dc} + 1 Vrms, f = 1 kHz		75		dB
Total harmonic distortion + noise	Po= 1 W, f=1 kHz		0.04		%
Switching frequency	Switching frequency selectable for AM interference avoidance		400		kHz
			500		
Internal common-mode input bias voltage	Internal bias applied to IN_N, IN_P pins		2.7		V
Voltage gain (Vo/ Vin)	Source impedance = 0 Ω, register 0x03 bits [7:6]= 00	19	20	21	dB
	Source impedance = 0 Ω, register 0x03 bits [7:6] = 01	25	26	27	
	Source impedance = 0 Ω, register 0x03 bits [7:6] = 10	31	32	33	
	Source impedance = 0 Ω, register 0x03 bits [7:6] = 11	35	36	37	
PWM OUTPUT STAGE					
FET drain-to-source resistance	T_J = 25°C		130		mΩ
Output offset voltage	Zero input signal, Gain = 20 dB	-25	0	+25	mV
PVCC OVERVOLTAGE (OV) PROTECTION					
PVCC overvoltage-shutdown set		19.5	21	22.5	V
PVCC overvoltage-shutdown hysteresis			0.8		V
PVCC UNDERVOLTAGE (UV) PROTECTION					
PVCC undervoltage-shutdown set		3.6	4.2	4.4	V
PVCC undervoltage-shutdown hysteresis			0.25		V
GVDD					

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
GVDD pin voltage		5.4	5.75	6.6	V
POWER-ON RESET (POR)					
PVCC voltage for POR			2.4		V
PVCC recovery hysteresis voltage for POR			0.2		V
OVERTEMPERATURE (OT) PROTECTION					
Junction temperature for over temperature shutdown(NOTE 3)		155	170		°C
Junction temperature overtemperature shutdown hysteresis			10		°C
OVERCURRENT (OC) SHUTDOWN PROTECTION					
Maximum current (peak output current)			4		A
$\overline{SDZ}$ &MUTE PIN					
$\overline{SDZ}$ pin current			2	4	μA
High-Level Input Voltage	$\overline{SDZ}$ &MUTE	1.3			V
Low-Level Input Voltage	$\overline{SDZ}$ &MUTE			0.5	V
DC DETECT					
DC detect threshold			2.9		V
DC detect step response time			550	700	ms
$\overline{FAULT}$ REPORT					
$\overline{FAULT}$ pin output voltage for logic-level high (open-drain logic output)	External 47kΩ pullup resistor to 3.3 V	1.3			V
$\overline{FAULT}$ pin output voltage for logic-level low (open-drain logic output)	External 47kΩ pullup resistor to 3.3 V			0.5	V
LOAD DIAGNOSTICS(NOTE 3)					
Resistance to detect a short from OUT pin(s) to PVCC or ground				200	Ω
Open-circuit detection threshold	Including speaker wires	70	85	120	Ω
Short-circuit detection threshold	Including speaker wires	0.9	1.3	1.5	Ω
I²C					
SDA/SCL High-level Input Voltage	R(PU_I²C) = 4.7kΩ pullup	1.3			V
SDA/SCL Low-level Input Voltage	R(PU_I²C) = 4.7kΩ pullup			0.5	V
Load capacitance for each bus line				400	pF

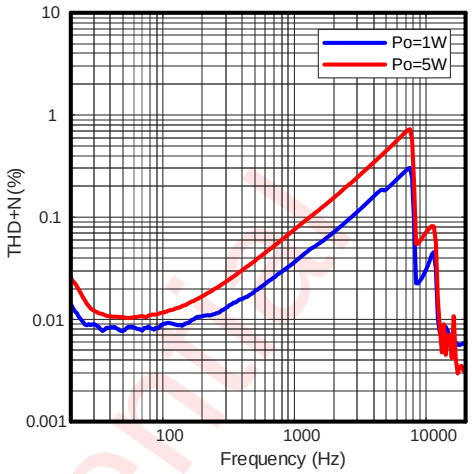
Note3: The data are obtained from laboratory test and design simulation for reference.

Typical Characteristics

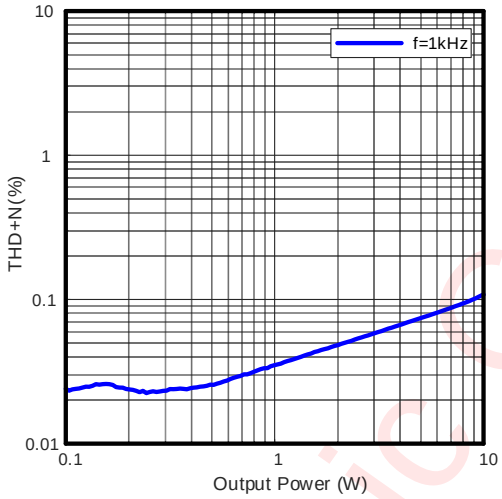
PVCC=14.4V, RL=4Ω, T_C=25°C, default I^2C settings (unless otherwise noted)



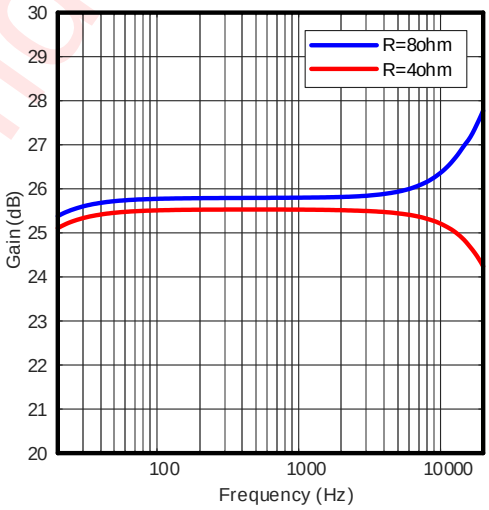
Efficiency vs Po



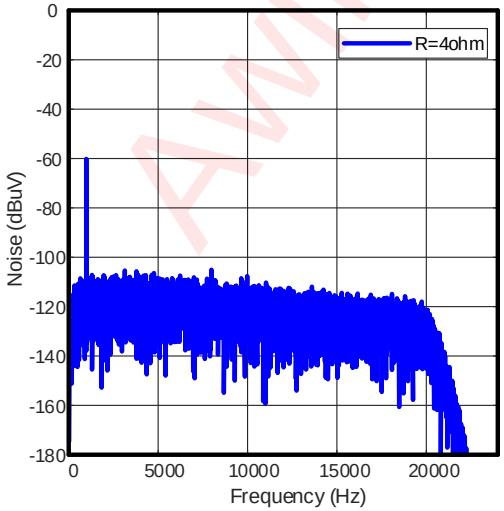
THD+N vs Frequency



THD+N vs Po



Gain vs Frequency



Noise vs Frequency

Detailed Functional Description

The AW83611TSR-Q1 is a Class D mono-channel high-efficiency audio power amplifier with I²C control that delivers up to 10W of power at 14.4V power with 4Ω load.

Device Modulation Scheme

The AW83611 has the option of running in either BD modulation or Low-Loss modulation; this is set by register REG_EN_LLM (0x53h).

EN_LLM=0: BD modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0V to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switch period, reducing the switching current, which reduces any I²R losses in the load.

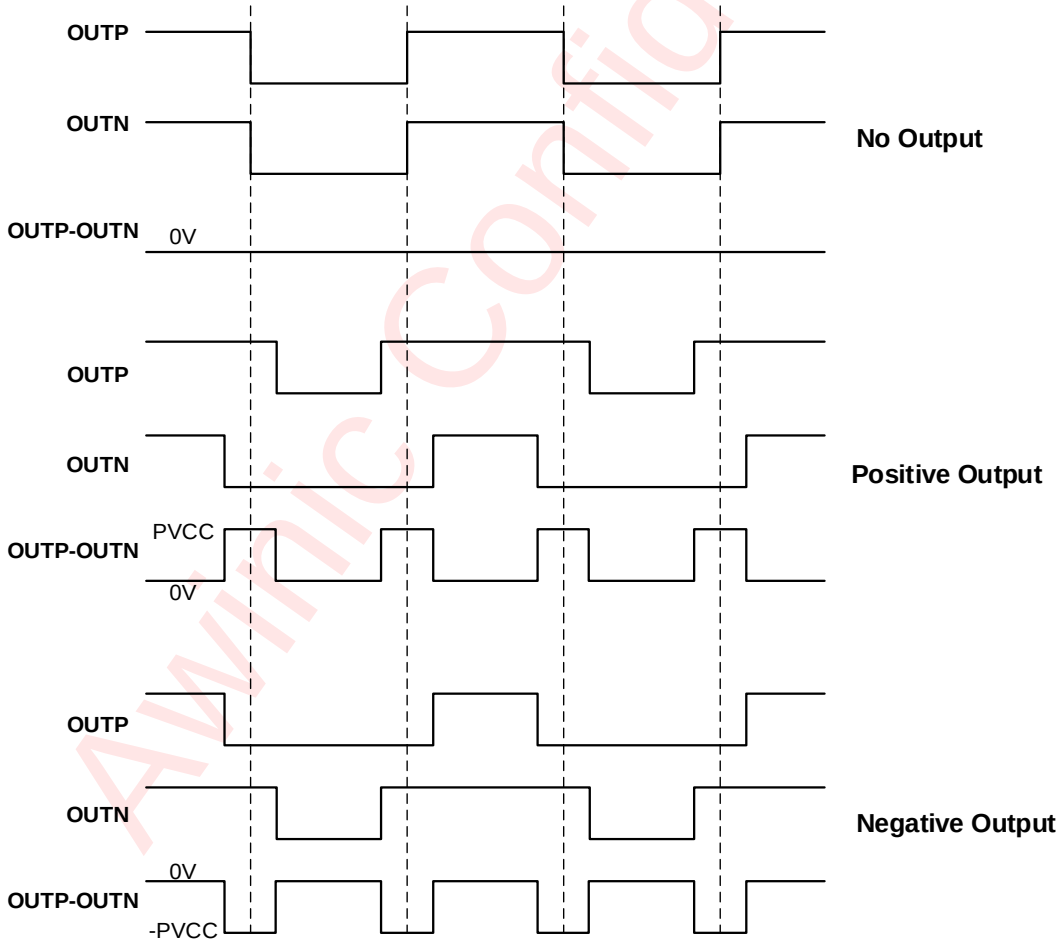


Figure 1 BD Mode Modulation

EN_LLM=1: Low-Loss modulation

The Low-Loss mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low-Loss mode the outputs operate at 20% modulation during idle conditions. When an audio signal is applied one output will

decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in Low-Loss mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

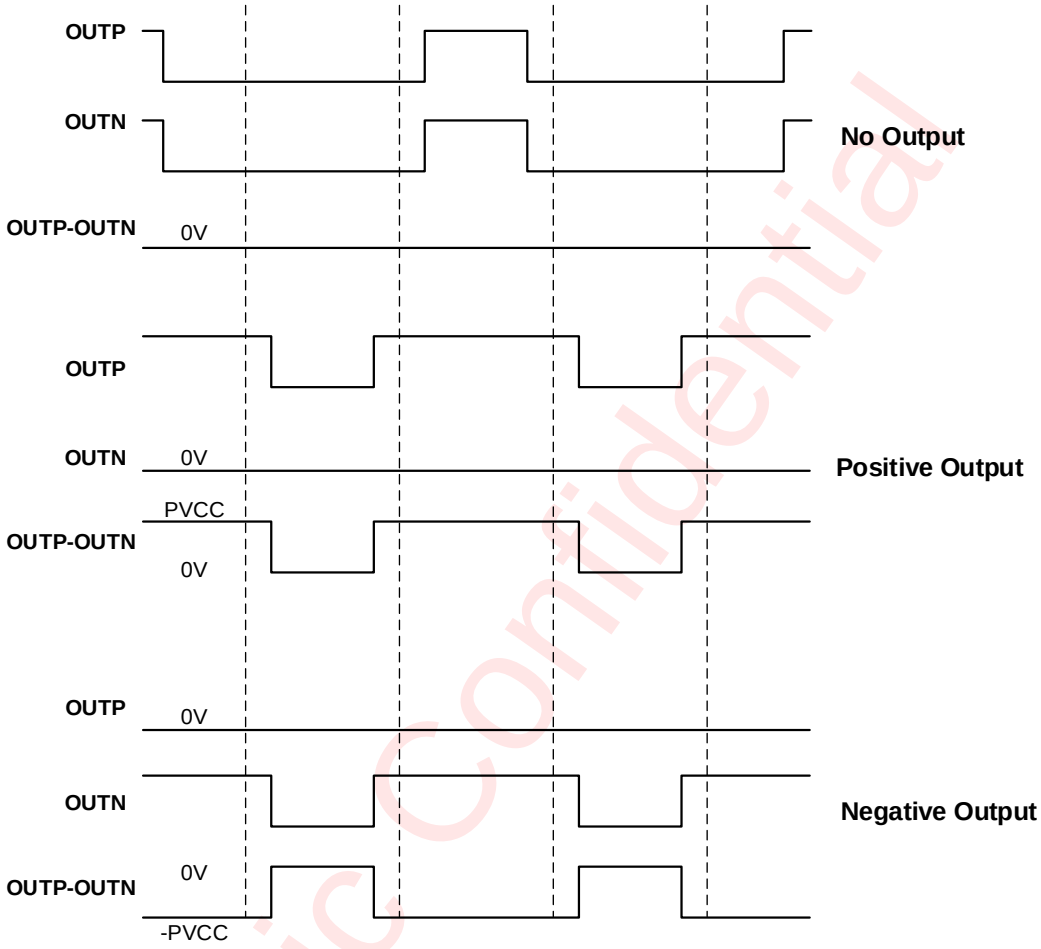


Figure 2 Low-Loss Mode Modulation

Load Diagnostics

The device incorporates load diagnostic circuitry designed for detecting and determining the status of output connections. The device supports the following diagnostics:

- Short to GND
- Short to PVCC
- Short across load
- Open load

The device reports the presence of any of the short or open conditions to the system via I²C register read.

The load diagnostic function runs on deassertion of $\overline{SDZ}$ or when the device is in a fault state (dc detect, overcurrent, overvoltage, undervoltage, or overtemperature). During this test, the outputs are in a Hi-Z state. The device determines whether the output is a short to GND, short to PVCC, open load, or shorted load. The load diagnostic test takes approximately 209 ms to run. On detection of an open load, the output still operates. On detection of any other fault condition, the output goes into a Hi-Z state, and the device checks the load continuously until removal of the fault condition. After detection of a normal output condition, the audio output starts. All faults have I²C and $\overline{FAULT}$ pin assertion.

The device performs load diagnostic tests as shown in Figure 3.

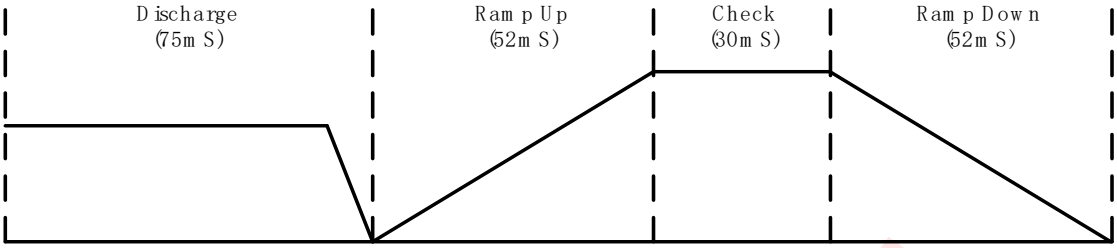


Figure 3 Load Diagnostics Sequence of Events

Figure 4 illustrates how the diagnostics determine the load based on output condition

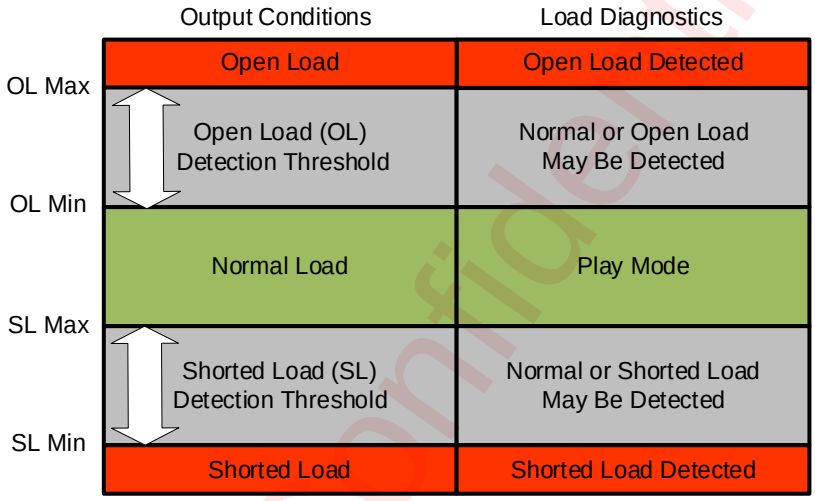


Figure 4 Load Diagnostics Reporting Thresholds

Analog Audio Input and Preamplifier

The differential input stage of the amplifier cancels common-mode noise that appears on the inputs. For a differential audio source, connect the positive lead to IN_P and the negative lead to IN_N. The inputs must be ac-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages. For good transient performance, the impedance seen at each of the two differentia inputs should be the same.

The gain setting impacts the analog input impedance of the amplifier.

GAIN	INPUT IMPEDANCE
20 dB	60 kΩ ± 20%
26 dB	30 kΩ ± 20%
32 dB	15 kΩ ± 20%
36 dB	9 kΩ ± 20%

Plimit Operation

The AW83611 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail, the amplifier simply operates as if it was powered by a lower supply voltage, and thereby limits the output power. This protection circuitry limits the output voltage to the value selected in I^2C register 0x03.

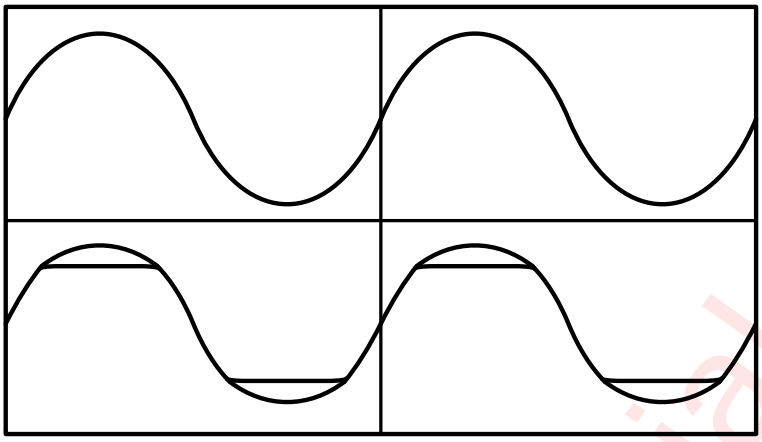


Figure 5 Power Limit Example

Thermal Foldback

The Thermal Foldback (TFB) is designed to protect AW83611 from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. It allows the AW83611 to play as loud as possible without triggering unexpected thermal shutdown. When the die temperature triggers the over-temperature warning level (140°C), an internal AGC (Automatic Gain Control) will reduce the gain gradually. Once the die temperature drops below the over-temperature warning level, the device's gain gradually returns to the former setting.

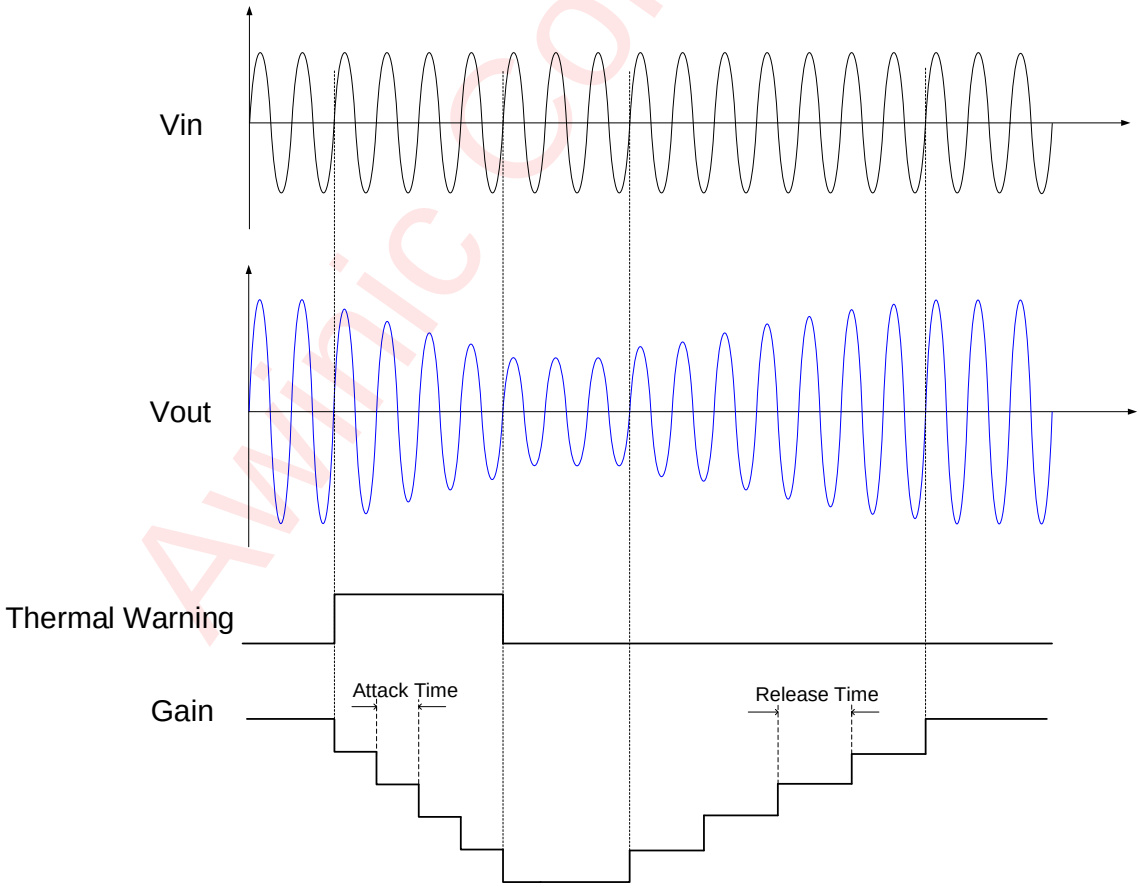


Figure 6 Thermal Foldback Operation Principle

Operating Modes and Faults

The following tables list operating modes and faults.

STATE NAME	OUTPUT	OSCILLATOR	I²C
Shut Down	To zero	Stopped	Stopped
Load Diagnostic	DC biased	Active	Active
Fault and mute	To zero	Active	Active
Play	Switching	Active	Active

FAULT EVENT	FAULT EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	CLEARING
POR	Voltage fault	All	Not applicable	Hard mute (no ramp)	Others stop(Bias and LDO working)	Self-clearing
UVP/OVP			I²C+$\overline{\text{FAULT}}$ pin		Output to zero	
Load Dump			$\overline{\text{FAULT}}$ pin			
OT	Thermal fault	Load Diagnostic, Mute, play	I²C+$\overline{\text{FAULT}}$ pin			
OC	Output channel fault	Play				
DC detect						
Load diagnostic-short	Diagnostic	Hi-Z		/	Hi-Z, rerun diagnostics	
Load diagnostic-open			I²C		/	Clears on next diagnostic cycle

Protection and Monitoring

• **Overcurrent Shutdown (OCSD)**—The overcurrent shutdown forces the output into Hi-Z. The device asserts the $\overline{\text{FAULT}}$ pin and updates the I²C register.

• **DC Detect**—This circuit checks for a dc offset continuously during normal operation at the output of the amplifier. If a dc offset occurs, the device asserts the $\overline{\text{FAULT}}$ pin and updates the I²C register. Note that the dc detection threshold follows PVCC changes.

• **Overtemperature Shutdown(OTSD)—**The device shuts down when the die junction temperature reaches the overtemperature threshold. The device asserts the $\overline{\text{FAULT}}$ pin and updates I²C register. Recovery is automatic when the temperature returns to a safe level.

• **Undervoltage(UV)**—The undervoltage (UV) protection detects low voltages on PVCC. In the event of an undervoltage condition, the device asserts the $\overline{\text{FAULT}}$ pin and resets the I²C register.

• **Power-On Reset(POR)**—Power-on reset (POR) occurs when PVCC drops below the POR threshold. A POR event causes the I²C bus to go into a high-impedance state. After recovery from the POR event, the device restarts automatically with default I²C register settings. The I²C is active as long as the device is not in POR.

• **Overvoltage(OV)and Load Dump**—The Overvoltage (OV) protection detects high voltages on PVCC. If PVCC reaches the overvoltage threshold, the device asserts the $\overline{\text{FAULT}}$ pin and updates the I²C register. The device can withstand 45V load-dump voltage spikes.

• **Plimit Protection**—This protection circuitry limits the output voltage to the value selected in I²C register 0x03. One can use this feature to improve battery life or protect the speaker from exceeding its excursion limits.

I²C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	1.3			μs
3	t_{HIGH}	SCL High level Duration	0.6			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

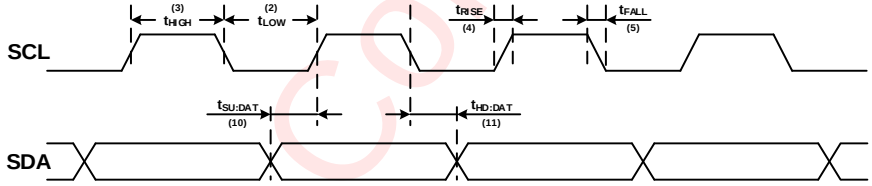


Figure 7 SCL and SDA timing relationships in the data transmission process

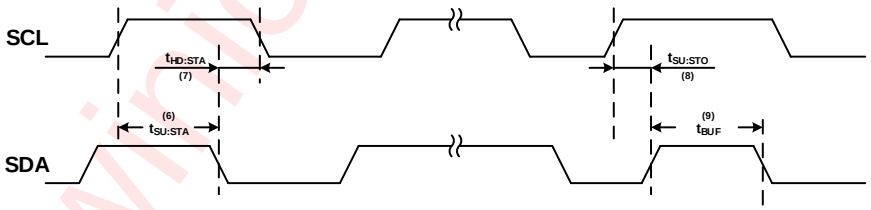


Figure 8 The Timing Relationship between START and STOP State

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. All data to start transmission and end of transmission requires the main device to issue START state and STOP status:

START state：The SCL maintain a high level, SDA from high to low level

STOP state：The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 9.

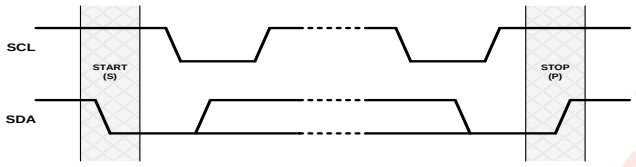


Figure 9 START and STOP State Generation Process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 10. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 11. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

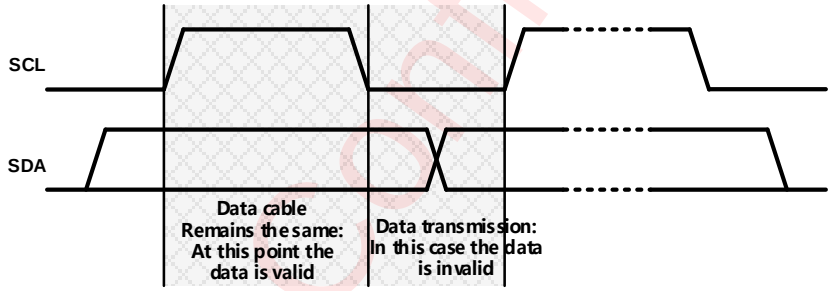


Figure 10 The Data Transfer Rules on the I²C Bus

The whole process of actual data transmission is shown in Figure 11. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

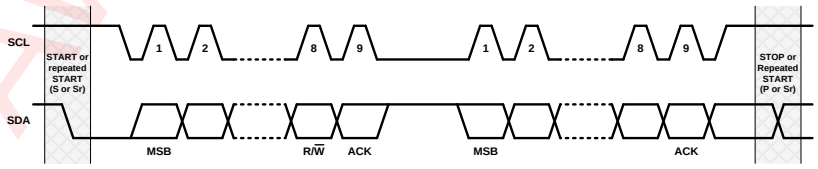


Figure 11 Data Transmission on the I²C Bus

I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW83611 as the slave device, the transmission process in accordance with the following steps, as shown in Figure 12:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW83611 register address to which the first data byte will written；

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW83611, within AW83611 each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.

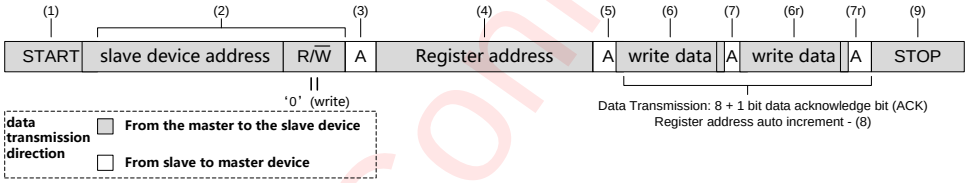


Figure 12　Writing Process (Data Transmission Direction Remains the Same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW83611 as the slave device, the transmission process carried out by following steps listed in Figure 13:

Master device asserts a start condition;

Master device transmits the 7 bits address of AW83611, and followed by a "read / write" flag ($R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device sends the 8bit address that the AW83611 register needs to read the data;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START.

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again.

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not.

The master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully.

AW83611 automatically increment register address once after the slave sent each acknowledge bit (ACK). The master device generates the STOP state to end the data transmission.

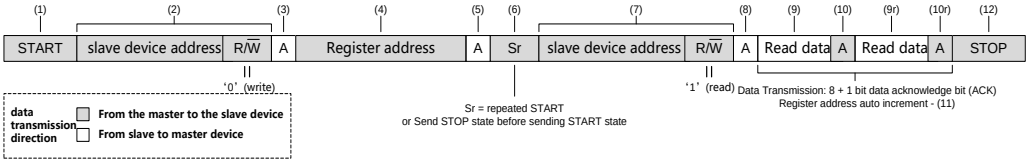


Figure 13 Reading Process (Data Transmission Direction Remains the Same)

Register Configuration

I2C ADDRESS

DESCRIPTION	FIXED ADDRESS							READ/WRITE BIT	I²C ADDRESS
	MSB	6	5	4	3	2	1	LSB	
I²C write	1	1	0	1	1	0	0	0	0xD8
I²C read	1	1	0	1	1	0	0	1	0xD9

Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	ID	RO	CHIPID								0x11
0x01	FAULT_REGISTER	RC	OT	DC	OVP	UVP	OC	LOAD_DIAGNOSTICS	00		0x00
0x02	STATUS_AND_LOAD_DIAGNOSTIC_REGISTER	RO	PLAY_MODE	MUTE_MODE	LOAD_DIAGNOSTICS_MODE	FAULT	SL	OL	S2G	S2P	0x90
0x03	CONTROL_REGISTER	R/W	REG_GAIN_SEL		REG_PLIMIT_SEL			REG_AM_IN			0x78

Register Detailed Description

FAULT_REGISTER: (Address 01h)

Bit	Symbol	R/W	Description	Default
7	OT	RC	Die Temperature is higher than 160degrees 0: Normal 1: OT	0
6	DC	RC	DC detect status indicator 0: Normal 1: DC DETECT	0
5	OVP	RC	System OVP status indicator 0: Normal 1: OVP	0
4	UVP	RC	PVCC under UVP threshold voltage indicator 0: Normal 1: UVP	0
3	OC	RC	Over current status in amplifier 0: Normal 1: OC	0
2	LOAD_DIAGNOSTICS	RC	Load diagnostics status indicator 0: Normal 1: Load diagnostics status	0
1:0	Reserved	RC	Not used	00

STATUS_AND_LOAD_DIAGNOSTIC_REGISTER: (Address 02h)

Bit	Symbol	R/W	Description	Default
7	PLAY_MODE	RO	Play mode status indicator 0: Normal 1: In play mode	1

6	MUTE_MODE	RO	Mute mode status indicator 0: Normal 1: In mute mode	0
5	LOAD_DIAGNOSTICS_MODE	RO	Load diagnostics status indicator 0: Normal 1: Load diagnostics status	0
4	FAULT	RO	Fault status indicator 0: In fault status 1: Normal	1
3	SL	RO	Short load status indicator 0: Normal 1: In short-load status	0
2	OL	RO	Open load status indicator 0: Normal 1: In open-load status	0
1	S2G	RO	Short to GND status indicator 0: Normal 1: In S2G status	0
0	S2P	RO	Short to PVCC status indicator 0: Normal 1: In S2P status	0

CONTROL_REGISTER: (Address 03h)

Bit	Symbol	R/W	Description	Default
7:6	REG_GAIN_SEL	RW	CLASSD Gain Set 00: 20dB 01: 26dB 10: 32dB 11: 36dB	01
5:3	REG_PLIMIT_SEL	RW	PLIMIT Threshold 000: 5V 001: 6V 010: 7V 011: 8.5V 100: 10V 101: 12V 110: 14V 111: Disable	111
2:0	REG_AM_IN	RW	Frequency Selection, User Input 000: 400kHz 001: 500kHz 010~111:Test mode	000

Application and Implementation

Design Requirements

Use the following for the design requirements:

- Power Supplies

The device needs only a single power supply compliant with the recommended operation range. The device is designed to work with either a vehicle battery or regulated power supply such as from a backup battery.

- Communication

The device communicates with the system controller with both discrete hardware control pins and with I²C. The device is an I²C slave and thus requires a master. If a master I²C-compliant device is not present in the system, it is still possible to use the device, but only with the default settings. Diagnostic information is limited to the discrete reporting $\overline{\text{FAULT}}$ pin.

- External Components

The table lists the components required for the device.

Component	QUANTITY	APPLICATION	SIZE	TYP.	UNIT
L1,L2	2	Amplifier output filtering	7.3mmx6.9mm	15	μH
L3	1	Power supply	13mmx13mm	10	μH
C11,C12	2	Amplifier output filtering	0805	3.3	μF
C13,C14	2	Output EMI filtering	0603	0.01	μF
C9,C10	2	Amplifier output snubbers	0603	470	pF
R1,R2	2	Output snubbers	0805	5.6	Ω
C7,C8	2	Bootstrap capacitors	0603	0.22	μF
C4,C5,C6	3	Analog audio input filter, bypass	0805	1	μF
R3,R4	2	Analog audio input filter	0805	49.9	kΩ
C1	1	Power supply	0603	0.1	μF
C2	1	Power supply	1206	10	μF
C3	1	Power supply	10mm	330	μF
C15	1	Power supply	0603	2.2	nF
C16	1	Power supply	0603	82	nF
C17,C18	2	Power supply	1206	4.7	μF

Detailed Design Procedure

Use the following steps for the design procedure:

1. Hardware Schematic Design: Using the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
2. Following the recommended layout guidelines, integrate the device and its supporting components into the system PCB file.
3. Thermal Design: The device has an exposed thermal pad which requires proper soldering.

Even if unused, always connect pins to a fixed rail; do not leave them floating. Floating input pins represent an ESD risk, so adhere to the following guidance for each pin.

MUTE Pin

If the MUTE pin is unused in the application, connect it to GND through a high-impedance resistor.

SDZ Pin

If the $\overline{\text{SDZ}}$ pin is unused in the application, connect it to a low-voltage rail such as 3.3 V or 5 V through a high-impedance resistor.

I²C Pins (SDA and SCL)

If there is no microcontroller in the system, use of the device without I2C communication is possible. In this situation, connect the SDA and SCL pins to 3.3V or 5V.

Terminating Unused Outputs

If the $\overline{\text{FAULT}}$ pin does not report to a system microcontroller in the application, connect it to GND.

Using a Single-Ended Audio Input

When using a single-ended audio source, ac-ground the negative input through a capacitor equal in value to the input capacitor on the positive input, and apply the audio source to the positive input. For best performance, the ac ground should be at the audio source instead of at the device input if possible.

PCB Layout Consideration

The AW83611TSR-Q1 is a Class D mono-channel high-efficiency audio power amplifier, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

a) The high-frequency decoupling capacitors should be placed as close to the PVCC terminals as possible. Large (330μF or greater) bulk power supply decoupling capacitors should be placed near the AW83611 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection.

b) The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the AW83611.

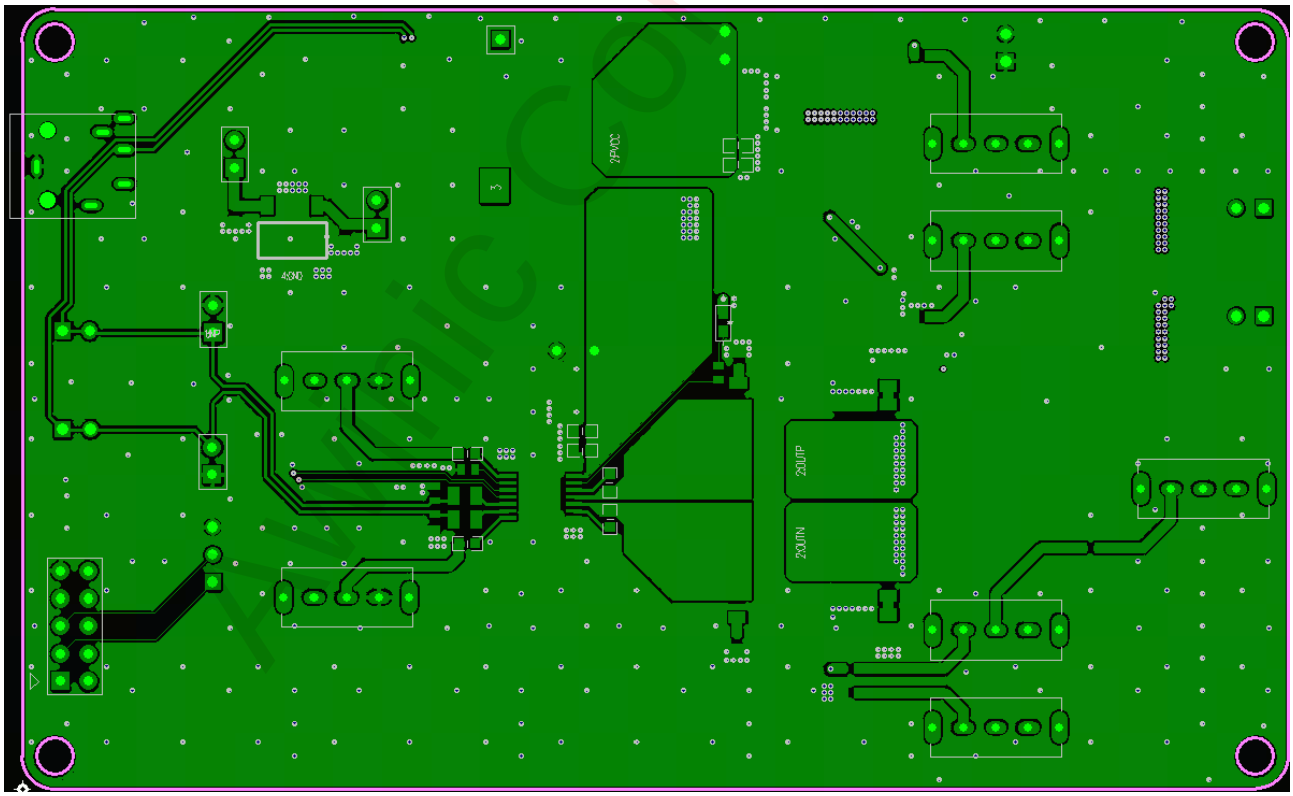
c) The LC filter should be placed as close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

d) Place the AW83611 device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.

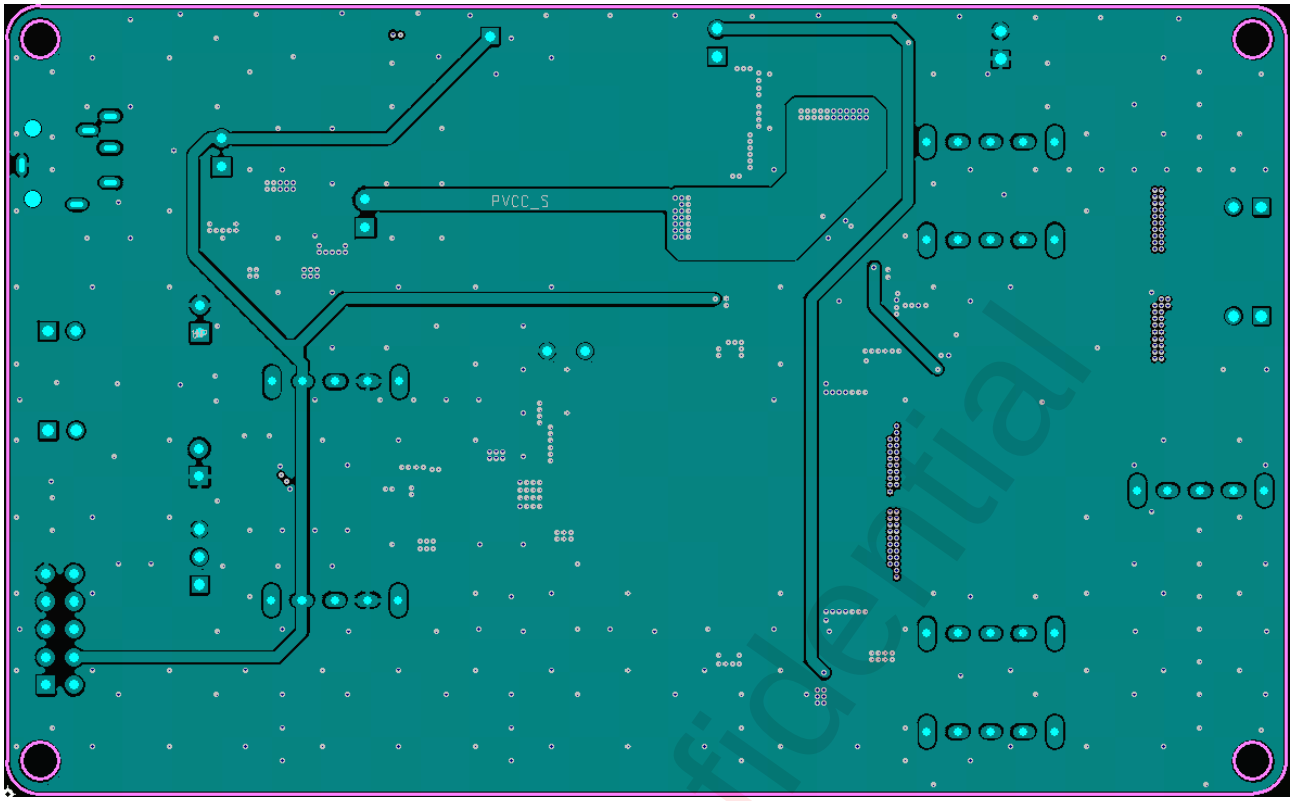
e) Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

f) Ensure the vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the AW83611 to open up the current path to and from the device.

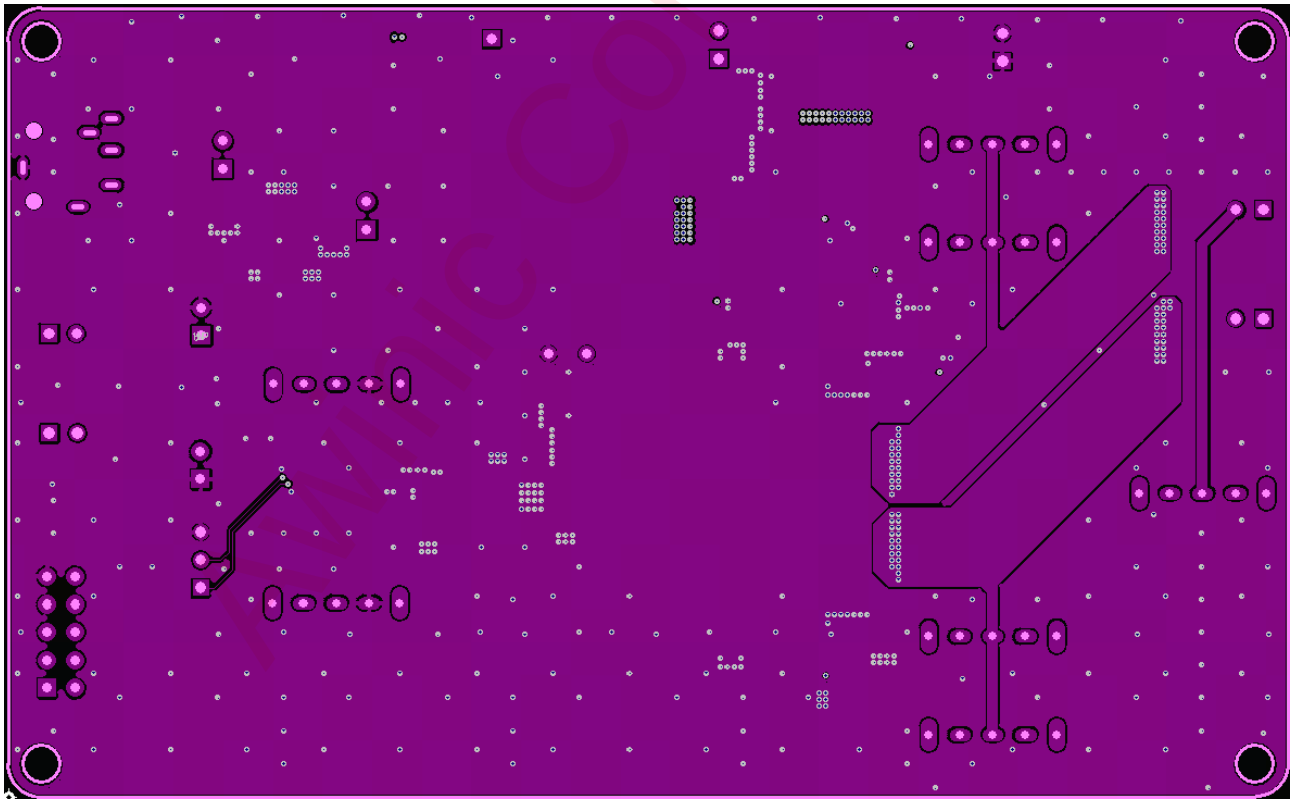
Layout Example



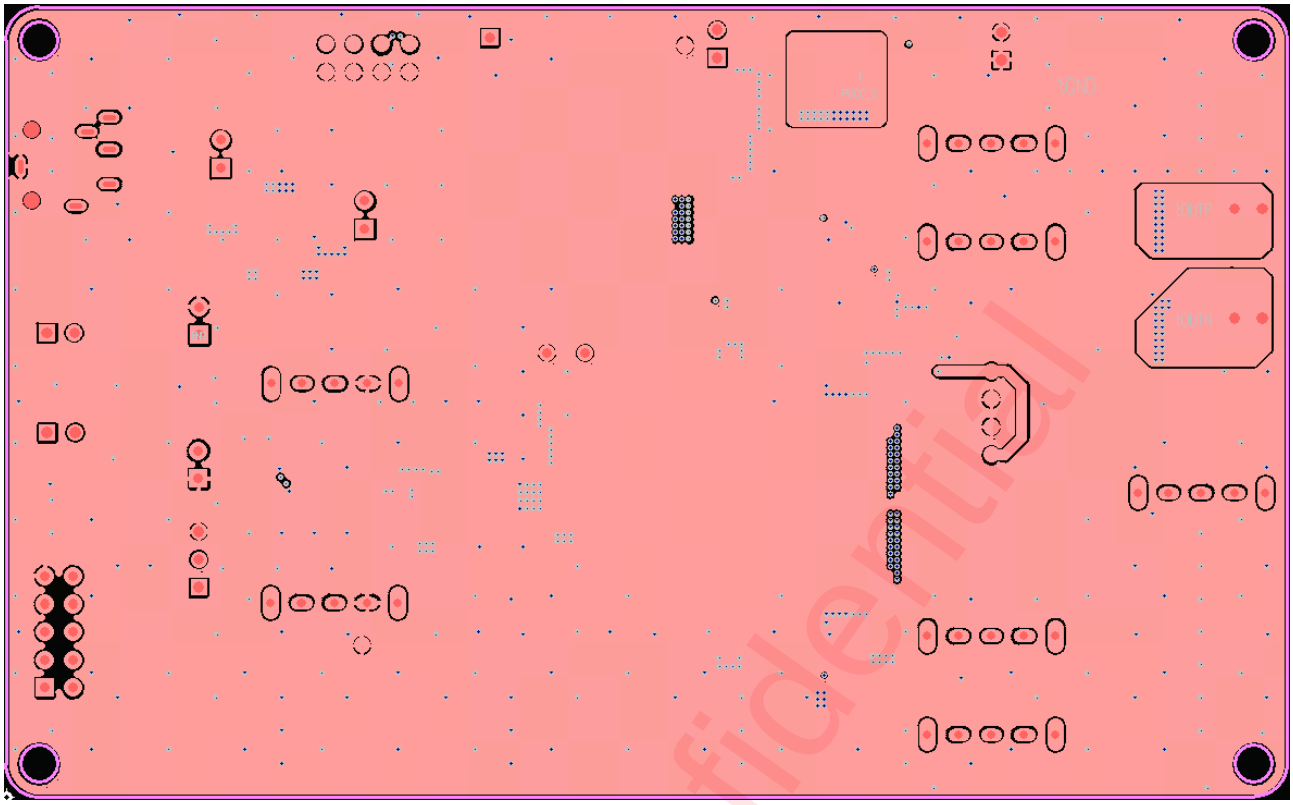
Layout Example Top



Layout Example Power



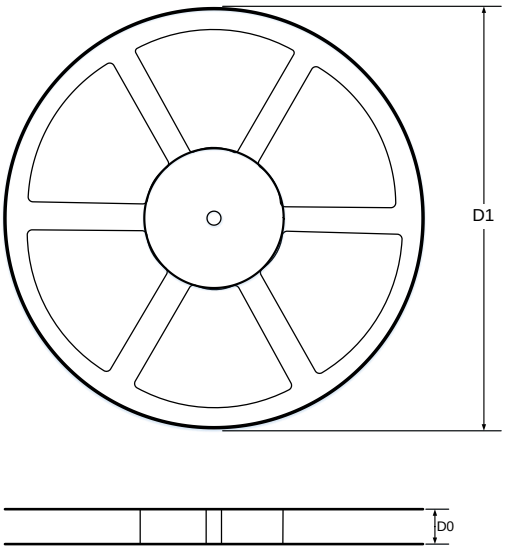
Layout Example Signal



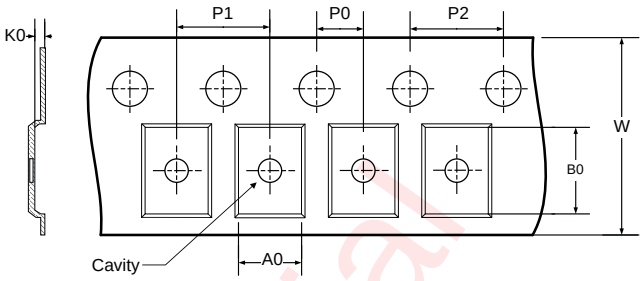
Layout Example Bottom

Tape And Reel Information

REEL DIMENSIONS

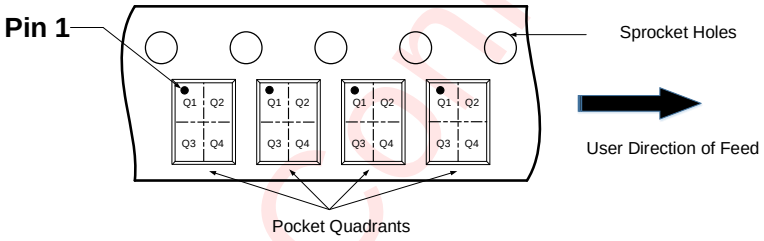


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



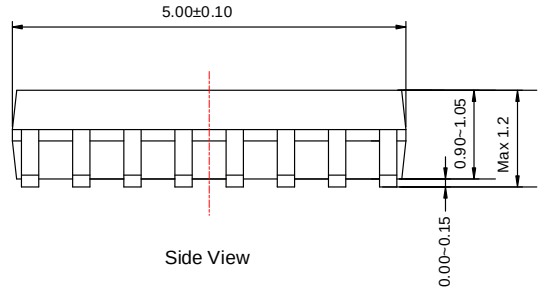
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

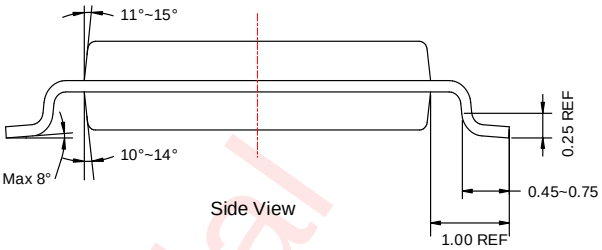
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	6.8	5.4	1.2	2	8	4	12	Q1

All dimensions are nominal

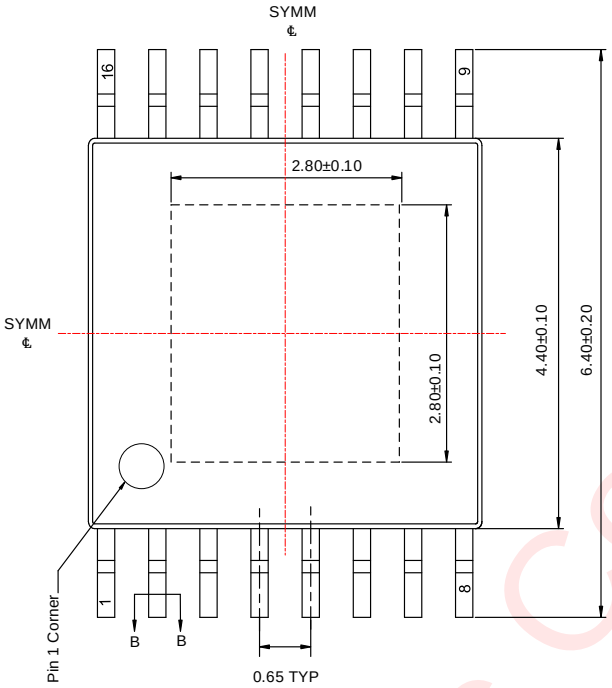
Package Description



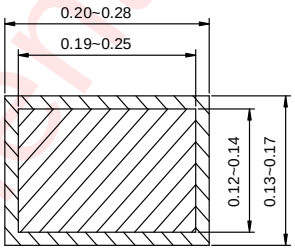
Side View



Side View



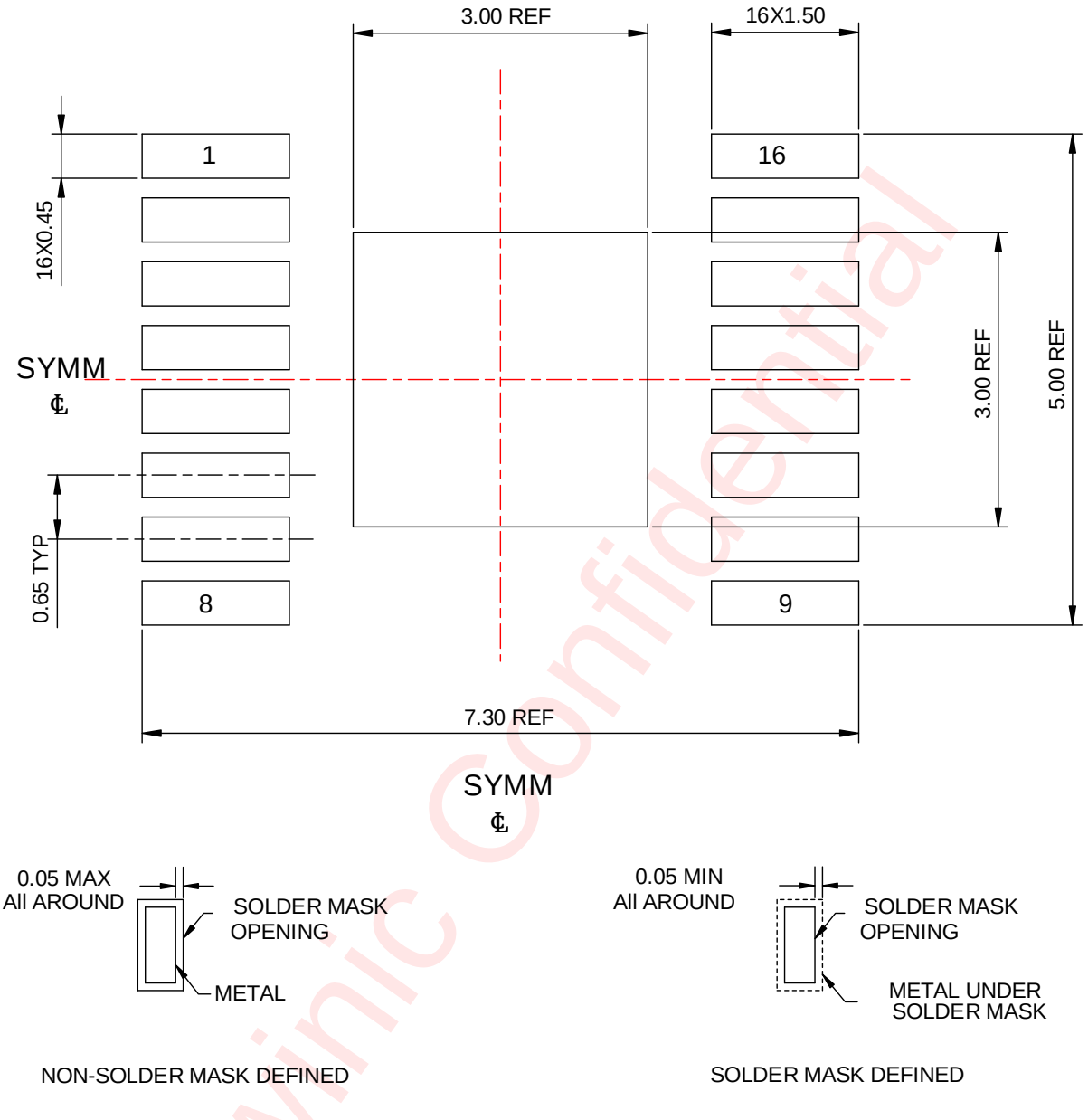
Top View



Section B-B

Uint:mm

Land Pattern Data



Unit：mm

Revision History

Version	Date	Change Record
V1.0	Oct. 2023	AW83611TSR-Q1 datasheet V1.0
V1.1	Dec.2023	Added 1.8V IIC interface application description
V1.2	May.2024	Update the following databoundaries： 1) TJ; 2) PVCC standby current; 3) PVDD overvoltage-shutdown set; 4) PVDD undervoltage-shutdown set; 5) Junction temperature for overtemperature shutdown; 6) STANDBY pin current; 7) IIC Load capacitance for each bus line.
V1.3	Sep.2024	Update the following description： 1) AEC-Q100 qualified for automotive applications； 2) I2C Address description.
V1.4	Jan.2025	Update PVCC overvoltage-shutdown hysteresis.

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