



Description

The CD4094BNSR is an 8-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs QP0 to QP7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (OE) signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of CD4094BNSR devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading CD4094BNSR devices when the clock has a slow rise time.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

Features

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: SOP16

Applications

- Serial-to-parallel data conversion
- Remote control holding register
- Dual-rank shift, hold, and bus applications

Ordering Information

Product Model	Package Type	Packing	Packing Qty
CD4094BNSR	SOP-16(SOIC-16)	Tape	2500Pcs/Reel



Block Diagram

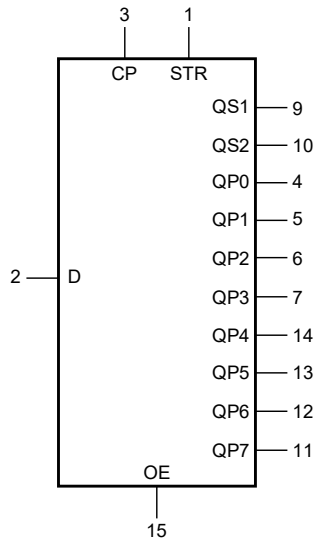


Figure 1. Logic symbol

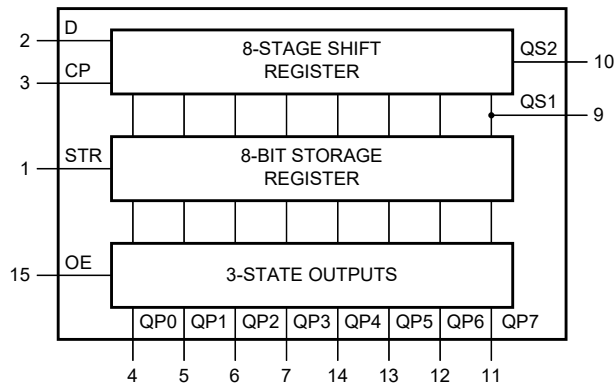


Figure 2. Functional diagram

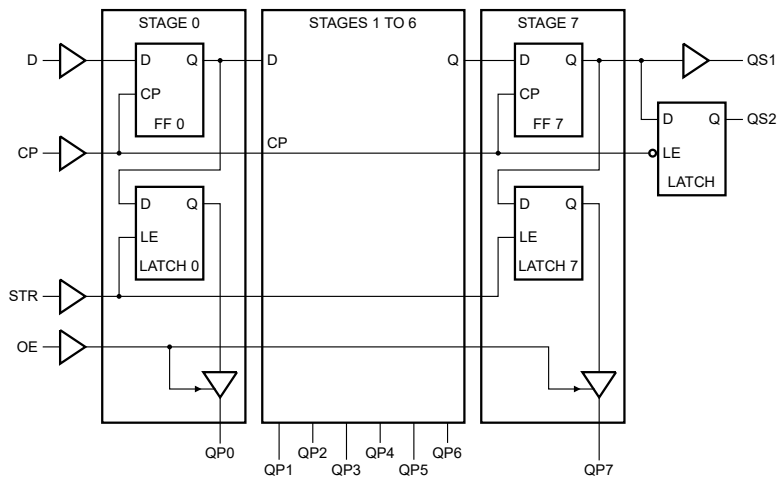
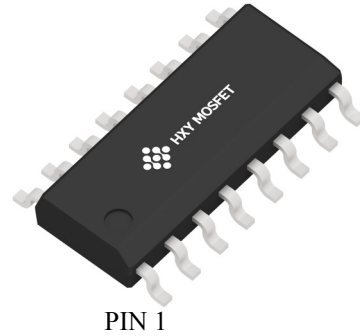
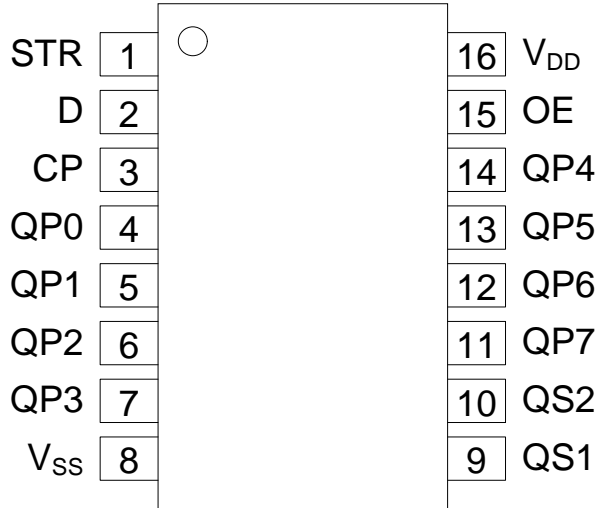


Figure 3. Logic diagram



Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	STR	strobe input
2	D	data input
3	CP	clock input
4	QP0	parallel output
5	QP1	parallel output
6	QP2	parallel output
7	QP3	parallel output
8	V _{SS}	ground (0V)
9	QS1	serial output
10	QS2	serial output
11	QP7	parallel output
12	QP6	parallel output
13	QP5	parallel output
14	QP4	parallel output
15	OE	output enable input
16	V _{DD}	supply voltage

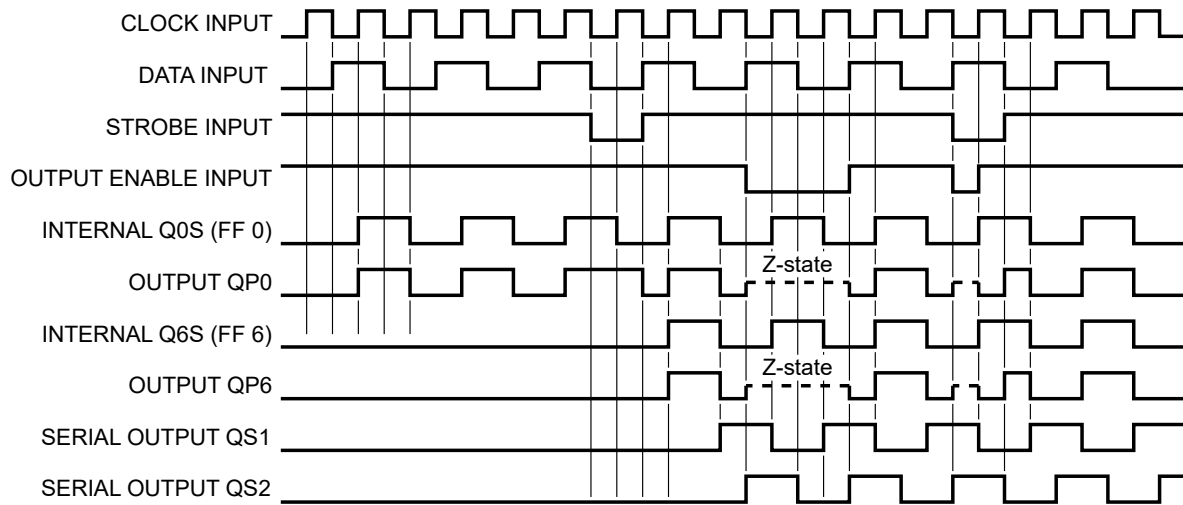


Figure 4. Timing diagram

Function Table

Input				Parallel output		Serial output	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn-1	Q6S	NC
↑	H	H	H	H	QPn-1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=HIGH-impedance OFF-state;

NC=no change; ↑=positive-going transition; ↓=negative-going transition;

Q6S=the data in register stage 6 before the LOW to HIGH clock transition;

Q7S=the data in register stage 7 before the HIGH to LOW clock transition.



Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{DD}	-	-0.5	+18	V
DC input current	I_{IK}	anyone input	-	± 10	mA
input voltage	V_I	all inputs	-0.5	$V_{DD}+0.5$	V
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
soldering temperature	T_L	10s	DIP	245	°C
			SOP/TSSOP	260	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+125	°C
data setup time	t_{su}	$V_{DD}=5V$	125	-	-	ns
		$V_{DD}=10V$	55	-	-	ns
		$V_{DD}=15V$	35	-	-	ns
clock pulse width	t_w	$V_{DD}=5V$	200	-	-	ns
		$V_{DD}=10V$	100	-	-	ns
		$V_{DD}=15V$	83	-	-	ns
clock input frequency	f_{max}	$V_{DD}=5V$	dc	-	1.25	MHz
		$V_{DD}=10V$		-	2.5	MHz
		$V_{DD}=15V$		-	3	MHz
clock rise and fall time	t_{rCL}, t_{fCL}	$V_{DD}=5V$	-	-	15	us
		$V_{DD}=10V$	-	-	5	us
		$V_{DD}=15V$	-	-	5	us
strobe setup time	t_w	$V_{DD}=5V$	200	-	-	ns
		$V_{DD}=10V$	80	-	-	ns
		$V_{DD}=15V$	70	-	-	ns



Electrical Characteristics

DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			$T_{amb}=25^{\circ}\text{C}$			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	-	5	μA
		-	0, 10	10	-	-	10	μA
		-	0, 15	15	-	-	20	μA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	-	± 1	μA
OFF-state output current	I_{OZ}	0, 15	0, 15	15	-	-	± 1	μA



DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	5	-	150	μA
		-	0, 10	10	-	10	-	300	μA
		-	0, 15	15	-	20	-	600	μA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.61	-	0.42	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	mA
		1.5	0, 15	15	4	-	2.8	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.61	-	-0.42	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	mA
		13.5	0, 15	15	-4	-	-2.8	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
input leakage current	I_i	-	0, 15	15	-	± 1	-	± 1	μA
OFF-state output current	I_{oz}	0, 15	0, 15	15	-	± 1	-	± 12	μA



DC Characteristics 3

($T_{amb}=-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+125^{\circ}\text{C}$		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	5	-	150	μA
		-	0, 10	10	-	10	-	300	μA
		-	0, 15	15	-	20	-	600	μA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.61	-	0.36	-	mA
		0.5	0, 10	10	1.5	-	0.9	-	mA
		1.5	0, 15	15	4	-	2.4	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.61	-	-0.36	-	mA
		2.5	0, 5	5	-1.8	-	-1.15	-	mA
		9.5	0, 10	10	-1.5	-	-0.9	-	mA
		13.5	0, 15	15	-4	-	-2.4	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	± 1	-	± 1	μA
OFF-state output current	I_{OZ}	0, 15	0, 15	15	-	± 1	-	± 12	μA



AC Characteristics

($T_{amb}=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$, $t_r, t_f=20\text{ns}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, unless otherwise specified.)

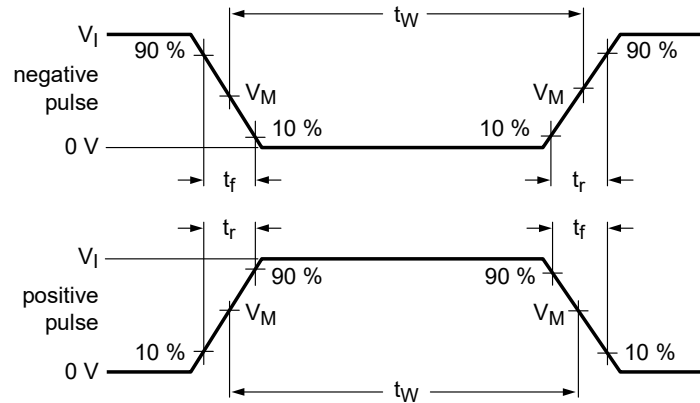
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
propagation delay time	t_{PHL}, t_{PLH}	CP to QS1; see Figure 6	$V_{DD}=5\text{V}$	-	300	600	ns
			$V_{DD}=10\text{V}$	-	125	250	ns
			$V_{DD}=15\text{V}$	-	95	190	ns
		CP to QS2; see Figure 6	$V_{DD}=5\text{V}$	-	230	460	ns
			$V_{DD}=10\text{V}$	-	110	220	ns
			$V_{DD}=15\text{V}$	-	75	150	ns
		CP to QPn; see Figure 6	$V_{DD}=5\text{V}$	-	420	840	ns
			$V_{DD}=10\text{V}$	-	195	390	ns
			$V_{DD}=15\text{V}$	-	135	270	ns
		STR to QPn; see Figure 7	$V_{DD}=5\text{V}$	-	290	580	ns
			$V_{DD}=10\text{V}$	-	145	290	ns
			$V_{DD}=15\text{V}$	-	100	200	ns
HIGH to OFF-state/OFF-state to HIGH propagation delay	t_{PHZ}, t_{PZH}	OE to QPn; see Figure 8	$V_{DD}=5\text{V}$	-	140	280	ns
			$V_{DD}=10\text{V}$	-	60	120	ns
			$V_{DD}=15\text{V}$	-	45	90	ns
LOW to OFF-state/OFF-state to LOW propagation delay	t_{PLZ}, t_{PZL}	OE to QPn; see Figure 8	$V_{DD}=5\text{V}$	-	100	200	ns
			$V_{DD}=10\text{V}$	-	50	100	ns
			$V_{DD}=15\text{V}$	-	40	80	ns
pulse width	t_w	minimum HIGH strobe pulse; see Figure 7	$V_{DD}=5\text{V}$	-	100	200	ns
			$V_{DD}=10\text{V}$	-	40	80	ns
			$V_{DD}=15\text{V}$	-	35	70	ns
		minimum LOW clock pulse; see Figure 6	$V_{DD}=5\text{V}$	-	100	200	ns
			$V_{DD}=10\text{V}$	-	50	100	ns
			$V_{DD}=15\text{V}$	-	40	83	ns
data setup time	t_{su}	D to CP; see Figure 9	$V_{DD}=5\text{V}$	-	60	125	ns
			$V_{DD}=10\text{V}$	-	30	55	ns
			$V_{DD}=15\text{V}$	-	20	35	ns
transition time	t_t	-	$V_{DD}=5\text{V}$	-	100	200	ns
			$V_{DD}=10\text{V}$	-	50	100	ns
			$V_{DD}=15\text{V}$	-	40	80	ns
clock input rise and fall time	t_{rCL}, t_{fCL}	-	$V_{DD}=5\text{V}$	15	-	-	us
			$V_{DD}=10\text{V}$	5	-	-	us
			$V_{DD}=15\text{V}$	5	-	-	us
maximum clock frequency	f_{max}	see Figure 6	$V_{DD}=5\text{V}$	1.25	2.5	-	MHz
			$V_{DD}=10\text{V}$	2.5	5	-	MHz
			$V_{DD}=15\text{V}$	3	6	-	MHz
input capacitance	C_i	any input	-	5	7.5	pF	

Note: t_t is the same as t_{TLH} and t_{THL} .

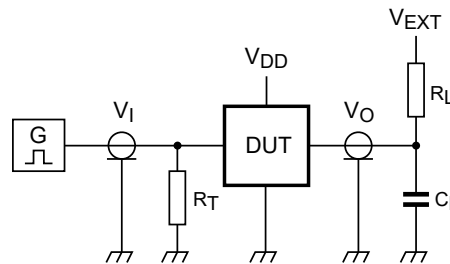


Testing Circuit

AC Testing Circuit



a. Input waveform



b. Test circuit

Figure 5. Test circuit for switching times

Definitions for test circuit: DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

V_{EXT} =External voltage for measuring switching times.



AC Testing Waveforms

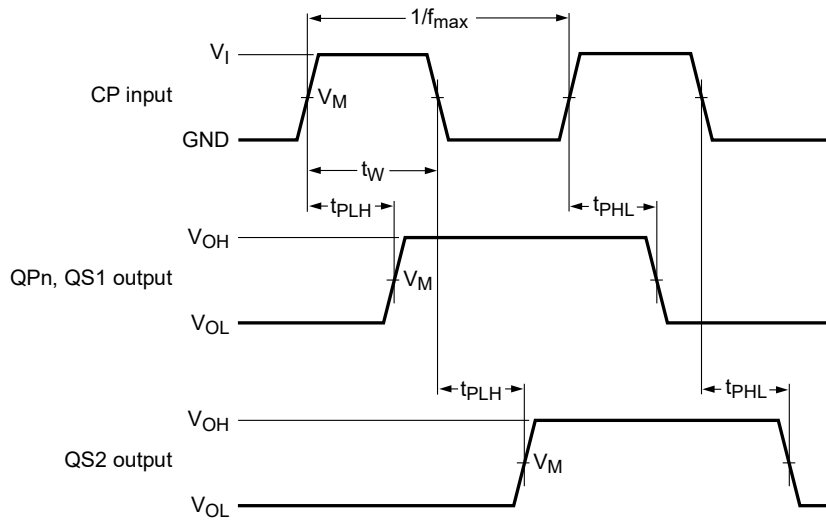


Figure 6. Clock to outputs propagation delays, and clock pulse width and maximum frequency

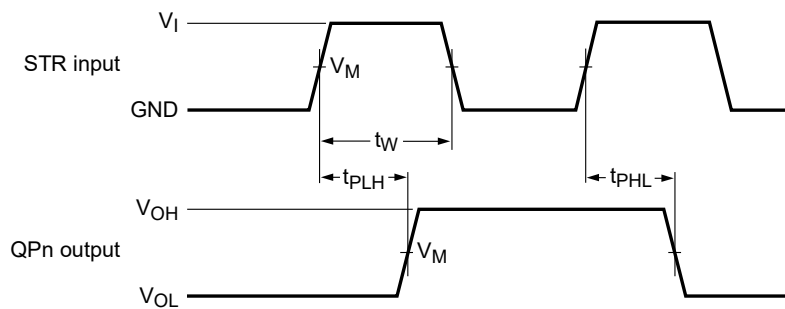


Figure 7. Strobe to output propagation delays, and strobe pulse width, setup and hold times

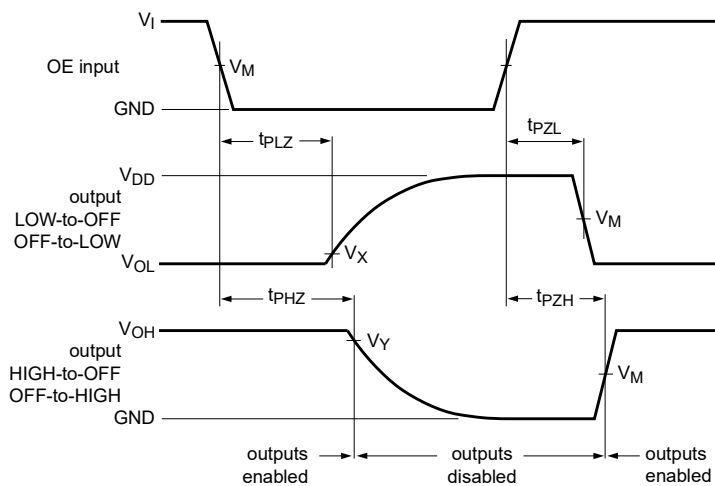


Figure 8. 3-state output enable and disable times for OE input

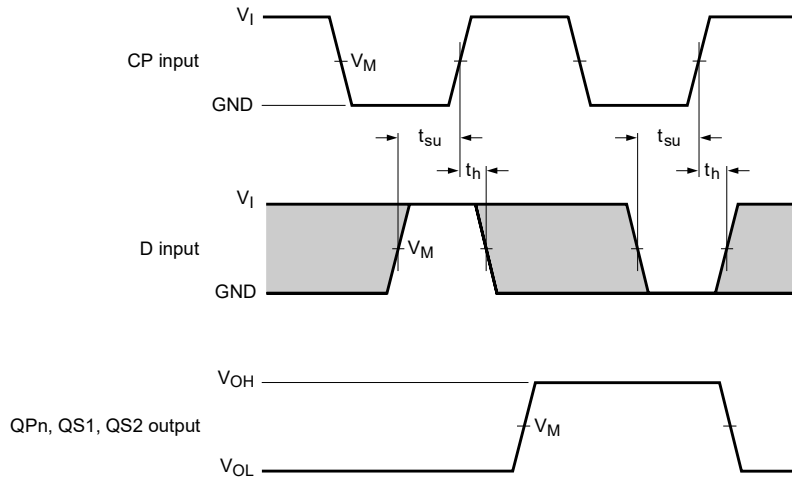


Figure 9. Data input data setup and hold times

Measurement Points

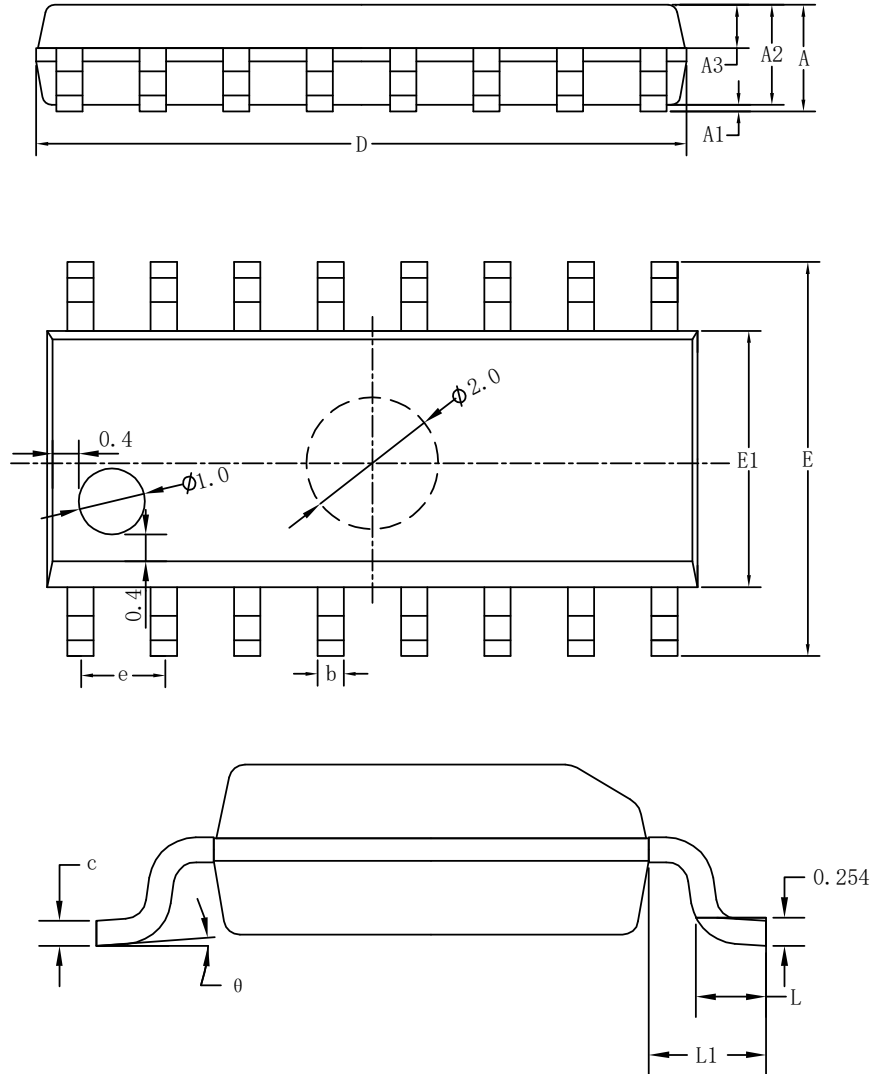
Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_x	V_y
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$	$0.1 \times V_{DD}$	$0.9 \times V_{DD}$

Test Data

Supply voltage	Input		Load		V_{EXT}		
V_{DD}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}
5V to 15V	V_{SS} or V_{DD}	$\leq 20ns$	50pF	1k Ω	open	V_{SS}	V_{DD}



Package Information
SOP-16(SOIC-16)



Symbol	Size	Dimensions In Millimeters			Symbol	Size	Dimensions In Inches		
		Min(mm)	Nom(mm)	Max(mm)			Min(in)	Nom(in)	Max(in)
A		1.500	1.600	1.700	A		0.059	0.063	0.067
A1		0.100	0.150	0.250	A1		0.004	0.006	0.010
A2		1.400	1.450	1.500	A2		0.055	0.057	0.059
A3		0.600	0.650	0.700	A3		0.024	0.026	0.028
b		0.300	0.400	0.500	b		0.012	0.016	0.020
c		0.150	0.200	0.250	c		0.006	0.008	0.010
D		9.800	9.900	10.00	D		0.386	0.390	0.394
E		5.800	6.000	6.200	E		0.228	0.236	0.244
E1		3.850	3.900	3.950	E1		0.152	0.154	0.156
e		1.27(BSC)			e		0.050(BSC)		
L		0.500	0.600	0.700	L		0.020	0.024	0.028
L1		1.05(BSC)			L1		0.041(BSC)		
theta		0°	4°	8°	theta		0°	4°	8°



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