4.5 V to 26.4 V, 33W Stereo, Inductor-Less, Digital Input, High Efficiency Class-D Audio Amplifier with SKTune Algorithm

Features

- **Integrates SKTune Algorithm**
  - Smart Protection (Anti-chip Voltage Limiter Thermal Limiter, Excursion Limiter and Auto Voltage Monitor)
  - Input Mixer, Output Crossbar
  - 2x15 Parametric Equalizers (EQ)
  - Dynamic Equalizer Enhancement (DEE)
  - Sound Field Expansion (SFE)
  - Multi-band Dynamic Range Control
  - Bass Booster
- **Output Power**
  - 2×33W@8Ω, 24V, THD+N<1% in BTL mode
  - 1×65W@4Ω, 24V, THD+N <1% in PBTL mode
- **Excellent Audio Performance**
  - THD+N≤0.02%@8Ω,1 W,1 kHz,PVDD = 12 V
  - SNR≥110dB@8Ω,1%,1 kHz,PVDD = 24 V, A-weighted
  - Noise Level < 34uVrms @LLM mode
  - Noise Level < 28uVrms @Low Noise Enable
- **High-efficiency Class-D Amplifier**
  - Power efficiency 90%, RDSon 110mΩ
  - Low quiescent current < 18 mA
  - Supports Low-Loss Mode
- **I2S/TDM interface**
  - I2S, Left-Justified and Right-Justified
  - Supports 1/2/4/6/8 Su7lots TDM
  - Supports 32k,44.1k,48k,88.2k,96k,192kHz Sample Rates
  - Data Width: 16, 20, 24, 32 Bits
- **I2C-bus control interface(1MHz)**
- **Extensive Pop-Click Suppression**
- **Volume control (from -96dB to 0dB)**
- **Multiple switching frequencies**
  - AM/FM avoidance
  - Supports 384kHz、480kHz、576kHz、768kHz、960 kHz、1200kHz switching frequencies
- **Support Spread Spectrum to Enhance EMI Performance**
- **Power Supplies**
  - PVDD: 4.5V~26.4V
  - DVDD: 1.8V/3.3V
- **Integrated Self-Protection**
  - Over-Current Protection (OCP)
  - Over-Temperature Protection (OTP)
  - Over / Under-Voltage Lock-out (OVLO/UVLO)
  - DC-detect and short-circuit protection
- ETSSOP-28L Package

Applications

- TV, Desktop PC, Notebook PC
- Soundbar,Wired Speaker, Wireless Speaker, Smart Speaker with Voice Assistant
- Smart Home and IoT Appliances

General Description

The AW85806 is a high-efficiency, stereo digital class D audio amplifier with low power dissipation and sound enrichment.

The device employs a multiple switching frequency option and Spread Spectrum technology to enhance EMI performance, avoid AM/FM interferences. And it supports Multichip synchronization and channel phase shift.

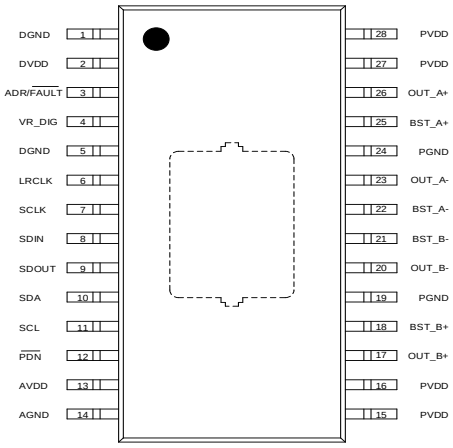
The AW85806 integrates SKTune algorithm that includes parametric audio path equalizer, dynamic range control, anti-clip voltage limiter and smart protection, etc. The SKTune algorithm maximizes speaker performance while maintaining safe working conditions.

The AW85806 supports Over-Current Protection, Over-Temperature Protection, DC Protection, Under-Voltage/Over-Voltage Protection, short-circuit Protection to protect the device.

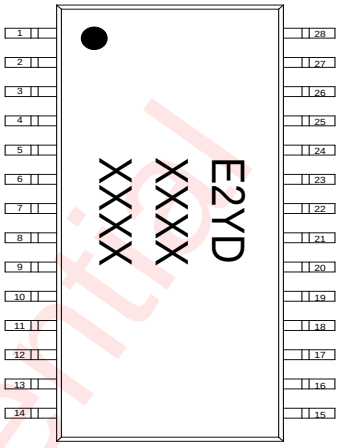
AW85806 is available in a ETSSOP-28L Package.

Pin Configuration and Top Mark

AW85806TSR
(Top View)



AW85806TSR Marking
(Top View)



E2YD—AW85806TSR
XXXX/XXXX—Production Tracing Code

Pin Description

Pin No	Pin Name	Description
1	DGND	Digital ground
2	DVDD	3.3V or 1.8V digital power supply
3	ADR/$\overline{\text{FAULT}}$	Different I2C device address can be set by selecting different pull up resistor to DVDD, after power up, ADR/$\overline{\text{FAULT}}$ can be redefine as $\overline{\text{FAULT}}$.
4	VR_DIG	Internally regulated 1.6V digital supply voltage.
5	DGND	Digital ground
6	LRCLK	I^2S word select input / TDM frame sync signal
7	SCLK	I^2S/TDM bit clock input
8	SDIN	I^2S/TDM data input
9	SDOUT	I^2S/TDM data out
10	SDA	I2C serial control data interface input/output
11	SCL	I2C serial control clock input
12	$\overline{\text{PDN}}$	Power Down, active-low. $\overline{\text{PDN}}$ place the amplifier in Shutdown, turn off all internal regulators. Low, Power Down Device; High, Enable Device
13	AVDD	Internally regulated 5V analog supply voltage.
14	AGND	Analog ground
15	PVDD	PVDD voltage input
16	PVDD	PVDD voltage input
17	OUT_B+	Positive pin for differential speaker amplifier output B+

18	BST_B+	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
19	PGND	Ground reference for power device circuitry.
20	OUT_B-	Negative pin for differential speaker amplifier output B-
21	BST_B-	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-
22	BST_A-	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-
23	OUT_A-	Negative pin for differential speaker amplifier output A-
24	PGND	Ground reference for power device circuitry.
25	BST_A+	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
26	OUT_A+	Positive pin for differential speaker amplifier output A+
27	PVDD	PVDD voltage input
28	PVDD	PVDD voltage input

Functional Block Diagram

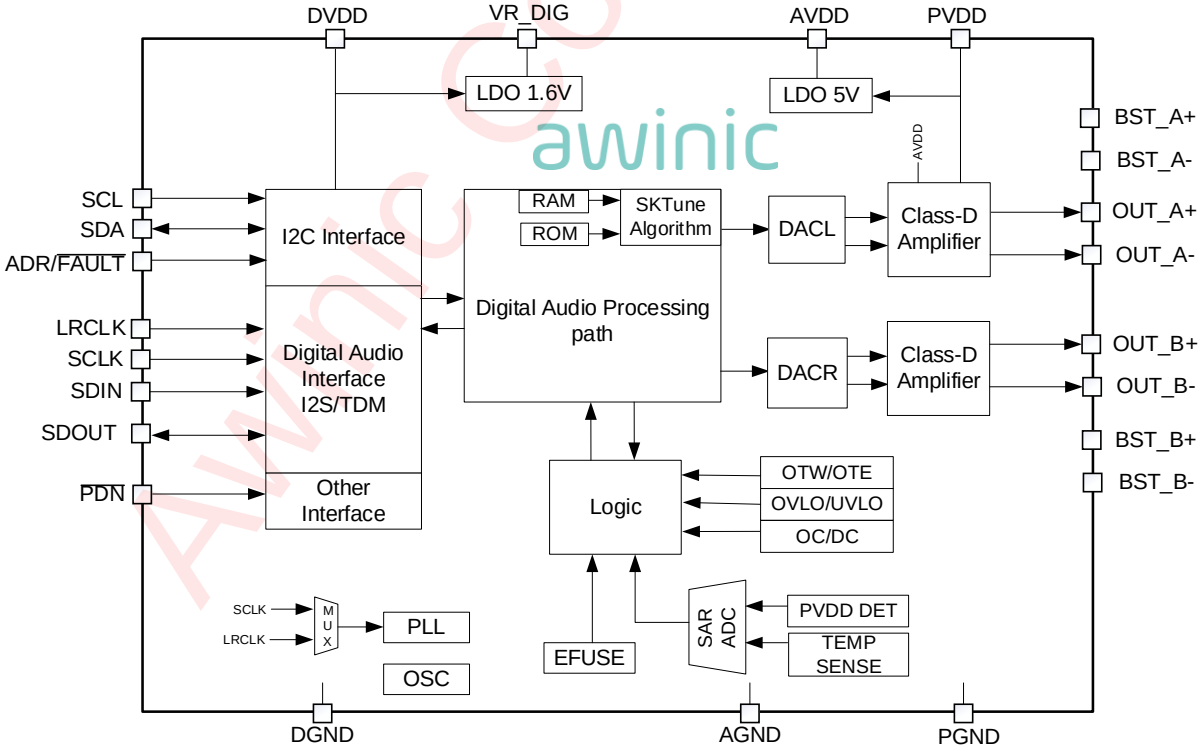


Figure 1 AW85806 Functional Diagram

Typical Application Circuit

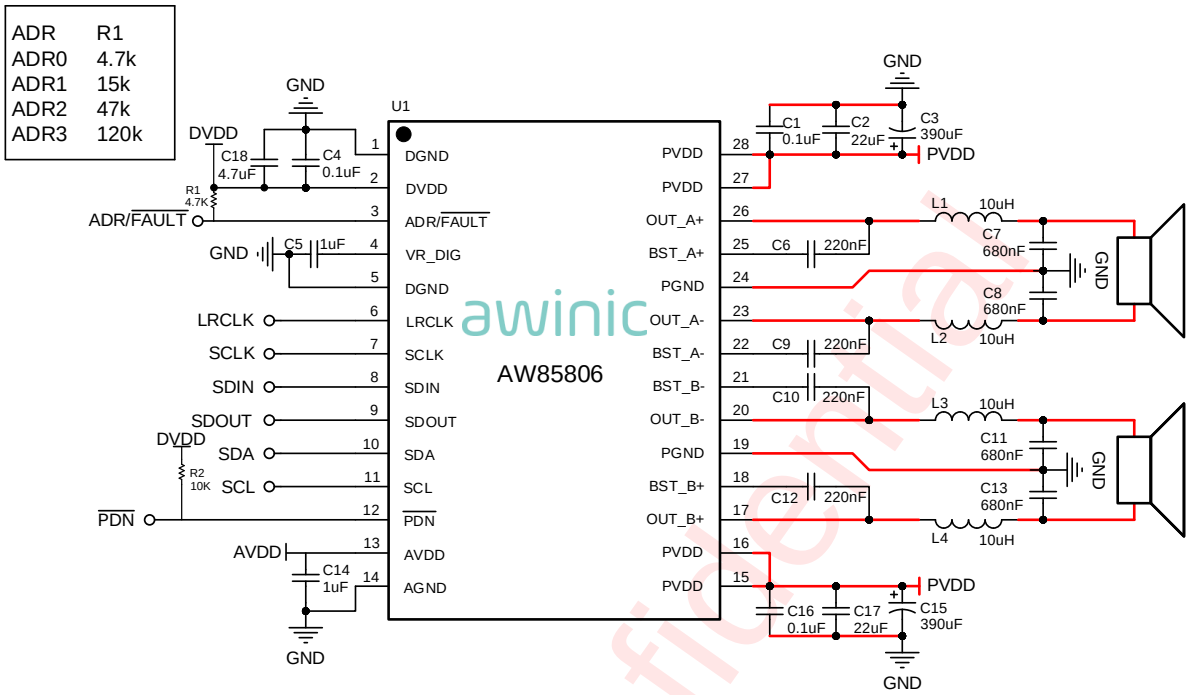


Figure 2 AW85806 BTL Application Circuit

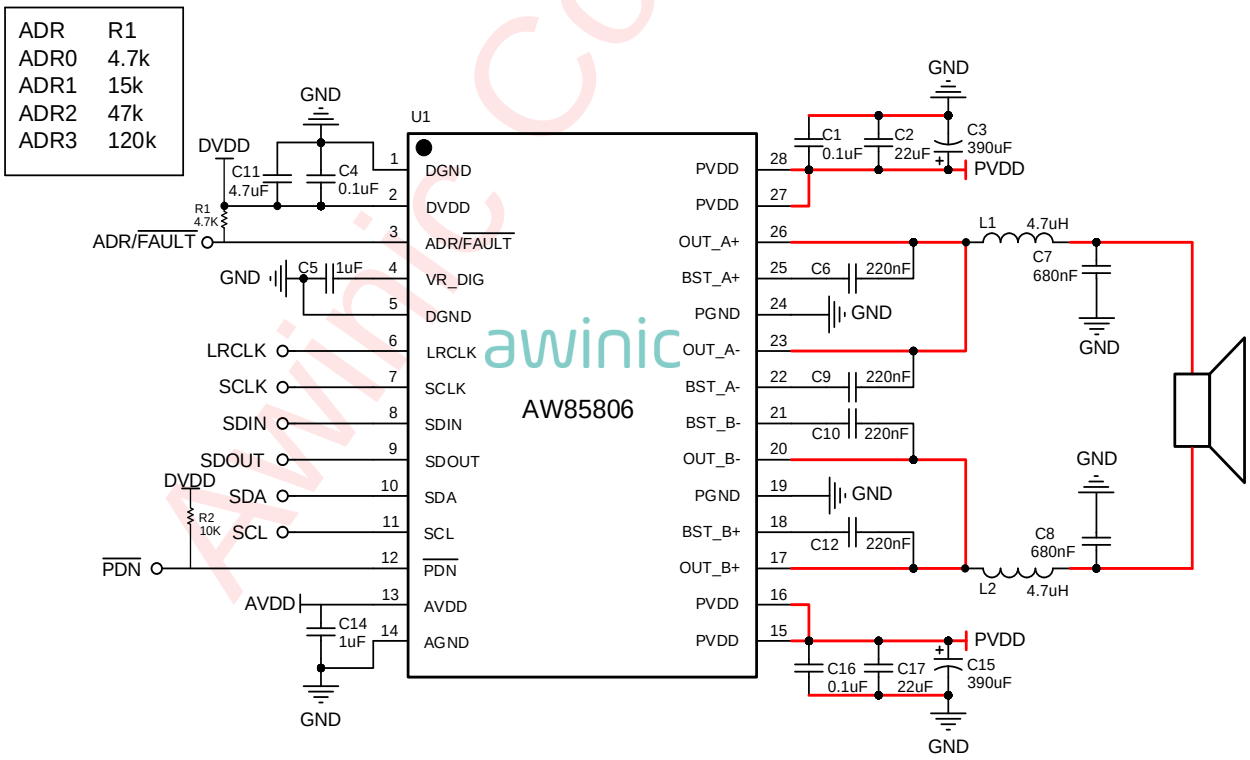


Figure 3 AW85806 PBTL Application Circuit

Notes:
1. Thermal pad at the bottom of the chip must be grounded
2. Traces carry high current are marked in red in the above figure

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW85806TSR	-40℃～85℃	ETSSOP-28L	E2YD	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings (NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{PVDD}		-0.3V to 30V
Digital voltage range V_{DVDD}		-0.3V to 3.9V
Input voltage range	DVDD referenced digital inputs (NOTE 2)	-0.5V to V_{DVDD}+0.5V
Output voltage range	Voltage at speaker output pins	-0.3V to 32V
Junction-to-ambient thermal resistance θ_{JA}		27.72°C /W
Junction-to-board thermal resistance θ_{JB}		1.09°C /W
Junction-to-case thermal resistance θ_{JC}		26.81°C /W
Junction-to-top characterization parameter ψ_{JT}		2.47°C /W
Junction-to-board characterization parameter ψ_{JB}		1.12°C /W
Ambient Temperature Range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		165°C
Storage temperature T_{STG}		-40°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD Rating (NOTE 3)		
HBM (human body model)		±2kV
CDM (charged-device model)		±1.5kV
Latch-Up		
Test Condition：JESD78F		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: DVDD referenced digital pins include: ADR, LRCLK, SCLK, SDIN, SCL, SDA, $\overline{\text{PDN}}$

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{PVDD}	Input voltage	4.5		26.4	V
V_{DVDD}	Input voltage	1.62		3.63	V
R_L	BTL Mode Minimum load resistance	3.2	4		Ω
	PBTL Mode Minimum load resistance	1.6	2		Ω
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition	1	4.7		μH

Electrical Characteristics

Characteristics

Test condition: T_A=25°C, PVDD=14.4V, DVDD=3.3V, R_L=4Ω, f=1kHz (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Digital Logical Interface						
V_{IH}	Logic input high level	BCLK,LRCLK,SDIN,SCL,SDA PIN	0.7 x V_{DVDD}			V
V_{IL}	Logic input low level				0.3 x V_{DVDD}	V
V_{OH}	Logic output high level	I_{OH} = 4 mA	80%			V_{DVDD}
V_{OL}	Logic output low level	I_{OH} = –4 mA			20%	V_{DVDD}
Speaker Amplifier (All Output Configurations)						
I_{DVDD}	Digital supply current	PDN = High, DVDD = 3.3 V, Play mode, SKTune Algorithm activated, running full enhancement (I2S signal input 0dB)		18.2		mA
		PDN = High, DVDD = 3.3 V, Play mode, SKTune Algorithm activated (I2S signal input 0)		5.9		mA
		PDN = High, DVDD = 3.3 V, Sleep mode		5.2		mA
		PDN = High, DVDD = 3.3 V, Deep Sleep mode		0.5		mA
		PDN = Low, DVDD = 3.3 V, Shutdown mode			1	μA
I_{PVDD}	PVDD supply current	PDN = High, PVDD = 13.5 V, No Load, LC filter = 10 μH + 0.68 μF, F_{SW} = 384 kHz, LLM Modulation, Play Mode		22		mA
		PDN = High, PVDD = 13.5 V, No Load, LC filter = 10 μH + 0.68 μF, F_{SW} = 384 kHz, Output Hiz Mode		9.7		mA
		PDN = High, PVDD = 13.5 V, No Load, LC filter = 10 μH + 0.68 μF, F_{SW} = 384 kHz, Sleep Mode		1.7		mA
		PDN = High, PVDD = 13.5 V, No Load, LC filter = 10 μH + 0.68 μF, F_{SW} = 384 kHz, Deep Sleep Mode		10		μA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		PDN = Low, PVDD = 13.5 V, No Load, LC filter = 10 μH + 0.68 μF, F_{SW} = 384 kHz, Shutdown Mode		10		μA
A_V	Programmable Gain	Value represents the "peak voltage" (disregarding clipping due to lower PVDD). Measured at 0 dB input (1FS)	4.95		29.5	V
$\triangle A_V$	Amplifier gain error	Gain = 29.5 V_P		±0.5		dB
F_{SW}	PWM Switching frequency			384		kHz
				768		kHz
R_{dson}	Drain-to-source on resistance of the individual output MOSFETs	FET+ Metallization		110		mΩ
OCP	Over-Current protection current	Any short to supply, ground, or other channels		7.5		A
OVP	Over-voltage protection voltage			28		V
UVP	Under-voltage protection voltage			4.3		V
OT_{SD}	Over temperature protection threshold			160		°C
OT_{SDR}	Over temperature protection recovery threshold			150		°C
OTW_{THRES}	Over temperature warning level 1			110		°C
	Over temperature warning level 2			120		°C
	Over temperature warning level 3			130		°C
	Over temperature warning level 4			140		°C
Speaker Amplifier (Stereo BTL)						
$\lvert V_{OS}\rvert$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.5 V_P gain, V_{PVDD} = 18 V	-3		3	mV
PO	Speaker Output Power (Per Channel)	V_{PVDD} = 14.4 V, ANA_GAIN = 29.5 V_P, R_L = 4 Ω, f = 1 kHz THD+N = 10%		26		W

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		V_{PVDD} = 14.4 V, ANA_GAIN = 29.5 V_P, R_L = 4 Ω, f = 1 kHz THD+N = 1%		21		W
		V_{PVDD} = 14.4 V, ANA_GAIN = 29.5 V_P, R_L = 6 Ω, f = 1 kHz THD+N = 10%		19		W
		V_{PVDD} = 14.4 V, ANA_GAIN = 29.5 V_P, R_L = 6 Ω, f = 1 kHz THD+N = 1%		15.5		W
		V_{PVDD} = 24 V, ANA_GAIN = 29.5 V_P, R_L = 8 Ω, f= 1 kHz THD+N = 10% (Continuous Output Power)		40		W
		V_{PVDD} = 24 V, ANA_GAIN = 29.5 V_P, R_L = 8 Ω, f= 1 kHz THD+N = 1% (Continuous Output Power)		33		W
THD+N	Total harmonic distortion and Noise (PO = 1 W, f = 1 kHz, R_L = 4 Ω)	V_{PVDD} = 12 V, ANA_GAIN = 20.9 V_P LC-filter		0.02%		
		V_{PVDD} = 24 V, ANA_GAIN = 29.5 V_P, LC-filter		0.02%		
E_N	Idle channel noise (A- weighted)	V_{PVDD} <16 V, LC-filter, R_L = 4 Ω, LOW NOISE Enable, LLM Modulation		28		μV
		V_{PVDD} = 12 V, LC-filter, R_L = 4 Ω, LLM Modulation		34		
		V_{PVDD} = 12 V, LC-filter, R_L = 4 Ω, BD Modulation		40		
		V_{PVDD} = 24 V, LC-filter, R_L = 4 Ω, LLM Modulation		35		
		V_{PVDD} = 24 V, LC-filter, R_L = 4 Ω, BD Modulation		41		
DNR	Dynamic range	A-Weighted, -60 dBFS method. PVDD = 24 V, ANA_GAIN = 29.5 Vp		113		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, PVDD = 24 V		113		dB
		A-Weighted, referenced to 1% THD+N Output Level, PVDD = 14.4 V		109		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 Vrms, PVDD = 14.4 V, input audio signal = digital zero		80		dB
CROSSTALK	Cross-talk (worst case between left-to-	f = 1 KHz		100		dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	right and right-to-left coupling)					
Speaker Amplifier (Mono PBTL)						
PO	Output Power	V_{PVDD} = 19 V, ANA_GAIN = 29.5 V_P, R_L = 2 Ω, f = 1kHz, THD+N = 1% (Instantaneous Output Power)		60		W
		V_{PVDD} = 19 V, ANA_GAIN = 29.5 V_P, R_L = 2 Ω, f = 1kHz, THD+N = 10% (Instantaneous Output Power)		87		W
		V_{PVDD} = 22 V, ANA_GAIN = 29.5 V_P, R_L = 4 Ω, f = 1kHz, THD+N = 1%		55		W
		V_{PVDD} = 22 V, ANA_GAIN = 29.5 V_P, R_L = 4 Ω, f = 1kHz, THD+N = 10%		67		W
		V_{PVDD} = 24 V, ANA_GAIN = 29.5 V_P, R_L = 4 Ω, f = 1kHz, THD+N = 1% (Continuous Output Power)		65		W
		V_{PVDD} = 24 V, ANA_GAIN = 29.5 V_P, R_L = 4 Ω, f = 1kHz, THD+N = 10% (Continuous Output Power)		80		W
THD+N	Total harmonic distortion and Noise (PO = 1 W, f = 1 kHz)	V_{PVDD} = 19 V, ANA_GAIN = 20.9 V_P, LC-filter R_L = 2 Ω)		0.02%		
		V_{PVDD} = 24 V, ANA_GAIN = 29.5 V_P, LC-filter R_L = 4 Ω)		0.02%		
DNR	Dynamic range	A-Weighted, -60 dBFS method, PVDD=19V		111		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, PVDD = 19 V		111		dB
		A-Weighted, referenced to 1% THD+N Output Level, PVDD = 24 V		113		dB

I2C INTERFACE TIMING

Parameter			Fast mode			Fast mode Plus			UNIT
No.	Sym	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.26			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			0.26			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	The Bus idle time START state to STOP state	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05			μs
11	$t_{HD:DAT}$	SDA hold time	10			10			ns

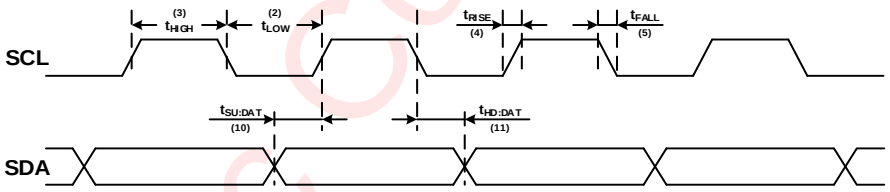


Figure 4 SCL and SDA timing relationships in the data transmission process

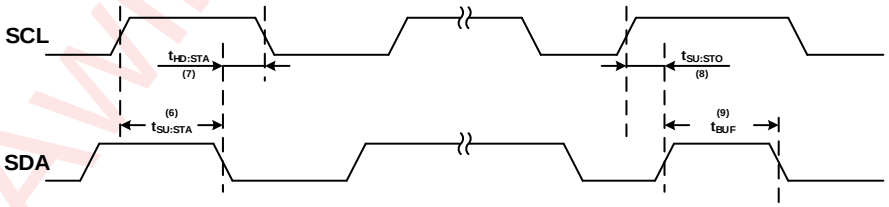


Figure 5 The timing relationship between START and STOP state

DIGITAL AUDIO INTERFACE TIMING

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin LRCLK	32		192	kHz
f_{bck}	Bit clock frequency, on pin SCLK	16*fs		24.576M (NOTE)	Hz
t_{su}	LRCLK, SDIN Setup time to SCLK	10			ns
t_h	LRCLK, SDIN hold time to SCLK	10			ns
t_d	SDOUT output delay time to SCLK			40	ns

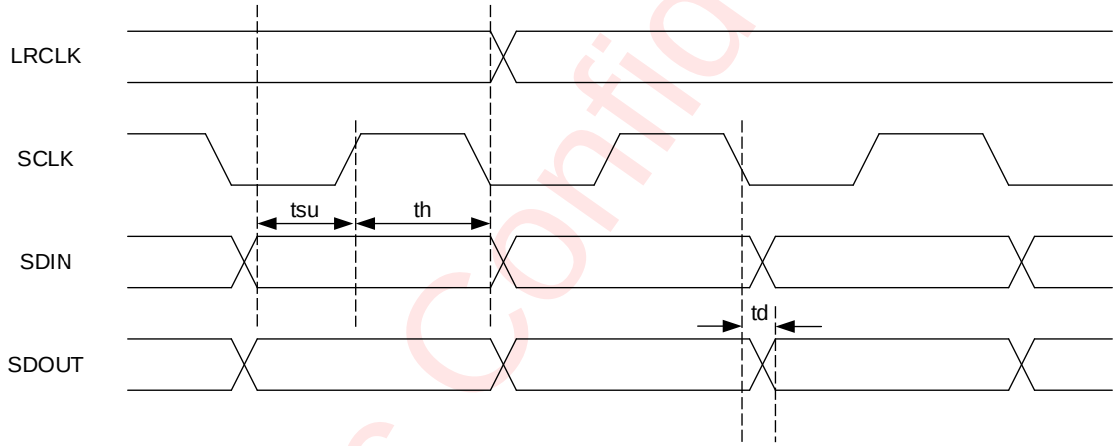


Figure 6 Digital Audio Interface Timing

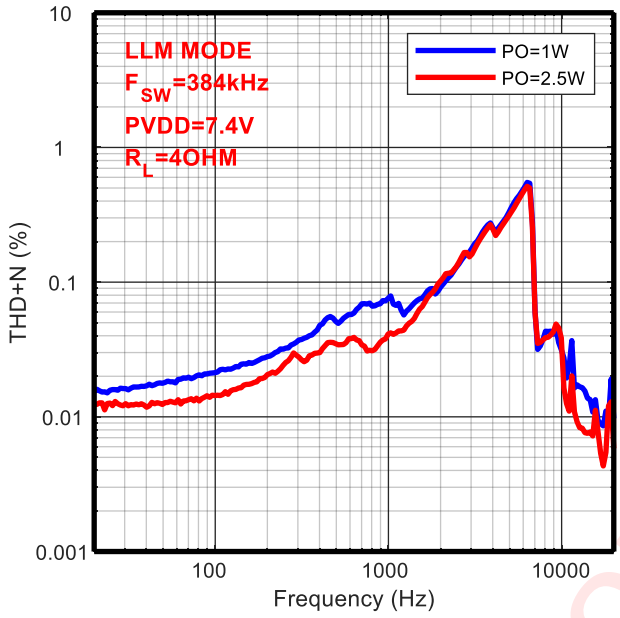
NOTES: The digital audio interface support up to 16 slots（32-bit） at a 32/44.1/48 kHz sample rate 8 slots（32-bit）at a 88.2/96 kHz and 4slots (32-bit) at a 192kHz sample rate

Typical Characteristics Curves

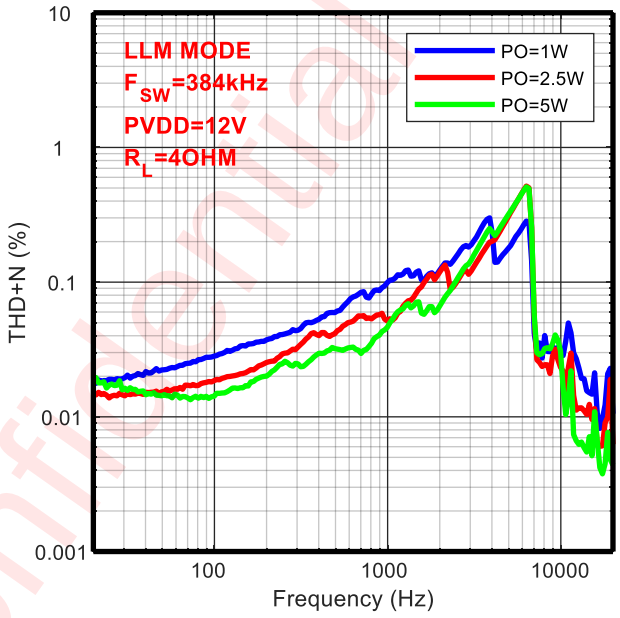
TA=25°C for typical values (unless otherwise noted).

BRIDGE TIED LOAD (BTL) CONFIGURATION CURVES WITH LLM MODULATION

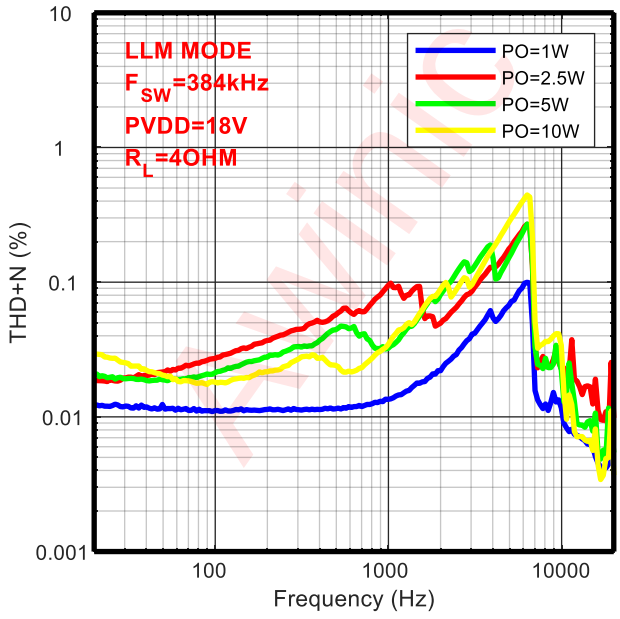
THD+N VS. FREQUENCY-BTL



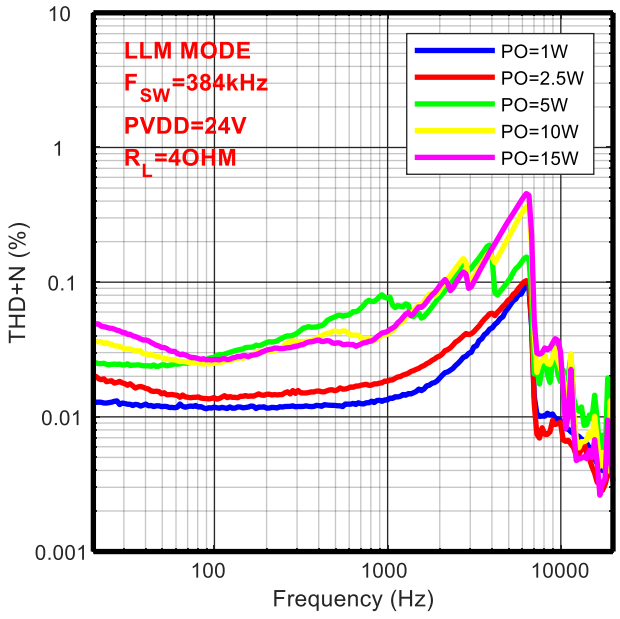
THD+N VS. FREQUENCY-BTL



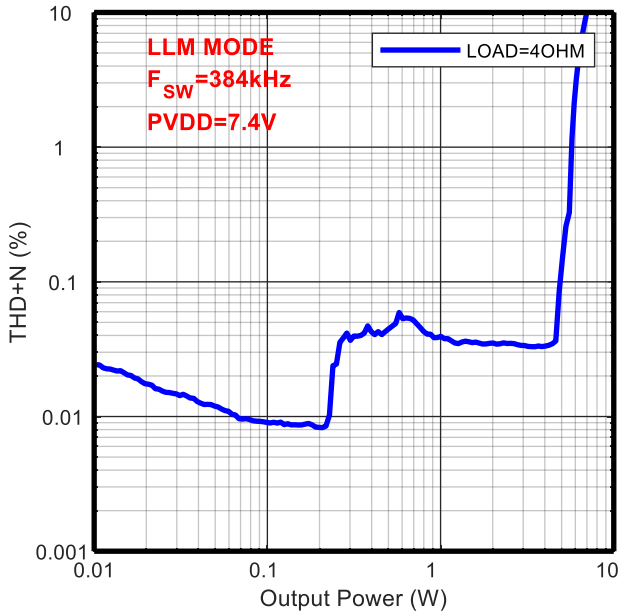
THD+N VS. FREQUENCY-BTL



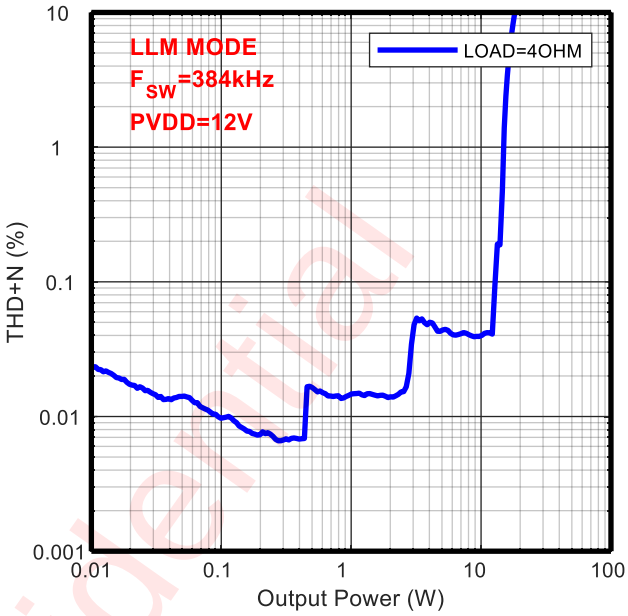
THD+N VS. FREQUENCY-BTL



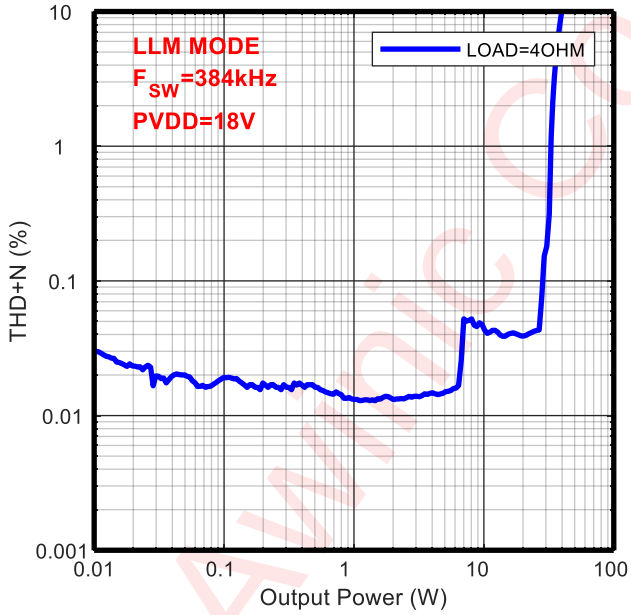
THD+N VS. OUTPUT POWER -BTL



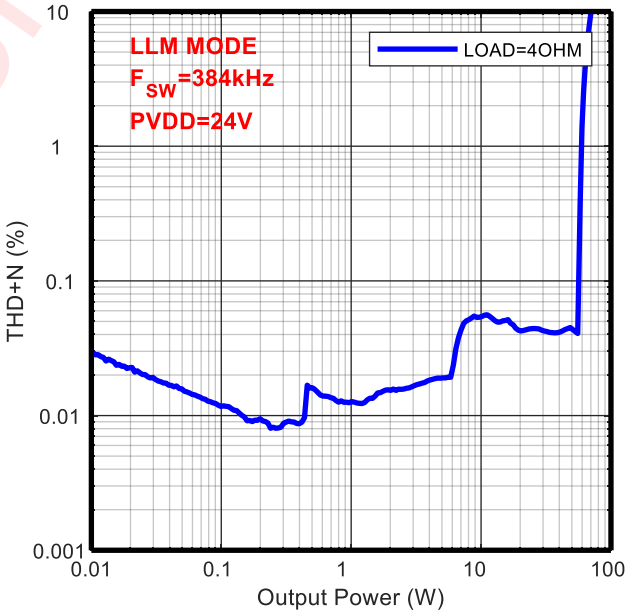
THD+N VS. OUTPUT POWER -BTL



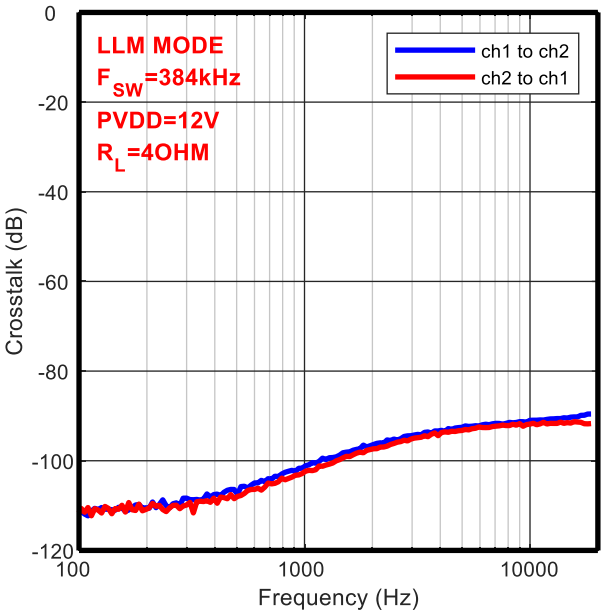
THD+N VS. OUTPUT POWER -BTL



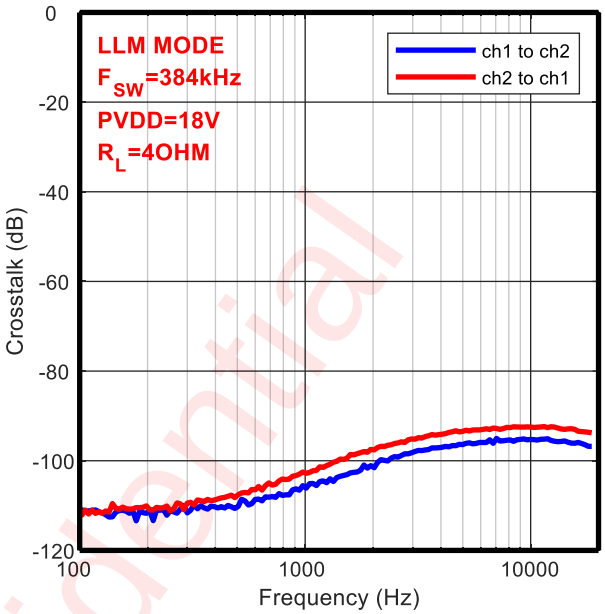
THD+N VS. OUTPUT POWER -BTL



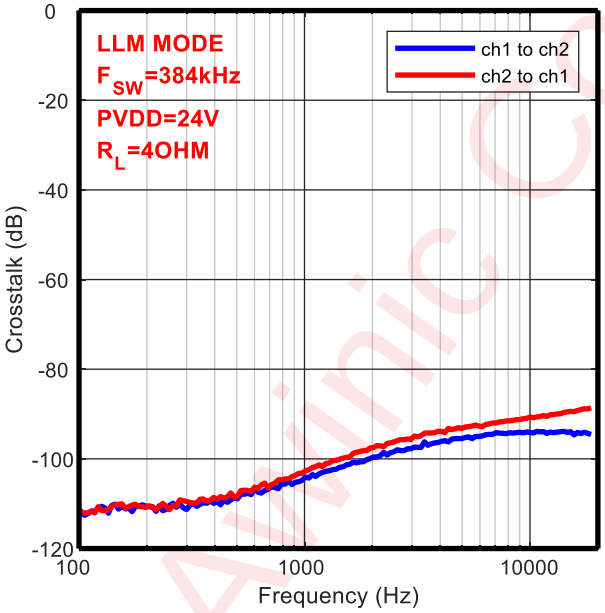
CROSSTALK -BTL



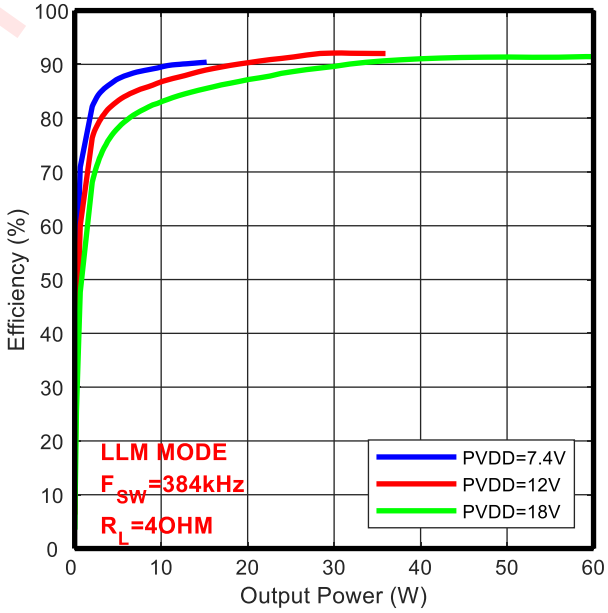
CROSSTALK -BTL



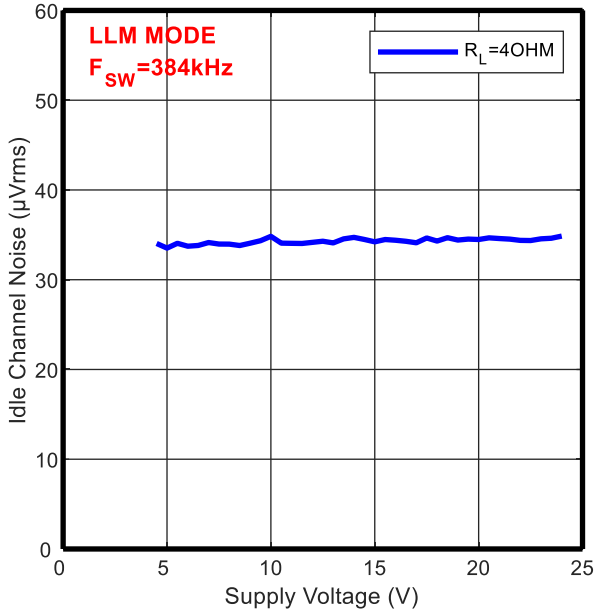
CROSSTALK -BTL



Efficiency vs Output Power -BTL

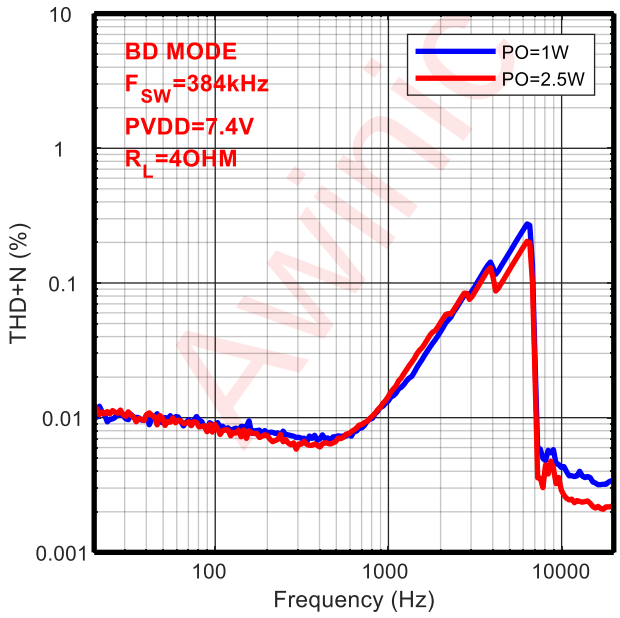


Idle Channel Noise vs Supply Voltage -BTL

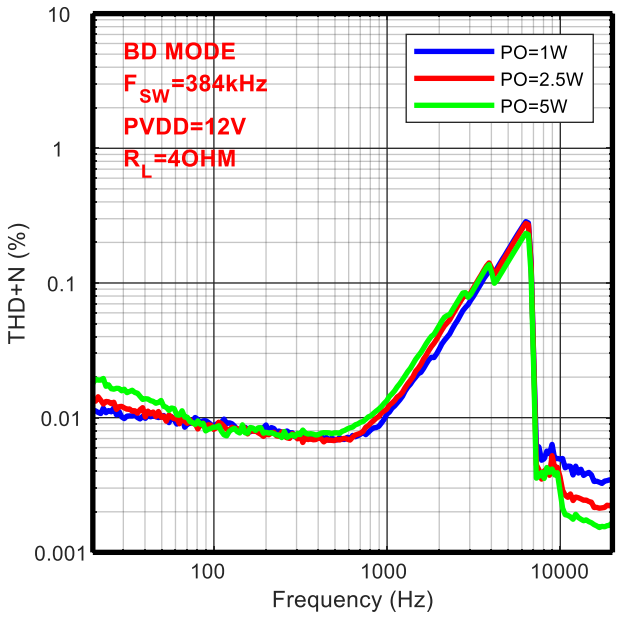


BRIDGE TIED LOAD (BTL) CONFIGURATION CURVES WITH BD MODULATION

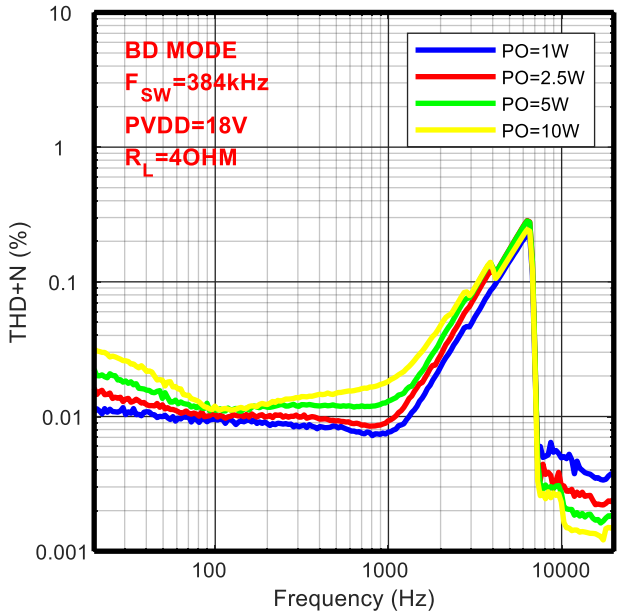
THD+N VS. FREQUENCY-BTL



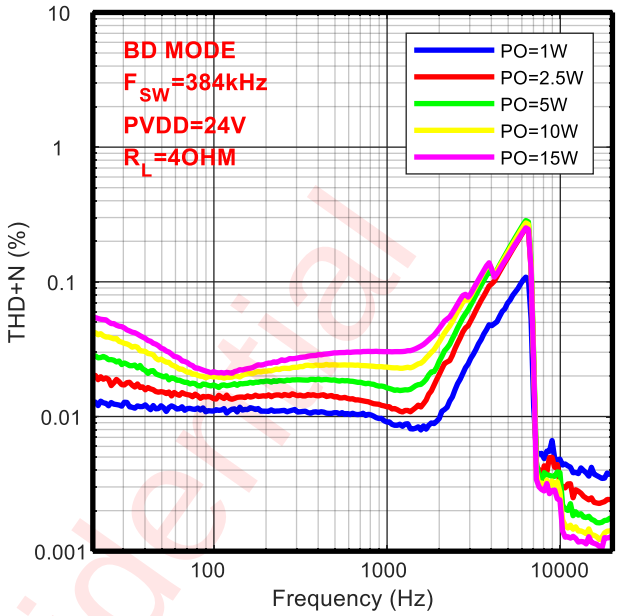
THD+N VS. FREQUENCY-BTL



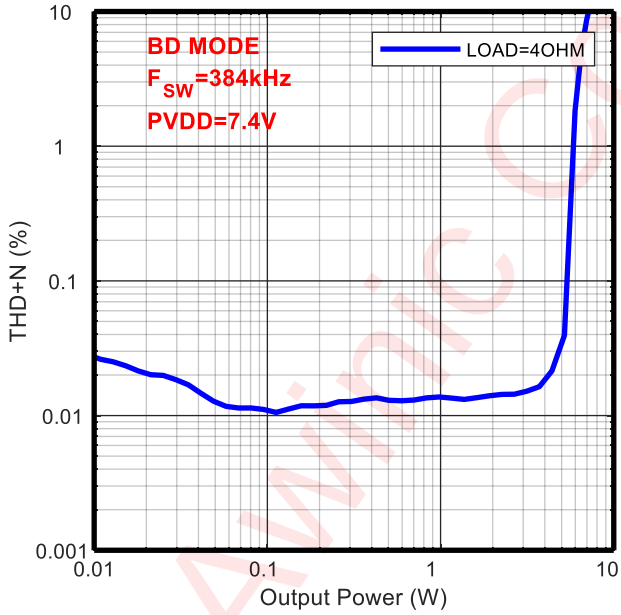
THD+N VS. FREQUENCY-BTL



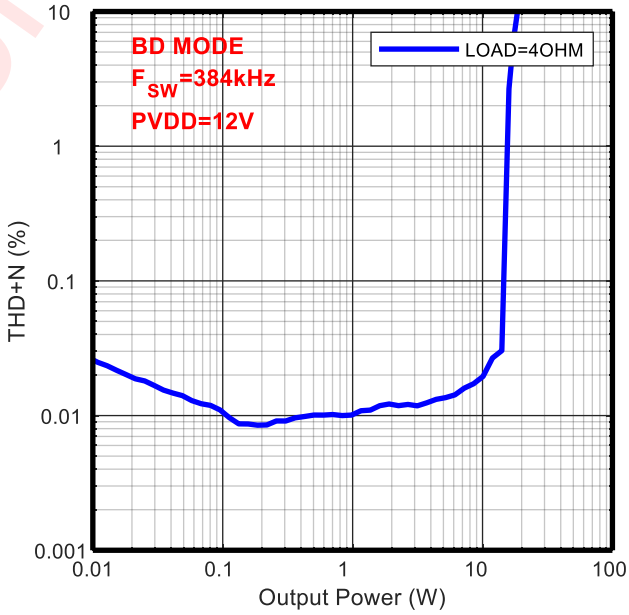
THD+N VS. FREQUENCY-BTL



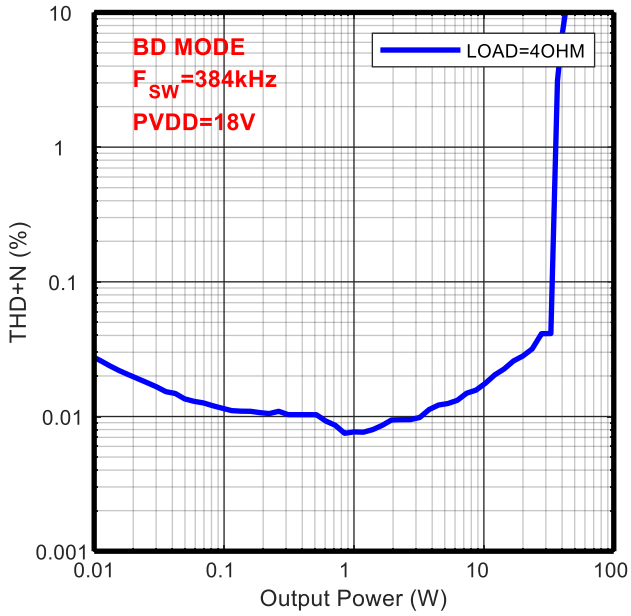
THD+N VS. OUTPUT POWER -BTL



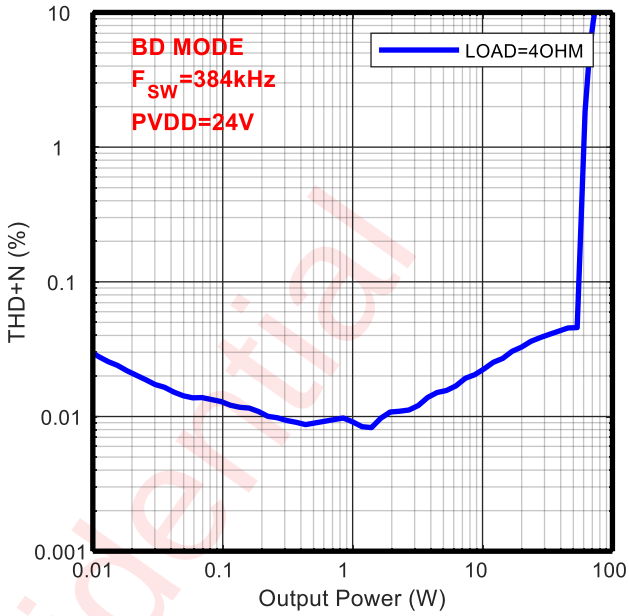
THD+N VS. OUTPUT POWER -BTL



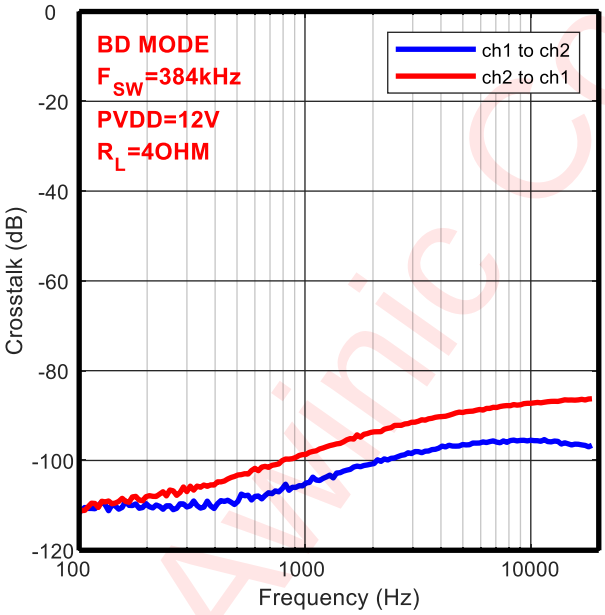
THD+N VS. OUTPUT POWER -BTL



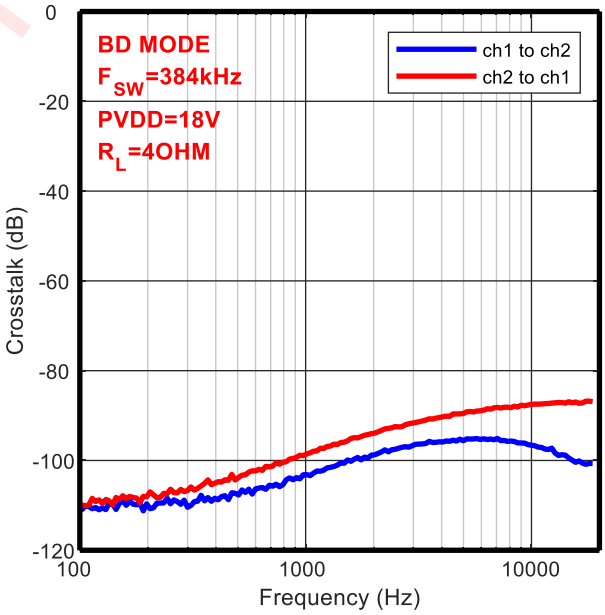
THD+N VS. OUTPUT POWER -BTL



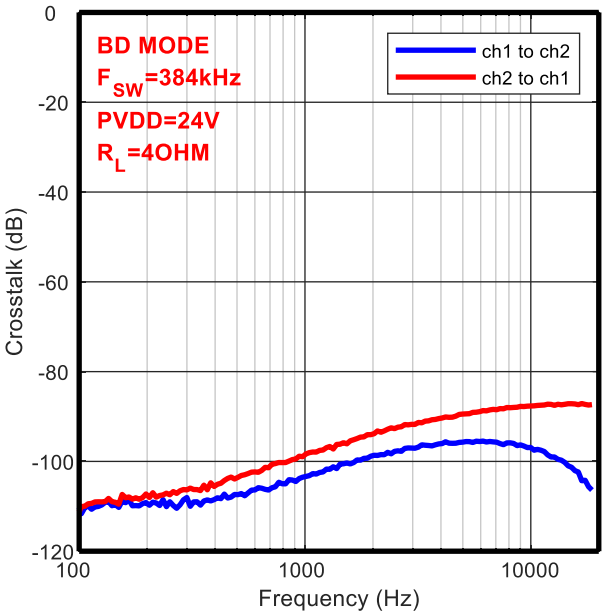
CROSSTALK -BTL



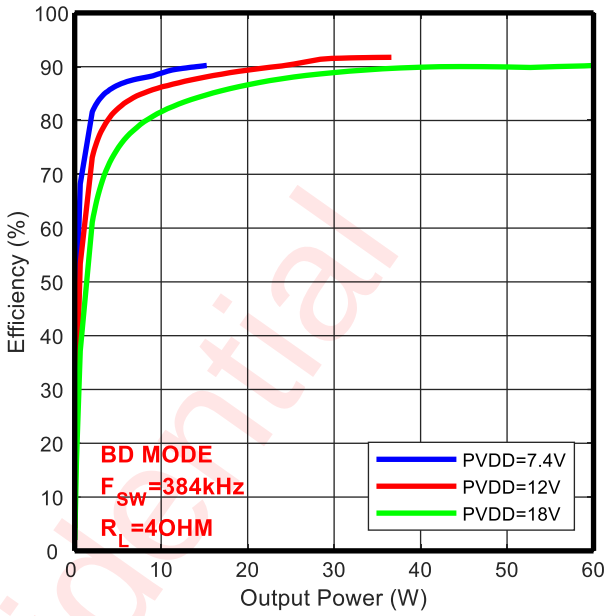
CROSSTALK -BTL



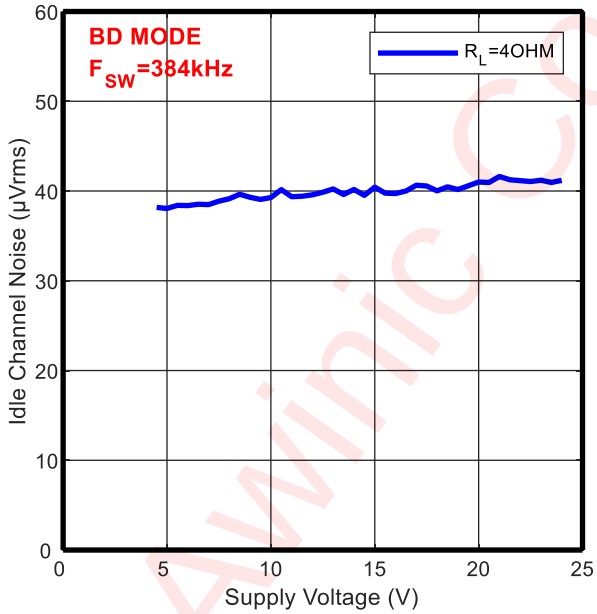
CROSSTALK -BTL



Efficiency vs Output Power -BTL

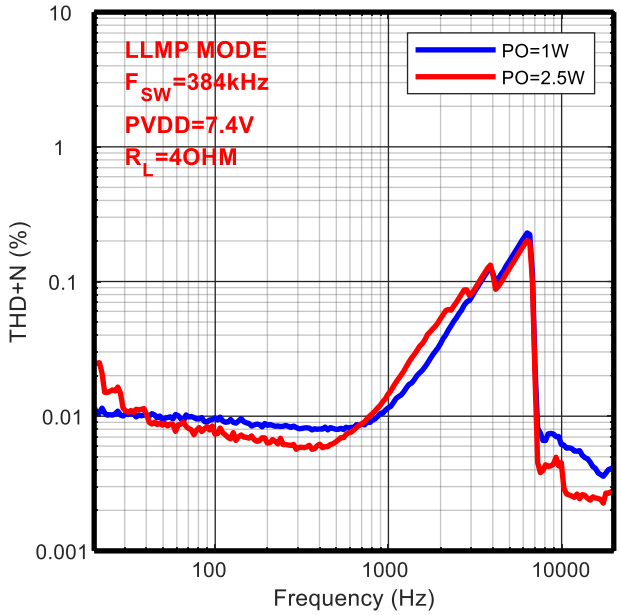


Idle Channel Noise vs Supply Voltage -BTL

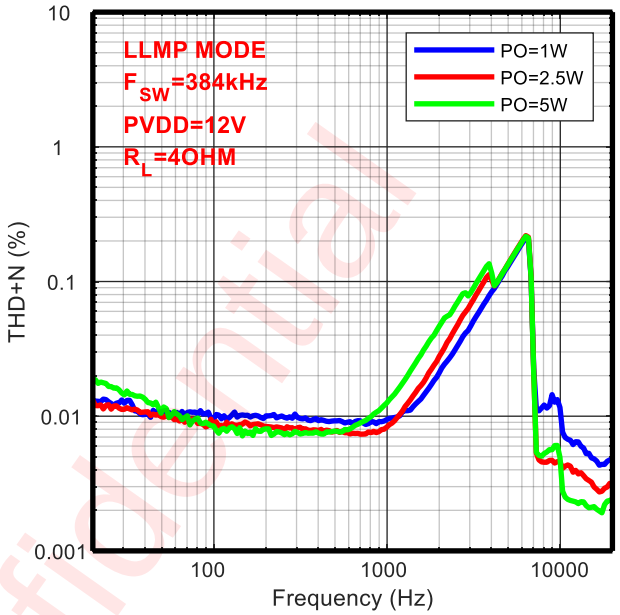


BRIDGE TIED LOAD (BTL) CONFIGURATION CURVES WITH LLMP MODULATION

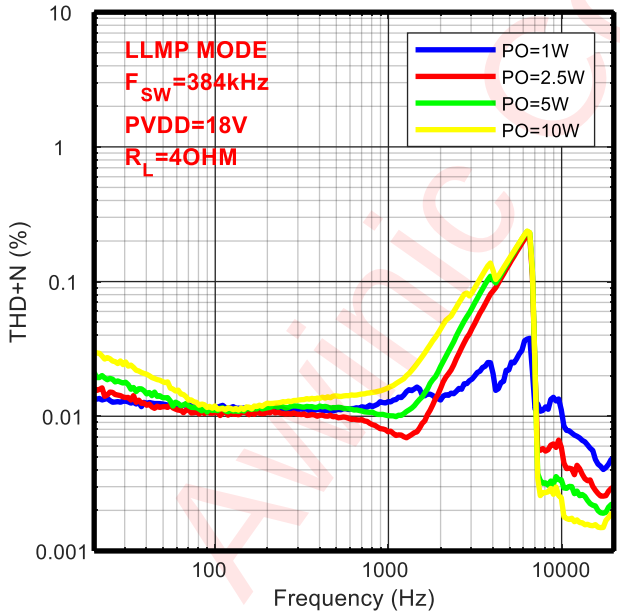
THD+N VS. FREQUENCY-BTL



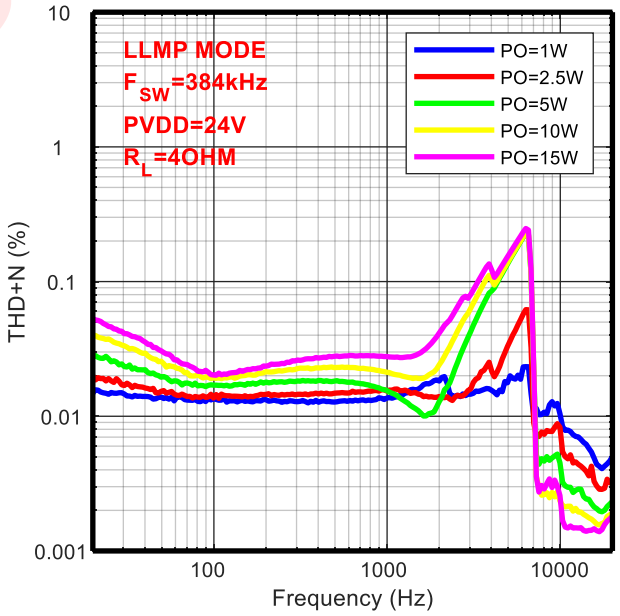
THD+N VS. FREQUENCY-BTL



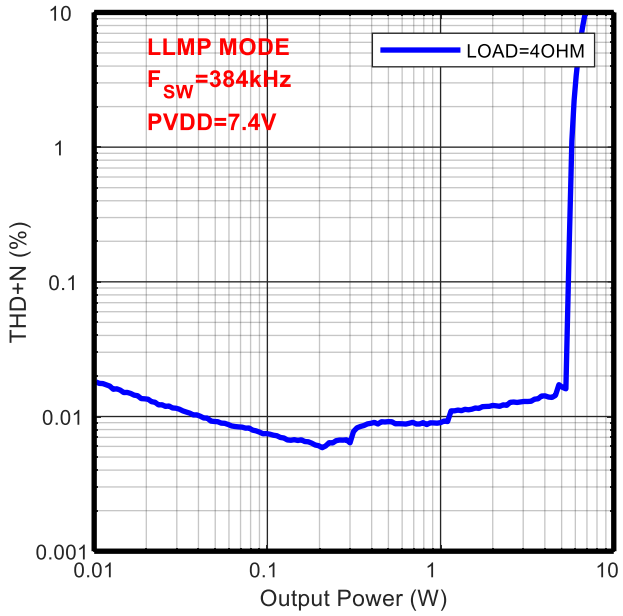
THD+N VS. FREQUENCY-BTL



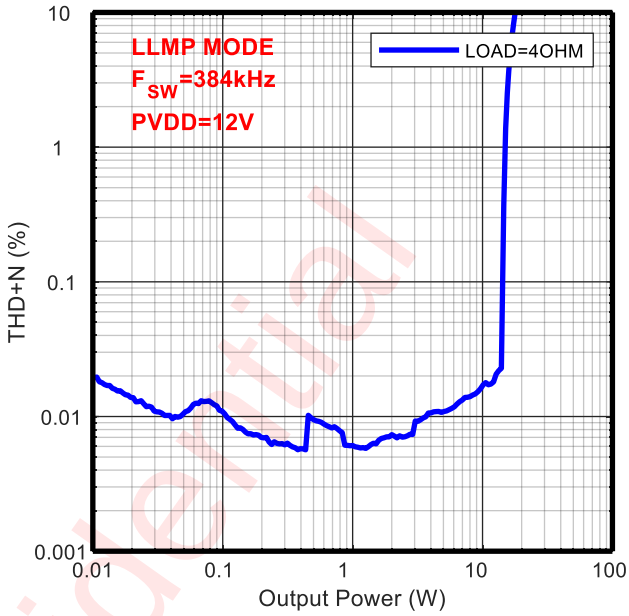
THD+N VS. FREQUENCY-BTL



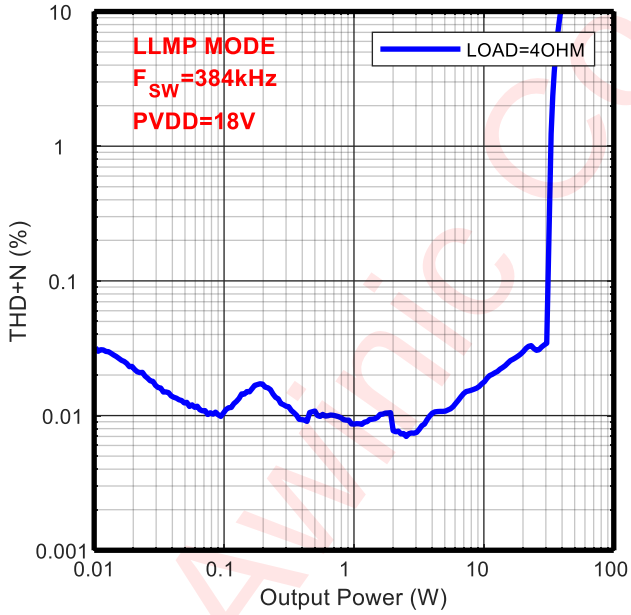
THD+N VS. OUTPUT POWER -BTL



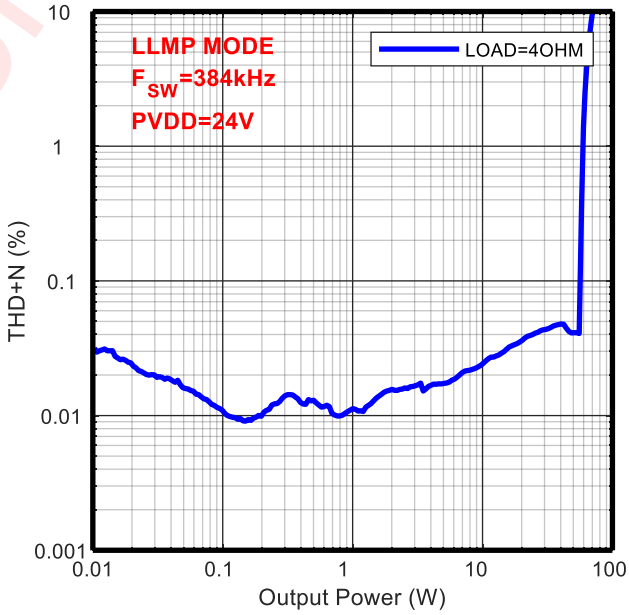
THD+N VS. OUTPUT POWER -BTL



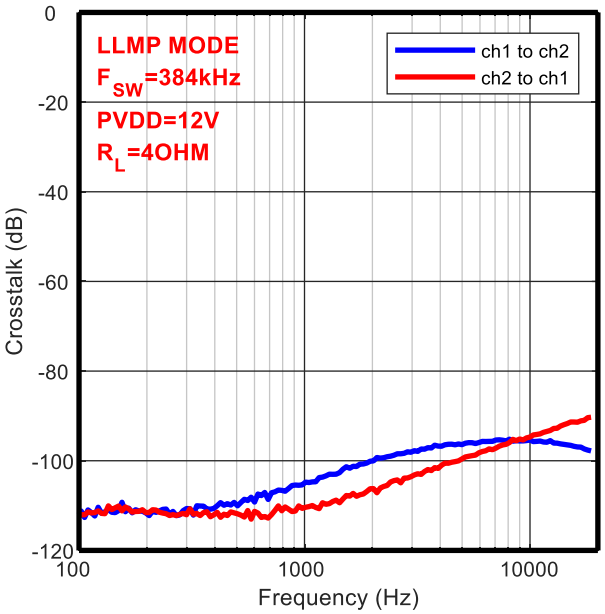
THD+N VS. OUTPUT POWER -BTL



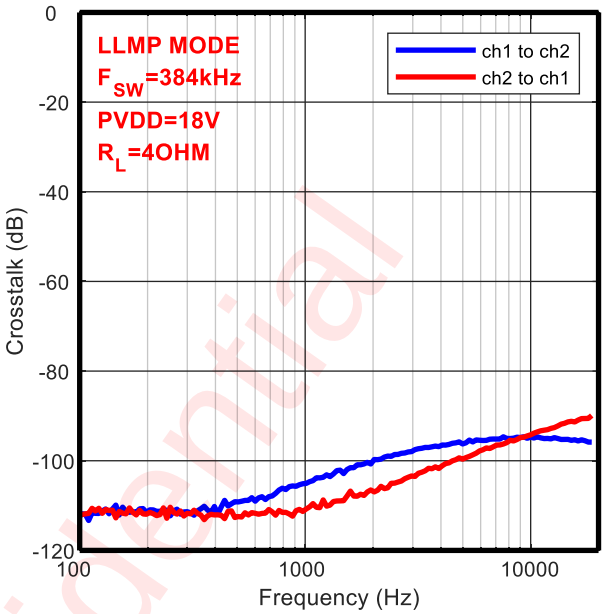
THD+N VS. OUTPUT POWER -BTL



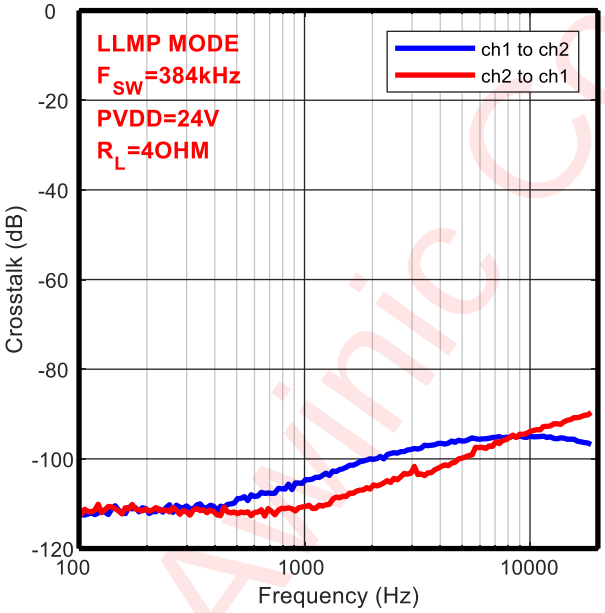
CROSSTALK -BTL



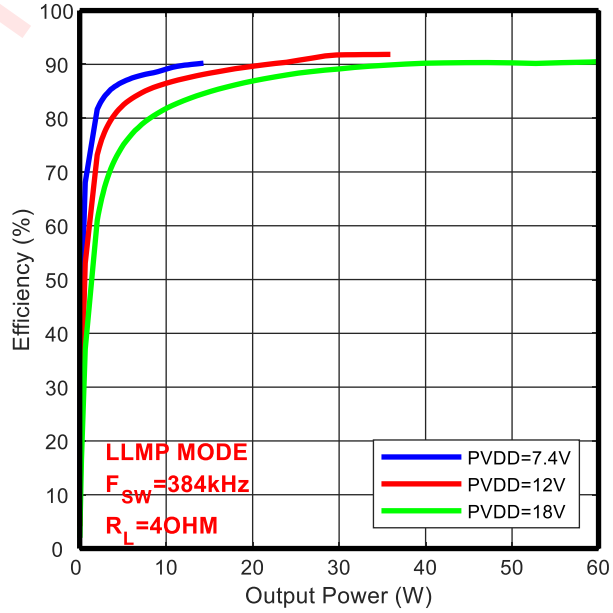
CROSSTALK -BTL



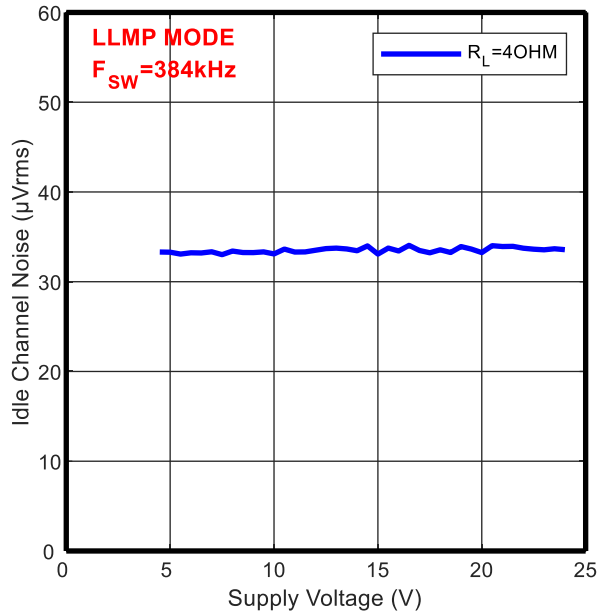
CROSSTALK -BTL



Efficiency vs Output Power -BTL

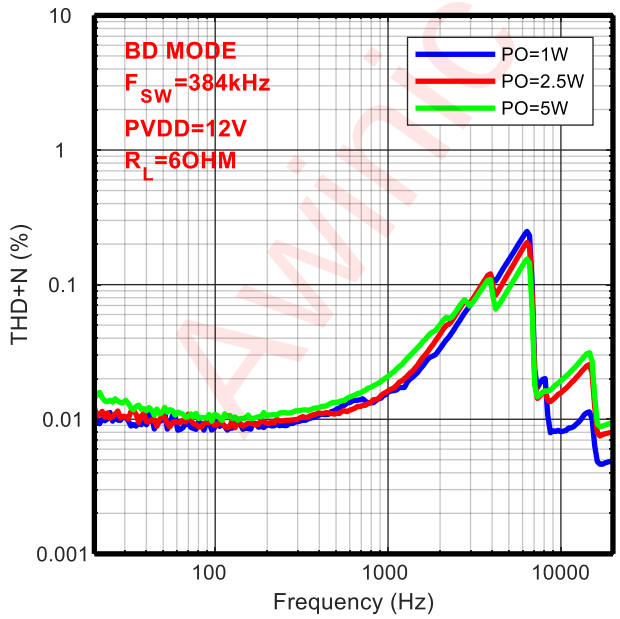


Idle Channel Noise vs Supply Voltage -BTL

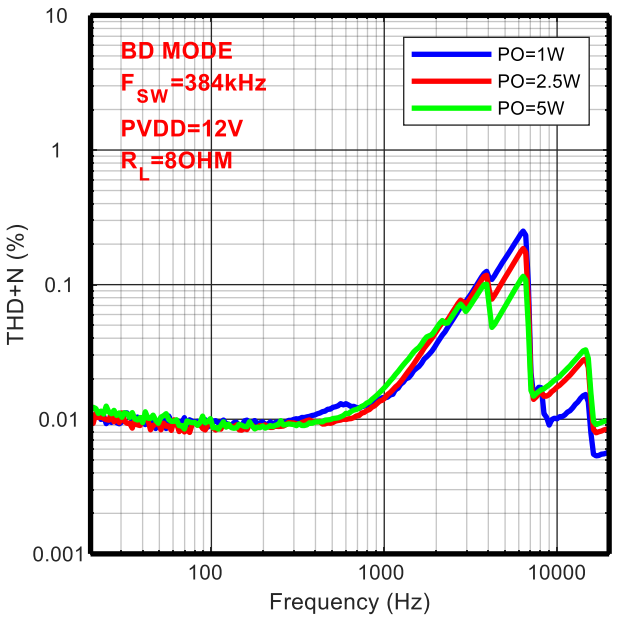


BRIDGE TIED LOAD (BTL) CONFIGURATION CURVES WITH FERRITE BEAD + CAPACITOR AS THE OUTPUT FILTER WITH BD MODULATION

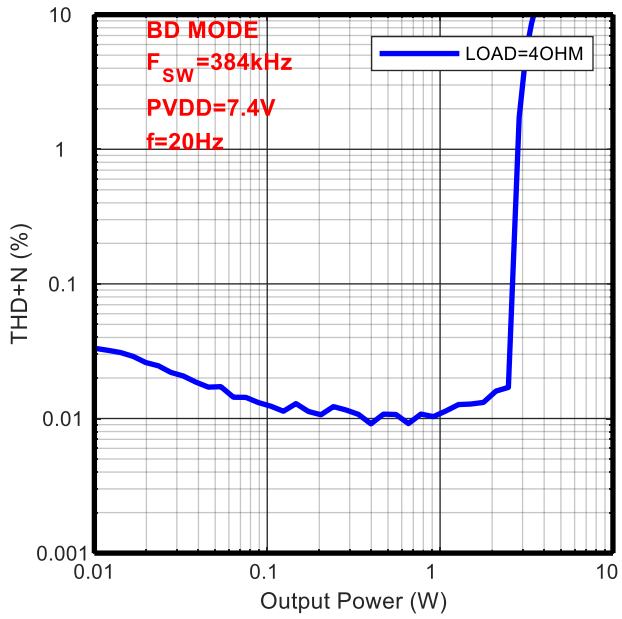
THD+N VS. FREQUENCY-BTL



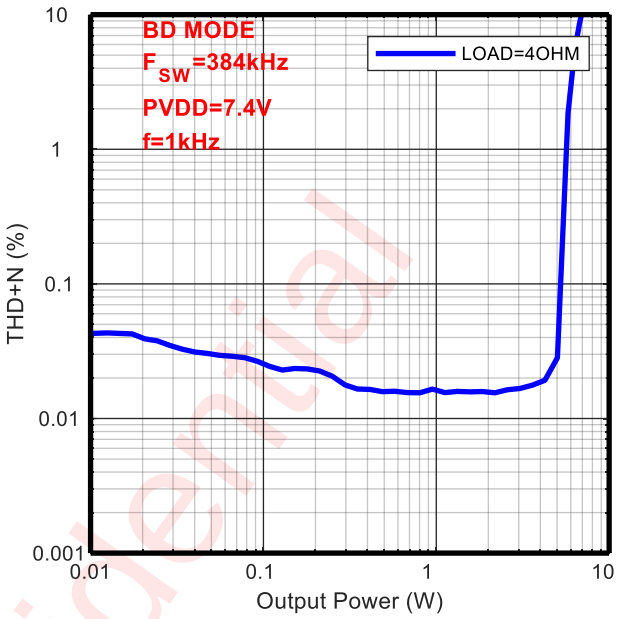
THD+N VS. FREQUENCY-BTL



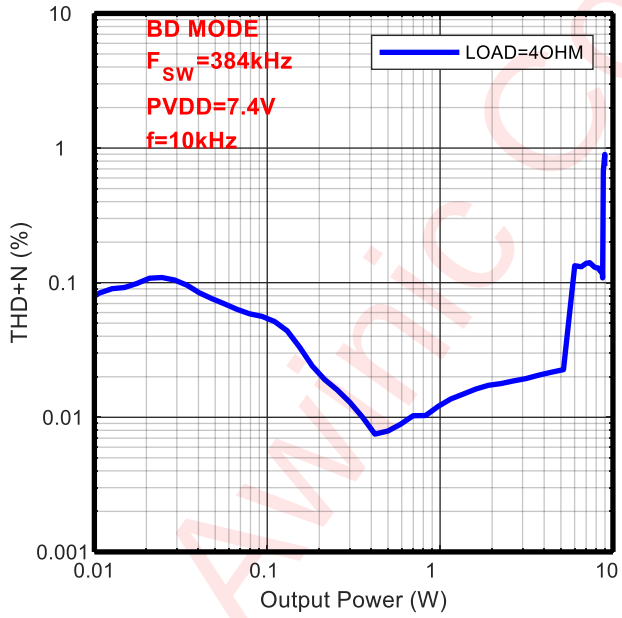
THD+N VS. OUTPUT POWER -BTL



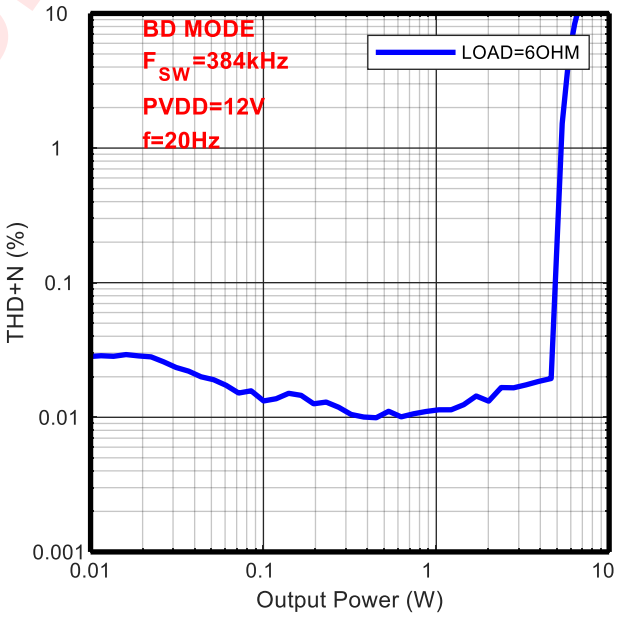
THD+N VS. OUTPUT POWER -BTL



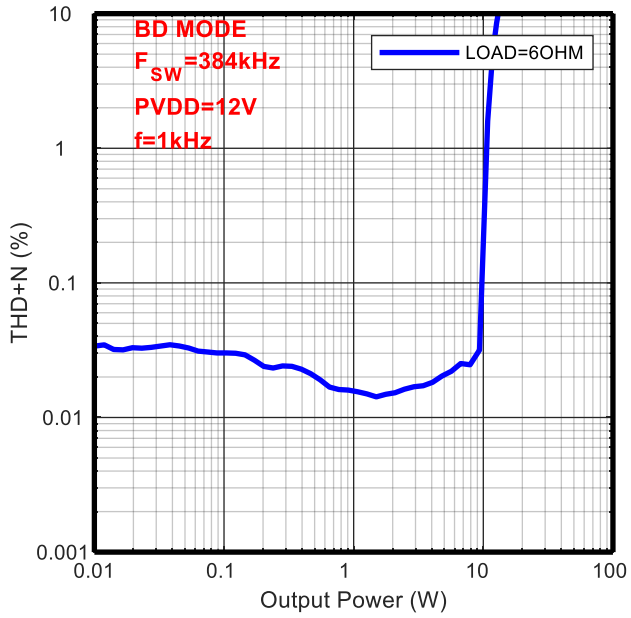
THD+N VS. OUTPUT POWER -BTL



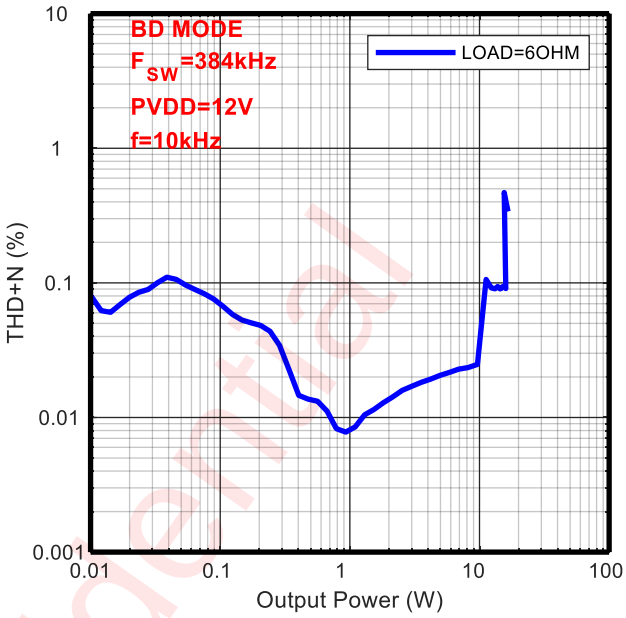
THD+N VS. OUTPUT POWER -BTL



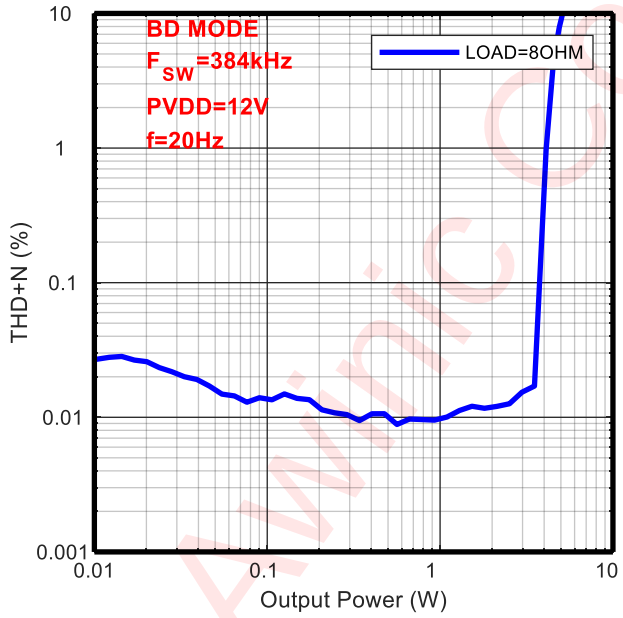
THD+N VS. OUTPUT POWER -BTL



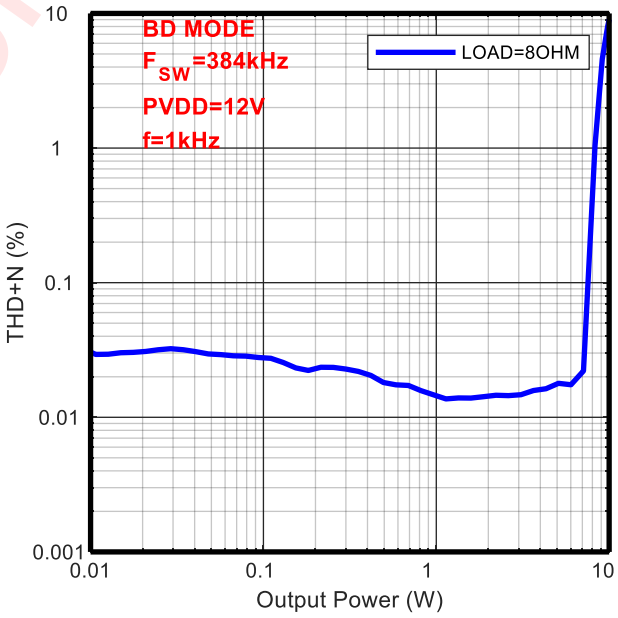
THD+N VS. OUTPUT POWER -BTL



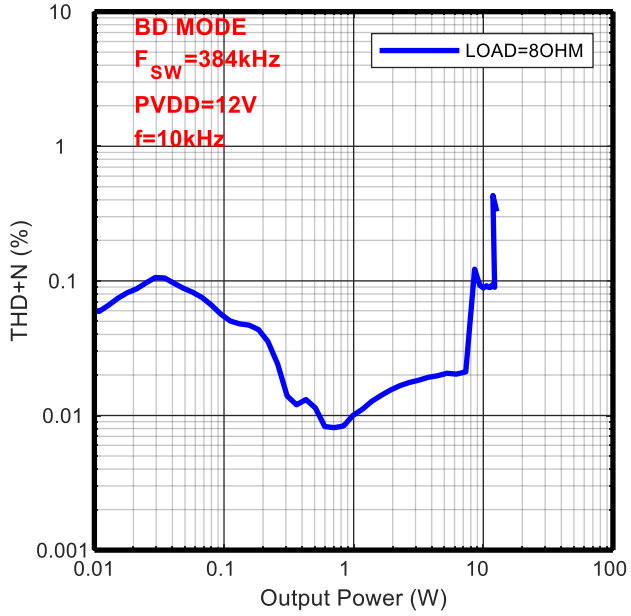
THD+N VS. OUTPUT POWER -BTL



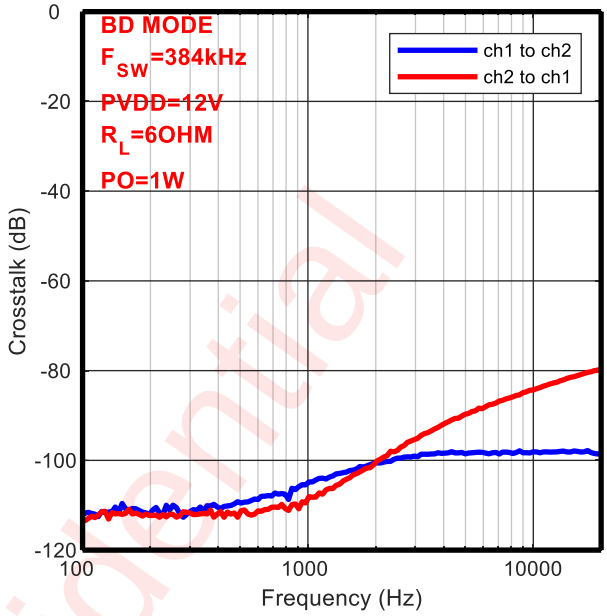
THD+N VS. OUTPUT POWER -BTL



THD+N VS. OUTPUT POWER -BTL

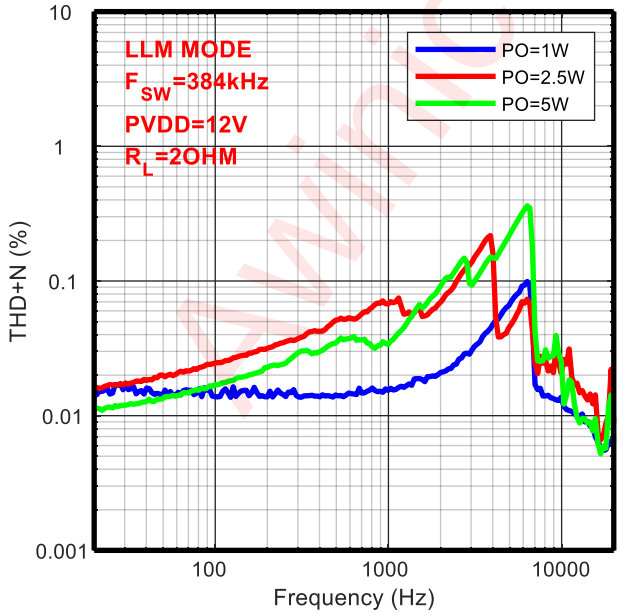


CROSSTALK -BTL

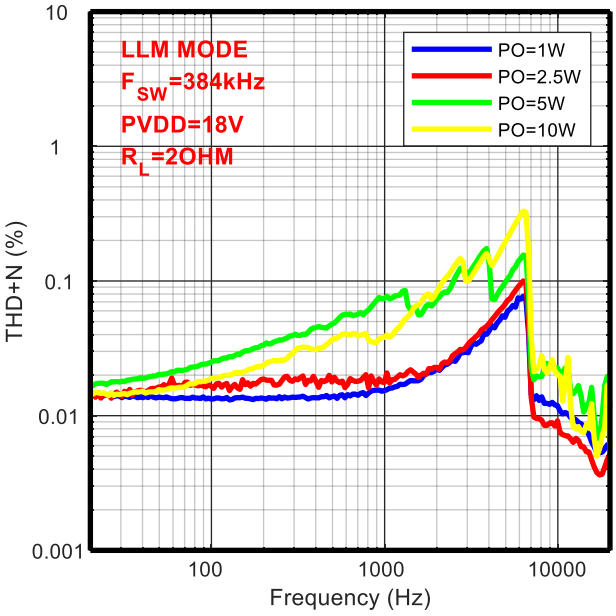


PARALLEL BRIDGE TIED LOAD (PBTL) CONFIGURATION WITH LLM MODULATION

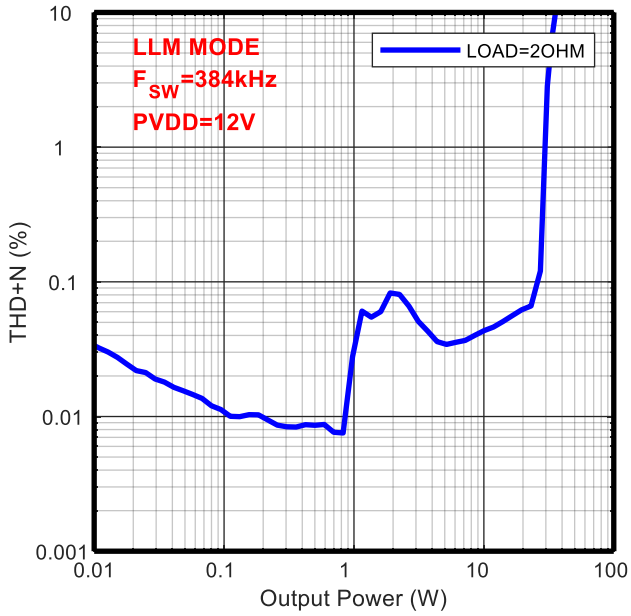
THD+N VS. FREQUENCY-PBTL



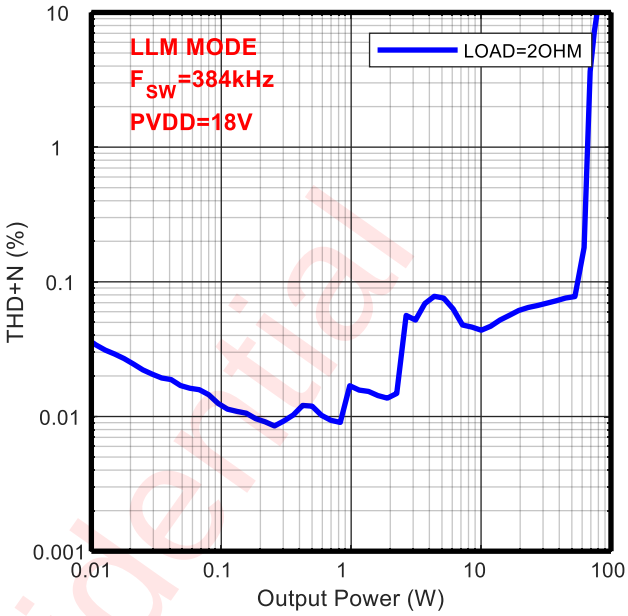
THD+N VS. FREQUENCY-PBTL



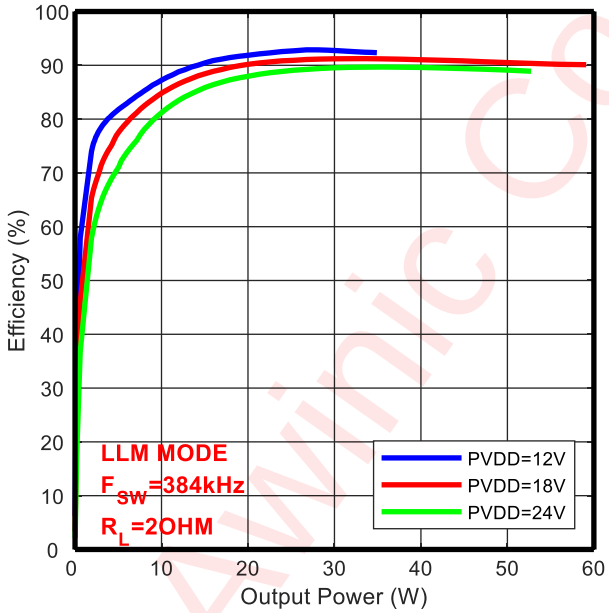
THD+N VS. OUTPUT POWER -PBTL



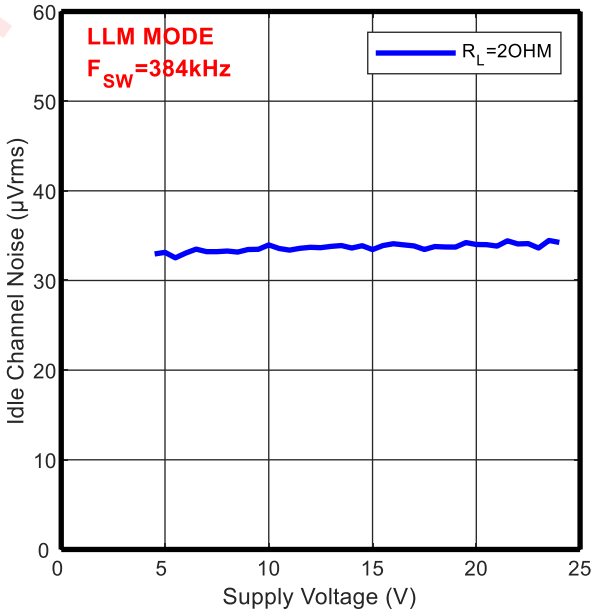
THD+N VS. OUTPUT POWER -PBTL



Efficiency vs Output Power -PBTL

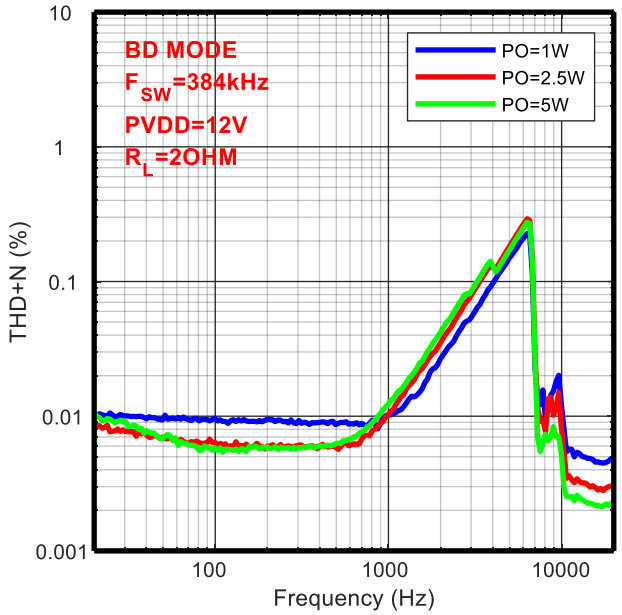


Idle Channel Noise vs Supply Voltage -PBTL

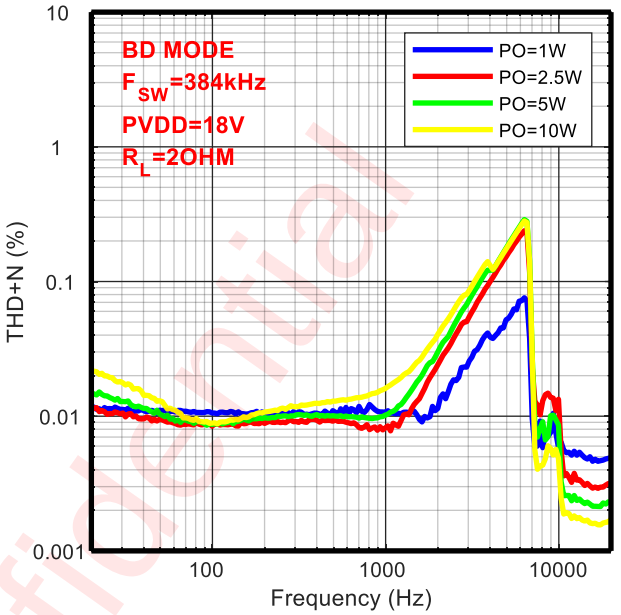


PARALLEL BRIDGE TIED LOAD (PBTL) CONFIGURATION WITH BD MODULATION

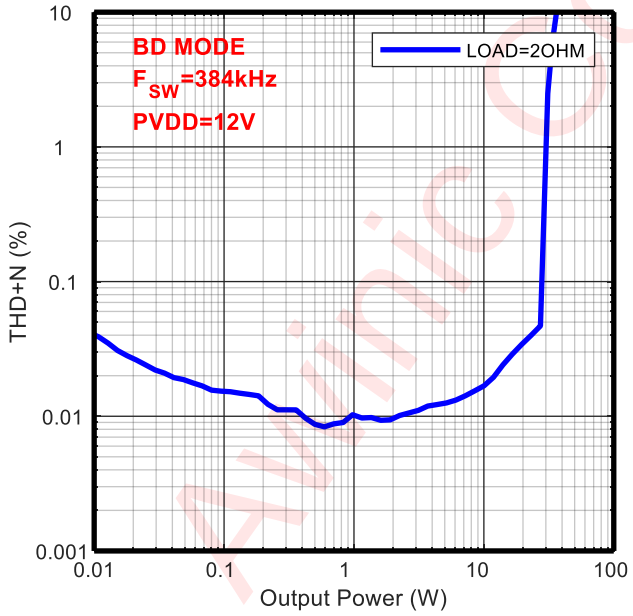
THD+N VS. FREQUENCY-PBTL



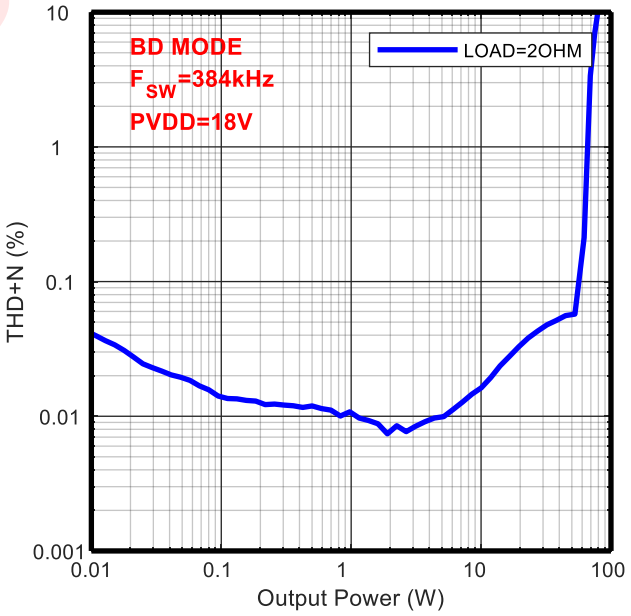
THD+N VS. FREQUENCY-PBTL



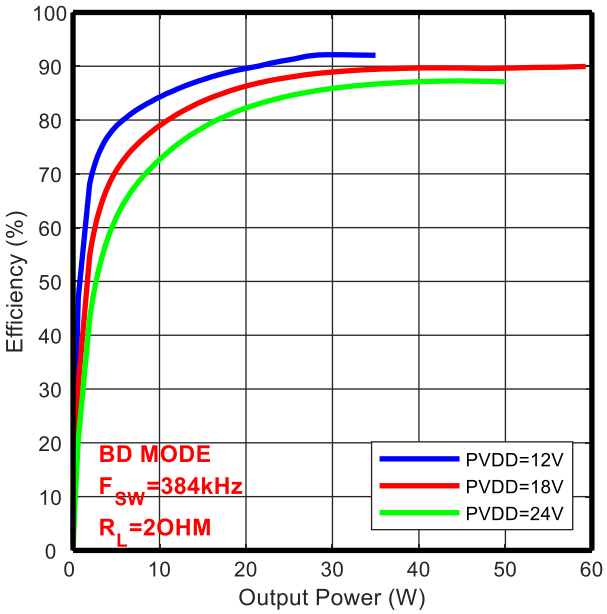
THD+N VS. OUTPUT POWER -PBTL



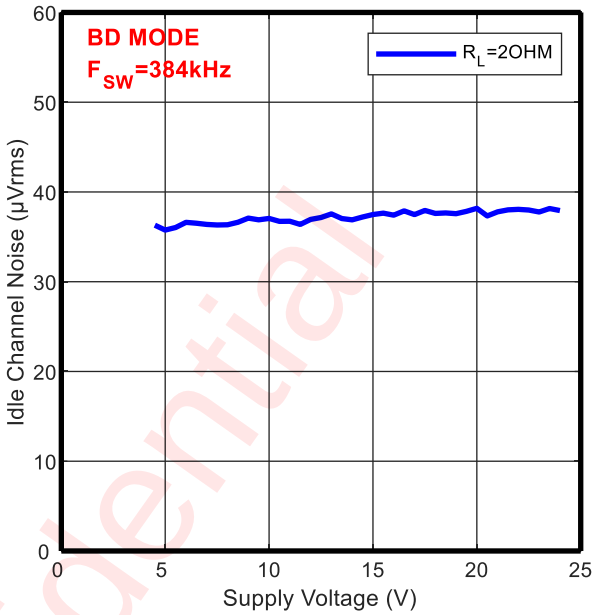
THD+N VS. OUTPUT POWER -PBTL



Efficiency vs Output Power -PBTL



Idle Channel Noise vs Supply Voltage -PBTL



Detailed Functional Description

POWER ON RESET

The device provides a power-on reset feature that is controlled by DVDD supply voltage. When the DVDD supply voltage raises from 0V to 1.1V. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 4 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	V_{PVDD} < 1.1V V_{DVDD} < 1.1V V_{PDN} < 0.7* V_{DVDD}	Power supply is not ready, chipset is power down.
Deep Sleep	V_{PVDD} ⩾4.5V V_{DVDD} > 1.65V V_{PDN} > 0.7* V_{DVDD}	Power supply is ready, most parts of the device are power down for low power consumption except I^2C interface
Sleep	PWDN = 0 AMPPD=0 PD_PA=1	Device is biased while class-D output is floating. System configuration carried out in this mode
Hiz	EN_GTDR=0	Amplifier Output HiZ
PLAY	PWDN = 0 AMPPD=0 PD_PA=0	Amplifier is fully operating

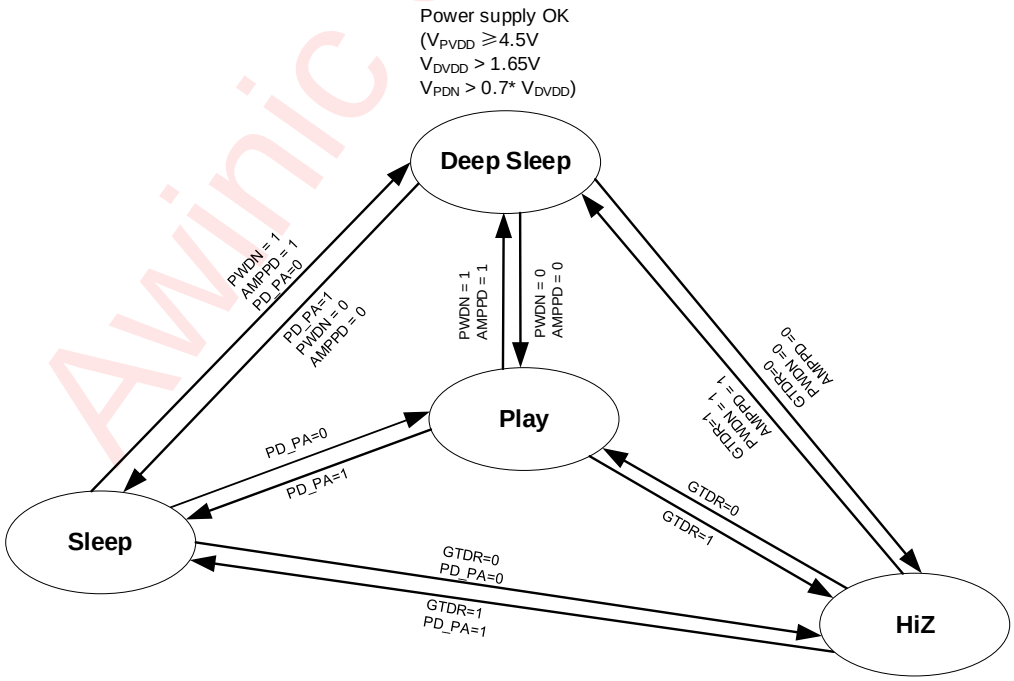


Figure 7 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- V_{PVDD} < 4.3V
- V_{DVDD} < 1.1 V
- V_{PDN}< 0.7* V_{DVDD}

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

V_{DVDD} > 1.65 V and V_{PVDD} ≥ 4.5V and V_{PDN} > 0.7* V_{DVDD}

DEEP SLEEP MODE

The device switches stand-by mode when the power supply voltages are OK. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to mode when the device is no needed to work.

SLEEP MODE

The device switches to Sleep mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.AMPPD = 0;
- PD_PA=1;

In this mode, I2C block, Digital core, and DSP Memory Keep Work ,Compare with Power-down Mode (Pull PDN Low), enter or exit Sleep Mode, DSP keeps active.

PLAY MODE

The device switches to Play mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.AMPPD = 0;
- PD_PA=0;

The device is fully operational in this mode. CLASSD loop and power stage circuits will start to work. Customer can set SYSCTRL.AMPPD = 0 to make device in this mode.

This device power up sequence is illustrated in the following figure:

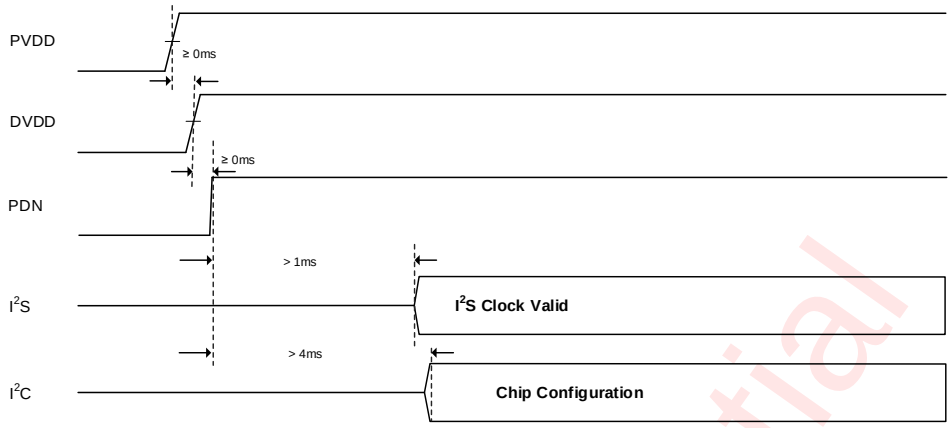
HIZ MODE

The device switches to HiZ mode when:

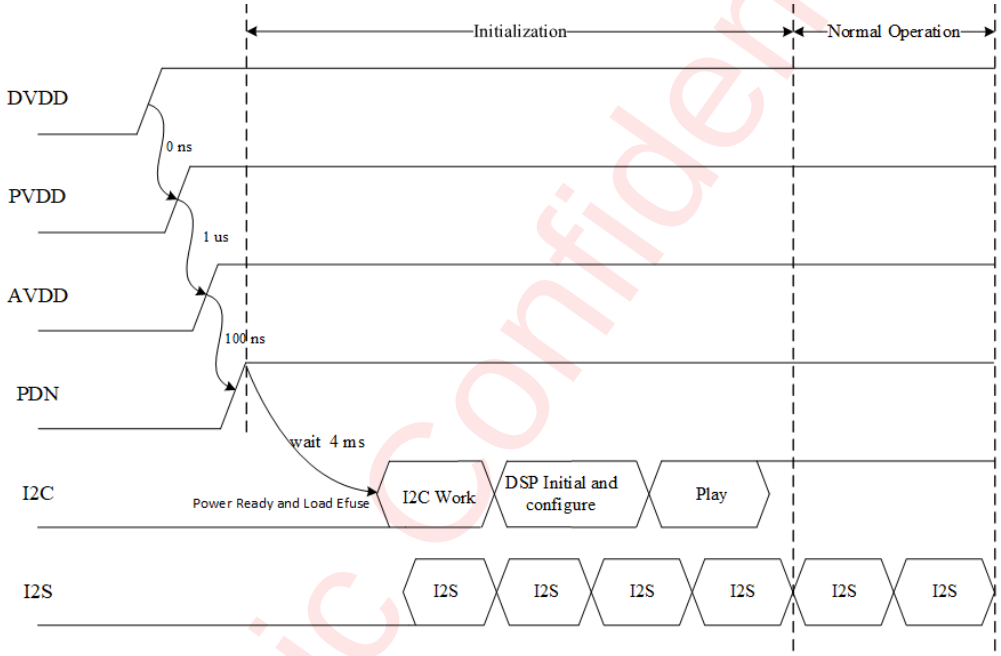
- SYSCTRL.PWDN = 0;
- SYSCTRL.AMPPD = 0;
- EN_GTDR=0

In this mode, only output driver set to be Hiz state, all other block work normally.

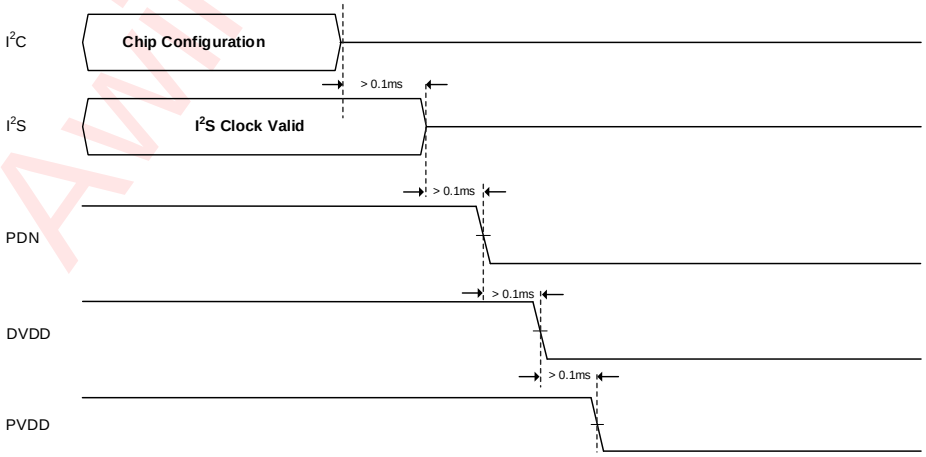
Power up sequence considering I²S, I²C timing shows as below (NOTE1):



AVDD external supply timing shows as below:



Power down sequence considering I²S, I²C timing shows as below:



NOTE1: PVDD power up time ＞ 10 mS

SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers.

DIGITAL I/O STATUS

The state of each digital input and output are shown in below table. After power on, the input signal pin BCK, WCK, DATAI are set to high impedance by default. If I2STXEN is enabled, SDOUT is actively driven when outputting data otherwise it is high impedance by default.

Table 2 Digital I/O status description

Digital I/O	Type	Description (Default State)
SCL	Input	Hi-Z
SDA	Input	Hi-Z
ADR	Input	Weak pull down
SCLK	Input	Hi-Z
LRCLK	Input	Hi-Z
SDIN	Input	Hi-Z
SDOUT	Output	Hi-Z

DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 4 dedicated pins:

- SCLK
- LRCLK
- SDIN
- SDOUT

Two-slot I²S and 1/2/4/6/8/16-slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL1.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL1.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 32kHz, 44.1kHz, 48kHz, 96kHz and 192kHz. It is selected via configurable register I2SCTRL1.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL1.I2SBCK. The frequency of BCK can be calculated according to the following equation:

BCK frequency = ***SampleRate*** * ***SlotLength*** * ***SlotNumber***

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of Sclk clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 1/2/4/6/8/16-slot supported in TDM mode.

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL). The frequency of word select signal should be larger than 32kHz when it is used as the reference clock of PLL.

The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL1.CHSEL_A/CHSEL_B.

Table 3 Supported I²S interface parameters

Interface format(MSB first)	Data width	Sclk frequency
Standard I²S	16b/20b/24b/32b	32fs/48fs/64fs
Left-justified	16b/20b/24b/32b	32fs/48fs/64fs
Right-justified	16b/20b/24b/32b	32fs /48fs/64fs

The output port SDOUT, can be enabled or disabled via bit I2SCTRL1.I2STXEN. The unused slots can be set to Hi-z or normal working, which is controlled by I2SCTRL3.DOHZ.

STANDARD I²S MODE

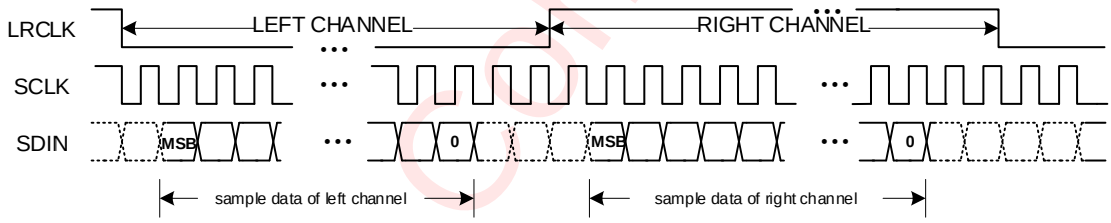


Figure 8 I²S Timing for Standard I²S Mode

- When LRCLK=0 indicating the left channel data, and LRCLK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

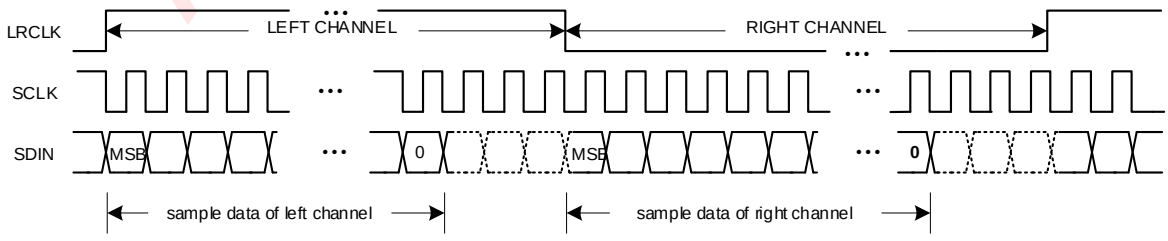


Figure 9 I²S Timing for Left-Justified Mode

- When LRCLK=1 indicating the left channel data, and LRCLK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

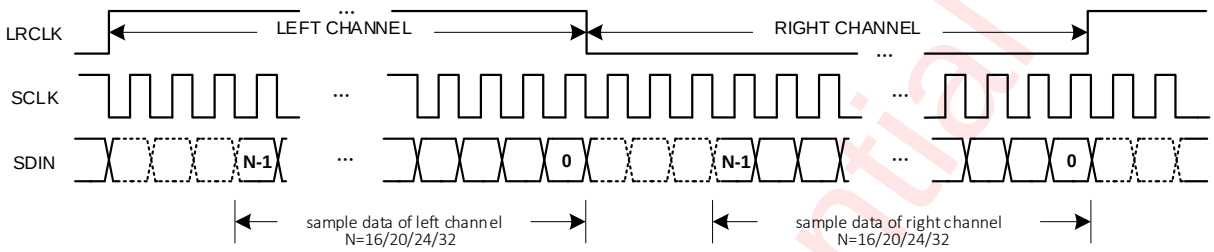


Figure 10 I²S Timing for Right-Justified Mode

- When LRCLK is high indicating the left channel data, and LRCLK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

TDM MODE

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 1/2/4/6/8/16-slot is supported in TDM mode, while 2-slot is supported in I²S mode

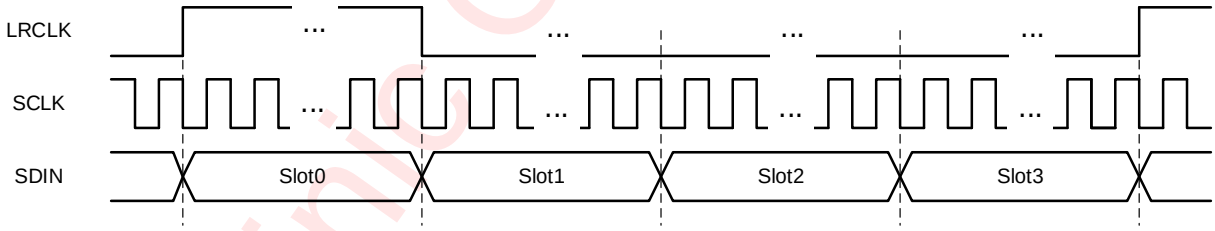


Figure 11 TDM Timing

Note: The high level pulse width of LRCLK signal can be one slot time or one period of SCLK.

DIGITAL AUDIO PROCESSING

This device incorporates one programmable Digital Audio Processor (DAP) block. It provides the algorithm for audio signal processing and speaker protection. The following functions are available in this module.

- HDCC
- Hardware AGC
- Volume control
- Mute

The signal processing flow in the Digital Audio Processor (DAP) is illustrated in the following figure.

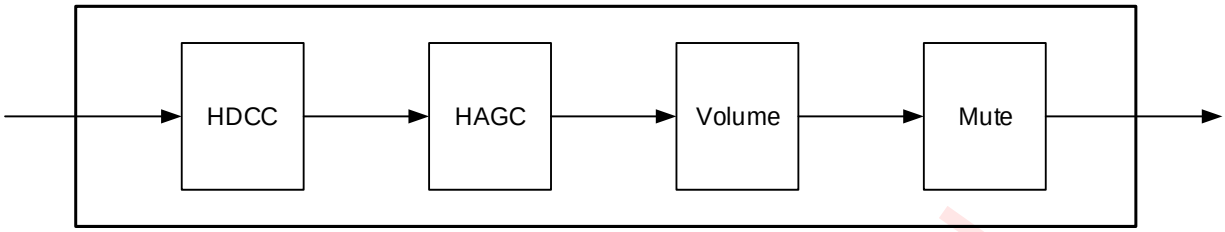


Figure 12 Block Diagram of DAP

HDCC

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

HAGC

System output power tends to be more than rated power of speaker in the actual audio application, the overload signal can cause damage to the speaker if there is no output power control. The audio power amplifier with HAGC can protect the speaker effectively. When the output power is not exceeds the setting threshold, the HAGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the HAGC module will reduce the internal gain of amplifier and restrict the output power under the setting threshold.

VOLUME CONTROL

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0dB to -96dB with 0.094dB/step.

MUTE

This module performs mute control for the audio stream.

DEVICE FUNCTIONAL MODES

SPEAKER AMPLIFIER OPERATING MODES

The AW85806 device can be used with two different amplifier configurations, can be configured by Register 0x53h -Bit [14], 0x54h -Bit [14]:

BTL Mode

In BTL mode, the AW85806 amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A+ and OUT_A-, the amplified right signal is presented on differential output pair shown as OUT_B+ and OUT_B-.

PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the

AW85806 device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the AW85806 device, the input signal to the PBTL amplifier is left frame of I2S or TDM data.

DEVICE MODULATION

AW85806 has 3 modulation schemes: BD modulation, LLM modulation and LLMP modulation. Select modulation schemes for AW85806 with Register 0x53h -Bit [12] or Bit [11].

BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0V to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switch period, reducing the switching current, which reduces any I^2R losses in the load.

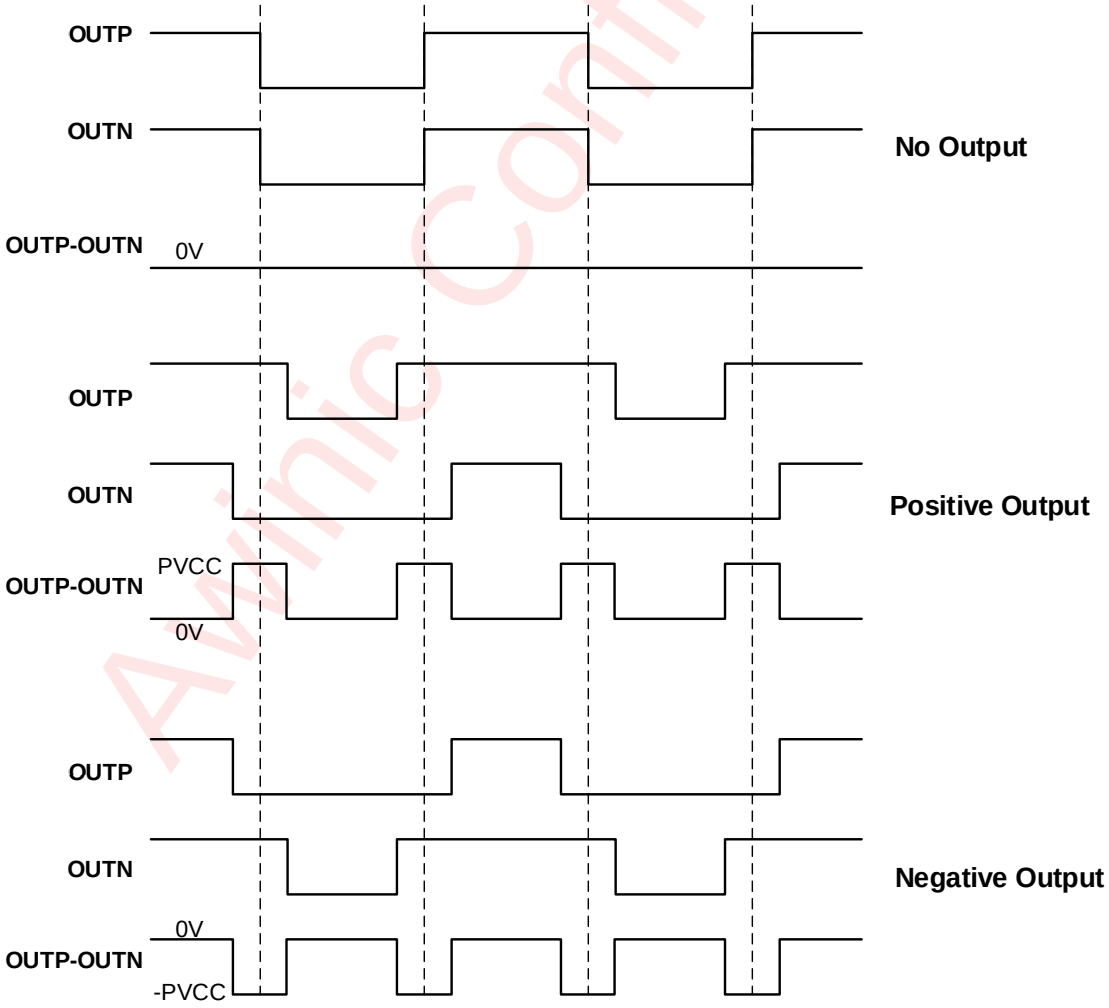


Figure 13 BD Mode Modulation

LLM Modulation

The Low-Loss mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low-Loss mode the outputs operate at 15% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in Low-Loss mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

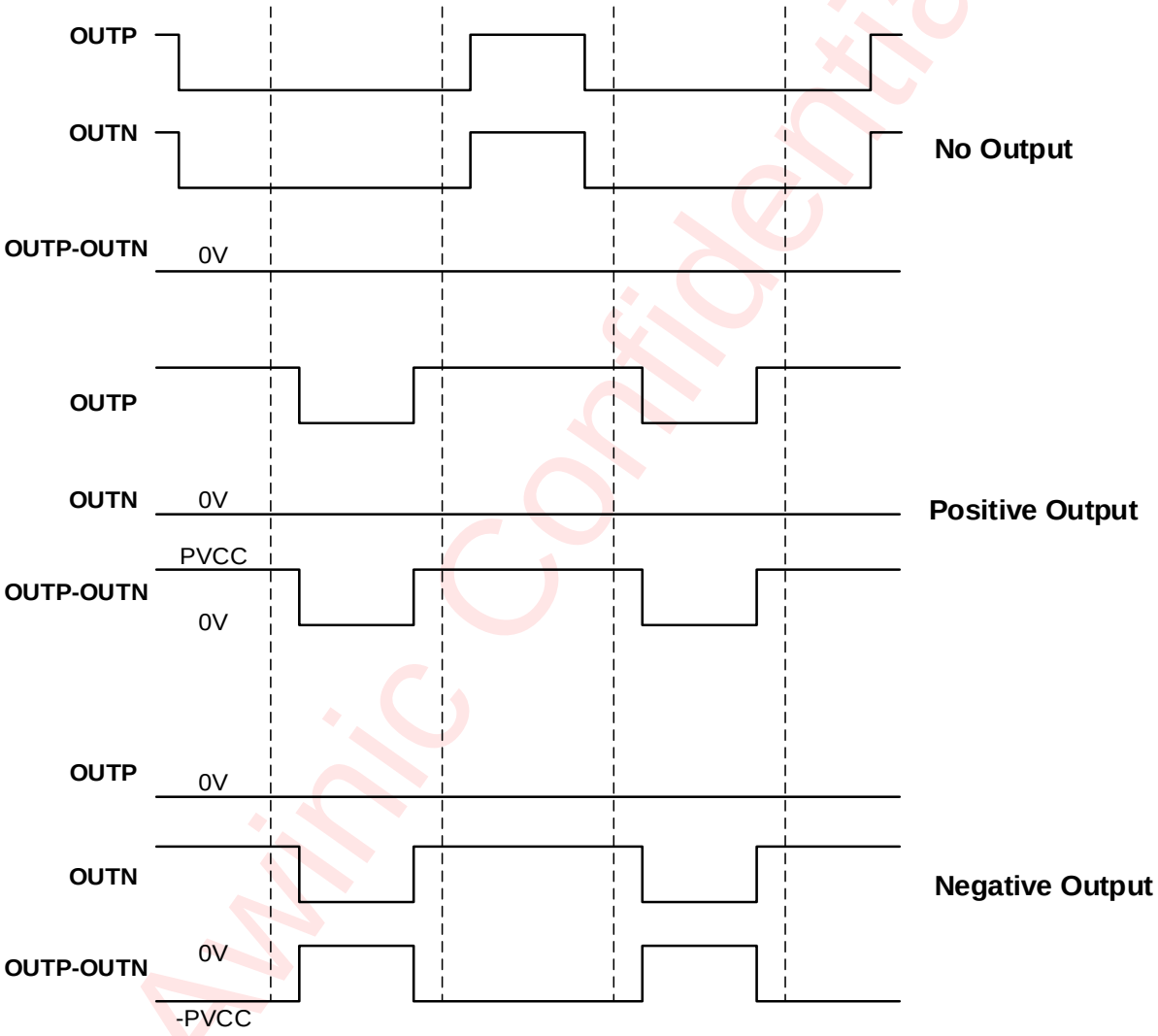


Figure 14 Low-Loss Mode Modulation

LLMP Modulation

LLMP Modulation is designed for minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With LLMP modulation, AW85806 detects the input signal level and adjust PWM duty cycle dynamically based on PVDD. LLMP modulation achieves ultra low idle current and maintains the same audio performance level as the BD Modulation.

DEVICE PROTECTION MECHANISMS

Over current Protection (OCP)

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the CLASSD Amplifier outputs enter high impedance immediately if the peak current increases to large enough. The Amplifier shutdown speed depends on some factors, such as the impedance of the short circuit, PVDD supply voltage, and PWM switching frequency. The host can restart the Amplifier via config I2C.The OCP event will be indicated on the fault pin, and the I2C register saves a fault record. If the output current is strong enough to exceed the peak current threshold but not severe enough to trigger the OCP, the peak current limiter works to prevent excess current from damaging the device, and the output returns to normal operate state while the short is removed.

DC Detect (DC)

If the AW85806 device detects the DC offset of the output voltage, if the different output exceed 2V for a long time, the device be judged as an DC error, the FAULT Pin is pulled low and the CLASSD outputs transition to high impedance, signifying a fault. The host can restart the Amplifier via config I2C.

Over Voltage Protection (OVP)

The circuit has integrated the over voltage protection control loop. When the output voltage PVDD is above the threshold, the CLASSD Amplifier will stop working, until the voltage of PVDD going down and under the normal fixed working voltage.

Under Voltage Detection (UVL)

The interrupt bit SYSINT.UVLI will be set to 1 when PVDD under voltage occurs, and the interrupt bits will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected under-voltage event has taken place.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 160°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 150°C), the output stages will start to operate normally again.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the ADR pin according to the following table: The ADR pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7-bit) through 0x37(7-bit).

Table 4 Address Selection

ADR	Address(7-bit)
4.7kΩ to DVDD	0x34
15kΩ to DVDD	0x35
47kΩ to DVDD	0x36
120kΩ to DVDD	0x37

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

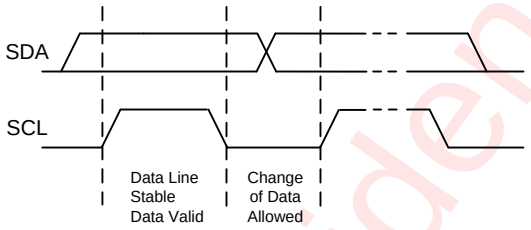


Figure 15 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

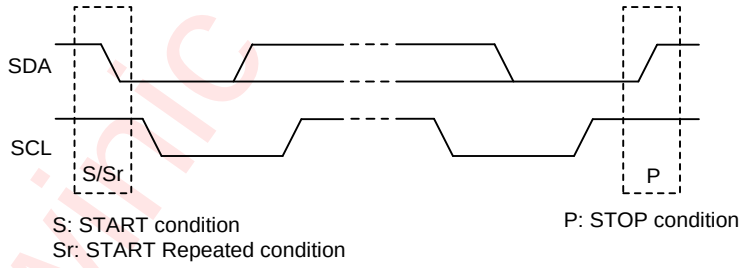


Figure 16 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

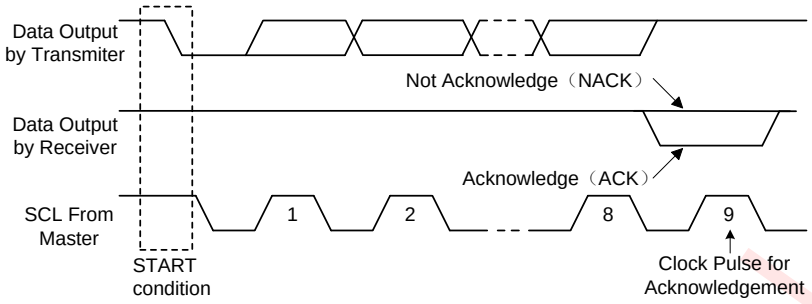


Figure 17 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master sends high data byte of 16-bit data to be written to the addressed register.

g) Slave sends acknowledge signal.

h) Master sends low data byte of 16-bit data to be written to the addressed register.

i) Slave sends acknowledge signal.

j) If master will send further 16-bit data bytes the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g).

k) Master generates STOP condition to indicate write cycle end.

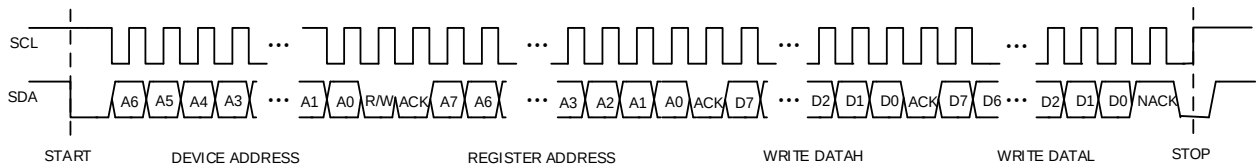


Figure 18 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master generates STOP condition followed with START condition or REPEAT START condition.

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 16-bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 16-bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.

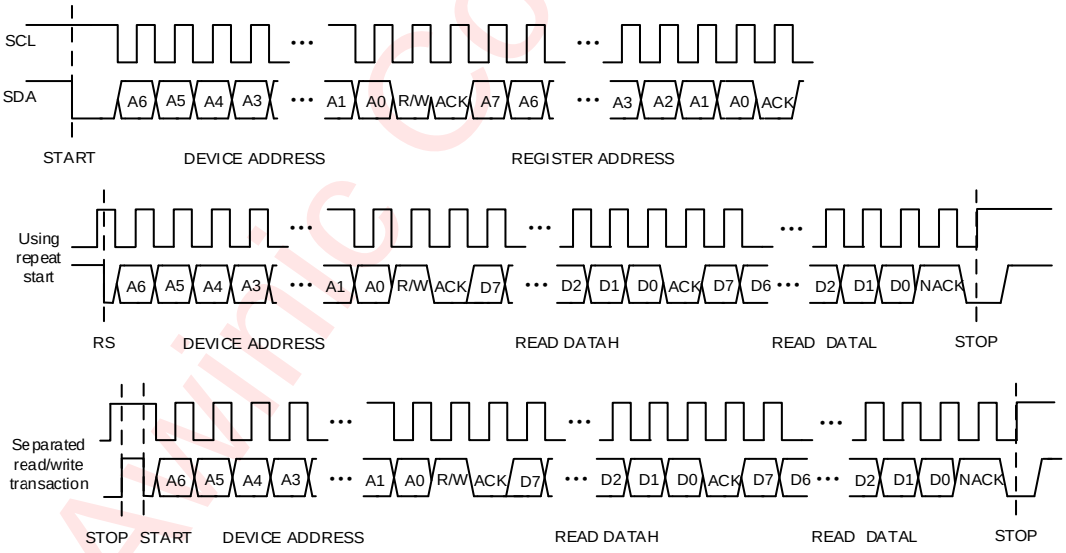


Figure 19 I²C Read Byte Cycle

SKTUNE ALGORITHM

This device integrates SKTune algorithm that maximizes the speaker performance while maintaining safe speaker conditions. The following functions are available in this module.

- Bass Booster

- Smart Protection
- Input Mixer, Output Crossbar
- Parametric Audio Path Equalizer (EQ)
- Dynamic Equalizer Enhancement (DEE)
- Sound Field Expansion (SFE)
- Multi-Band Dynamic Range Compressor (MBDRC)

The signal processing flow in the SKTune algorithm is illustrated in the following figure:

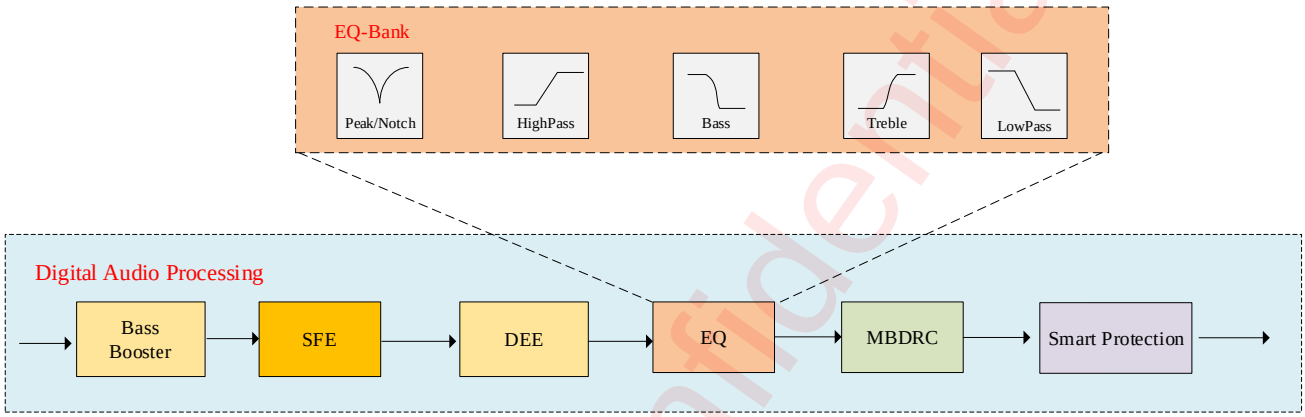


Figure 20 Block Diagram of SKTune algorithm

BASS BOOSTER

Small loudspeakers have poor performance in display low frequency audio signal, which can't meet people's demand for high quality sound. BASS BOOSTER uses psychoacoustic technology to highly elevate the low frequency performance in small loudspeaker.

SMART PROTECTION

This device has integrated four protection schemes for the speaker.

- **Anti-Clip Voltage Limiter:** avoiding output signal from exceeding the amplifier clip level
- **Auto Voltage Monitor:** avoiding distortion caused by power supply sudden transients
- **Excursion Limiter:** avoiding speaker membrane over-excursion
- **Thermal Limiter:** avoiding speaker voice coil over-temperature

Anti-Clip Voltage Limiter

The anti-clip voltage limiter is used to protect the output signal from exceeding the amplifier clip level. When signal is over the amplifier clip level it will be attenuated automatically and limited below the threshold without clipping.

Auto Voltage Monitor

When the supply voltage changes due to sudden transients and declining battery life, the AVM automatically

optimizes the signal amplitude to ensure consistent distortion and listening levels.

Excursion Limiter

The speaker membrane excursion is proportional to the amplitude of input signal. This device controls the membrane excursion by control the signal amplitude. It predicted the speaker membrane excursion according to the input signal at first. Then it'll attenuate the amplitude of the input signal automatically once the predicted excursion over the threshold.

Thermal Limiter

By modeling the temperature of the speaker, the temperature of the speaker voice coil can be monitored in real time according to the power value of the input signal. When the coil temperature is near the threshold, it controls the amplitude of signal sending to speaker.

INPUT MIXER

The input mixer is used to mix the left and right channel input signals.

OUTPUT CROSSBAR

Output crossbar provides users with a very flexible way to control the output signal in the amplifier.

PARAMETRIC AUDIO PATH EQUALIZER

Fifteen Parametric Audio Path Equalizers (EQ) are available and each of the equalizer can be fully programmable. It's possible to be implemented as any type of filter (high-pass, low-pass, peak, notch, bass, treble etc.) with different design methodologies to achieve the required frequency response.

DYNAMIC EQUALIZER ENHANCEMENT

Dynamic Equalizer Enhancement (DEE) processes signals in one frequency band without affecting other frequency bands. Like a precise surgery, different amplitude signals may have different effects which depend on the type of the equalizer and parameter of that.

SOUND FIELD EXPANSION

Sound Field Expansion (SFE) achieves the field of sound expansion and spatial enhancement by frequency selection and gain control of the input signals.

MULTI-BAND DYNAMIC RANGE CONTROL

A highly configurable and scalable MBDRC is available to improve audio performance. A block diagram of the MBDRC is illustrated in the following figure:

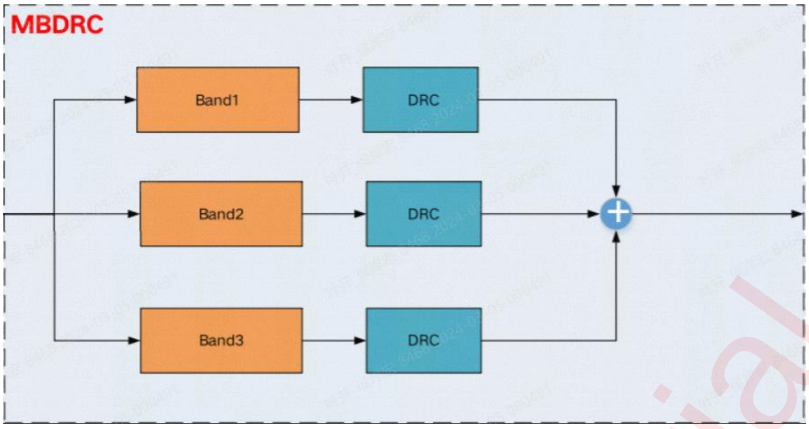


Figure 21 Simplified MBDRC block diagram

Application Information

BOOTSTRAP CAPACITORS

The output stage of the AW85806 uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22μF capacitors to connect the appropriate output pin (OUT_X) to the bootstrap pin (BST_X). For example, connect a 0.22μF capacitor between OUT_A and BST_A for bootstrapping the A channel. Similarly, connect another 0.22μF capacitor between the OUT_B and BST_B pins for the B channel inverting output.

INDUCTOR SELECTIONS

AW85806 requires that the peak current is smaller than the OCP (Over-Current protection current) value which is 7.5 A, there are 3 cases which cause high peak current flow through inductor.

1.During power up (idle state, no audio input), the duty cycle increases from 0 to D.

$$I_{peak\_power\ up} \approx PVDD \times \sqrt{C/L} \times sin(1/\sqrt{L \times C} \times D/F_{SW})$$

Note: D=0.5(BD Modulation),0.15(LLM Modulation), 0.10(LLMP Modulation)

2. During music playing, some audio burst signal (high frequency) with very hard PVDD clipping causes PWM duty cycle increases dramatically. This is the worst case and rarely happens.

$$I_{peak\_clipping} \approx PVDD \times (1 - D)/(F_{sw} \times L)$$

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor here.

$$I_{peak\_output\ power} \approx \sqrt{2 \times Max\ output\ power/R_{Load}}$$

Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation. It's suggested that inductor saturation current I_{SAT}, is larger than the amplifier peak current during power-up and play audio.

$$I_{SAT} \geq \mathrm{Max}(I_{peak\_power\ up}, I_{peak\_clipping}, I_{peak\_output\ power})$$

In addition, the effective inductance at the peak current is required to be at least 80% of the inductance value in Table 5 to meet data sheet specifications.

Table 5 Inductor Requirements

PVDD(V)	Switching Frequency (kHz)	Minimum Inductance (L) (μH)
≤12V	384	4.7
>12V	384	10

For higher switching frequencies (F_{SW}), select the inductors with minimum inductance to be 384 kHz / F_{SW} × L.

POWER SUPPLY DECOUPLING

To make sure of high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22μF. These capacitors bypass low frequency noise to the ground plane. For high frequency decoupling, place 1μF or 0.1μF capacitors as close as possible to the PVDD pins of the device.

OUTPUT EMI FILTERING

The AW85806 device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the LC Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.
The LC filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the LC filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics.

Register Configuration

Register List

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	ID	*RO*	IDCODE																0x21D9
0x01	SYSST	*RO*	I2S_AUTO_DET_ERRS	UVLS	OVPS		UVP_OVPS	DC_AS	DC_BS	ANA_READYS		WDS	NOCLKS	CLKS	OCD_AS	OCD_BS	OTHS	PLLS	0x0000
0x02	SYSINT	*RC*	I2S_AUTO_DET_ERRI	UVLI	OVPI		UVP_OVPI	DC_AI	DC_BI	ANA_READYI		WDI	NOCLKI	CLKI	OCD_AI	OCD_BI	OTHI	PLLI	0x0000
0x03	SYSINTM	*RW*	I2S_AUTO_DET_ERRM	UVLM	OVPM		UVP_OVPM	DC_AM	DC_BM	ANA_READYM		WDM	NOCLKM	CLKM	OCD_AM	OCD_BM	OTHM	PLLM	0xFF7F
0x04	SYSCTRL	*RW*	SET_GAIN					HAGCE	HDCCE	HMUTE_A	HMUTE_B	I2SEN	WSINV	BCKINV	IPLL	DSPBY	AMPPD	PWDN	0x0387
0x05	SYSCTRL2	*RW*	EN_MPD			RMSE	INTMODE	INTN	VOL										0x8000
0x06	I2SCTRL1	*RW*							I2SMD		I2SFS		I2SBCK		I2SSR				0x00FC
0x07	I2SCTRL2	*RW*	FSYNC_TYPE	SLOT_NUM			I2S_TX_SLOTVLD				I2S_RXR_SLOTVLD				I2S_RXL_SLOTVLD				0x0010
0x08	I2SCTRL3	*RW*		I2SDOSEL	DOHZ	I2SCHS		I2SRXEN	I2STXEN	I2S_TXEDGE	INPLEV		LPBK		CHSEL_A		CHSEL_B		0x2C06
0x09	DACCFG1	*RW*	RVTH								AVTH								0x3940

0x0a	DACCFG2	RW	ATTH														0x0030
0x0b	DACCFG3	RW	RTTH														0x01E0
0x0c	DACCFG4	RW											HOLDTH				0x1C64
0x1f	GPIOCTRL	RW	GPIO_INPUT_SEL								SDOUT_SEL						0x00D1
0x21	TEMP	RO											TEMP _DET				0x0019
0x22	PVDD	RO											PVDD_DET				0x02A0
0x53	CDACTRL1	RW	PR_EN_CLASSD_A	PR_EN_CLASSD_B		PR_EN_LLM	PR_EN_LLMP					PR_MUTE_A	PR_MUTE_B		PR_LOP_GBW_CTRL	PR_EN_PHSFT_A	0XE10A
0x54	CDACTRL2	RW	PR_EN_PHSFT_B	PR_PBTL_MD		PR_IBVCM_RTCL											0x0713
0x56	RAMPGEN1	RW	RAMP_SEL_CK	RAMP_PHASE_SEL			RAMP_DIG_N							RAMP_ICTL_CRAMP			0x9019
0x58	RAMPGEN3	RW	RAMP_EN_SS_TRI	RAMP_SS_TRI_CTRL											RAMP_EN_SS_RDM	RAMP_SS_RDM_PERIOD	0x0000
0x5f	BIASVDD3	RW														PR_PD_OUVP	0x0660
0x63	DC_DRIVER	RW	PR_PD_DC_DTC														0x0A98
0x67	PROTECT_LOG1	RW											PR_PD_PA			PR_EN_GTDR_A	PR_EN_GTDR_B	0x5507

Register Detailed Description

ID: (Address 00h)				
Bit	Symbol	R/W	Description	Default
15:0	IDCODE	RO	Chip ID (21D9) will be returned after read. All configuration registers will be reset to default value after 0x55aa is written	0x21D9

SYSST: (Address 01h)				
Bit	Symbol	R/W	Description	Default
15	I2S_AUTO_DET_ERRS	RO	The I2S auto detect error signal 0: normal 1: detect error	0
14	UVLS	RO	PVDD under voltage indicator 0: Normal 1: UVLO	0
13	OVPS	RO	PVDD OVP status indicator 0: Normal 1: OVP	0
12	Reserved	RO	Not used	0
11	UVP_OVPS	RO	The indicate signal of OVP_UVP 0: Normal 1: OVP_UVP	0
10	DC_AS	RO	The indicate signal of A channel DC 0: Normal 1: DC	0
9	DC_BS	RO	The indicate signal of B channel DC 0: Normal 1: DC	0
8	ANA_READYS	RO	The indicate signal of ANA_READY 0: IDLE 1: ANA_READY	0
7	Reserved	RO	Not used	0
6	WDS	RO	DSP watch-dog status 0: Normal 1: Abnormal	0
5	NOCLKS	RO	The reference clock of PLL is not available 0: Clock Ok 1: No Clock	0
4	CLKS	RO	Internal clocks status flag, status 0 means At least one clock are not stable 0: Not stable 1: Stable	0
3	OCD_AS	RO	The indicate signal of A channel OCD 0: Normal 1: OCD	0

2	OCD_BS	RO	The indicate signal of B channel OCD 0: Normal 1: OCD	0
1	OTHS	RO	Die Temperature is higher than 150℃ 0: Normal 1: OT	0
0	PLLS	RO	PLL locked status. 0: Unlocked 1: Locked	0

SYSINT: (Address 02h)

Bit	Symbol	R/W	Description	Default
15	I2S_AUTO_DET_ERRI	RC	Interrupt indicator for I2S auto detect error	0
14	UVLI	RC	Interrupt indicator for Power On and UVLS	0
13	OVPI	RC	Interrupt indicator for OVPS.	0
12	Reserved	RC	Not used	0
11	UVP_OVPI	RC	Interrupt indicator for OVP_UVP	0
10	DC_AI	RC	Interrupt indicator for A channel DC	0
9	DC_BI	RC	Interrupt indicator for B channel DC	0
8	ANA_READYI	RC	Interrupt indicator for ANA_READY	0
7	Reserved	RC	Not used	0
6	WDI	RC	Interrupt indicator for WDS	0
5	NOCLKI	RC	Interrupt indicator for NOCLKS.	0
4	CLKI	RC	Interrupt indicator for CLKS.	0
3	OCD_AI	RC	Interrupt indicator for A channel OCD	0
2	OCD_BI	RC	Interrupt indicator for B channel OCD	0
1	OTHI	RC	Interrupt indicator for OTHS.	0
0	PLLI	RC	Interrupt indicator for PLLS.	0

SYSINTM: (Address 03h)

Bit	Symbol	R/W	Description	Default
15	I2S_AUTO_DET_ERRM	RW	Interrupt mask for I2S auto detect error	1
14	UVLM	RW	Interrupt mask for UVLI.	1
13	OVPM	RW	Interrupt mask for OVPI	1
12	Reserved	RW	Not used	0
11	UVP_OVPM	RW	Interrupt mask for OVP_UVP	1
10	DC_AM	RW	Interrupt mask for A channel DC	1
9	DC_BM	RW	Interrupt mask for B channel DC	1
8	ANA_READYM	RW	Interrupt mask for ANA_READY	1
7	Reserved	RW	Not used	0
6	WDM	RW	Interrupt mask for WDI.	1
5	NOCLKM	RW	Interrupt mask for NOCLKI.	1
4	CLKM	RW	Interrupt mask for CLKI.	1
3	OCD_AM	RW	Interrupt mask for A channel OCD	1
2	OCD_BM	RW	Interrupt mask for B channel OCD	1
1	OTHM	RW	Interrupt mask for OTHI.	1
0	PLLM	RW	Interrupt mask for PLLI.	1

SYSCTRL: (Address 04h)				
Bit	Symbol	R/W	Description	Default
15:11	SET_GAIN	RW	Configuration for initial gain Gain = 29.5*10^(-SETGAIN/40) 00000: 29.5 AV(15.5dB) 00001: 27.84980 AV(15dB) ..... 11111: 4.95 AV(0dB)	0
10	HAGCE	RW	Disable/Enable Hardware AGC 0: Disable 1: Enable	0
9	HDCCE	RW	Disable/Enable Hardware DC Canceling module 0: Disable 1: Enable	1
8	HMUTE_A	RW	Disable/Enable Hardware A channel mute module 0: Disable 1: Enable	1
7	HMUTE_B	RW	Disable/Enable Hardware B channel mute module 0: Disable 1: Enable	1
6	I2SEN	RW	Disable/Enable whole I2S interface module 0: Disable 1: Enable	0
5	WSINV	RW	I2S Left/Right channel switch control 0: Not switch 1: Switch	0
4	BCKINV	RW	I2S bit clock invert control 0: Not invert 1: Inverted	0
3	IPLL	RW	PLL reference clock selection 0: BCK 1: WCK	0
2	DSPBY	RW	DSP bypass control bit 0: Working 1: Bypass	1
1	AMPPD	RW	Amplifier power down control bit, Power Down until system configuration finished 0: Working 1: Power Down	1
0	PWDN	RW	System power down control bit 0: Working 1: Power Down	1

SYSCTRL2: (Address 05h)				
Bit	Symbol	R/W	Description	Default

15	EN_MPD	RW	Disable/Enable MPD multi stage power mode, Gain will be automatically adjusted only when EN_MPD is high. It can enable the small-signal detection or not, based on the audio input, so that the quiescent current could be reduced and the noise level will be smaller. 0: Disable 1: Enable	1
14:13	Reserved	RW	Not used	0
12	RMSE	RW	Hardware AGC mode selection 0: Peak AGC 1: RMS AGC	0
11	INTMODE	RW	Interrupt pad GPIO (when GPIO_SEL is 0x4) output mode selection 0: Open-drain 1: Push&Pull	0
10	INTN	RW	Interrupt pad INTN pin-source selection 0: SYSINT 1: SYSST	0
9:0	VOL	RW	Volume control, from +0.376 to -95.786dB, in unit of -0.094dB 0000000000:0.376dB 0000000001:0.282 dB 0000000010:0.188dB 0000000011:0.094dB 0000000100:0dB 0000000101: -0.094dB ... 1111111111: -95.786dB	0

I2SCTRL1: (Address 06h)

Bit	Symbol	R/W	Description	Default
15:12	Reserved	RW	Not used	0
11:10	Reserved	RW	Not used	0
9:8	I2SMD	RW	I2S interface mode selection 00: Philip Standard 01: MSB justified 10: LSB justified 11: Reserved	0
7:6	I2SFS	RW	I2S data resolution selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits	3
5:4	I2SBCK	RW	I2S BCK mode 00: 32*fs 01: 48*fs 10: 64*fs 11: Auto detect	3

3:0	I2SSR	RW	I2S interface sample rate configuration 0110: 32 kHz 0111: 44.1 kHz 1000: 48 kHz 1001: 88.2 kHz 1010: 96 kHz 1011: 192KHz 1100: Auto Detect Others: Reserved	0xc

I2SCTRL2: (Address 07h)

Bit	Symbol	R/W	Description	Default
15	FSYNC_TYPE	RW	Audio Frame synchronization signal (WCK) pulse width configuration 0: One-slot 1: One-BCK	0
14:12	SLOT_NUM	RW	I2S TDM mode control. 000: I2S mode 001: TDM1s 010: TDM2s 011: TDM4s 100: TDM6s 101: TDM8s 110: TDM16s 111: Reserved	0
11:8	I2S_TX_SLOTVLD	RW	TX slot selection, data will be sent to one of the slots. 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 ..... 1111: Slot 15	0
7:4	I2S_RXB_SLOTVLD	RW	RX B channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 ..... 1111: Slot 15	1
3:0	I2S_RXA_SLOTVLD	RW	RX A channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 ..... 1111: Slot 15	0

I2SCTRL3: (Address 08h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14	I2SDOSEL	RW	I2S unused channel data selection 0: Zeros 1: TXData	0
13	DOHZ	RW	Unused channel Data control, when it is set to 0, all Channels are available. Otherwise Unused channel is set to be HiZ. 0: All 1: HiZ	1
12	I2SCHS	RW	I2S Tx Channel selection 0: Left 1: Right	0
11	Reserved	RW	Not used	1
10	I2SRXEN	RW	Disable/Enable I2S receiver module 0: Disable 1: Enable	1
9	I2STXEN	RW	Disable/Enable I2S transmitter module 0: Disable 1: Enable	0
8	I2S_TXEDGE	RW	I2S TX clock edge selection 0: negedge 1: posedge	0
7	INPLEV	RW	Input level selection bit, i2s input signal will be attenuated by -6dB at first when this register is set to 1. 0: 0dB 1: -6dB	0
6	Reserved	RW	Not used	0
5:4	LPBK	RW	I2S data Loopback control bits 00: Disable 01: Far-Back 10: Near-Back 11: Reserved	0
3:2	CHSEL_A	RW	A channel selection for I2S input 00: Reserved 01: Left 10: Right 11: Mono	1
1:0	CHSEL_B	RW	B channel selection for I2S input 00: Reserved 01: Left 10: Right 11: Mono	2

DACCFG1: (Address 09h)

Bit	Symbol	R/W	Description	Default
15:8	RVTH	RW	Release Amplitude threshold, in percent of signal full scale	0x39

7:0	AVTH	RW	Attack Amplitude threshold, in percent of signal full scale RMSE = 0 (Peak AGC): P0= ((i/256*Gain)**2)/RLoad/2 RMSE = 1 (RMS AGC): P0=(i/256)*(Gain**2)/RLoad i is the register value, default 0x40 Gain is the Speaker Gain configured by SYSCTRL.SPK_GAIN and SYSCTRL2.VOL . RLoad is 8ohm	0x40

DACCFG2: (Address 0Ah)

Bit	Symbol	R/W	Description	Default
15:0	ATTH	RW	Attack time threshold in unit of 20.8μs 0: Reserved n: n*20.8us	0x0030

DACCFG3: (Address 0Bh)

Bit	Symbol	R/W	Description	Default
15:0	RTTH	RW	Release time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	0x01E0

DACCFG4: (Address 0Ch)

Bit	Symbol	R/W	Description	Default
15:9	Reserved	RW	Not used	0x0E
8	Reserved	RW	Not used	0
7:0	HOLDTH	RW	Hold time before release control, in unit of about 1.33ms 0: Reserved n: n*1.33ms	0x64

GPIOCTRL: (Address 1Fh)

Bit	Symbol	R/W	Description	Default
15	GPIO_INPUT_SEL	RW	Select GPIO input data 0: reserve 1: ramp gen sync	0
14:9	Reserved	RW	Not used	0
8:6	SDOUT_SEL	RW	Select SDOUT function 000: input 001: Reserved 010: ANA_FAULT 011: I2S_DATAO 100: INTN 101: Reserved 110: Reserved 111: Reserved	3
5:3	Reserved	RW	Not used	2
2:0	Reserved	RW	Not used	1

TEMP: (Address 21h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	TEMP_DET	RO	Detected Die Temperature (2's Complement), typical values are as follows. 0x3D8: -40 ℃ 0x00: 0 ℃ 0x01: 1 ℃ 0x19: 25 ℃ 0x37: 55 ℃ Please convert it to decimal number.	0x019

PVDD: (Address 22h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	PVDD_DET	RO	Detected Voltage of PVDD, and the fullscale is 30V PVDD=(PVDD_DET)/1023×30	0x2a0

CDACTRL1: (Address 53h)

Bit	Symbol	R/W	Description	Default
15	PR_EN_CLASSD_A	RW	A-channel CLASSD power amplifier enable signal: 0: disable 1: enable	1
14	PR_EN_CLASSD_B	RW	B-channel CLASSD power amplifier enable signal: 0: disable 1: enable	1
13	Reserved	RW	Not used	1
12	PR_EN_LLM	RW	Low Loss Mode enable signal; 0: disable 1: enable	0
11	PR_EN_LLMP	RW	LLM PLUS mode enable signal; 0: disable 1: enable	0
10	Reserved	RW	Not used	0
9	Reserved	RW	Not used	0
8:7	Reserved	RW	Not used	2
6	Reserved	RW	Not used	0
5	PR_MUTE_A	RW	A channel power amplifier MUTE control signal 0: normal 1: mute	0
4	PR_MUTE_B	RW	B channel power amplifier MUTE control signal 0: normal 1: mute	0
3	Reserved	RW	Not used	1

2:1	PR_LOP_GBW_CTRL	RW	CLASSD loop bandwidth selection signal; 00:230K 01:130K 10:100K 11:80K	1
0	PR_EN_PHSFT_A	RW	A channel phase shift enable signal; 0: disable 1: enable	0

CDACTRL2: (Address 54h)

Bit	Symbol	R/W	Description	Default
15	PR_EN_PHSFT_B	RW	B channel phase shift enable signal; 0: disable 1: enable	0
14	PR_PBTL_MD	RW	PBTL mode enable signal; 0: disable 1: enable	0
13	Reserved	RW	Not used	0
12:11	PR_IBVCM_RTCL	RW	Source negative feedback resistance adjustment register of IB_VCM 00: PVDD<16 01: Reserved 10: Reserved 11: PVDD>16	0
10:9	Reserved	RW	Not used	3
8:7	Reserved	RW	Not used	2
6	Reserved	RW	Not used	0
5	Reserved	RW	Not used	0
4	Reserved	RW	Not used	1
3	Reserved	RW	Not used	0
2	Reserved	RW	Not used	0
1	Reserved	RW	Not used	1
0	Reserved	RW	Not used	1

RAMPGEN1: (Address 56h)

Bit	Symbol	R/W	Description	Default
15	RAMP_SEL_CK	RW	RAMP_GEN clock input selection signal. 0: digital clock mode 1: Analog clock mode.	1
14:13	RAMP_PHASE_SEL	RW	Selection signal for output DCLK_SW phase. 00: 0° 01: 45° 10: 90° 11: 135°	0
12:5	RAMP_DIG_N	RW	Digital clock mode select Fsw (RAMP_SEL_CK=0) when sample rate is 32k: 00011010: 1.2MHz(26); 00100001: 960kHz(33);	128

			00101010: 768kHz(42); 00111000: 576kHz(56); 01000011: 480kHz(67); 01010100: 384kHz(84); when sample rate is 44.1k/88.2k: 00100101: 1.2MHz(37); 00101110: 960kHz(46); 00111010: 768kHz(58); 01001101: 576kHz(77); 01011101: 480kHz(93); 01110101: 384kHz(117); when sample rate is 48k/96k/192k: 00101000: 1.2MHz(40); 00110010: 960kHz(50); 00111111: 768kHz(63); 01010100: 576kHz(84); 01100101: 480kHz(101); 10000000: 384kHz(128); Others: Reserved;	
4:1	RAMP_ICTL_CRAMP	RW	Analog clock mode select Fsw (RAMP_SEL_CK=1) 0000: 768kHz 0100: 576kH 1000: 480kHz 1100: 384kHz 1001: 960kHz 1011: 1.2MHz others: reserved	0xC
0	Reserved	RW	Not used	1

RAMPGEN3: (Address 58h)

Bit	Symbol	R/W	Description	Default
15	RAMP_EN_SS_TRI	RW	Triangle spread spectrum enable signal. 0: Triangle spread spectrum off 1: Triangle spread spectrum is on.	0

14:11	RAMP_SS_TRI_CTRL	RW	Configure the spread spectrum frequency and range of triangular spread spectrum. 0000: spread spectrum range 5%，spread spectrum step 1 0001: spread spectrum range 10%，spread spectrum step 1 0010: spread spectrum range 15%，spread spectrum step 1 0011: spread spectrum range 20%，spread spectrum step 1 0100: spread spectrum range 25%，spread spectrum step 1 0101: spread spectrum range 5%，spread spectrum step 2 0110: spread spectrum range 10%，spread spectrum step 2 0111: spread spectrum range 15%，spread spectrum step 2 1000: spread spectrum range 20%，spread spectrum step 2 1001: spread spectrum range 25%，spread spectrum step 2 others: reserved	0
10:7	Reserved	RW	Not used	0
6:3	Reserved	RW	Not used	0
2	RAMP_EN_SS_RDM	RW	Random spread spectrum enable signal. 0: random spread spectrum off 1: The random spread spectrum is turned on	0
1	RAMP_SS_RDM_PERIOD	RW	Configure the pseudorandom code period of random spread spectrum. 0: random spread cycle is 15 1: random spread cycle is 31	0
0	Reserved	RW	Not used	0

BIASVDD3: (Address 5Fh)

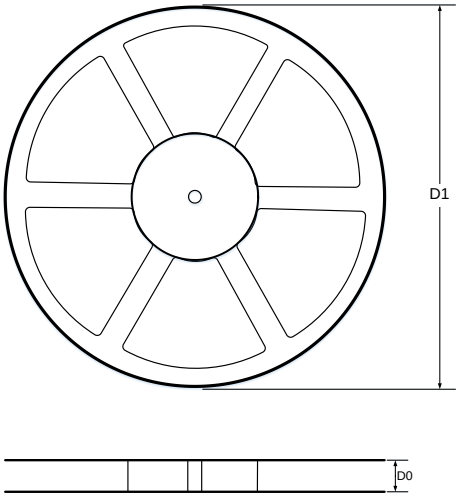
Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14	Reserved	RW	Not used	0
13:11	Reserved	RW	Not used	0
10	Reserved	RW	Not used	1
9:7	Reserved	RW	Not used	0x4
6	Reserved	RW	Not used	1
5:3	Reserved	RW	Not used	0x4
2	Reserved	RW	Not used	0
1	PR_PD_OUVP	RW	PVDD_ UVP_ OVP off control register; 0: Normal operation 1: Turn off PVDD_ UVP_ OVP function;	0
0	Reserved	RW	Not used	0

DC_DRIVER: (Address 63h)				
Bit	Symbol	R/W	Description	Default
15	PR_PD_DC_DTC	RW	DC detection shutdown control register; 0: Normal operation 1: Close	0
14	Reserved	RW	Not used	0
13:10	Reserved	RW	Not used	0x2
9	Reserved	RW	Not used	1
8:7	Reserved	RW	Not used	1
6:4	Reserved	RW	Not used	0x1
3	Reserved	RW	Not used	0x6
2	Reserved	RW	Not used	0
1	Reserved	RW	Not used	0
0	Reserved	RW	Not used	0

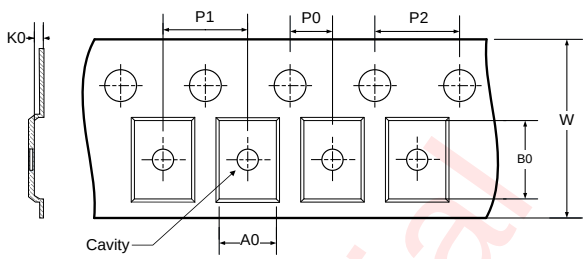
PROTECT_LOG1: (Address 67h)				
Bit	Symbol	R/W	Description	Default
15:14	Reserved	RW	Not used	1
13:12	Reserved	RW	Not used	1
11	Reserved	RW	Not used	0
10:9	Reserved	RW	Not used	0x1
8:7	Reserved	RW	Not used	0x2
6	PR_PD_PA	RW	PA off control signal 0: Normal operation 1: Close	0
5	Reserved	RW	Not used	0
4	Reserved	RW	Not used	0
3	Reserved	RW	Not used	0
2	PR_EN_GTDR_A	RW	A Channel GTDR enable 0: Disable 1: Enable	1
1	PR_EN_GTDR_B	RW	B Channel GTDR enable 0: Disable 1: Enable	1
0	Reserved	RW	Not used	1

Tape and Reel Information

REEL DIMENSIONS

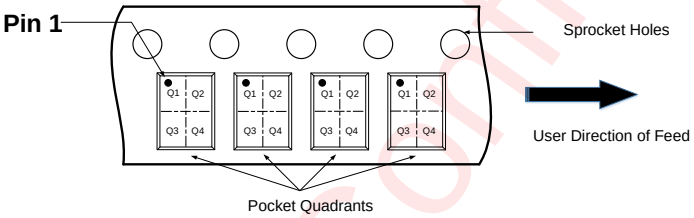


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



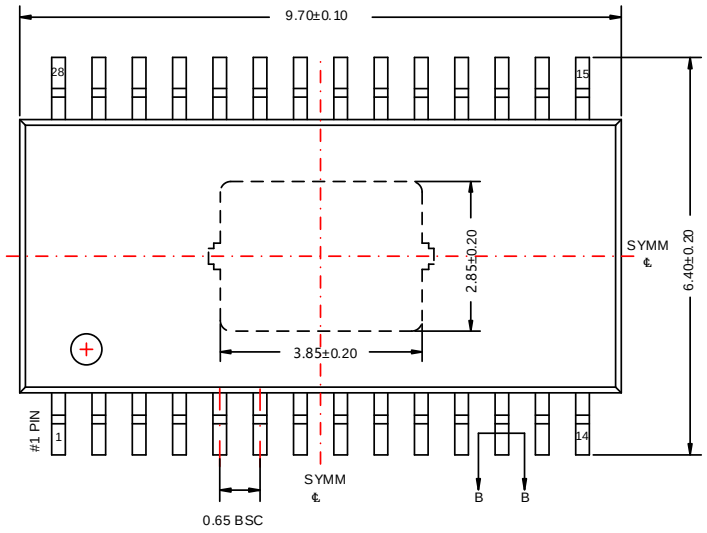
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

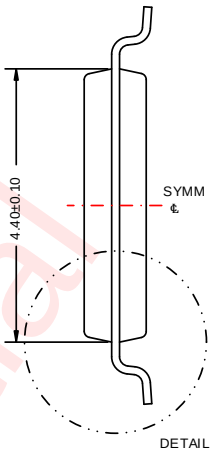
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	16.4	6.8	10.2	1.6	2	8	4	16	Q1

All dimensions are nominal

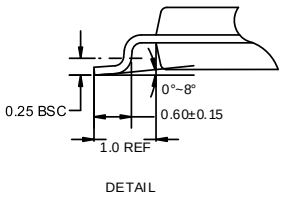
Package Description

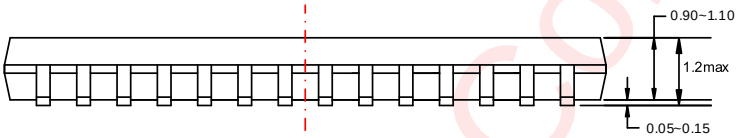


Top View

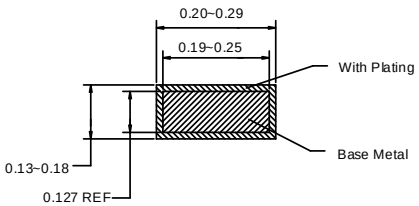


Side View





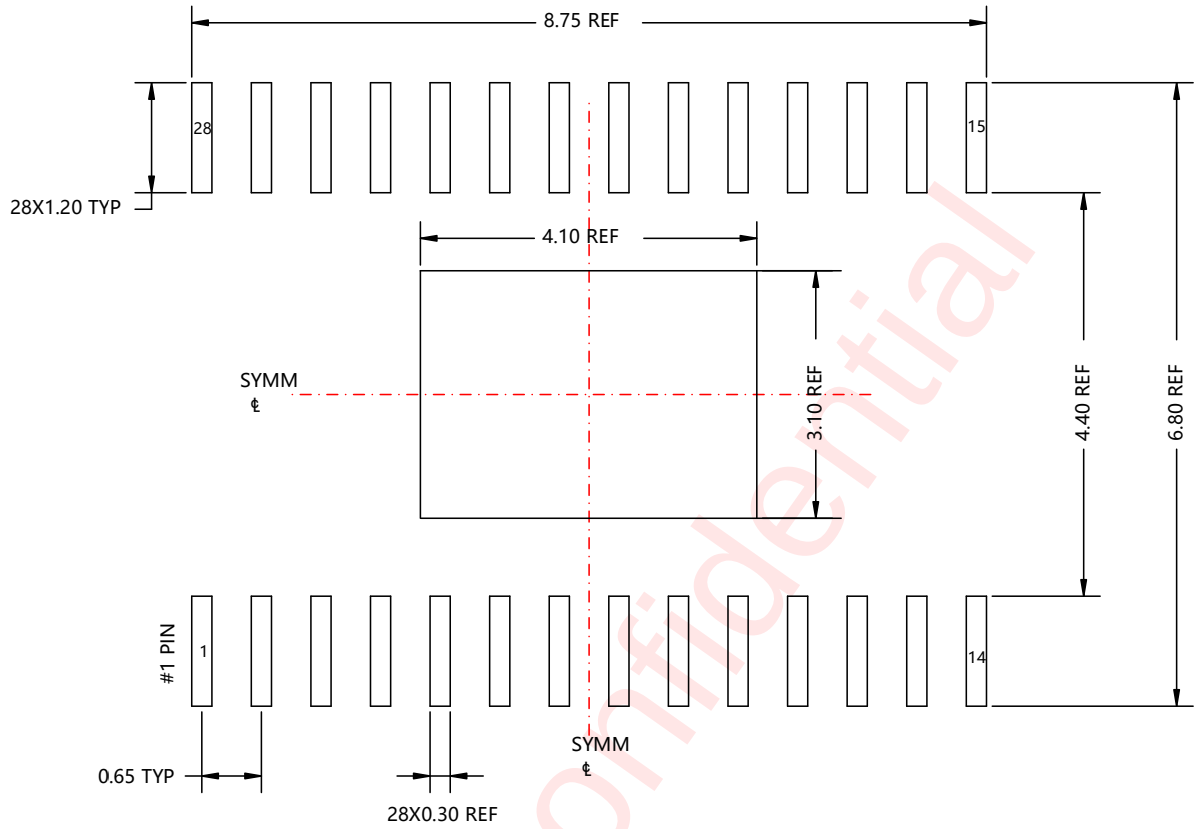
Side View

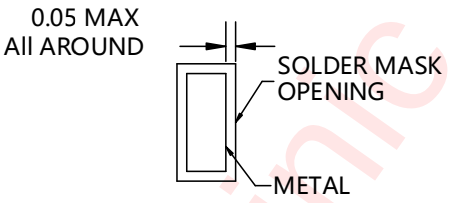


Section B-B

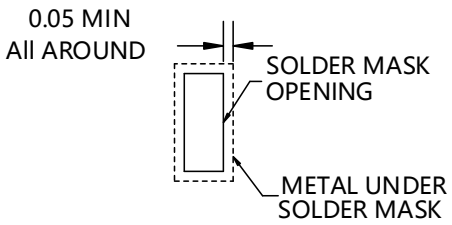
Unit:mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Changed Record
V1.0	Apr 2024	Officially released
V1.1	Dec 2024	Updated register detailed description

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