6.5A 2.4MHz I²C Programmable Synchronous Buck Regulator

Features

- Input voltage range: 2.5V to 5.5V
- I²C Programmable output voltage:
  0.603V to 1.233V in 10mV steps
- I²C Programmable slew rate for voltage transitions
- 6.5A continuous current capability
- 2.4MHz switching frequency
- I²C-Compatible interface up to 3.4MHz
- Selection by I²C interface:
  PFM or forced PWM mode
  Output Discharge
- Input under-voltage lockout(UVLO)
- Input over-voltage protection(OVP)
- Short-circuit protection with Hiccup Mode
- Internal soft-start
- Thermal shutdown and overload protection
- I²C salve address: 0xC0
- Available in WLCSP2.0mmX1.6mmX0.586mm -20B package

General Description

The AW37460 is a high efficiency synchronous step-down converter with I²C interface which provide digitally programmable output from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I²C interface capable of operating up to 3.4MHz.

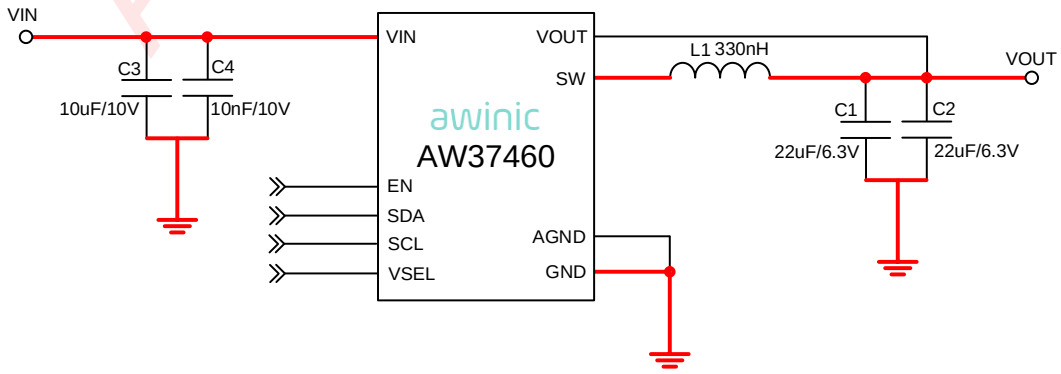
The converter operates at a nominal fixed frequency of 2.4MHz, which reduces the value of the external components. At medium to heavy loads, the converter operates in PWM mode and automatically enters PFM operation at light load to maintain high efficiency over the entire load current range. The converter can also be forced in PWM mode operation for smallest output voltage ripple. Through the I²C interface, the output voltage is quickly adjusted to adapt the power consumption of the load to the ever-changing performance needs of the application.

The AW37460 is available in WLCSP 2.0mmX1.6mmX0.586mm-20B package.

Applications

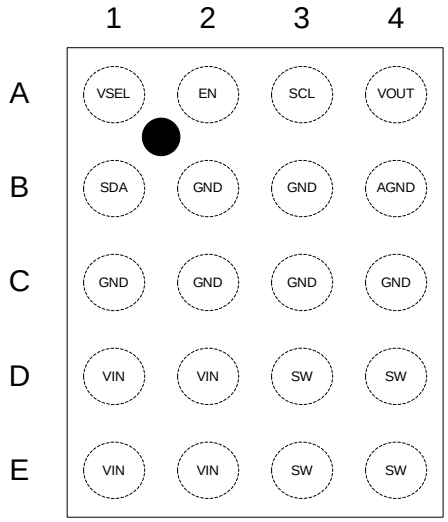
Application, Graphic and DSP Processors
Hard Disk Drives, LPDDR3, LPDDR4
Tablets, Notebooks
Smart phones
Gaming Devices

Typical Application Circuit

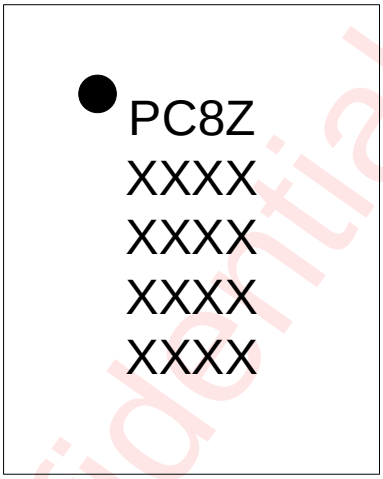


Pin Configuration And Top Mark

AW37460CSR
(Top View)



AW37460CSR Marking
(Top View)

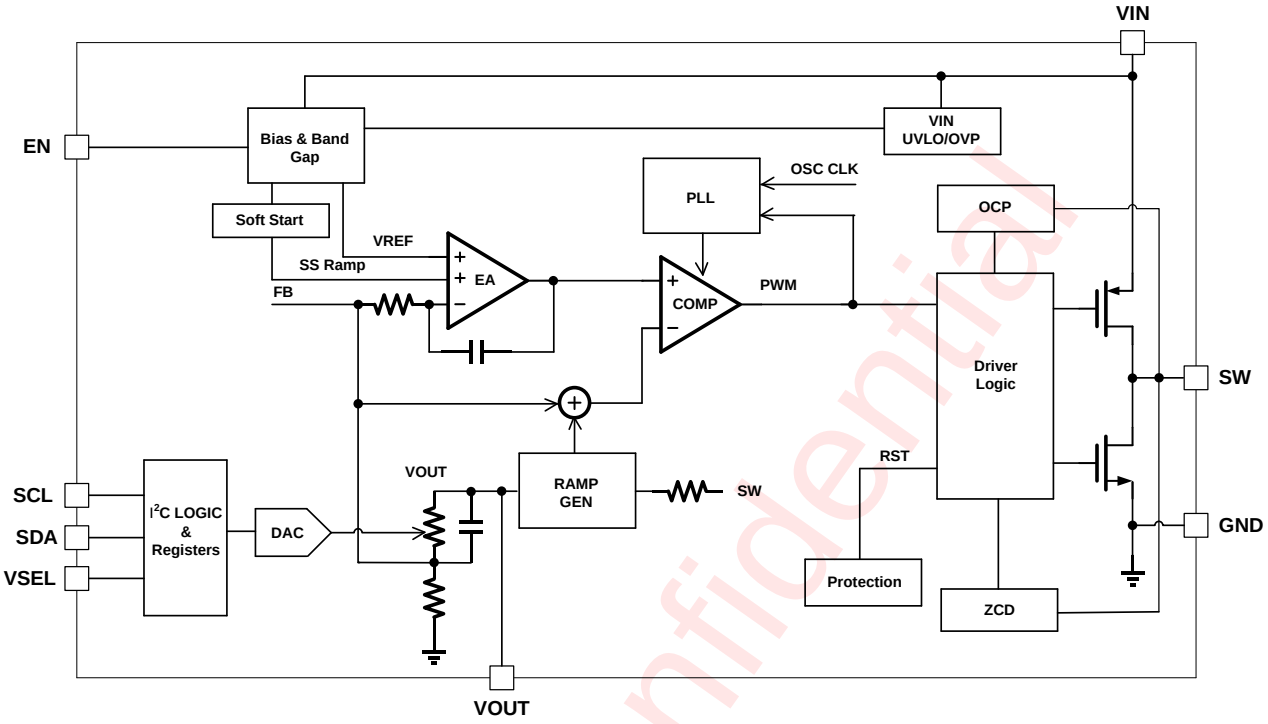


PC8Z - AW37460CSR
XXXX/XXXX/XXXX/XXXX – Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
A1	VSEL	Voltage Select. Set this pin to LOW, VOUT is set by the VSEL0 register. Set this pin to HIGH, VOUT is set by the VSEL1 register.
A2	EN	Enable pin. Set this pin to High to enable the device, low to shutdown. If pulled up to a low−impedance voltage source greater than 1.8 V, use at least 100Ω series resistor, do not leave floating.
A3	SCL	I²C Serial Clock pin.
A4	VOUT	Output voltage sense pin. Connect directly to the output capacitor.
B1	SDA	I²C Serial Data pin.
B2, B3, C1-C4	GND	Power GND pin.
B4	AGND	Analog ground pin.
D1, D2, E1, E2	VIN	Power supply Input Voltage pin.
D3, D4, E3, E4	SW	Switch pin of the power stage.

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37460CSR	-40°C～85°C	WLCSP 2.0mmX1.6mmX0.586 mm-20B	PC8Z	MSL1	ROHS+HF	4500

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Voltage on VIN,SW pins	IC Not Switching	-0.3V to 7V
	IC Switching	-0.3V to 6.5V
Voltage on EN pin	Tied without Series Resistance	-0.3V to 2V
	Tied through Series Resistance of at least 100Ω	-0.3V to VIN
Voltage on VOUT pin		-0.3V to 3V
Voltage on All Other pins	IC Not Switching	-0.3V to VIN
Junction-to-ambient thermal resistance θ_{JA}		49°C /W
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM)		
HBM(NOTE 2)		±2kV
CDM(NOTE 3)		±1.5kV
Latch-Up		
Test condition: JESD78F		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023

NOTE3: All pins. Test Condition: ESDA/JEDEC JS -002-2022

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Supply Voltage Range	2.5		5.5	V
I_{OUT}	Output Current	0		6.5	A
L	Inductor	0.15	0.33	1.2	μH
C_{IN}	Input Capacitor		10		μF
C_{OUT}	Output Capacitor		44		μF
T_A	Ambient temperature	-40		+85	°C

Electrical Characteristics

Typical values are at T_A= 25°C, V_{IN}=5V and EN=High.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_Q	Quiescent Current	I_{LOAD}=0		60	100	μA
		I_{LOAD} =0, Mode Bit=1 (Forced PWM)		40		mA
I_{SD}	Shutdown current	EN=0		0.1	5	μA
		EN=V_{IN}, BUCK_EN$_X$=0		0.1	5	μA
V_{UVLO}	Under−Voltage Lockout Threshold	V_{IN} Rising		2.35		V
V_{UVHYST}	Under−Voltage Lockout Hysteresis			350		mV
V_{IH}	high−Level Input Voltage		1.1			V
V_{IL}	low−Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			160		mV
I_{IN}	Input current	EN=0/V_{IN}		0.01	1	μA
V_{OUT}	Output Voltage Accuracy	I_{LOAD}=0,Auto PFM	-3.5		3.5	%
		I_{LOAD}=0,Forced PWM	-1.5		1.5	%
		V_{IN}=2.5V~5.5V,I_{LOAD}=0~6.5A, Auto PFM	-3.5		3.5	%
LOAD$_{REG}$	Load Regulation	I_{LOAD}=0 to 6.5A,Auto PFM		0.5		%/A
LINE$_{REG}$	Line Regulation	V_{IN}=3V to 4V		0.04		%/A
$R_{DS(ON)}$P	P-MOS On Resistance	V_{IN}=5V,I_{SW}=1A		24		mΩ
$R_{DS(ON)}$N	N-MOS On Resistance	V_{IN}=5V,I_{SW}=1A		12		mΩ
I_{LIMPK}	P−MOS Peak Current Limit		8.5	10.0	11.5	A
t_{SS}	Softstart time	V_{IN}=4V,V_{OUT}=0.9V,C_{OUT}=44μF, no load, 0 to 90%*V_{OUT}		60		μs
t_{TRAN}	Transition time falling	V_{IN}=4V,V_{OUT}=0.9V,C_{OUT}=44μF, Load=100mA,1.05V to 0.6V		100		μs
$I_{LOAD\_DC\_MAX}$	Max Continuous Load Current	V_{IN}=2.5V~5.5V, V_{OUT}=0.9V, T_A=-40°C to 65°C,		5.5		A
		V_{IN}=3.2V~5.5V, V_{OUT}=0.9V, T_A=-40°C to 65°C		6.5		A

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		V_{IN}=2.5V~5.5V, V_{OUT}=0.9V, T_A=-40°C to 85°C		5		A
		V_{IN}=3V~5.5V, V_{OUT}=0.9V, T_A=-40°C to 85°C		5.5		A
V_{OUT_RIPPLE}	Output Ripple	V_{IN}=2.5V~5.5V, V_{OUT}=0.9V, I_{LOAD}=0~6.5A, T_A=-40°C to 65°C, Auto mode		30		mV
		V_{IN}=2.5V~5.5V, V_{OUT}=0.9V, I_{LOAD}=0~6.5A, T_A=-40°C to 65°C, FPWM mode		10		mV
$V_{undershoot}$	Load Transient Response	V_{IN}=2.5V~5.5V, V_{OUT}=0.9V, Load=1.5A to 6A, tr=4μs, tf=2μs		-60		mV
$V_{overshoot}$				60		mV
T_{LIMIT}	Thermal Shutdown			150		℃
T_{HYST}	Thermal Shutdown Hysteresis			20		℃
V_{SDWN}	Input OVP Shutdown	Rising Threshold		6.15		V
		Falling Threshold		5.85		V
f_{SW}	Oscillator Frequency		2.05	2.40	2.75	MHz
Rdis	Output Discharge Resistance	EN=0 or V_{IN}<UVLO		12		Ω

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		Fast Mode Plus			1000	
		High−Speed Mode, C_B ≤ 100 pF			3400	
		High−Speed Mode, C_B ≤ 400 pF			1700	
t_{BUF}	Bus−Free Time between STOP and START Conditions	Standard Mode		4.7		μs
		Fast Mode		1.3		
		Fast Mode Plus		0.5		

$t_{HD;STA}$	START or REPEATED START Hold Time	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		μs
		Fast Mode		1.3		μs
		Fast Mode Plus		0.5		μs
		High−Speed Mode, C_B ≤ 100 pF		160		ns
		High−Speed Mode, C_B ≤ 400 pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode, C_B ≤ 100 pF		60		ns
		High−Speed Mode, C_B ≤ 400 pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		μs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		Fast Mode Plus		50		
		High−Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	μs
		Fast Mode	0		900	ns
		Fast Mode Plus	0		450	ns
		High−Speed Mode, C_B ≤ 100 pF	0		70	ns

		High−Speed Mode, C_B ≤ 400 pF	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	20+0.1C_B		1000	ns
		Fast Mode	20+0.1C_B		300	
		Fast Mode Plus	20+0.1C_B		120	
		High−Speed Mode, C_B ≤ 100 pF		10	80	
		High−Speed Mode, C_B ≤ 400 pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	20+0.1C_B		300	ns
		Fast Mode	20+0.1C_B		300	
		Fast Mode Plus	20+0.1C_B		120	
		High−Speed Mode, C_B ≤ 100 pF		10	40	
		High−Speed Mode, C_B ≤ 400 pF		20	80	
t_{RCL1}	Rise Time of SCL After a REPEATED START Condition and After ACK Bit	High−Speed Mode, C_B ≤ 100 pF		10	80	ns
		High−Speed Mode, C_B ≤ 400 pF		20	160	
t_{RDA}	SDA Rise Time	Standard Mode	20+0.1C_B		1000	ns
		Fast Mode	20+0.1C_B		300	
		Fast Mode Plus	20+0.1C_B		120	
		High−Speed Mode, C_B ≤ 100 pF		10	80	
		High−Speed Mode, C_B ≤ 400 pF		20	160	
t_{FDA}	SDA Fall Time	Standard Mode	20+0.1C_B		300	ns
		Fast Mode	20+0.1C_B		300	
		Fast Mode Plus	20+0.1C_B		120	
		High−Speed Mode, C_B ≤ 100 pF		10	80	
		High−Speed Mode, C_B ≤ 400 pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		120		ns

		High−Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

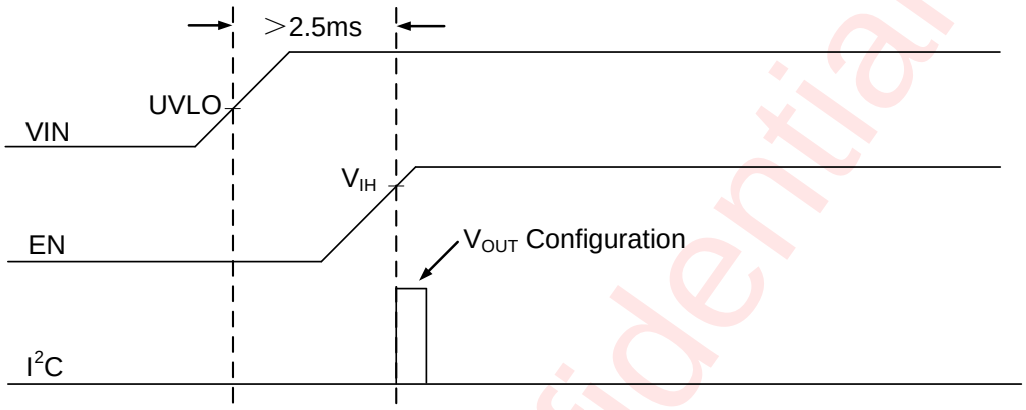


Figure 1. Power on control sequence

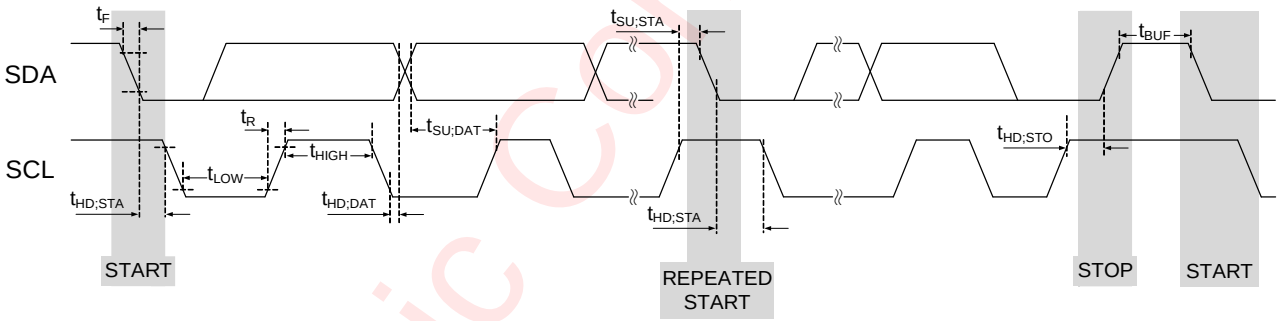
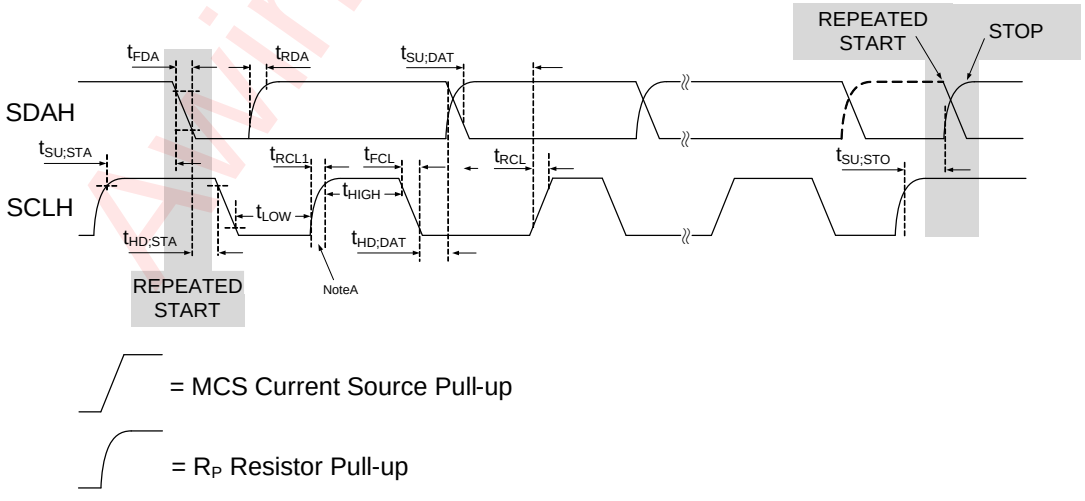


Figure 2. I2C Interface Timing for Fast Plus, Fast, and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit

Figure 3. I²C Interface Timing for High−Speed Mode

Typical Characteristics

Unless otherwise specified, Auto PFM/PWM, VIN = 3.6 V, VOUT = 1.1 V, SCL = SDA = VSEL = EN = 1.8 V, TA = 25°C;

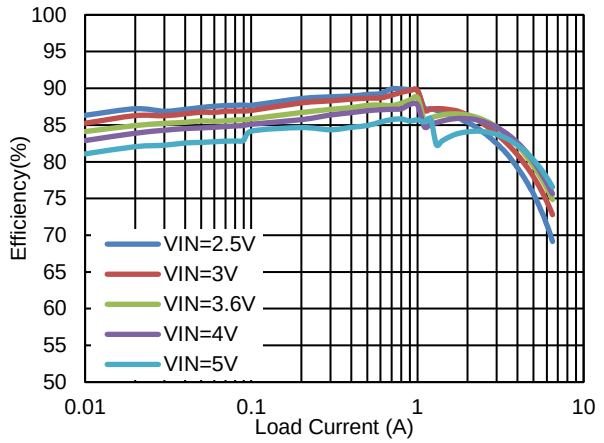


Figure 3. Efficiency vs.Load Current and Input Voltage, V_{OUT}=0.9V

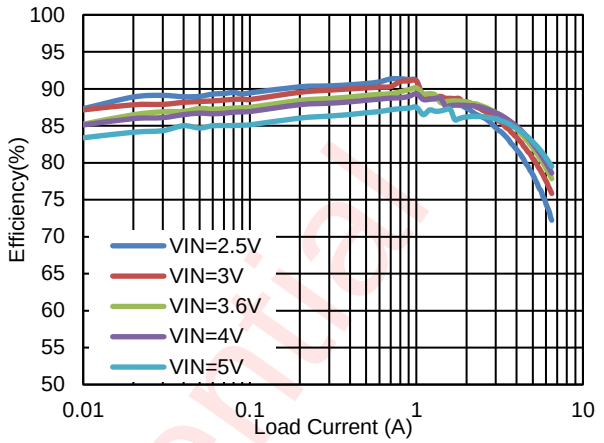


Figure 4. Efficiency vs.Load Current and Input Voltage, V_{OUT}=1.1V

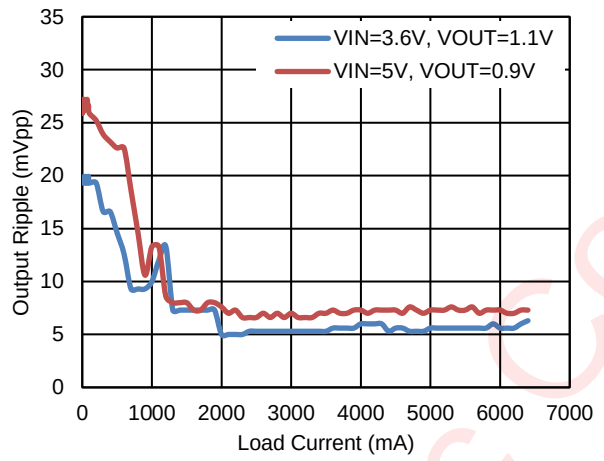


Figure 5. Output Ripple vs.Load Current, V_{IN}=3.6V/5V, V_{OUT}=0.9V/1.1V, Auto

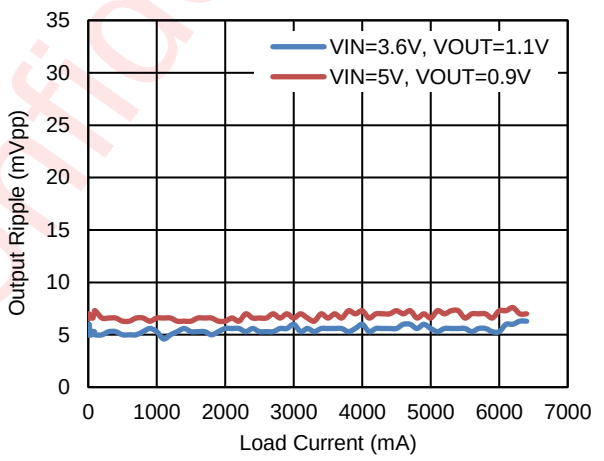


Figure 6. Output Ripple vs.Load Current, V_{IN}=3.6V/5V, V_{OUT}=0.9V/1.1V, FPWM

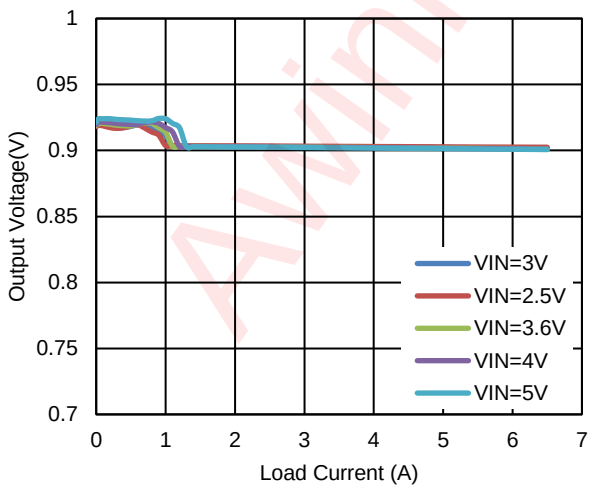


Figure 5. Output Regulation vs.Load Current and Input Voltage, V_{OUT}=0.9V

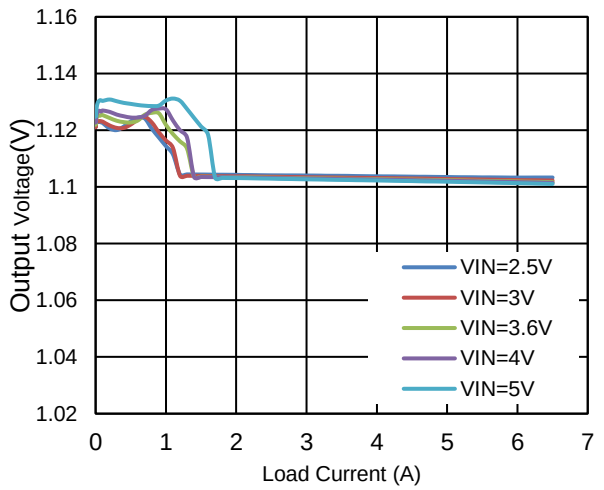


Figure 6. Output Regulation vs.Load Current and Input Voltage, V_{OUT}=1.1V

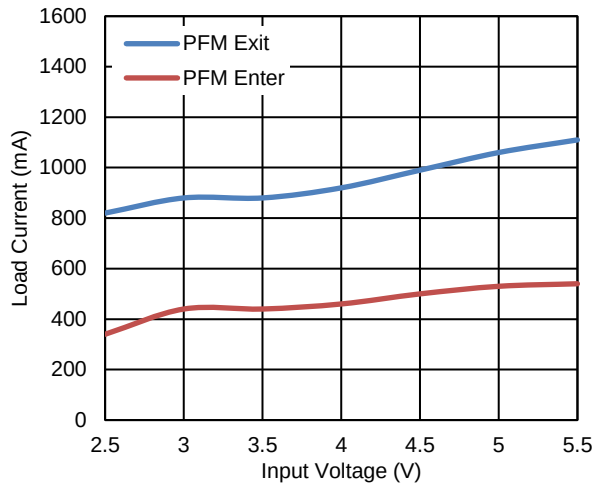


Figure 7. PFM Entry/Exit Level vs.Input Voltage, V_{OUT}=0.9V

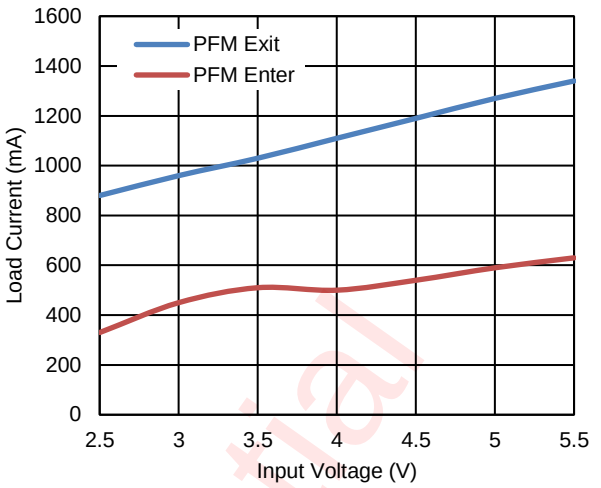


Figure 8. PFM Entry/Exit Level vs.Input Voltage, V_{OUT}=1.1V

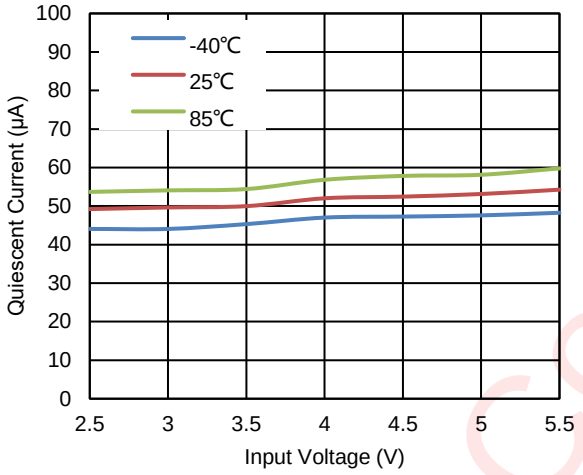


Figure 9. Quiescent Current vs.Input Voltage and Temperature, Auto

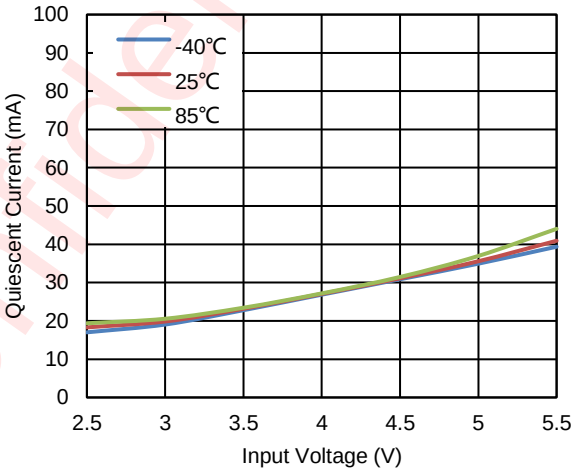


Figure 10. Quiescent Current vs.Input Voltage and Temperature, FPWM

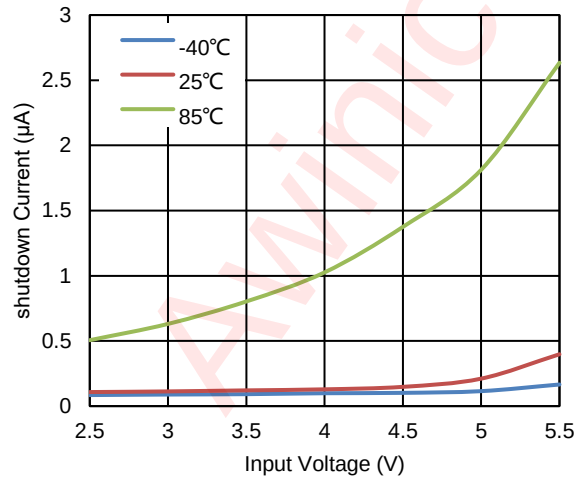


Figure11. Shutdown Current vs.Input Voltage and Temperature

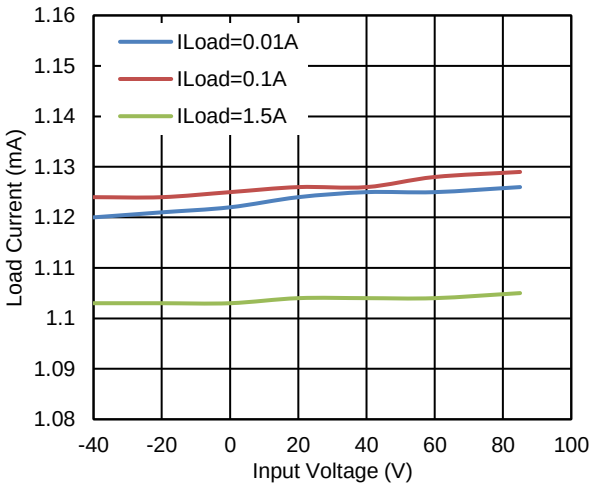


Figure12. Output Voltage vs.Temperature and Load Current

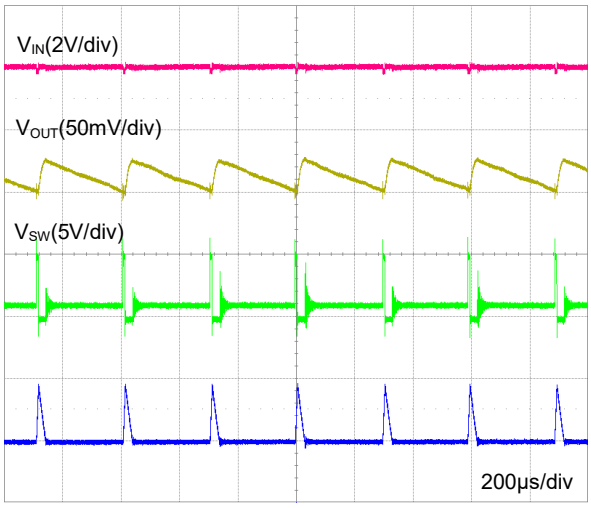


Figure13. PFM Operation, V_{OUT}=1.1V, 0.1A Load

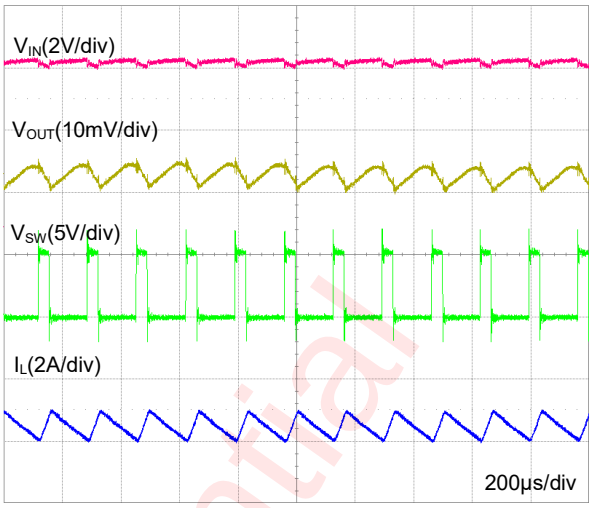


Figure14. PWM Operation, V_{OUT}=1.1V, 3A Load

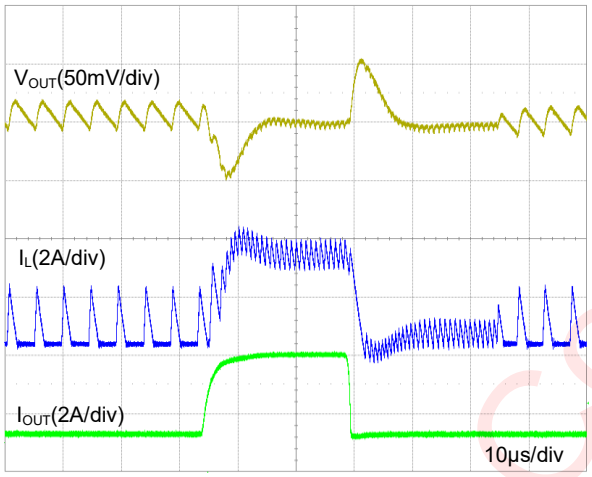


Figure15. Load Transient, V_{OUT}=1.1V, 0.3~3A, t_R=1μs,t_F=100ns

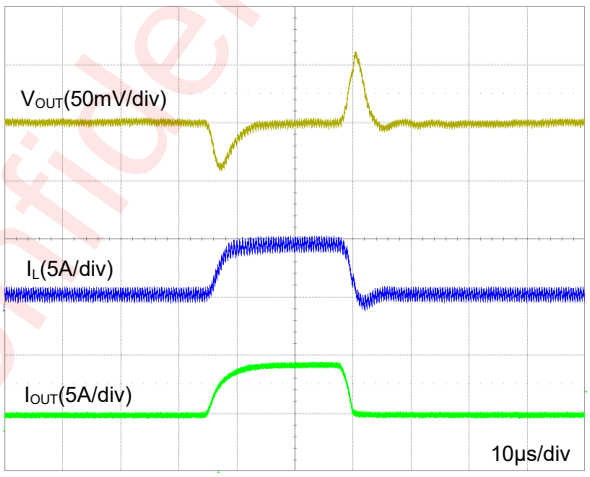


Figure16. Load Transient, V_{OUT}=1.1V, 1.5A~6A, t_R=4μs,t_F=2μs

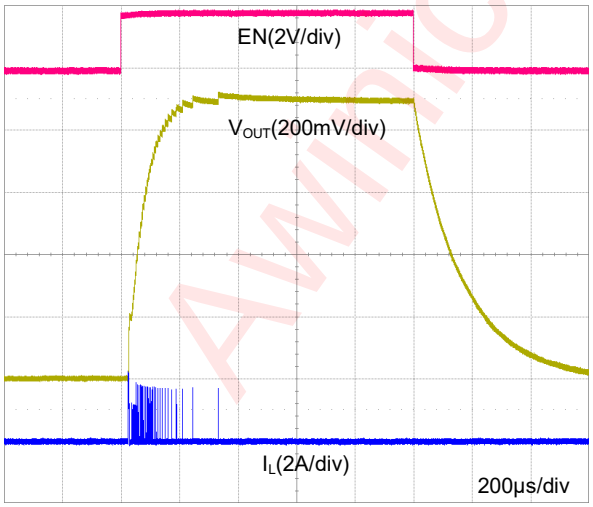


Figure17. Startup/Shutdown, No Load

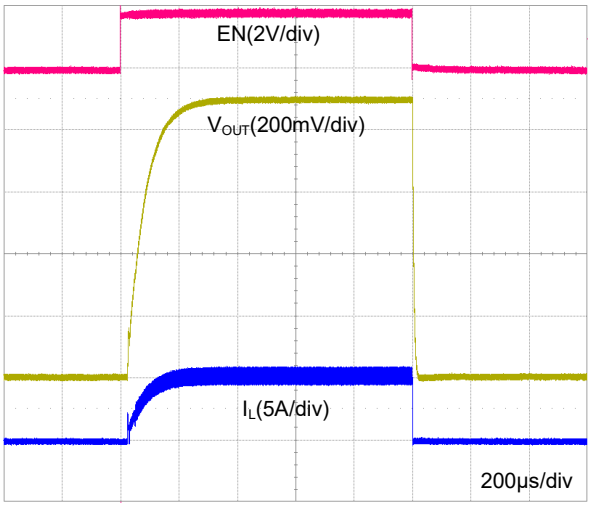


Figure18. Startup/Shutdown, 180mΩ Load

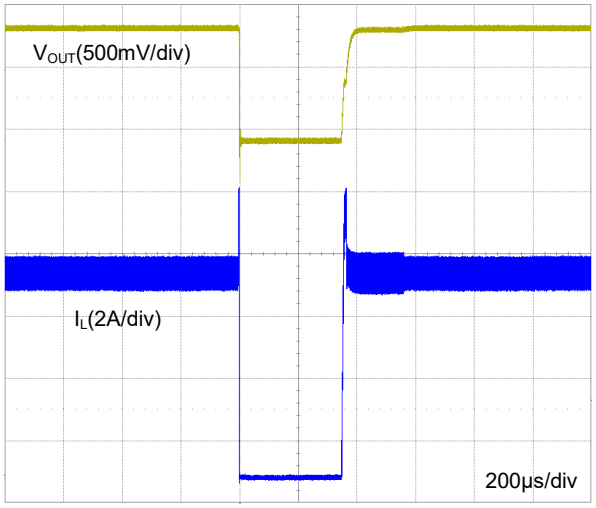


Figure19. Overload Protection and Recovery

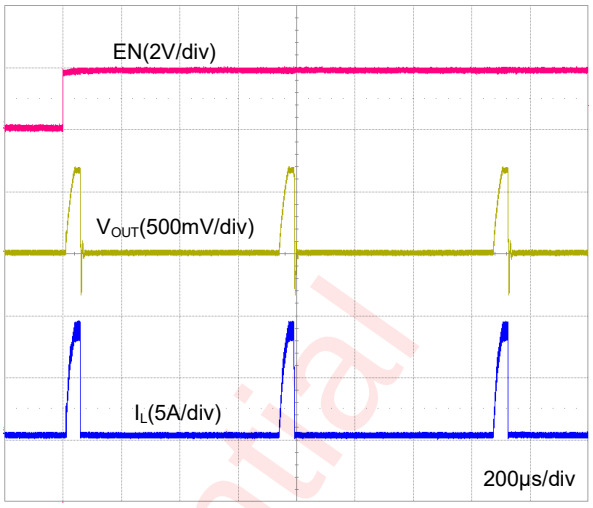


Figure20. Output Short Protection

Detailed Functional Description

The AW37460 is a high efficiency synchronous step-down converter with I²C interface which provide digitally programmable output from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I²C interface capable of operating up to 3.4MHz.The I²C interface can also Control voltage transition slew rate and enable/disable the regulation.

Control Schemme

The AW37460 uses a proprietary non-linear, fixed-frequency PWM modulator to deliver a fast transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the AW37460 operates in DCM single-pulse PFM, which produces low output ripple compare with other PFM architectures. Transition between PWM and PFM is relatively seamless, providing a smooth transition between DCM and CCM Modes.

PFM can be disabled by programming the MODEx bits HIGH (bit6=1 in register 0x00/0x01).

Enable and Soft-Start

When EN pin is LOW, the IC is shut down, all internal circuits are off, and the parts draws very little current. In this state, I²C can be written to or read from as long as input voltage is above the UVLO. The registers keep the content when EN pin is LOW. The registers are reset to default values during a Power On Rese (POR).When the OUTPUT_DISCHARGE bit in the Control register is HIGH (bit7=1 in register 0x02) and EN pin is LOW or the BUCK_ENx bit is LOW (bit7=0 in register 0x00/0x01), an 12Ω load is connected from VOUT to GND to discharge the output capacitors.

Raising EN while the BUCK_ENx bit is HIGH activates the part and begins the soft−start cycle. During soft-start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. Synchronous rectification is inhibited, allowing the IC to start into a pre−charged capacitive load.

If large values of output capacitance are used, the regulator may fail to start. The maximum C_{OUT} capacitance for starting with a heavy constant−current load is approximately:

$$C_{OUTMAX} \approx (I_{LMPK} - I_{LOAD}) \times \frac{320\mu s}{V_{OUT}}$$

where C_{OUTMAX} is expressed in μF and I_{LOAD} is the load current during soft−start, expressed in A.

If the regulator is at its current limit for 16 consecutive current limit cycles, the regulator shuts down and enters tri−state before reattempting soft−start 1700μs later. This limits the duty cycle of full output current during soft−start to prevent excessive heating.

The IC allows for software enable of the regulator, when EN is HIGH, through the BUCK_EN bits. BUCK_EN0 and BUCK_EN1 are both initialized HIGH. These options start after a POR, regardless of the state of the VSEL pin.

Pins		Bits		Output	Mode
EN	VSEL	BUCK_EN0	BUCK_EN1		
0	X	X	X	OFF	Shutdown
1	0	0	X	OFF	Shutdown
1	0	1	X	ON	Auto
1	1	X	0	OFF	Shutdown
1	1	X	1	ON	Auto

VSEL Pin and I²C Programming Output Voltage

The output voltage is set by the NSELx control bits in VSEL0 and VSEL1 registers. The output is given as:

$$C_{OUTMAX}=0.603V+NSELx\times10mV$$

Output voltage can also be controlled by toggling the VSEL pin LOW or HIGH. VSEL LOW corresponds to VSEL0 and VSEL HIGH corresponds to VSEL1. Upon POR, VSEL0 and VSEL1 are reset to their default voltages.

Transition Slew Rate Limiting

When transitioning from a low to high voltage, the IC can be programmed for one of eight possible slew rates using the SLEW bits in the Control register.

Bin	Slew Rate	
000	64	mV/μs
001	32	mV/μs
010	16	mV/μs
011	8	mV/μs
100	4	mV/μs
101	2	mV/μs
110	1	mV/μs
111	0.5	mV/μs

Transitions from high to low voltage rely on the output load to discharge V_{OUT} to the new set point. Once the high−to−low transition begins, the IC stops switching until V_{OUT} has reached the new set point.

Under-Voltage Lockout(UVLO)

When EN is HIGH, the under−voltage lockout keeps thepart from operating until the input supply voltage rises HIGH enough to properly operate. This ensures proper operation of the regulator during startup or shutdown.

Input Over-Voltage Protection(OVP)

When V_{IN} exceeds V_{SDWN} (6.15V), the IC stops switching to protect the circuitry from internal pikes above 6.5 V. An internal filter prevents the circuit from shutting down due to noise spikes.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from causing damage. 16 consecutive current limit cycles in current limit, cause the regulator to shut down and stay off for about 1700μs before attempting a restart.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 20°C hysteresis.

Monitor Register

The Monitor register indicates of the regulation state of the IC. If the IC is enabled and is regulating, its value is (00000101).

I²C Interface

The serial interface is compatible with Standard, Fast, Fast Plus, and HS Mode I²C Bus_ specifications. The SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I²C Slave Address

In hex notation, the slave address assumes a 0 LS Bit. The hex slave address is C0.

Hex	Bits							
	7	6	5	4	3	2	1	0
C0	1	1	0	0	0	0	0	R/ $\overline{W}$

Bus Timing

As shown in Figure 3 data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow sufficient time for the data to set up before the next SCL rising edge.

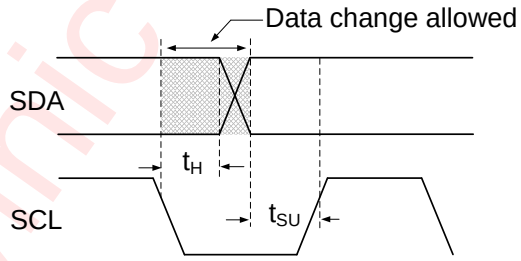


Figure 4. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 4.

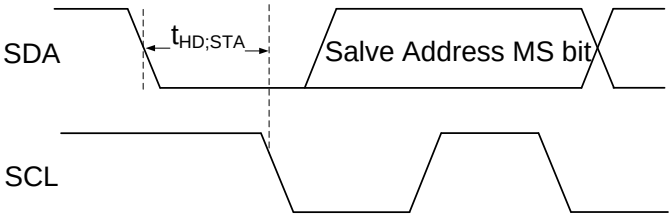


Figure 5. Start Bit

A transaction ends with a STOP condition, defined as SDA transitioning from 0 to 1 with SCL high, as shown in Figure 5.

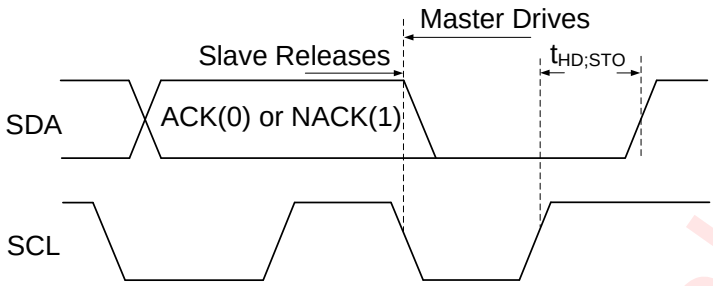


Figure 6. STOP Bit

During a read from the AW37460, the master issues a REPEATED START after sending the register address and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 6.

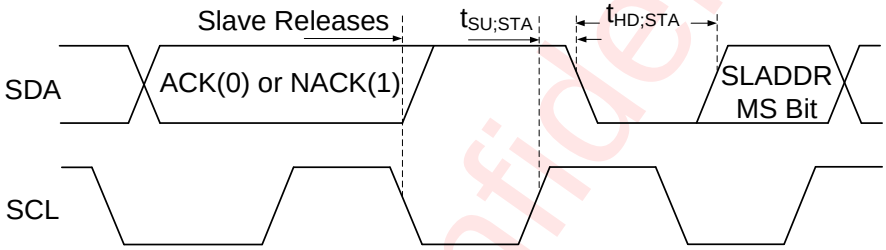


Figure 7. REPEATED START Timing

High-Speed(HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical; except the bus speed for HS Mode is 3.4MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition (Figure 4). The master code is sent in Fast or Fast−Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition (Figure 6) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing. The bus remains in HS Mode until a STOP bit (Figure 5) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 6).

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as:

Master Drives Bus

Slaves Drives Bus

All addresses and data are MSB first.

Symbol	Definition
S	START
P	STOP
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\bar{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	REPEATED START

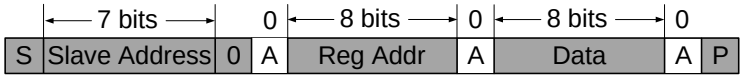


Figure 8. Write Transaction

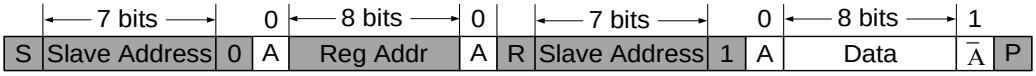


Figure 9. Write Transaction Followed by a Read Transaction

Register configuration

Register Map

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	VSEL0	RW	BUCK_EN0	Mode0	NSEL0						0x9E
0x01	VSEL1	RW	BUCK_EN1	Mode1	NSEL1						0x9E
0x02	Control	RW	Output_Discharge	Slew			Reserve	Reserve	Reserve	Reserve	0x00
0x03	ID1	RO	Vendor			Pgood	DIE ID				0x31
0x04	ID2	RO	Reserve				DIE REV				0x08
0x05	Monitor	RO	Reserve	UVLO	OVP	POS	NEG	RESET_STATUS	OTP	BUCK_STATUS	0x00

Bit Definitions

Bold indicates the default value.

Bit	Name	Value	Description
VSEL0 R/W Register Address: 0x00			
7	BUCK_EN0	**1**	Software buck enable. When EN pin is LOW, the converter is OFF. When EN pin is HIGH, ON/OFF is contolled by BUCK_EN0 bit.
6	Mode0	**0**	The converter operating in Auto PFM mode.
		1	The converter operating in forced PWM mode.
5:0	NSEL0	**011110**	Set output voltage from 0.603V~1.233V in 10mV steps.
VSEL1 R/W Register Address: 0x01			
7	BUCK_EN1	**1**	Software buck enable. When EN pin is LOW, the converter is OFF. When EN pin is HIGH, ON/OFF is contolled by BUCK_EN1 bit.
6	Mode1	**0**	The converter operating in Auto PFM mode.
		1	The converter operating in forced PWM mode.
5:0	NSEL1	**011110**	Set output voltage from 0.603V~1.233V in 10mV steps.
Control R/W Register Address: 0x02			
7	Output_Discharge	**0**	When the converter is disabled, Output is not discharged.
		1	When the converter is disabled, Output discharges through an internal pull-down resister.
6:4	Slew	**000**-111	Set the slew rate of positive output voltage transitions.
3	Reserve	**0**	Reserve
2	Reserve	**0**	Reserve
1:0	Reserve	**00**	Reserve
ID1 RO Register Address: 0x03			

7:5	Vendor	**001**	Signifies AWINIC as the IC vendor
4	Pgood	**0**	1: Buck is enabled and soft-start is completed.
3:0	DIE_ID	**0001**	DIE ID
ID2 RO Register Address: 0x04			
7:4	Reserve	**0000**	Reserve
3:0	DIE_REV	**1000**	DIE REVISION
Monitor RO Register Address: 0x05			
7	Reserve	**0**	Reserve
6	UVLO	**0**	1: Signifies the input voltage is less than the UVLO threshold.
5	OVP	**0**	1: Signifies the input voltage is greater than the OVP threshold.
4	POS	**0**	1: Signifies a positive output voltage transition is in progress and the output voltage has not yet reached its new setpoint. This bit is also set to 1 during soft-start.
3	NEG	**0**	1: Signifies a negative output voltage is in progress and the output voltage has not yet reached its new setpoint.
2	RESET_STATUS	**0**	1: Signifies that a register reset was performed. This bit is cleared after register 0x05 is read.
1	OTP	**0**	1: Signifies the over-temperature protection is active.
0	BUCK_STATUS	**0**	1: The converter is enabled. 0: The converter is disabled

Application information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \times \left(\frac{V_{IN}-V_{OUT}}{L \times f_{SW}}\right)$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current such that:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2}$$

The AW37460 is optimized for operation with L=330nH, but is stable with inductances up to 1.0μH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so decreases the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin−effect losses:

$$I_{RMS} = \sqrt{I_{OUT(DC)}^2 + \frac{\Delta I^2}{12}}$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs and the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Inductor Current Rating

The current−limit circuit can allow substantial peak currents to flow through L1 under worst case conditions. If

it is possible for the load to draw such currents, the inductor should be capable of sustaining the current or failing in a safe manner.

For space−constrained applications, a lower current rating for L1 can be used. The AW37460 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor.

Output Capacitor and V_{OUT} Ripple

If space is at a premium, 0603 capacitors may be used.

Increasing C_{OUT} has negligible effect on loop stability and can be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple(CCM), ΔV_{OUT}, is calculated by:

$$\Delta V_{OUT}=\Delta I_L\left[\frac{f_{SW}\times C_{OUT}\times ESR^2}{2\times D\times(1-D)}+\frac{1}{8\times f_{SW}\times C_{OUT}}\right]$$

where C_{OUT} is the effective output capacitance.

The capacitance of C_{OUT} decreases at higher output voltages, which results in higher ΔV_{OUT}.

The AW37460 can be used with 2 x 22μF output capacitor. If a tighter ripple and transient specification is need, then the 4 x 22μF is recommended.

The lowest ΔV_{OUT} is obtained when the IC is in PWM Mode and, therefore, operating at 2.4 MHz. In PFM Mode, f_{SW} is reduced, causing ΔV_{OUT} to increase.

ESL Effects

The Equivalent Series Inductance (ESL) of the output capacitor network should be kept low to minimize the square−wave component of output ripple that results from the division ratio C_{OUT} ESL and the output inductor (L_{OUT}). The square−wave component due to the ESL can be estimated as:

$$\Delta V_{OUT(SQ)}\approx V_{IN}\times\frac{ESL_{COUT}}{L1}$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value. For example, to obtain C_{OUT}=20μF, a single 22μF 0805 would produce twice the square wave ripple as two × 10μF 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805s have lower ESL than 1206s. If low output ripple is a chief concern, some vendors produce 0508 capacitors with ultra−low ESL. Placing additional small value capacitors near the load also reduces the high−frequency ripple components.

Input Capacitor

The ceramic input capacitors should be placed as close as possible between the VIN and PGND pins to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce under−damped ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective C_{IN} capacitance value decreases as V_{IN} increases due to DC bias effects. This has no significant impact on regulator performance.

Thermal Considerations

Heat is removed from the IC through the solder bumps to the PCB copper. The junction−to−ambient thermal resistance (θ_{JA}) is largely a function of the PCB layout (size, copper weight, and trace width) and the temperature rise from junction to ambient (ΔT).

For the AW37460, θ_{JA} is 49°C/W when mounted on its four−layer with vias evaluation board in still air with 2 oz. outer layer copper weight and 1 oz. inner layer.

For long−term reliable operation, the junction temperature (T_J) should be maintained below 125°C.

To calculate maximum operating temperature (<125°C) for a specific application:

1. Use efficiency graphs to determine efficiency for the desired V_{IN}, V_{OUT}, and load conditions.
2. Calculate total power dissipation using:

$$P_T=V_{OUT}\times I_{LOAD}\times\left(\frac{1}{\eta}-1\right)$$

3. Estimate inductor copper losses using:

$$P_L=I_{LOAD}^2\times DCR_L$$

4. Determine IC losses by removing inductor losses from total dissipation:

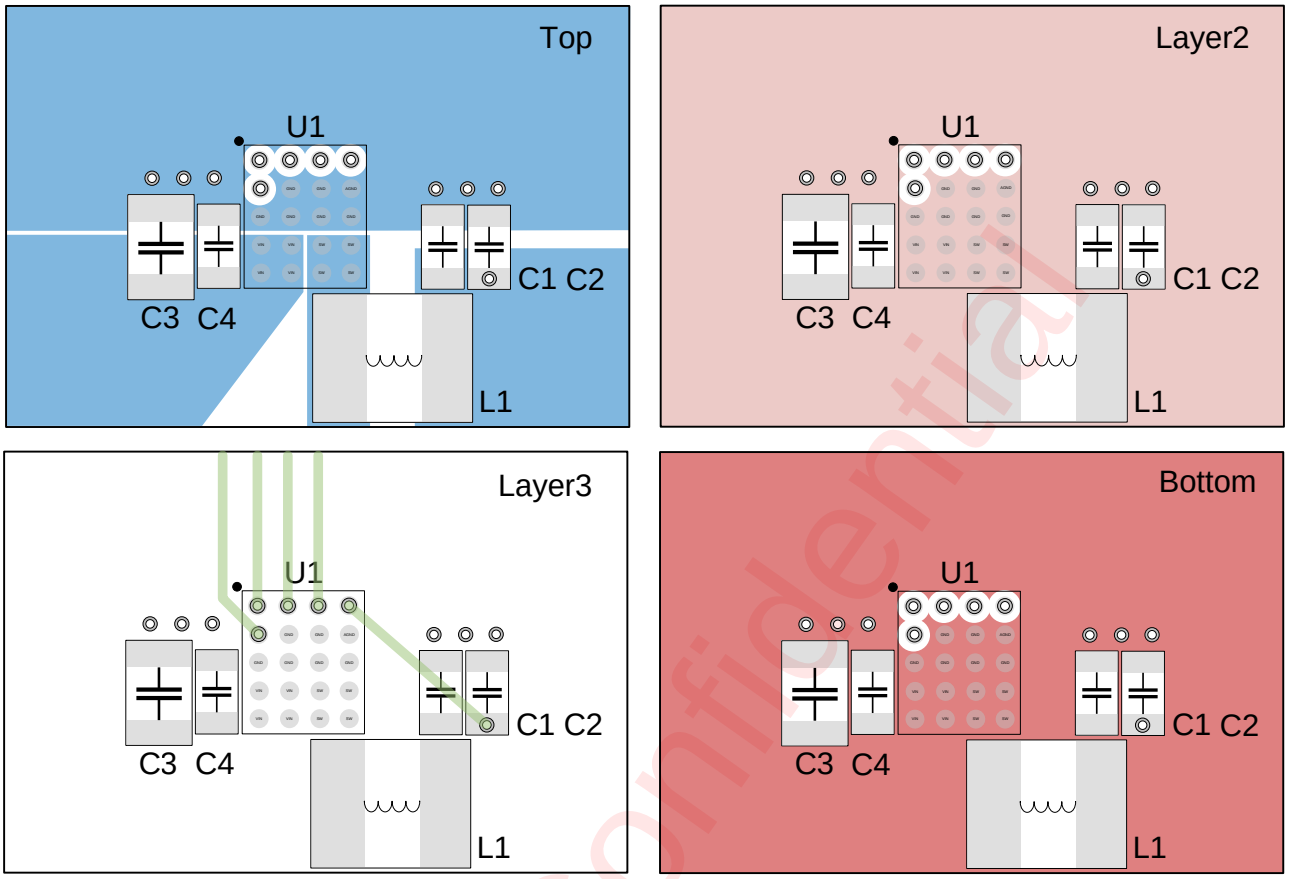
$$P_{IC}=P_T-P_L$$

5. Determine device operating temperature:

$$\Delta T=P_{IC}\times\theta_{JA}$$

$$T_{IC}=T_A+\Delta T$$

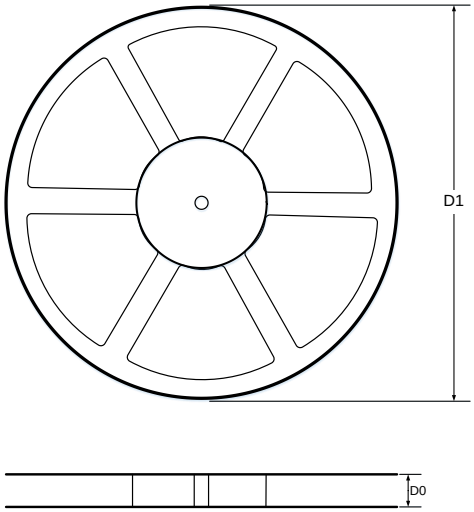
PCB Layout Consideration



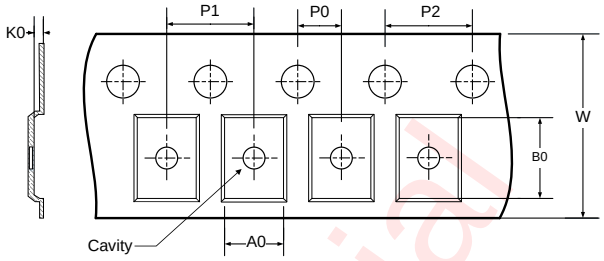
1. The input capacitor (C3, C4) should be connected as close as possible to the VIN and GND pins. Connection to GND better be on top metal.
2. Place the inductor (L1) as close as possible to the IC. Use short wide traces for the main current paths.Do not roure through vias.
3. The output capacitor (C1, C2) should be placed as close as possible to the IC. Connection to GND better be on top metal.
4. Feedback signal connection to VOUT should be routed away from noisy components and traces (e.g. SW line).

Tape And Reel Information

REEL DIMENSIONS

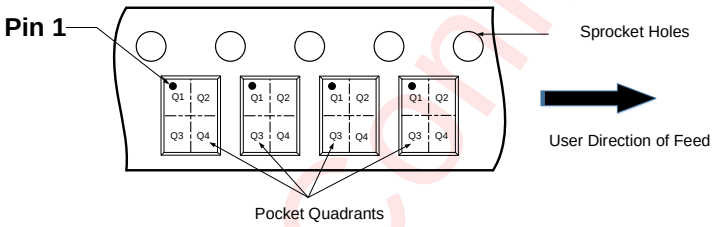


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



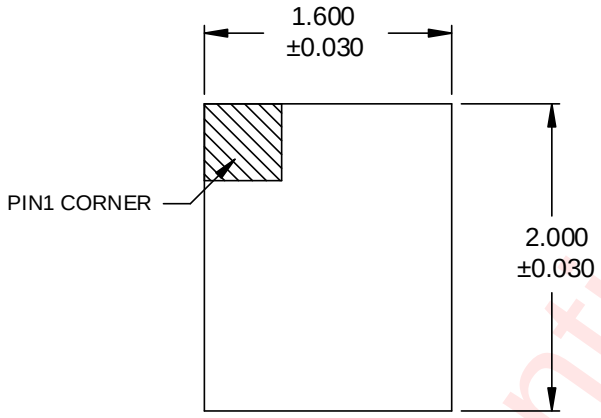
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

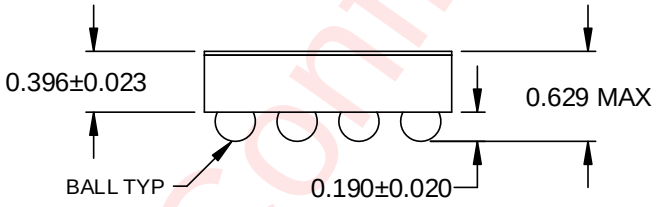
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.69	2.19	0.68	2	4	4	8	Q1

All dimensions are nominal

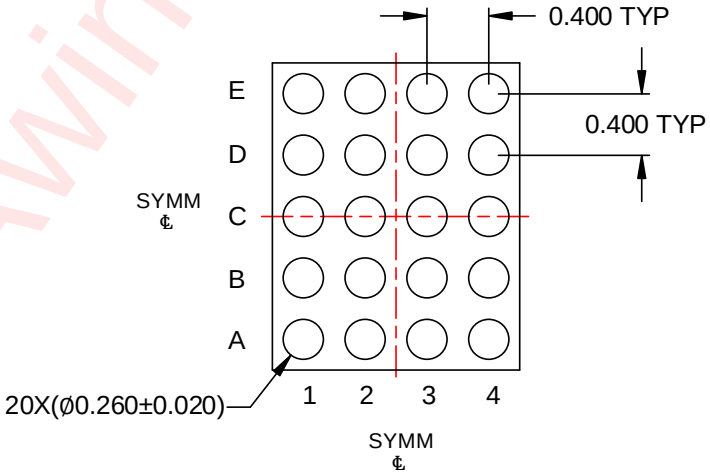
Package Description



Top View



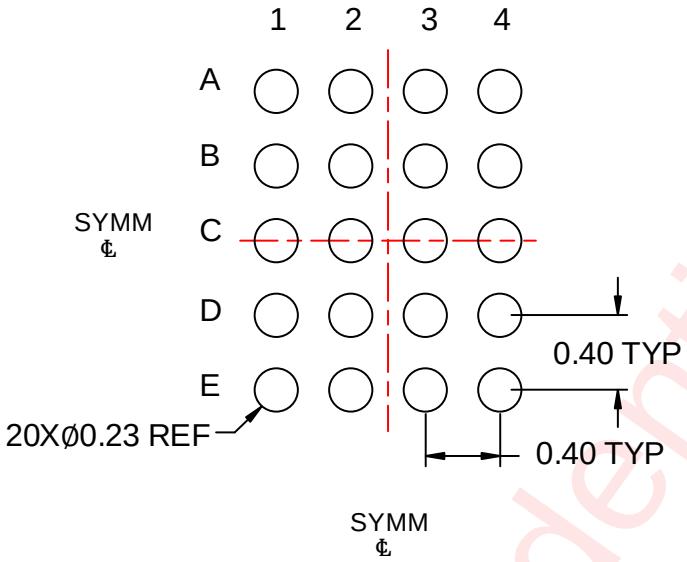
Side View

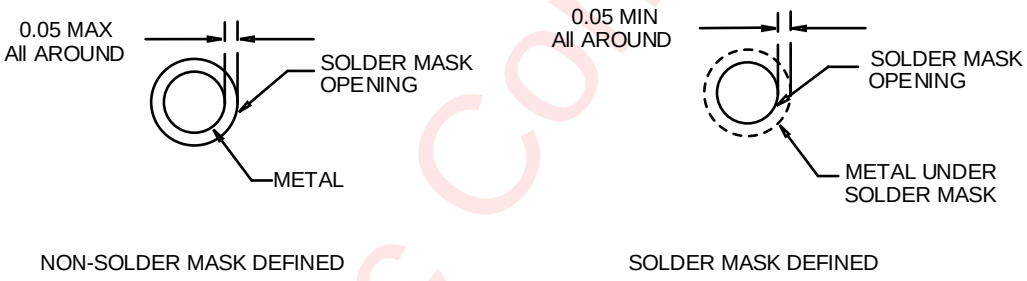


Bottom View

Unit:mm

Land Pattern Data





NON-SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jun. 2024	Officially released
V1.1	Dec. 2024	Add electrical characteristics of t_{SS}, t_{TRAN}, $I_{LOAD\_DC\_MAX}$, V_{OUT_RIPPLE}, $V_{undershoot}$, $V_{overshoot}$ (P5, P6) Add Power on sequence(P9)

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