

High Current, High Accuracy, Low Noise Linear Regulator

Features

- Input voltage range:
1.4V \leq VIN<7.5V, Without Bias
1.1V \leq VIN<7.5V, With Bias
- ANY-OUT Operation:
0.80V to 3.95V Output Voltage Range
- Adjustable Operation:
0.80V to 5.2V Output Voltage Range
- Output Voltage Accuracy: 1%(Max) Over Line, Load and Temperature With Bias
- Low Dropout Voltage:180mV (Max.) @ 3A
- Output Voltage Noise:
5 μ Vrms @ 0.8V Output
11 μ Vrms @ 5.0V Output
- PSRR: typical 40dB @ 10kHz
- Excellent Load Transient Response
- Adjustable Soft-Start Control
- Open-Drain Power-Good Output
- Current Limit Protection
- Over Temperature Protection
- Stable with A 47 μ F or Larger Ceramic Output Capacitor
- QFN 3.5mmx3.5mm-20L package

Applications

Macro remote radio units (RRU)
Outdoor backhaul units
Lab and field instrumentation
Sensor, imaging, and radar

General Description

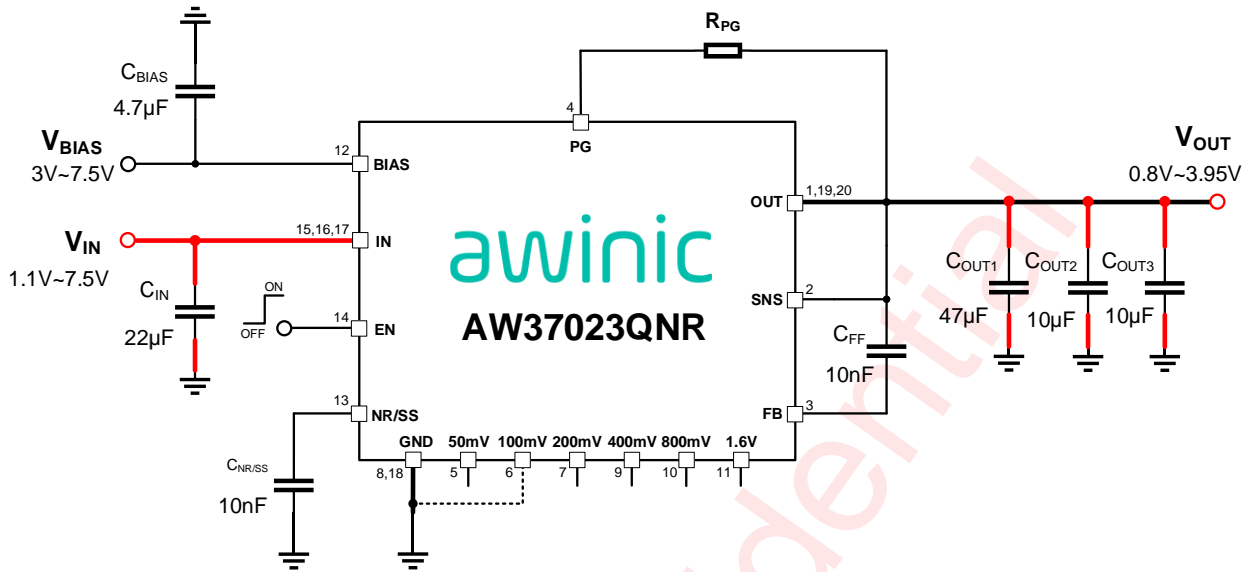
The AW37023 is a low-noise (5 μ Vrms), low-dropout linear regulator capable of sourcing 3A with only 160mV of maximum dropout. The combination of low noise, high PSRR, and high output current capability makes the AW37023 an excellent choice to power noise-sensitive components, such as those found in radar power and infotainment applications.

The AW37023 output voltage is pin-programmable from 0.8V to 3.95V, and adjustable from 0.8V to 5.2V using an external resistor divider.

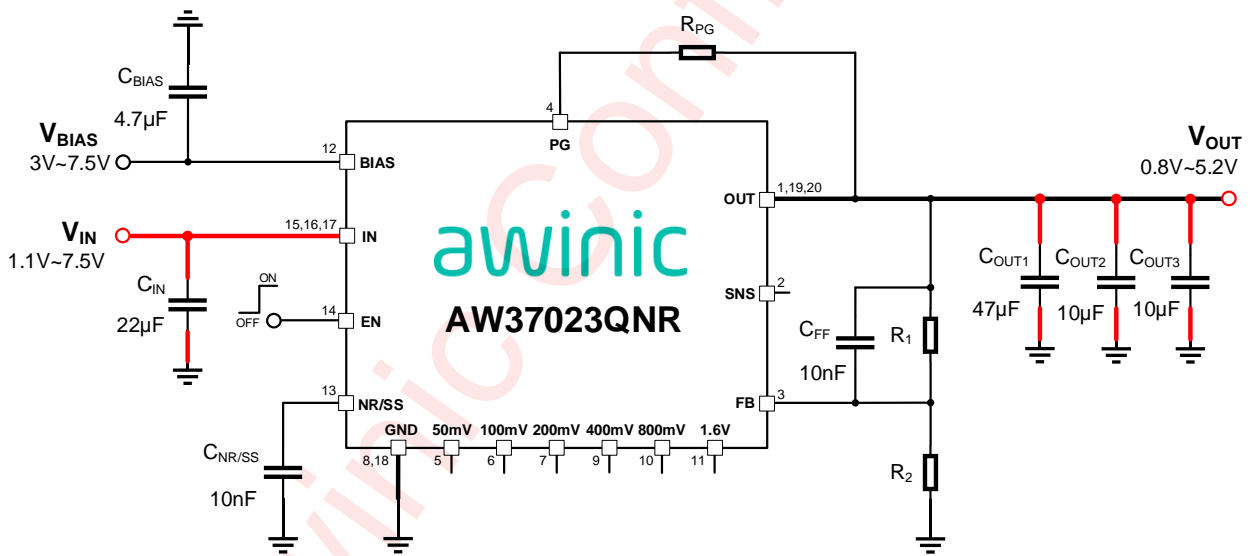
The high performance of the AW37023 limits power supply generated phase noise and clock jitter, making the AW37023 ideal for powering RF amplifiers, radar sensors, and chipsets. Specifically, RF amplifiers benefit from the high-performance and 5.0V output capability of the device.

For digital loads such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs) that require low-input, low-output (LILO) voltage operation, the exceptional accuracy (1% over load and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the AW37023 provide optimal system performance.

Typical Application Circuit

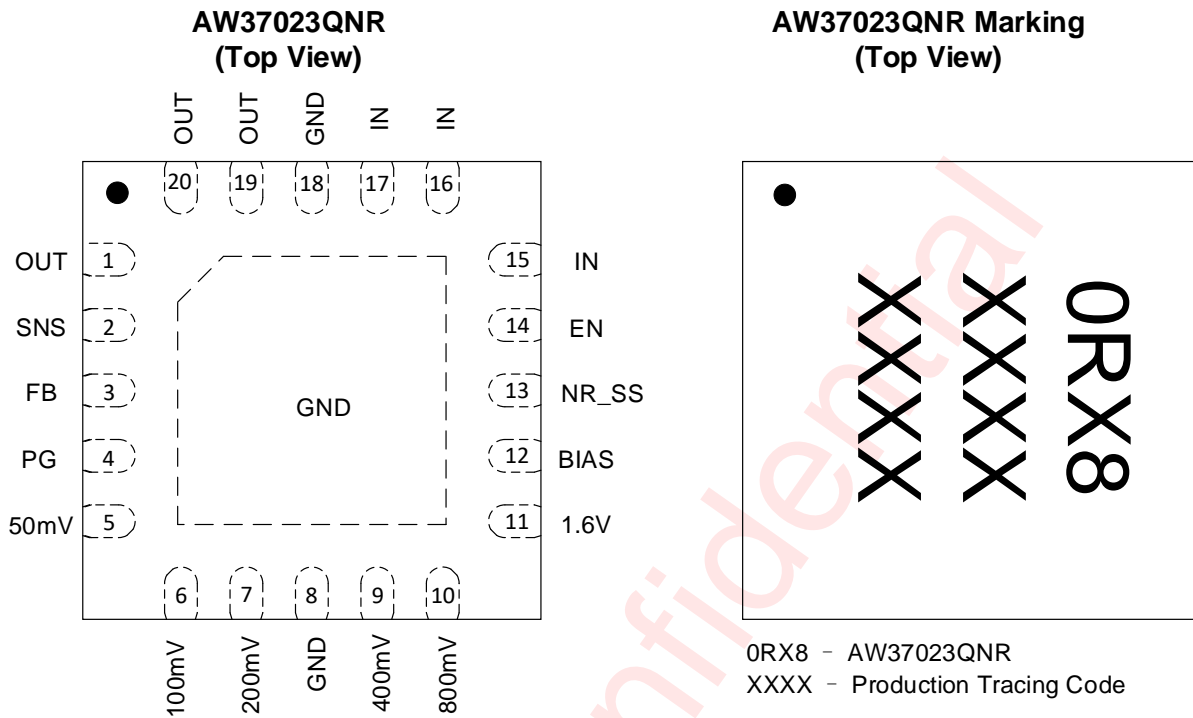


Application Circuit with ANY-OUT Configuration



Application Circuit with External Resistance Configuration

Pin Configuration And Top Mark

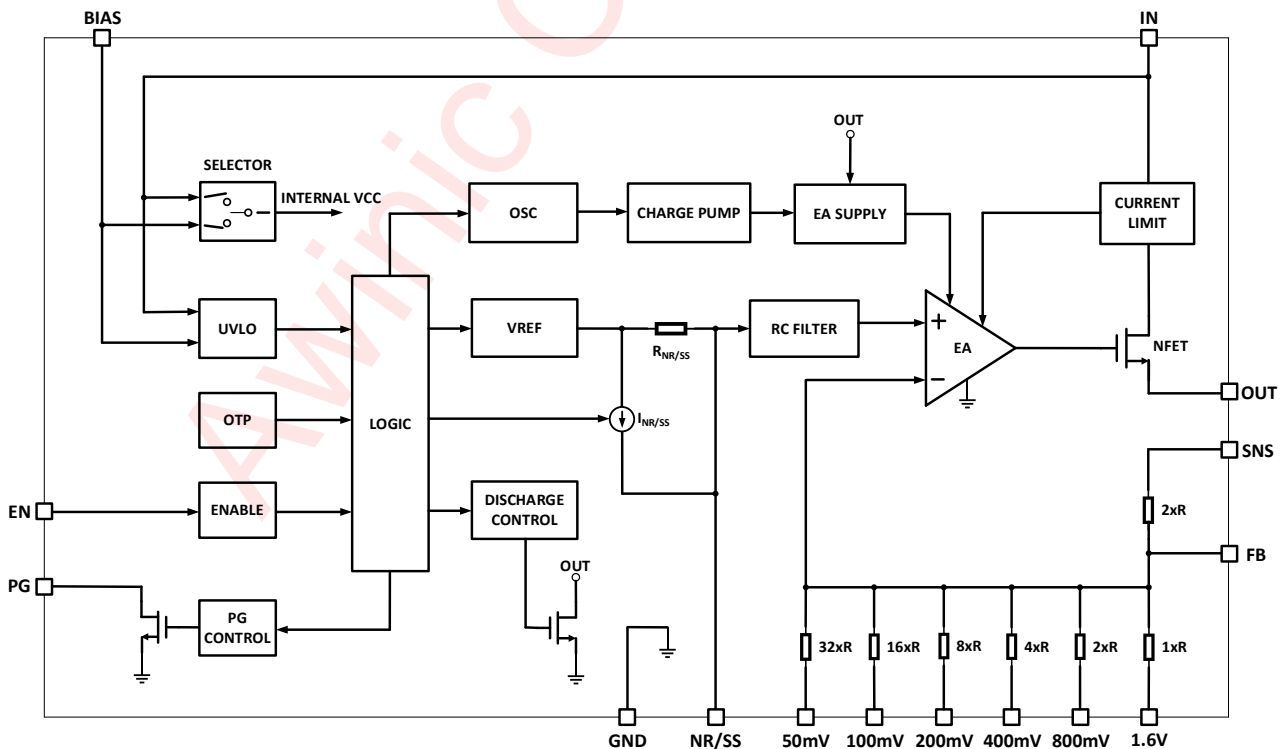


Pin Definition

No.	NAME	DESCRIPTION
1, 19, 20	OUT	Regulated output pin. A 47 μ F or larger ceramic capacitor from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load.
2	SNS	Output voltage sense input pin. This pin connects the internal R1 resistor to the output. Connect this pin to the load side of the output trace only if the ANY-OUT feature is used. If the ANY-OUT feature is not used, leave this pin floating.
3	FB	Feedback pin connected to the error amplifier. Although not required, a 10nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended to maximize ac performance. The use of a feed-forward capacitor can disrupt PG (power good) functionality.
4	PG	Active-high, power-good pin. An open-drain output indicates when the output voltage reaches V_{IT_PG} of the target. The use of a feed-forward capacitor can disrupt PG (power good) functionality.
5	50mV	ANY-OUT voltage setting pins. Connect these pins to ground, SNS, or leave floating. Connecting these pins to ground increases the output voltage, whereas connecting these pins to SNS increases the resolution of the ANY-OUT network but decreases the range of the network; multiple pins can be simultaneously connected to GND or SNS to select the desired output voltage. Leave these pins floating (open) when not in use.
6	100mV	
7	200mV	
9	400mV	
10	800mV	
11	1.6V	

12	BIAS	BIAS supply voltage. This pin enables the use of low-input voltage, low-output (LILo) voltage conditions (that is, $V_{IN}=1.2V$, $V_{OUT}=1V$) to reduce power dissipation across the die. The use of a BIAS voltage improves dc and ac performance for $V_{IN} \leq 2.2V$. A $4.7\mu F$ capacitor or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
13	NR/SS	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a $10nF$ or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance.
14	EN	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN. If enable functionality is required, V_{EN} must always be high after V_{IN} is established when a BIAS supply is used.
15, 16, 17	IN	Input supply voltage pin. A $22\mu F$ or larger ceramic capacitor from IN to ground is recommended to reduce the impedance of the input supply. Place the input capacitor as close to the input as possible.
8, 18	GND	Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection.

Functional Block Diagram



Typical Application Circuit

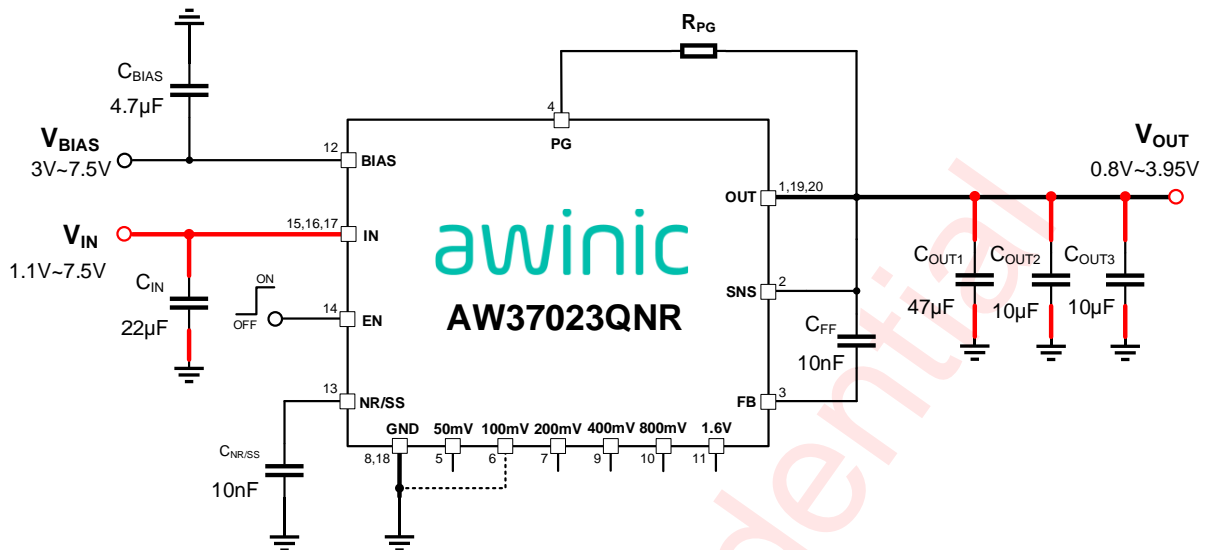


Figure 1 Application Circuit with ANY-OUT Configuration

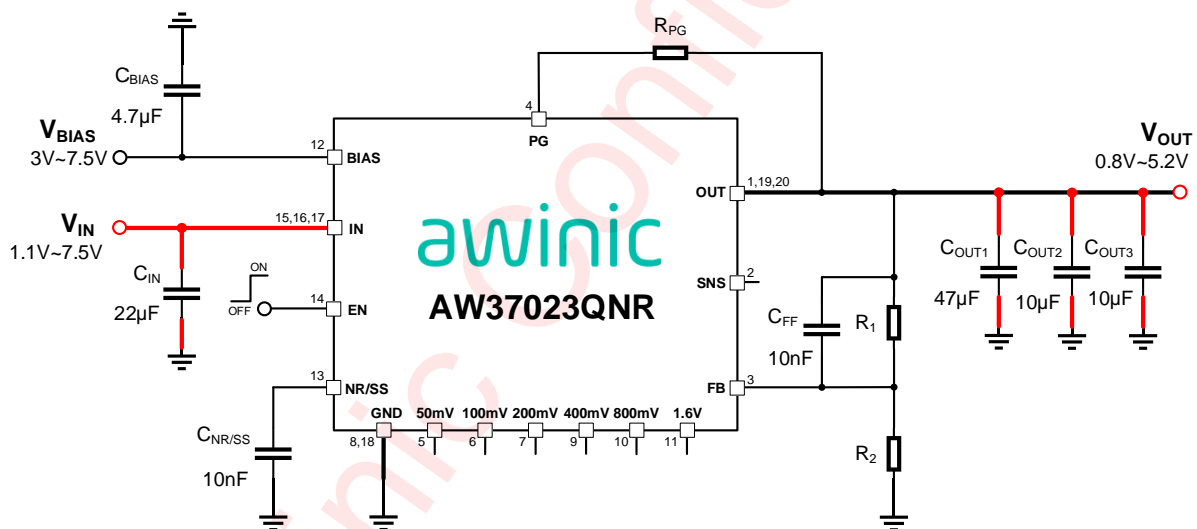


Figure 2 Application Circuit with External Resistance Configuration

Notice for typical application circuits:

1. Capacitance of C_{IN} should be $22\mu F$ or more and C_{OUT} should be $47\mu F$ or more.
2. A $4.7\mu F$ capacitor or larger must be connected between BIAS pin and ground.
3. A $10nF$ feed-forward capacitor from FB to OUT and a $10nF$ or larger capacitor from NR/SS to GND (as close to the device as possible) is recommended to maximize ac performance.
4. The rated voltage of C_{IN} and C_{OUT} should be higher than V_{IN} and V_{OUT} voltage.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37023QNR	$-40^{\circ}C \sim 125^{\circ}C$	QFN 3.5mm×3.5mm-20L	0RX8	MSL3	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
IN, BIAS, PG, EN	-0.3V to 9V
SNS, OUT	-0.3V to $V_{IN}+0.3V$
NR/SS, FB	-0.3V to 3.6V
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	-0.3V to $V_{OUT}+0.3V$
Maximum operating junction temperature T_{J_MAX}	150°C
Operating free-air temperature range	-40°C to 125°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
Junction-to-ambient thermal resistance θ_{JA} ^(NOTE2)	51.08°C/W
ESD	
HBM (Human body model) ^(NOTE3)	±4.5kV
CDM (Charged device model) ^(NOTE4)	±2kV
Latch-Up	
Latch-Up ^(NOTE5)	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient follows JEDEC 2S2P standards, and is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001:2023.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002:2022.

NOTE5: Test Condition: JESD78F.02: 2023.

Recommended Operating Conditions^(NOTE1)

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT
V _{IN}	IN Supply Voltage Range	1.1		7.5	V
V _{BIAS}	BIAS Supply Voltage Range ^(NOTE2)	3		7.5	V
V _{OUT}	Output Supply Voltage Range ^(NOTE3)	0.8		5.2	V
V _{EN}	Enable Voltage Range	0		V _{IN}	V
I _{OUT}	Output Current	0		3	A
C _{IN}	IN Input Capacitor	22	47		μF
C _{OUT}	Output Capacitor	47	47//10/10 ^(NOTE4)	1000	μF
C _{BIAS}	BIAS Input Capacitor	4.7			μF
C _{NR/SS}	NR/SS Capacitor	0	10	100	nF
C _{FF}	Feed-Forward Capacitor		10		nF
R _{PG}	Power-Good Pull-up Resistance	10		100	kΩ
R ₁	Top Resistor Value in Feedback Network for Adjustable Operation		12.1 ^(NOTE5)		kΩ
R ₂	Bottom Resistor Value in Feedback Network for Adjustable Operation			160 ^(NOTE6)	kΩ
T _J	Operating Junction Temperature	-40		125	°C

NOTE1: Over junction temperature range (unless otherwise noted).

NOTE2: BIAS supply is required when the V_{IN} supply is below 1.4V. Conversely, no BIAS supply is required when the V_{IN} supply is higher than or equal to 1.4V.

NOTE2: This output voltage range does not include device accuracy or accuracy of the feedback resistors.

NOTE4: The recommended output capacitors are selected to optimize PSRR for the frequency range of 400 kHz to 700 kHz. This frequency range is a typical value for dc-dc supplies.

NOTE5: The 12.1kΩ resistor is selected to optimize PSRR and noise by matching the internal R₁ value.

NOTE6: The upper limit for the R₂ resistor is to ensure accuracy by making the current through the feedback network much larger than the leakage current into the feedback node.

Electrical Characteristics

$V_{IN}=1.4V$ or $V_{IN}=V_{OUT(SET)}+0.4V$ (whichever is greater), $V_{BIAS}=\text{open}$, $V_{OUT(SET)}=0.8V$, $V_{EN}=1.1V$, $C_{IN}=22\mu F$, $C_{OUT}=47\mu F$, $C_{NR/SS}=10nF$, $C_{FF}=10nF$, and PG pin pulled up to V_{IN} with $10k\Omega$, unless otherwise noted. $T_A=25^\circ C$, unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		1.1		7.5	V
V_{BIAS}	BIAS Voltage Range		3		7.5	V
V_{OUT}	Output Voltage Range	Using the ANY-OUT Pins	0.8		3.95	V
		Using External Resistors	0.8		5.2	V
V_{OUT_ACC}	Output Voltage Accuracy	$1.4V \leq V_{IN} \leq 7V$, without V_{BIAS} , $5mA \leq I_{OUT} \leq 3A$, Adjustable Operation	-0.7		0.7	%
		$V_{IN}=1.2V$, $3V \leq V_{BIAS} \leq 7V$, $5mA \leq I_{OUT} \leq 3A$, Adjustable Operation	-0.7		0.7	%
		$I_{OUT}=5mA$, ANY-OUT Operation	-1.4		1.4	%
V_{UVLO1_IN}	Input Supply UVLO with BIAS	V_{IN} Rising, $V_{BIAS}=3V$		0.89	1.05	V
		Hysteresis		55		mV
V_{UVLO2_IN}	Input Supply UVLO without BIAS	V_{IN} Rising		1.09	1.35	V
		Hysteresis		55		mV
V_{UVLO_BIAS}	Bias Supply UVLO	V_{BIAS} Rising, $V_{IN}=1.1V$		2.5	2.8	V
		Hysteresis		75		mV
V_{FB}	Feedback Voltage			0.8		V
$V_{NR/SS}$	NR/SS Pin Voltage			0.8		V
$LINE_{Reg}$	V_{IN} Line Regulation	$I_{OUT}=5mA$, $1.4V \leq V_{IN} \leq 7V$		0.05	2	mV/V
$LOAD_{Reg}$	Load Regulation	$V_{IN}=1.2V$, $3V \leq V_{BIAS} \leq 7V$, $5mA \leq I_{OUT} \leq 3A$		0.1	2.7	mV/A
		$5mA \leq I_{OUT} \leq 3A$		0.1	2.7	
		$5mA \leq I_{OUT} \leq 3A$, $V_{OUT}=5V$		0.7	5	
V_{DROP}	V_{IN} Dropout Voltage	$V_{IN}=1.4V$, without V_{BIAS} , $I_{OUT}=3A$, $V_{FB}=0.776V$		120	150	mV
		$V_{IN}=5.2V$, without V_{BIAS} , $I_{OUT}=3A$, $V_{FB}=0.776V$		120	150	mV
		$V_{IN}=1.2V$, $V_{BIAS}=5V$, $I_{OUT}=3A$, $V_{FB}=0.776V$		120	150	mV
I_{LIM}	Output Current Limit	$V_{OUT}=90\% * V_{OUT(SET)}$	3.1	4.2		A
I_{SC}	Short Current Limit	$V_{OUT}=0V$		1.2		A
I_{GND}	GND Pin Current	$V_{IN}=7V$, $I_{OUT}=5mA$		4.3	7	mA
		$V_{IN}=1.4V$, $I_{OUT}=3A$		4.3	7	

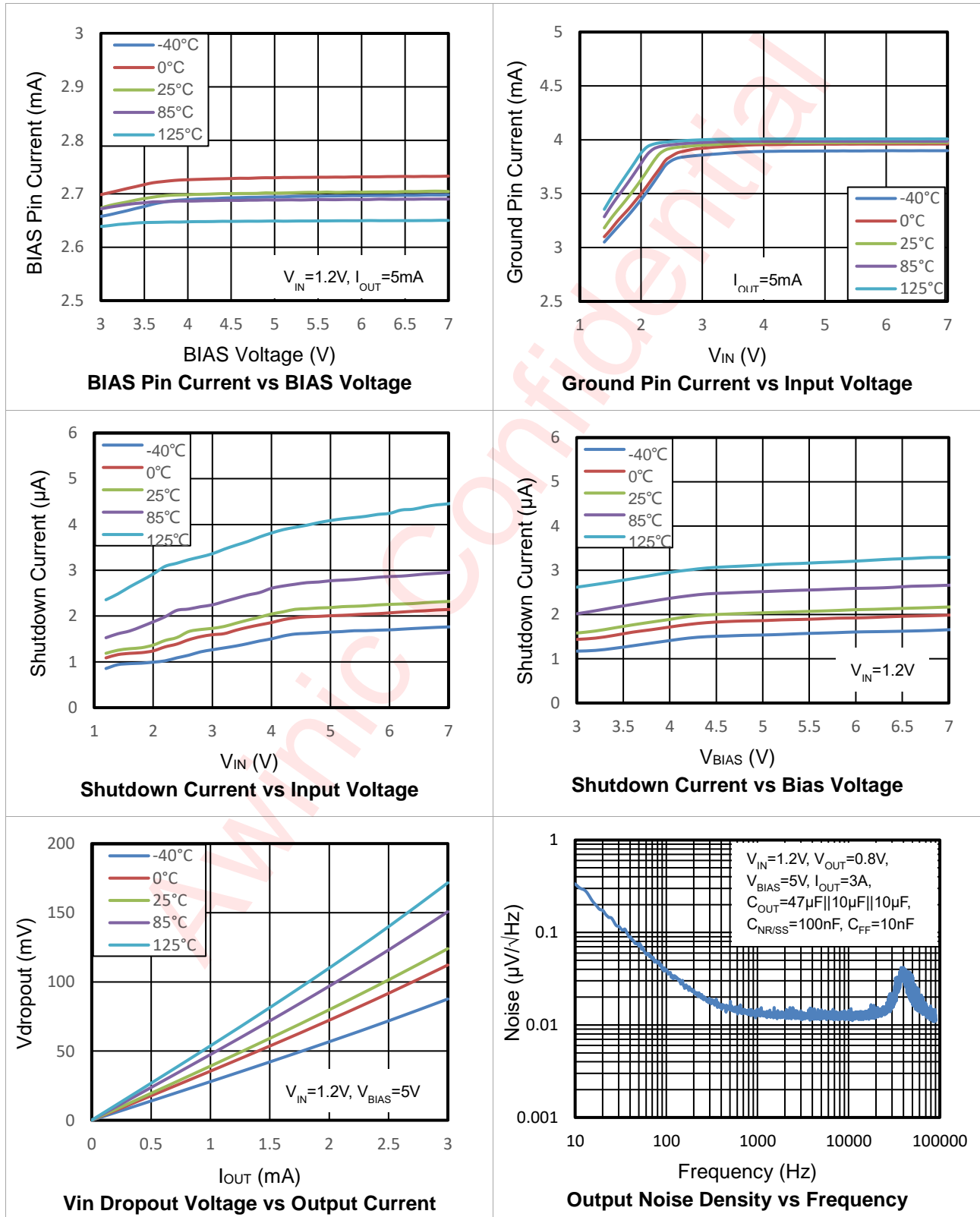
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I _{SHDN}	Shutdown Current	Shutdown, PG=open, V _{IN} =7V, V _{EN} =0.5V		2.5	8	μA
I _{EN}	EN Pin Current	V _{IN} =7V, V _{EN} =0V and 7V	-1.5		1.5	μA
I _{BIAS}	BIAS Pin Current	V _{IN} =1.2V, V _{BIAS} =7V, V _{OUT(SET)} =0.8V, I _{OUT} =3 A		3.5	5.5	mA
I _{FB}	FB Pin Leakage Current	V _{IN} =7V	-0.1		0.1	μA
PSRR_ V _{IN}	Power Supply Ripple Rejection	V _{IN} -V _{OUT} =0.4V, I _{OUT} =3A, C _{NR/SS} =100nF, C _{FF} =10nF, C _{OUT} =22μF	f=10kHz, V _{OUT} =0.8V, V _{BIAS} =5.0V	42		dB
			f=500kHz, V _{OUT} =0.8V, V _{BIAS} =5.0V	36		dB
			f=10kHz, V _{OUT} =5V	40		dB
			f=500kHz, V _{OUT} =5V	25		dB
V _N	Output Voltage Noise	BW=10Hz to 100kHz, V _{IN} =1.1V, V _{OUT} =0.8V, V _{BIAS} =5.0V, I _{OUT} =3A, C _{NR/SS} =100nF, C _{FF} =10nF, C _{OUT} =47μF 10μF 10μF		5		μVrms
			BW=10Hz to 100kHz, V _{OUT} =5V, I _{OUT} =3A, C _{NR/SS} =100nF, C _{FF} =10nF, C _{OUT} =47μF 10μF 10μF		11	
V _{ENH}	EN Threshold Voltage	EN Input Voltage "H"	1.05			V
V _{ENL}		EN Input Voltage "L"			0.55	V
V _{IT_PG}	PG Pin Threshold	For Falling V _{OUT}	84%* V _{OUT}	89%* V _{OUT}	93%* V _{OUT}	V
V _{HYS_PG}	PG Pin Hysteresis	For Rising V _{OUT}		0.88% * V _{OUT}		V
V _{OL_PG}	PG Pin Low-Level Output Voltage	V _{OUT} <V _{IT_PG} , I _{PG} =-1mA (Current into Device)		0.15	0.4	V
I _{LKG_PG}	PG pin leakage current	V _{OUT} >V _{IT_PG} , V _{PG} =7V		0.01	0.8	μA
I _{NR/SS}	NR/SS Pin Charging Current	V _{NR/SS} =GND, V _{IN} =7V	3.1	5.7	8.5	μA
R _{DIS}	Output Discharge Resistance	V _{IN} =1.4V, V _{EN} =0V, V _{OUT} =0.5V	100	260	450	Ω
T _{ON}	Turn-On Time	From Assertion of V _{EN} to V _{OUT} =90%*V _{OUT}		300		μs

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
T _{SDH}	Thermal Shutdown Threshold	Temperature Rising		160		°C
T _{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling		140		°C

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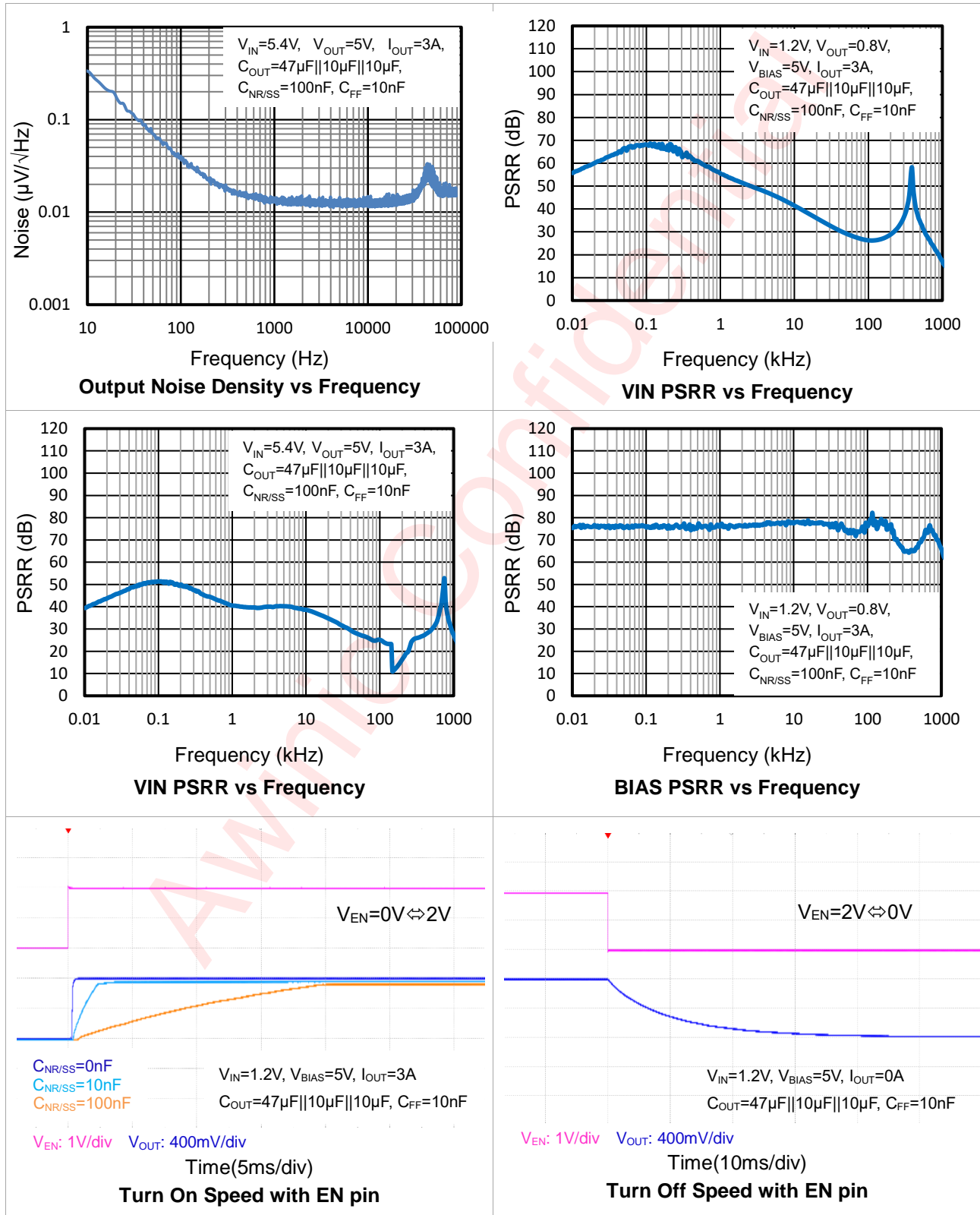
Typical Characteristics

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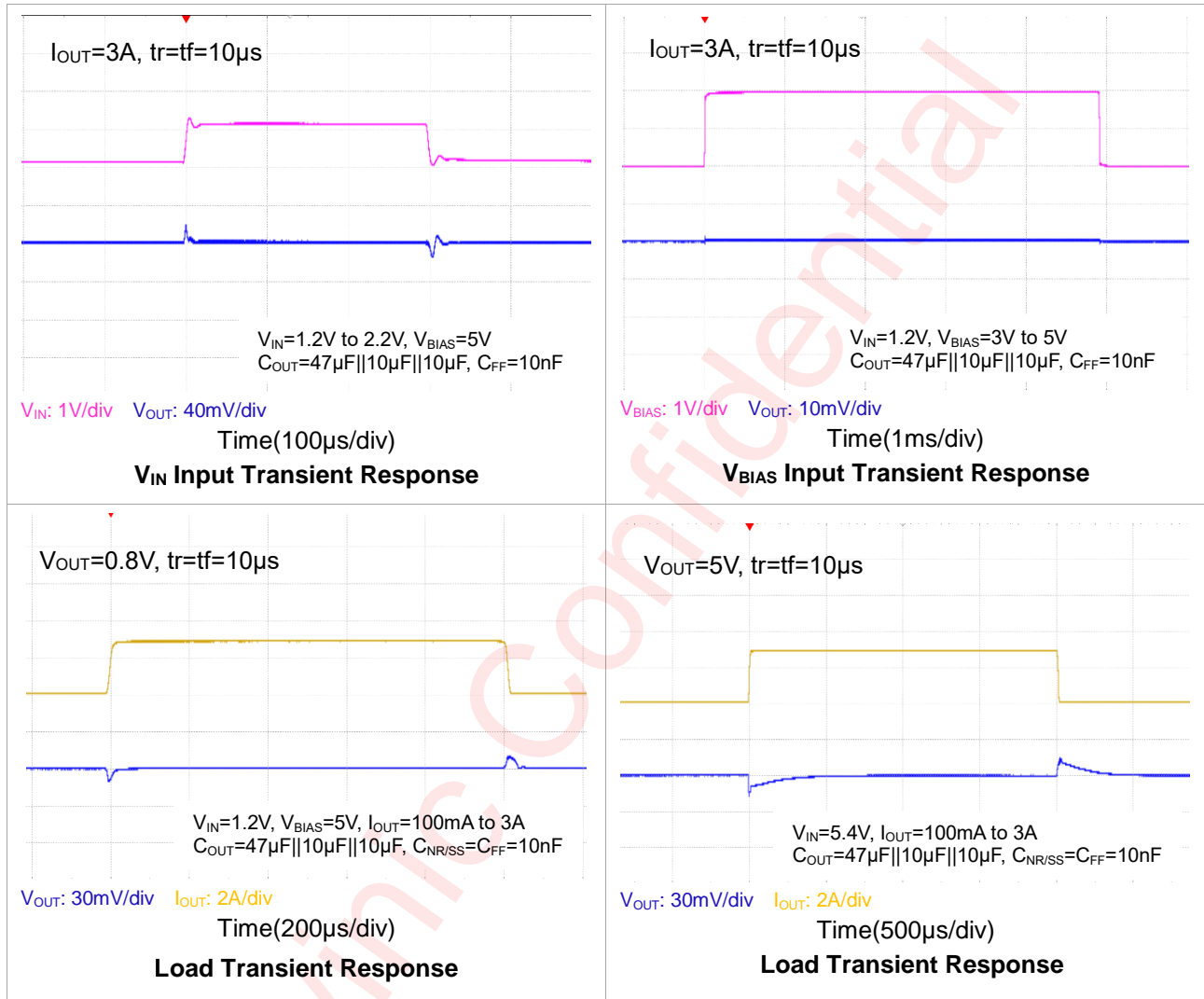
Typical Characteristics (Continued)

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Typical Characteristics (Continued)

$V_{IN}=1.4V$ or $V_{IN}=V_{OUT(SET)}+0.4V$ (whichever is greater), $V_{BIAS}=\text{open}$, $V_{OUT(SET)}=0.8V$, $V_{EN}=1.1V$, $C_{IN}=22\mu F$, $C_{OUT}=47\mu F$, $C_{NR/SS}=10nF$, $C_{FF}=10nF$, and PG pin pulled up to V_{IN} with $10k\Omega$, $T_A=25^\circ C$, unless otherwise specified.



Detailed Functional Description

The AW37023 is a high current (3A), low noise ($5\mu\text{Vrms}$), high accuracy (1%) low dropout linear voltage regulator. These features make the device a robust solution to solve many challenging problems in generating a clean, accurate power supply. The high performance also makes the AW37023 useful in a variety of applications. The AW37023 provides the protection functions for output current limit, output short-circuit condition and over temperature.

Low Noise, High PSRR Output

The AW37023 includes a low noise reference and error amplifier ensuring minimal noise during operation. The NR/SS capacitor ($C_{\text{NR/SS}}$) and feed-forward capacitor (C_{FF}) are the easiest way to reduce device noise. $C_{\text{NR/SS}}$ filters the noise from the reference and C_{FF} filters the noise from the error amplifier. The noise contribution from the charge pump is minimal. The overall noise of the system at low output voltages can be reduced by using a bias rail because this rail provides more headroom for internal circuitry.

The high PSRR of the AW37023 ensures minimal coupling of input supply noise to the output. The PSRR performance is primarily results from a high-bandwidth and high-gain error amplifier.

Bias Rail

The AW37023 features a bias rail to enable low-input voltage, low-output (LILLO) voltage operation by providing power to the internal circuitry of the device. The bias rail is required for operation with $V_{\text{IN}} < 1.4\text{V}$.

An internal power MUX supplies the greater of either the input voltage or the bias voltage to an internal charge pump to power the internal circuitry. Unlike other LDOs that have a bias supply, the AW37023 does not have a minimum bias voltage with respect to the input supply because an internal charge pump is used instead.

Soft-Start

Soft-start refers to the ramp-up time of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltages. The noise-reduction capacitor ($C_{\text{NR/SS}}$) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp time during turn-on. The start-up ramp is monotonic.

Enable Operation

The enable pin for the AW37023 is active high. When the EN pin voltage is lower than V_{ENL} , the device is in shutdown state, there is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 260Ω (Typ.) resistor.

When the EN pin voltage is higher than V_{ENH} , the device is in active state, the input voltage is regulated to the output voltage and the automatic discharge transistor is turned off.

When the enable functionality is not desired, EN must be tied to V_{IN} . However, when the enable functionality is desired, the enable voltage must come after V_{IN} is above $V_{\text{UVLO1_IN}}$ when a BIAS rail is used.

Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage ($V_{\text{IT_PG}} + V_{\text{HYS_PG}}$), the PG pin open-drain output engages and pulls the PG pin close to GND. When the feedback voltage exceeds the $V_{\text{IT_PG}}$ by an amount greater than $V_{\text{HYS_PG}}$, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for

sequencing. Using a pullup resistor from 10kΩ to 100kΩ is recommended.

The use of a feed-forward capacitor (C_{FF}) can cause glitches on start-up, and the power-good circuit may not function normally below the minimum input supply range.

The state of PG is only valid when the device operates above the minimum supply voltage. During short UVLO events and at light loads, power-good does not assert because the output voltage is sustained by the output capacitance.

Output Current Limit and Short-Circuit Protection

AW37023 integrates current limit function, protecting IC from excessive current. the output current is internally limited to 4.2A (Typ.); therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high power dissipation typically found in these conditions. Continuous operation in current limit is not recommended.

Meanwhile, AW37023 integrates fold-back current limit function, when the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 1.2A (Typ.).

Undervoltage Lockout (UVLO)

The UVLO circuit monitors the input and bias voltage to prevent the device from turning on before V_{IN} and V_{BIAS} rise above the lockout voltage. The UVLO circuit also disables the output of the device when V_{IN} or V_{BIAS} fall below the lockout voltage. The UVLO circuit responds quickly to glitches on V_{IN} or V_{BIAS} and attempts to disable the output of the device if either of these rails collapse. As a result of the fast response time of the input supply UVLO circuit, fast and short line transients well below the input supply UVLO falling threshold can cause momentary glitches when asserted or when recovered from the transient.

ANY-OUT Programmable Output Voltage

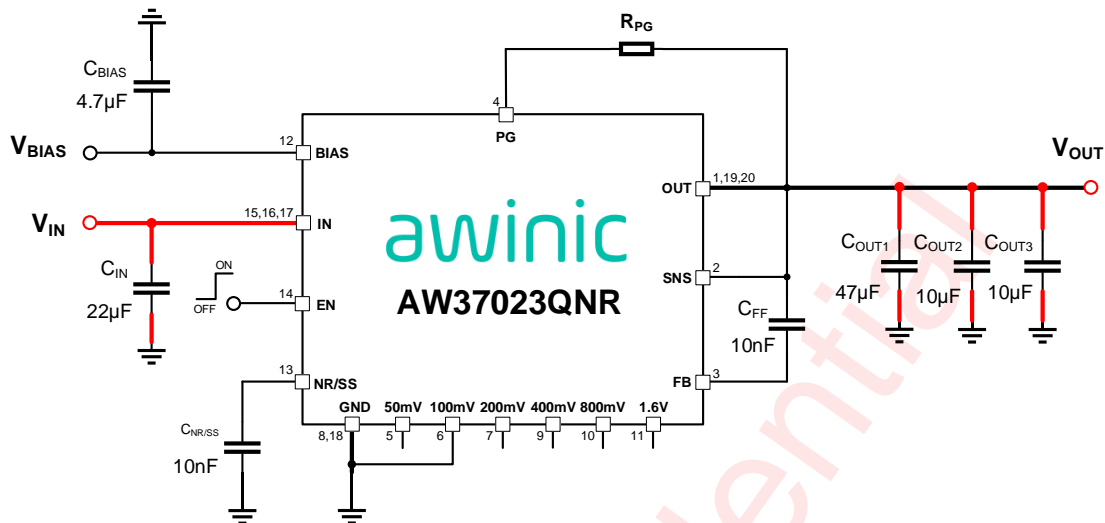
An internal feedback resistance network is provided, allowing the AW37023 output voltage to be programmed easily between 0.8V to 3.95V with a 50mV step by tying the ANY-OUT pins to ground. The ANY-OUT resistors are accessible via pin 2 and pins 5 to 11 and are used to program the regulated output voltage. Each pin can be connected to ground or left open, or connected to SNS. ANY-OUT programming is set by Equation 1 as the sum of the internal reference voltage ($V_{NR/SS}=0.8V$) plus the accumulated sum of the respective voltages assigned to each active pin. Table 1 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{FB} .

$$V_{OUT}=V_{NR/SS}+(\sum \text{ANY-OUT Pins to Ground}) \quad (1)$$

Table 1 ANY-OUT Programmable Output Voltage

ANY-OUT Program Pins (Active Low)	Additive Output Voltage Level
Pin5 (50mV)	50mV
Pin6 (100mV)	100mV
Pin7 (200mV)	300mV
Pin9 (400mV)	400mV
Pin10 (800mV)	800mV
Pin11 (1.6V)	1.6V

The following figure show a 0.9V output voltage:



$$V_{OUT} = V_{NR/SS} + 0.1 \text{ V} = 0.8 \text{ V} + 0.1 \text{ V} = 0.9 \text{ V}$$

Adjustable Output Voltage Setting

The AW37023 can be set either with the internal feedback resistance network or by connecting with external resistors to achieve different output voltages. External resistors must be used as shown in Figure 2. The output voltage is determined by the following Equation 2:

$$V_{OUT_ADJ} = V_{FB} \left(1 + \frac{R_1}{R_2} \right) \quad (2)$$

Where:

- V_{OUT_ADJ} is output voltage of the circuit with resistor divider
- V_{FB} is 0.8V , the LDO's reference voltage

One parallel capacitor ($C_{FF}=10\text{nF}$) with R_1 can be used to improve the feedback loop stability and PSRR, increase the transient response and reduce the output noise. Typical application circuits gives the connections for the adjustable output voltage application.

Thermal shutdown

AW37023 integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 160°C , AW37023 detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 140°C . At this moment, the over-temperature protection-state is released, IC resumes to work again .The hysteresis avoids IC's turning off and on frequently around the Thermal Shutdown threshold.

Auto Discharge

AW37023 makes output voltage decrease quickly when in disable state or thermal shutdown state, benefit from integrating auto discharge function.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW37023 advises to use a 22 μ F or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit, the input decoupling capacitor is necessary to be connected as close as possible to the V_{IN} pin for ensuring the device stability. When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance.

OUT pin: Output Capacitor C_{OUT}

AW37023 advises to use a 0805 sized, 47 μ F ceramic capacitor in parallel with two 0805 sized, 10 μ F ceramic capacitors or more at OUT pin as shown in Typical Application Circuit. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of C_{OUT} must be considered in design. This 47 μ F||10 μ F||10 μ F combination ensures that at high input voltage and high output voltage configurations, the minimum effective capacitance is met. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

BIAS pin: BIAS Capacitor C_{BIAS}

AW37023 advises to use a 4.7 μ F or more X5R or X7R ceramic capacitor at BIAS pin as shown in Typical Application Circuit.

NR/SS pin: Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

AW37023 advises to use a 10nF X5R or X7R ceramic capacitor at NR/SS pin as shown in Typical Application Circuit. The AW37023 features a programmable soft-start that is set with an external capacitor ($C_{NR/SS}$). The use of an external $C_{NR/SS}$ is highly recommended, it not only minimizes the inrush current but also helps reduce the noise component from internal reference.

FB pin: Feed-Forward Capacitor (C_{FF})

AW37023 advises to use a 10nF X5R or X7R ceramic capacitor at FB pin as shown in Typical Application Circuit. Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance.

Application Information

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance $R_{\theta JA}$.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where $T_{J_MAX} = 150^\circ\text{C}$:

$$PD_{MAX_ABS} = (T_{J_MAX} - T_A) / R_{\theta JA}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where $T_{J_REC} = 125^\circ\text{C}$:

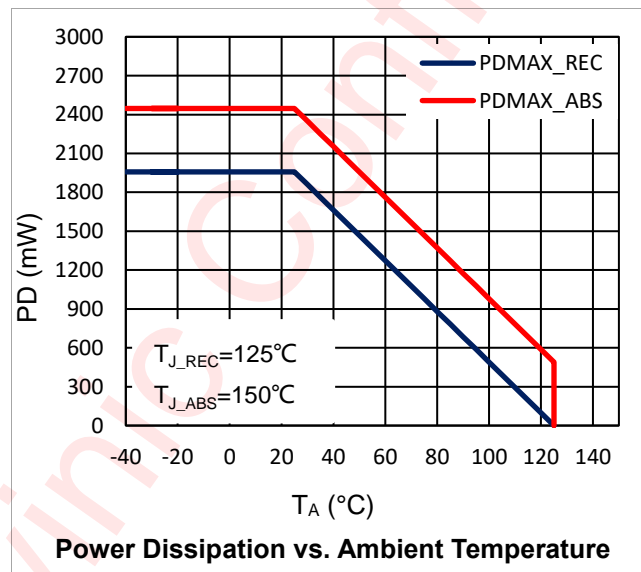
$$PD_{MAX_REC} = (T_{J_REC} - T_A) / R_{\theta JA}$$

The actual power being dissipated in the device can be represented by Equation below:

$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :

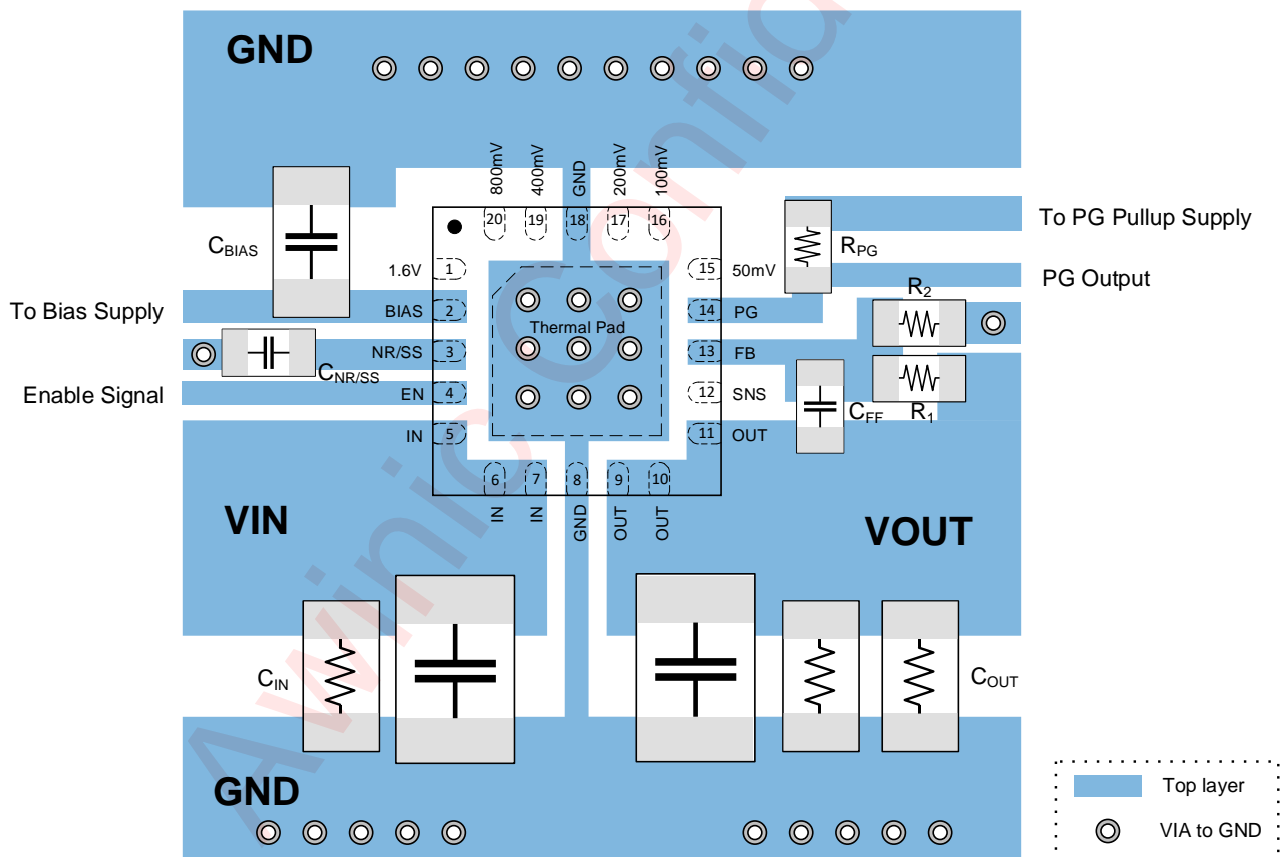


The above graphs show the maximum power dissipation of the respective package at $T_{J_REC} = 125^\circ\text{C}$ and $T_{J_MAX} = 150^\circ\text{C}$. Operating the device in the region between PD_{MAX_REC} and PD_{MAX_ABS} might have a negative influence on its lifetime.

PCB Layout Consideration

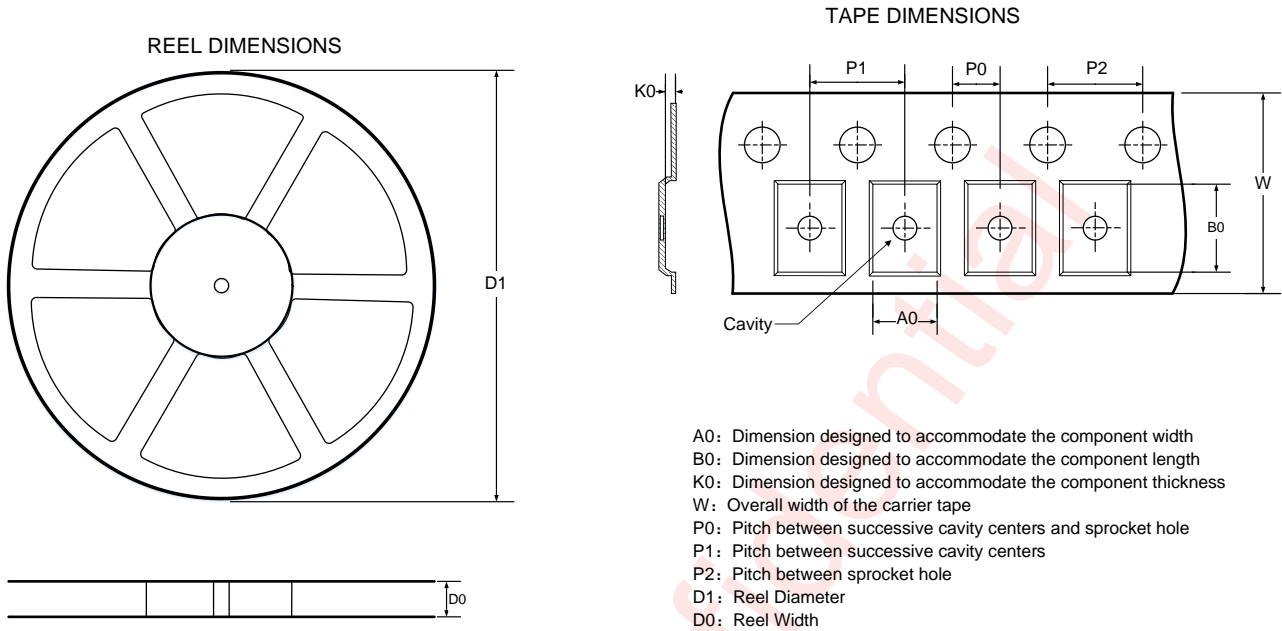
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout should be obeyed:

1. All peripheral components should be placed as close to the chip as possible. C_{IN} , C_{OUT} , $C_{NR/SS}$, C_{FF} should be close to pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN,OUT are the large current input and output of the chip, make IN, OUT and GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient via holes below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

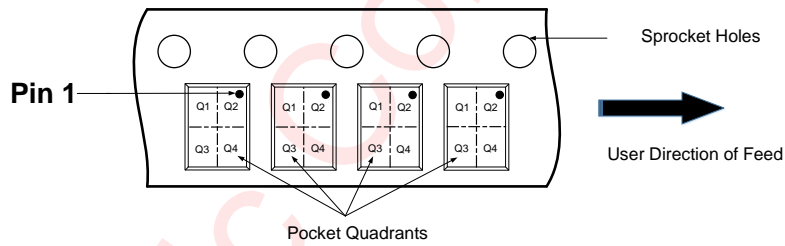


PCB layout example

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



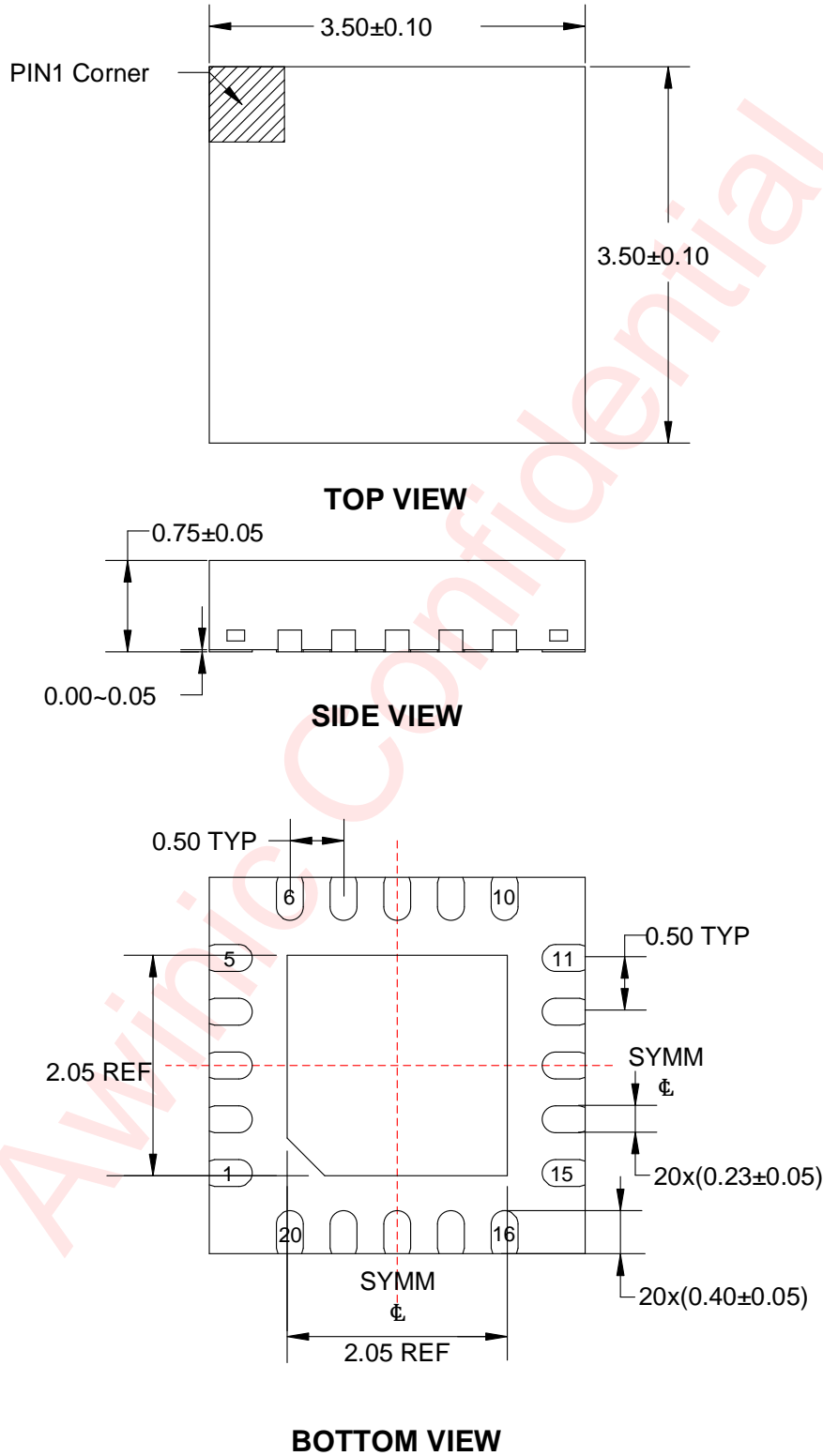
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	3.70	3.70	1.10	2.00	8.00	4.00	12.00	Q2

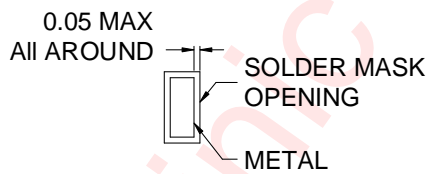
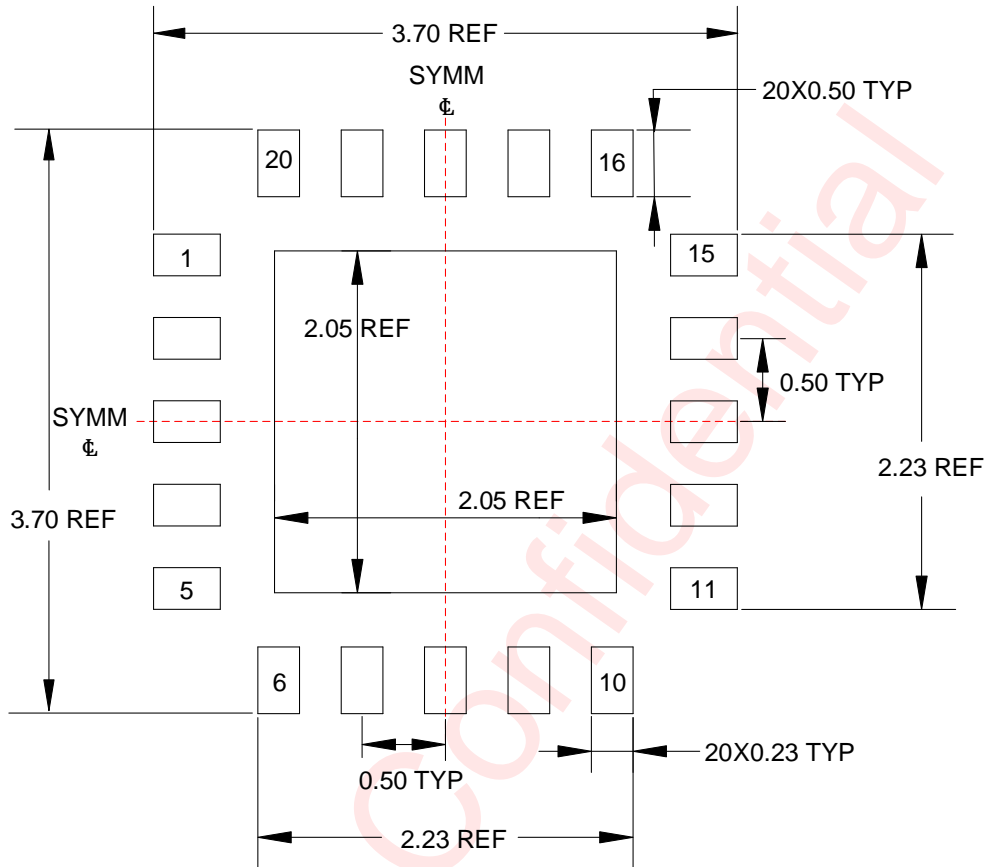
All dimensions are nominal

Package Description

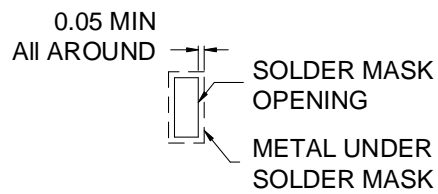


Unit: mm

Land Pattern Data



NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Nov. 2024	Officially released
V1.1	Aug. 2025	1. Update the "Operating free-air temperature range".(P6) 2. Update the "Electrical Characteristics".(P8~P10)

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