IXYS

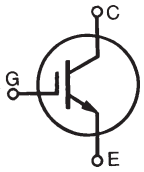
Preliminary Technical Information

High Voltage IGBT

IXGA20N250HV

V_{CES} = 2500V
I_{C110} = 12A
$V_{CE(sat)}$ ≤ 3.1V

For Capacitor Discharge Applications



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	2500	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	2500	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	30	A
I_{C110}	T_C = 110°C	12	A
I_{CM}	T_C = 25°C, V_{GE} = 19V, 1ms	105	A
	10ms	55	A
SSOA	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 20Ω	I_{CM} = 60	A
(RBSOA)	Clamped Inductive Load	1500	V
P_C	T_C = 25°C	150	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		2.3	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	2500			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			25	μA
	T_J = 125°C			750	μA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 20A, V_{GE} = 15V, Note 1			3.1	V

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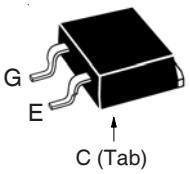


G = Gate C = Collector
E = Emitter Tab = Collector

Features

- International Standard Package
- High Voltage Package
- Electrically Isolated Tab
- High Peak Current Capability
- Low Saturation Voltage
- Molding Epoxies Meet UL 94 V-0 Flammability Classification

Advantages

- High Power Density
- Easy to Mount

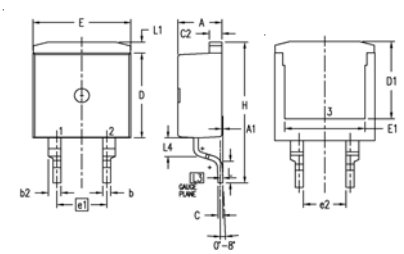
Applications

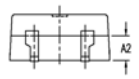
- Capacitor Discharge
- Pulser Circuits

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 20A, V_{CE} = 10V, Note 1	8	13	S
$I_{C(ON)}$	V_{GE} = 20V, V_{CE} = 15V, Note 1		190	A
C_{ies}	V_{CE} = 15V, V_{GE} = 25V, f = 1MHz		1190	pF
C_{oes}			53	pF
C_{res}			18	pF
Q_g	I_C = 20A, V_{GE} = 15V, V_{CE} = 1000V		53	nC
Q_{ge}			8	nC
Q_{gc}			22	nC
$t_{d(on)}$	**Resistive Switching Times**		57	ns
t_r	I_C = 40A, V_{GE} = 15V, Note 1		160	ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 10Ω		136	ns
t_f			930	ns
R_{thJC}				0.83 °C/W

Note 1. Pulse test, t < 300μs, duty cycle, d < 2%.

TO-263 (HV) Outline





PIN: 1 - Gate
2 - Emitter
3 - Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETER MIN	MILLIMETER MAX
A	.170	.185	4.30	4.70
A1	.000	.008	0.00	0.20
A2	.091	.098	2.30	2.50
b	.028	.035	0.70	0.90
b2	.046	.054	1.18	1.38
C	.018	.024	0.45	0.60
C2	.049	.055	1.25	1.40
D	.354	.370	9.00	9.40
D1	.311	.327	7.90	8.30
E	.386	.402	9.80	10.20
E1	.307	.323	7.80	8.20
e1	.200 BSC		5.08 BSC	
(e2)	.163	.174	4.13	4.43
H	.591	.614	15.00	15.60
L	.079	.102	2.00	2.60
L1	.039	.055	1.00	1.40
L3	.010 BSC		0.254 BSC	
(L4)	.071	.087	1.80	2.20

PRELIMANARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

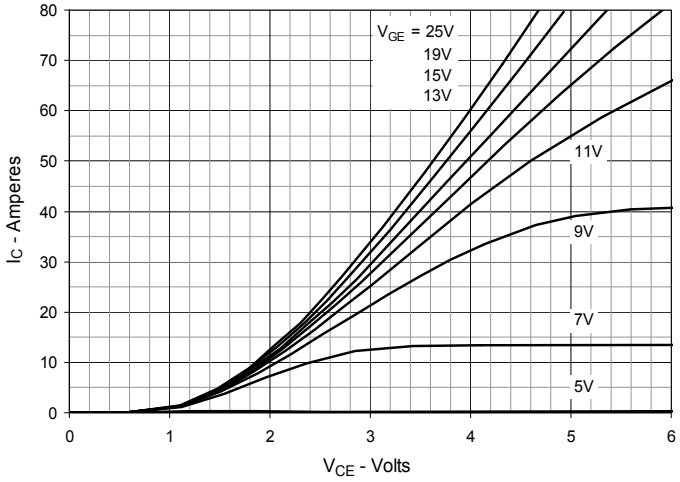


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

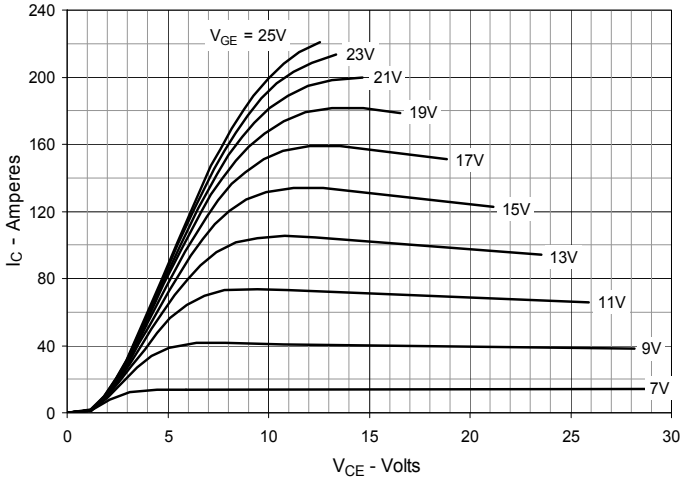


Fig. 3. Output Characteristics @ T_J = 125ºC

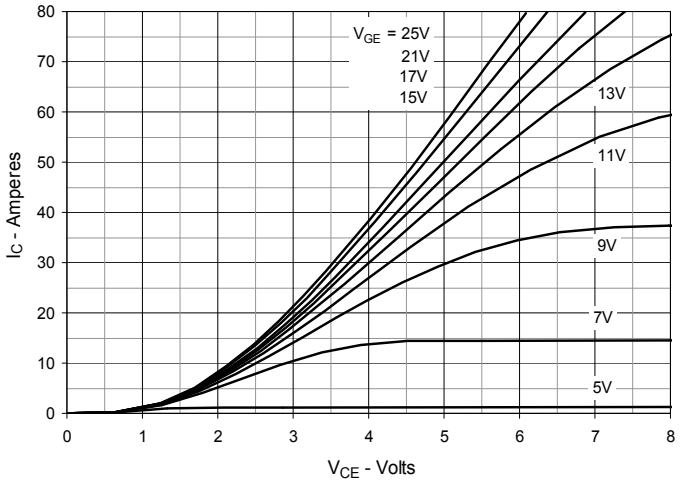


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

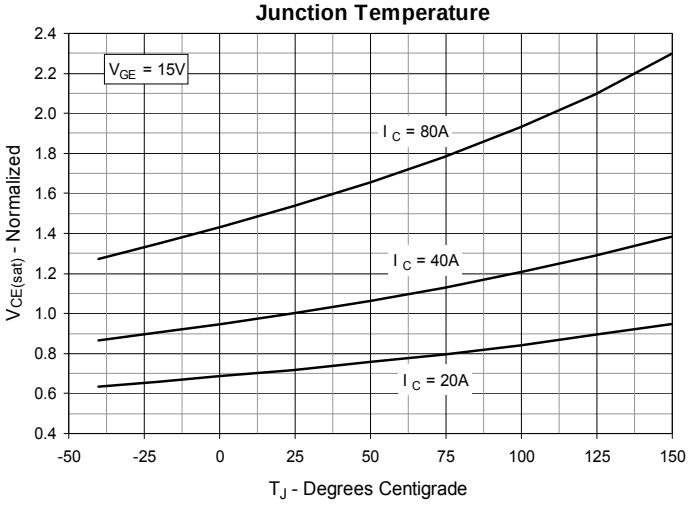


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

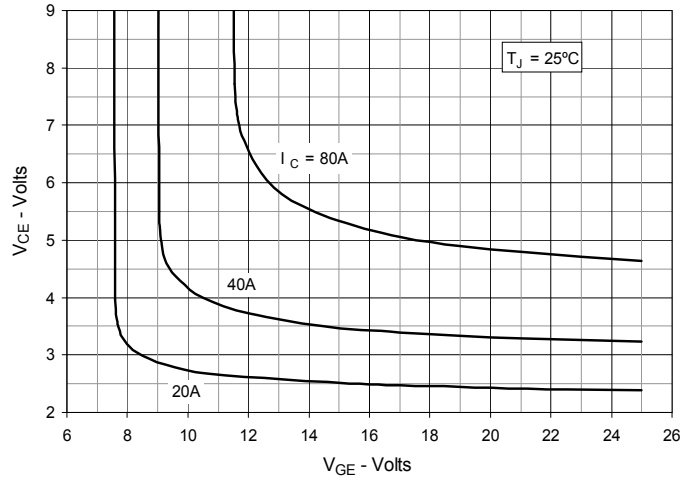


Fig. 6. Input Admittance

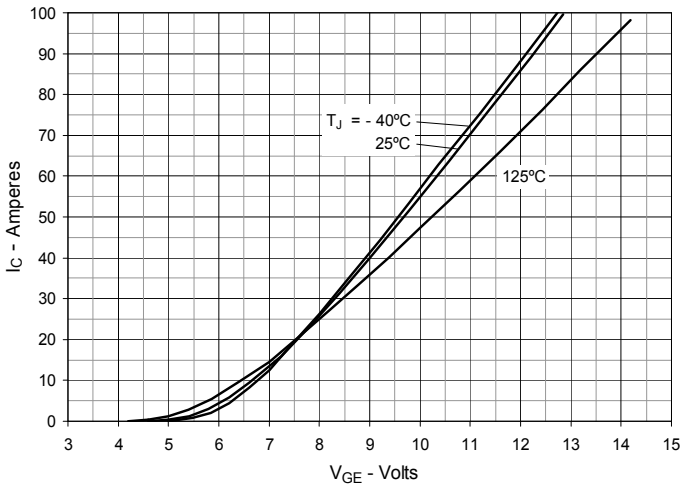


Fig. 7. Transconductance

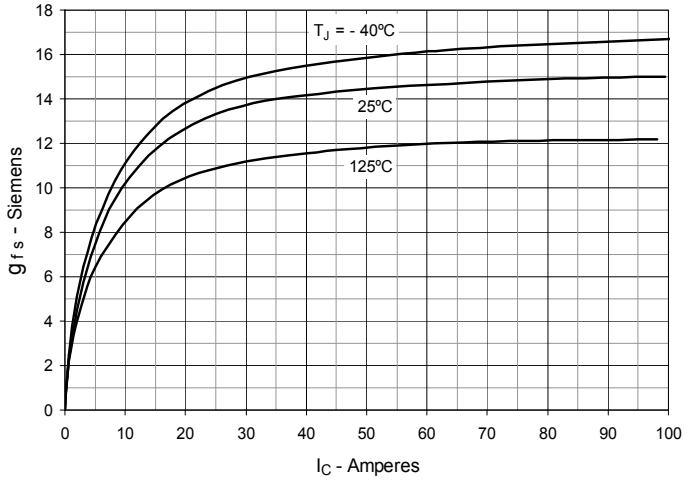


Fig. 8. Gate Charge

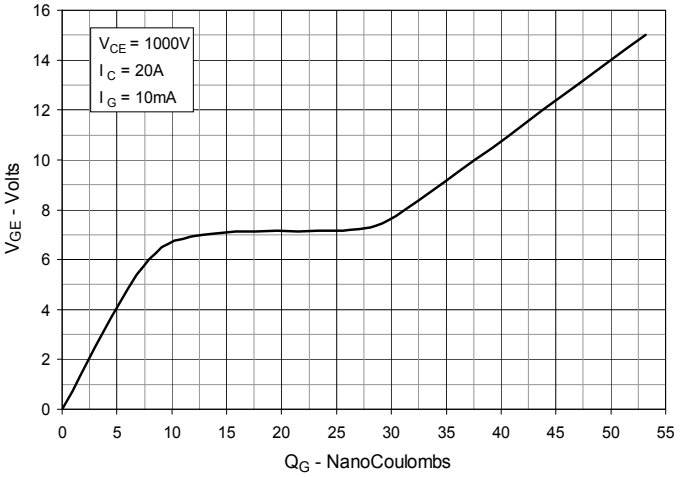


Fig. 9. Reverse-Bias Safe Operating Area

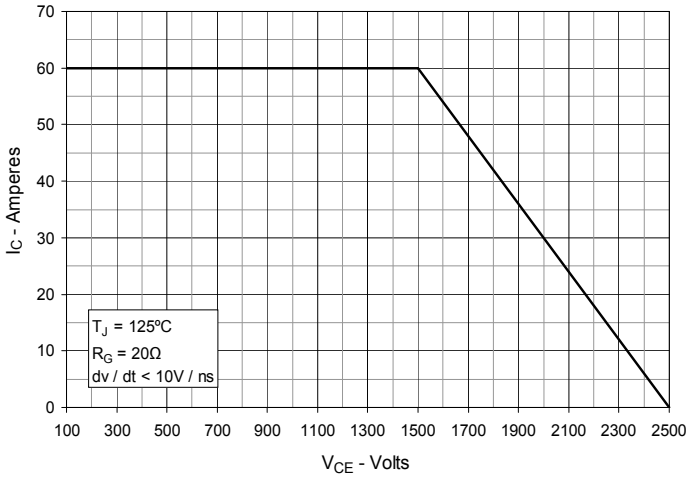


Fig. 10. Capacitance

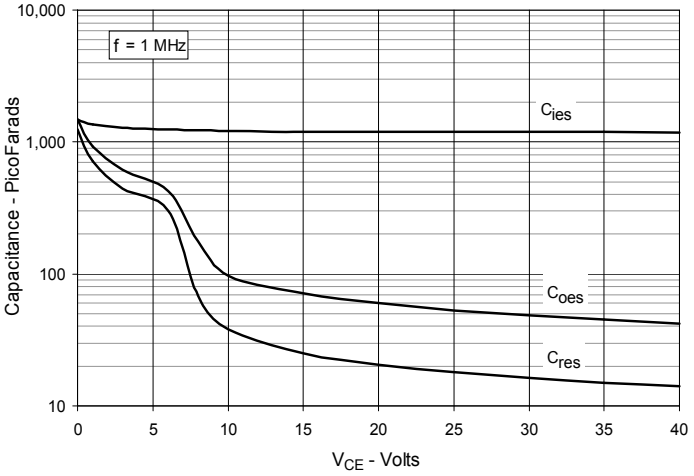


Fig. 13. Maximum Transient Thermal Impedance

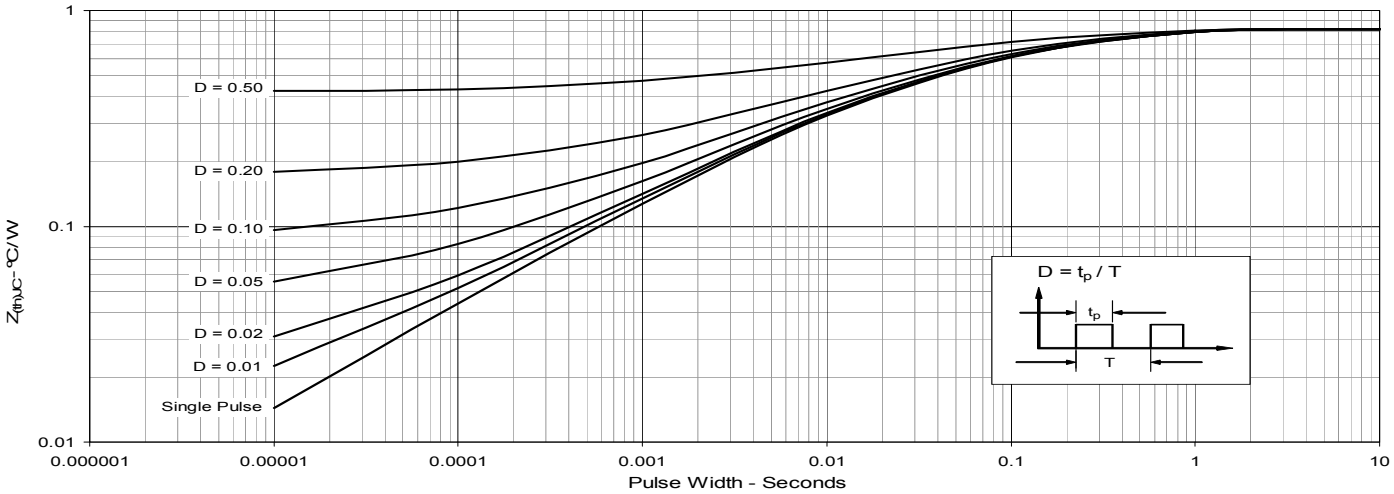


Fig. 12. Resistive Turn-on Rise Time vs. Junction Temperature

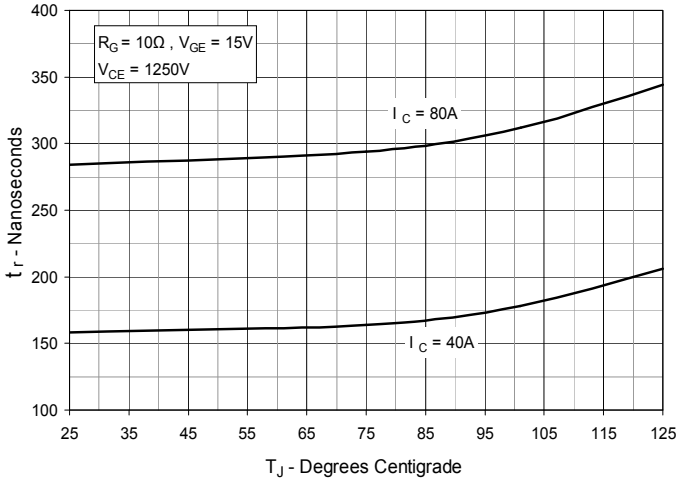


Fig. 13. Resistive Turn-on Rise Time vs. Collector Current

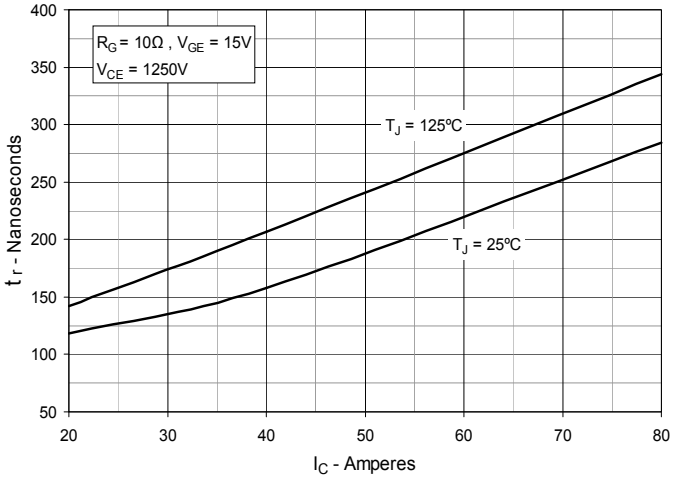


Fig. 14. Resistive Turn-on Switching Times vs. Gate Resistance

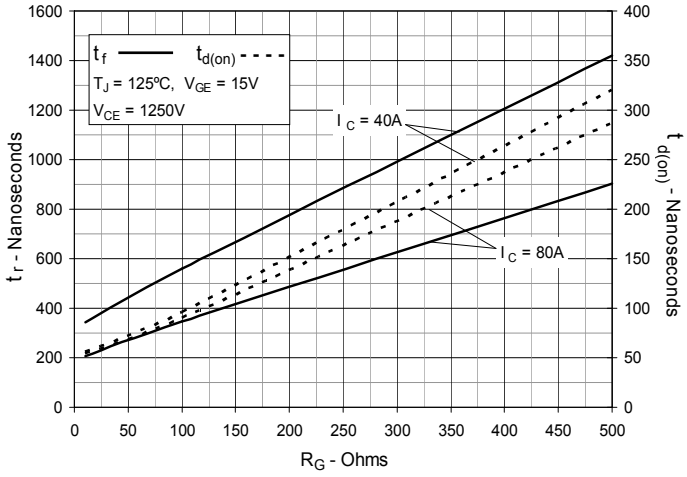


Fig. 15. Resistive Turn-off Switching Times vs. Junction Temperature

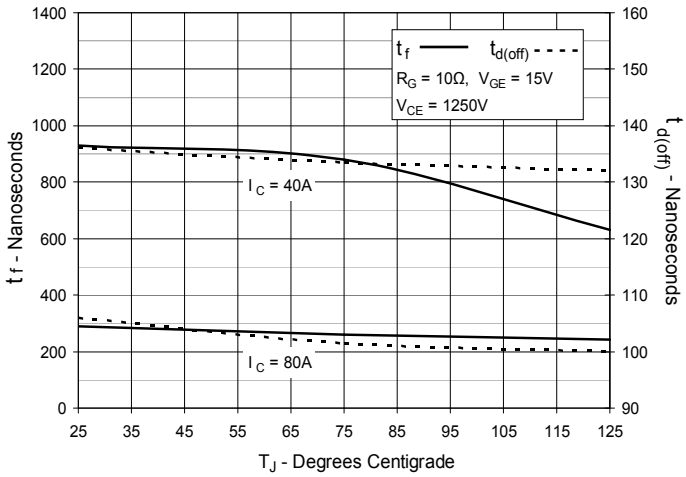


Fig. 16. Resistive Turn-off Switching Times vs. Collector Current

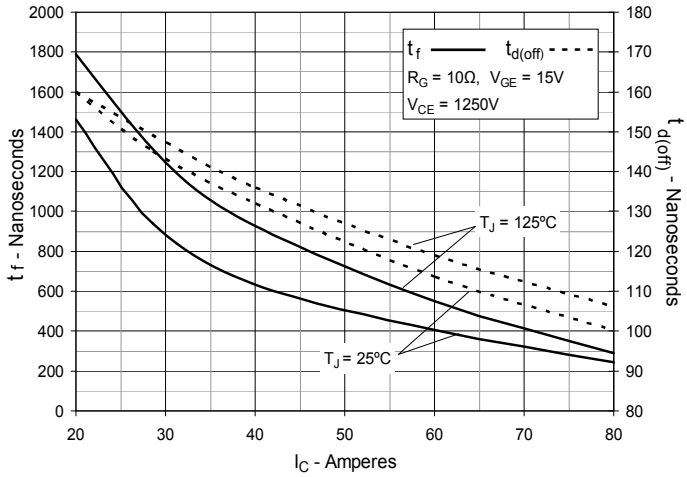


Fig. 17. Resistive Turn-off Switching Times vs. Gate Resistance